MP7770

2 x 45W Stereo Single-Ended or 90W Mono BTL Class-D Audio Amplifier

The Future of Analog IC Technology

DESCRIPTION

MP7770 is an analog class-D audio amplifier that can drive either stereo speakers in single-ended configuration or a mono speaker in a bridge-tied-load configuration. It is part of MPS's family of fully-integrated audio amplifiers that dramatically reduce footprint size by integrating:

- 100mΩ power MOSFETs
- Startup/Shutdown pop elimination
- Short-circuit protection circuits

The MP7770 is capable of delivering 45W per channel into 4Ω speaker in single-ended output structure, or delivering 90W into 8Ω speaker in bridge-tied-load output structure under 36V VDD. MPS's class D audio amplifiers exhibit the high fidelity of a Class A/B amplifier at higher efficiencies. The circuit is based on the MPS's proprietary variable-frequency topology, which delivers excellent linearity, fast response time and operates from a single power supply.

FEATURES

- 9.5V-to-36V Operation from a Single Supply
- ±8.5A Peak Current Output
- Output Power at 36V and 10%THD:
  - Stereo Single-Ended: 2 x 45W into 4Ω Load,
  - Bridge-Tied Load: 90W into 8Ω Load
- THD+N = 0.03% at 1W, 8Ω
- > 90% Efficiency at 10%THD
- Low Noise
- Switching Frequency of up to 1MHz
- Integrated Startup and Shutdown Pop Elimination Circuit
- Programmable UVP
- Thermal and Short-Circuit Protection
- Output Fault Flag and Thermal Warning
- Integrated Power FETs
- TSSOP28-EP Package with Exposed Pad

APPLICATIONS

- DVD Receiver
- Mini Combo System
- Home Theater Systems
- Surround Sound Systems
- Audio Docking or High-Power Sound Box

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance

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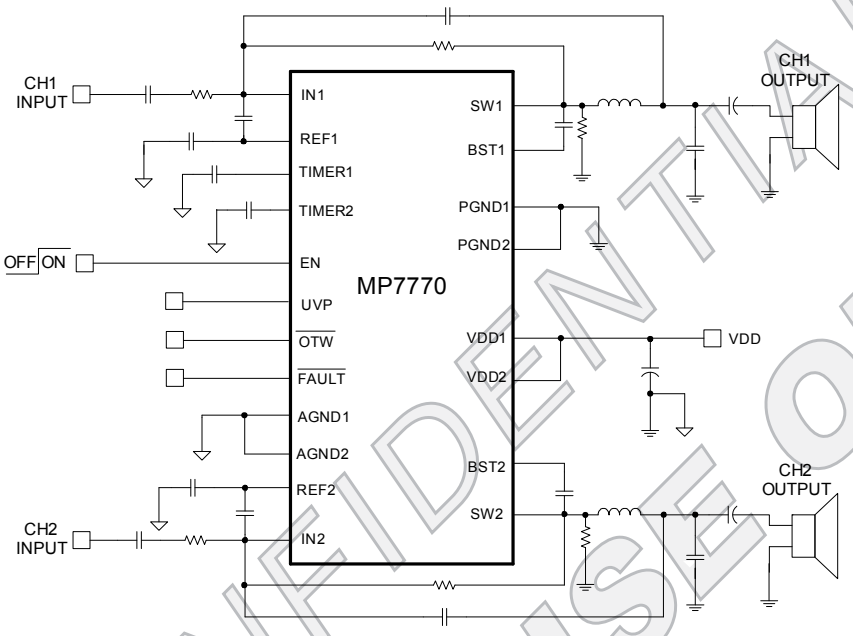
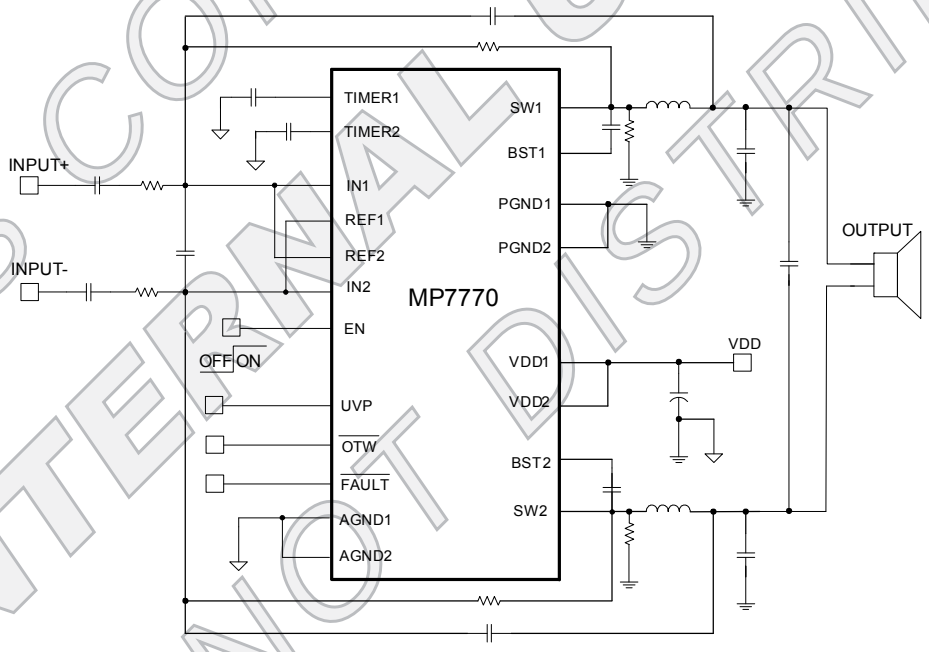
TYPICAL APPLICATIONS



Stereo SE Application Circuit



Mono BTL Application Circuit

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP7770GF	TSSOP28-EP	*See Below*

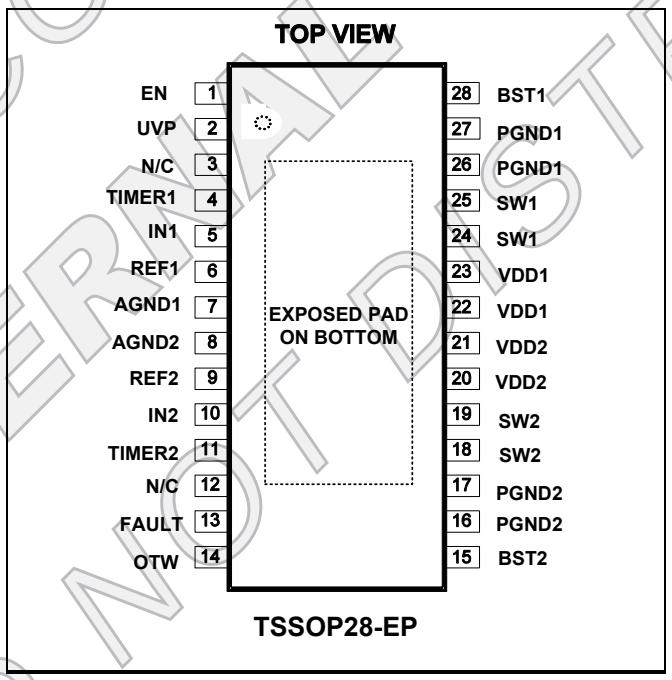
* For Tape & Reel, add suffix –Z (e.g. MP7770GF–Z);

TOP MARKING (MP7770GF)

MPSYYWW
MP7770
LLLLLLLLL

MP7770: product code of MP7770GF;
MPS: MPS prefix;
Y: year code;
WW: week code:
LLL: lot number;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DD} 40V
BS Voltage ..... (V_{SW} - 0.3V) to (V_{SW} + 6.5V)
V_{OTW}, V_{FAULT}, V_{UVP}, V_{TIMER}, V_{EN} .....–0.3V to +6V
V_{SW} .....–0.3V to (V_{DD} + 1V)
V_{REF}, V_{IN} .....–0.3V to +34V
AGND to PGND .....–0.3V to +0.3V
Continuous Power Dissipation (T_A = 25°C) (2) ..... 3.9 W
Junction Temperature ..... 150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{DD} ..... 9.5V to 36V
Operating Junction Temp. (T_J). ..... -40°C to +125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}
TSSOP28-EP	32	6 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5, 6)

V_{DD} = 24V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Standby Current		V_{EN} = 0V,REF=IN=Float		120	140	μA
Quiescent Current	I_Q	SW=Low		3	4	mA
SW ON Resistance		Sourcing and Sinking		0.1	0.15	Ω
Short-Circuit Current		Sourcing and Sinking	6.2	8.5		A
EN Enable Threshold Voltage		V_{EN} Rising		1.4	2.0	V
		V_{EN} Falling	0.4	1.0		V
EN Enable Input Current		V_{EN} = 5V		5		μA
External Under-Voltage Detection	V_{UVP}		2	2.2	2.4	V
External Under-Voltage Detection Hysteresis Voltage	V_{Hys}			0.3		V
Thermal Shutdown Trip Point (7)		T_J Rising		150		°C
Thermal Shutdown Hysteresis(7)				20		°C
Thermal Warning Trip Point(7)				125		°C
Thermal Warning Hysteresis(7)				10		°C

Notes:

5) The device is not guaranteed to function outside its operating rating.
6) Electrical Characteristics are for the IC only with no external components except bypass capacitors.
7) Not production tested.

OPERATING SPECIFICATIONS (8)

Circuit of Figure 6, Single-Ended Output Configuration; V_{DD} = 34V, Gain=8.2V/V; V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Standby Current		V_{EN} = 0V			120		μA
Quiescent Current		Switching, no load			29		mA
Power Output		f = 1kHz, THD+N = 10%, 4Ω Load			41		W
		f = 1kHz, THD+N = 1%, 4Ω Load			32		W
		f = 1kHz, THD+N = 10%, 8Ω Load			22		W
		f = 1kHz, THD+N = 1%, 8Ω Load			17		W
THD + Noise		P_{OUT} = 1W, f = 1kHz, 4Ω Load			0.05		%
		P_{OUT} = 1W, f = 1kHz, 8Ω Load			0.03		%
Efficiency		f = 1kHz, P_{OUT} = 41W, 4Ω Load			91		%
		f = 1kHz, P_{OUT} = 22W, 8Ω Load			95		%
Maximum Power Bandwidth					20		kHz
Dynamic Range					102		dB
Noise Floor		A-Weighted			90		μV
Power Supply Rejection		V_{RIPPLE}=300mV$_{PP}$ C_R=100μF	f = 1k Hz		-60		dB
			f = 217 Hz		-60		dB

Circuit of Figure 7, BTL Output Configuration; V_{DD} = 34V, Gain=15V/V; V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Standby Current		V_{EN} = 0V			120		μA
Quiescent Current		Switching, no load			32		mA
Power Output		f = 1kHz, THD+N = 10%, 6Ω Load			108		W
		f = 1kHz, THD+N = 1%,6Ω Load			83		W
THD+ Noise		P_{OUT} = 1W, f = 1kHz, 6Ω Load			0.06		%
		P_{OUT} = 1W, f = 1kHz, 8Ω Load			0.04		%
Efficiency		f = 1kHz, P_{OUT} = 108W, 6Ω Load			91		%
		f = 1kHz, P_{OUT} = 84W, 8Ω Load			95		%
Maximum Power Bandwidth					20		kHz
Dynamic Range					105		dB
Noise Floor		A-Weighted			120		μV
Power Supply Rejection		V_{RIPPLE}=300mV$_{PP}$	f = 1k Hz		-60		dB
			f = 217 Hz		-60		dB

Note:

8) Operating Specifications are for the IC in Typical Application circuit (Figure 6 and Figure 7).

PIN FUNCTIONS

EP on Bottom Pin #	Name	Description
1	EN	Enable Input for Amplifier 1. Drive EN1 high to turn on the Amplifier 1, low to turn it off.
2	UVP	Under-Voltage Protection Reference Input.
3, 12	N/C	Not Connected.
4	TIMER1	Internal Timer Input for Amplifier 1. A capacitor from TIMER1 to AGND sets the internal timer which is used for start-up pop elimination.
5	IN1	Inverting Input for Amplifier 1 .
6	REF1	Internal Analog Reference (VDD/2) for Amplifier 1. For SE configuration, connect a bypass capacitor from REF1 to AGND (10μF).
7	AGND1	Analog Ground for Amplifier 1. Connect AGND1 to AGND2. Connect PGND to AGND at a single point.
8	AGND2	Analog Ground for Amplifier 2. Connect AGND2 to AGND1.
9	REF2	Internal Analog Reference (VDD/2) for Amplifier 2. For BTL configuration, connect a bypass capacitor from REF2 to AGND (10μF).
10	IN2	Inverting Input for Amplifier 2.
11	TIMER2	Internal Timer Input for Amplifier 2. Use a capacitor from TIMER2 to AGND to set the internal timer for start-up pop elimination.
13	FAULT	Fault Output. A low output at FAULT indicates that the IC has detected an over-temperature or over-current condition. This output is open drain.
14	OTW	Over Temperature Warning. A low output at OTWB indicates that the die temperature rises above 125°C. This output is open drain.
15	BST2	High-Side MOSFET Bootstrap Input for Amplifier 2. Connect a capacitor from BST2 to SW2 to supplies the gate drive to the internal High-Side MOSFET.
16, 17	PGND2	Power Ground for Amplifier 2. Connect PGND2 to PGND1.
18, 19	SW2	Switched Power Output for Amplifier 2.
20, 21	VDD2	Power Supply Input for Amplifier 2. Bypass VDD2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the VDD2 and PGND2 pins.
22, 23	VDD1	Power Supply Input for Amplifier 1. Bypass VDD1 to PGND1 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the VDD1 and PGND1 pins.
24, 25	SW1	Switched Power Output for Amplifier 1.
26,27	PGND1	Power Ground for Amplifier 1. Connect PGND1 to PGND2. Connect PGND to AGND at a single point.
28	BST1	High-Side MOSFET Bootstrap Input for Amplifier 1. A capacitor from BST1 to SW1 supplies the gate drive current to the internal High-Side MOSFET.