PRODUCT RELIABILITY REPORT

Product: MPQ2179A-AEC1

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1. Device Information

Product:	MPQ2179A-AEC1
Package:	8-PIN FC-QFN(1.5mm×2.0mm)
Process Technology:	BCD
Report Date:	10/29/2020

2. Summary of Test Results

TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS					
Test	**#**	**Test Condition**	**Lot# or Date Code**	**Test Results (S.S./Rej)**	**Comment**
Preconditioning, prior to THB/HAST, AC/UHAST, TC, HTSL and PTC	A1	J-STD-020 Reflow: Tp>=260°C, tp>=30sec, 3×reflows	1921 1941 1946	308/0 308/0 308/0	MSL=1
Steady State Temperature Humidity Bias Life Test (THB)/ Highly Accelerated Temperature and Humidity Stress Test (HAST)	A2	JESD22-A110, @130°C/85%RH static bias at Vinmax for 96 hours or equivalent	1921 1941 1946	77/0 77/0 77/0	
Unbiased Autoclave (AC)/ Unbiased HAST(UHAST)	A3	JESD22-A118, @130°C/85%RH for 168 hours or equivalent	1921 1941 1946	77/0 77/0 77/0	
Temperature Cycling (TC)	A4	JESD22-A104, from -65°C to 150°C for 1000 cycles or equivalent.	1921 1941 1946	77/0 77/0 77/0	
Power Temperature Cycling (PTC)	A5	JESD22-A105, from -40°C to 125°C for 1000 cycles.	SJD0967	45/0	
High Temperature Storage Life (HTSL)	A6	JESD22-A103, @175°C for 1000 hours.	1921 1941 1946	77/0 77/0 77/0	
TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS					
Test	**#**	**Test Condition**	**Lot# or Date Code**	**Test Results (S.S./Rej)**	**Comment**
High Temperature Operating Life (HTOL)	B1	JESD22-A108, @Tj=150°C for 1000 hours or equivalent	SJ14326 SJD0967 SI33348	77/0 77/0 77/0	
Early Life Failure Rate (ELFR)	B2	AEC-Q100-008, @Tj=150°C for 48 hours, or equivalent	SI33348 SJ04552 SJD0967	800/0 800/0 800/0	

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS					
Test	**#**	**Test Condition**	**Lot# or Date Code**	**Test Results (S.S./Rej)**	**Comment**
Solderability (SD)	C3	JESD22-B102 J-STD-002D >95% lead coverage	1921	15/0	
Physical Dimensions (PD)	C4	JESD22-B100/108 AEC-Q003 C_{PK} >1.67	1921 1941 1946	30/0 30/0 30/0	
Bump Shear Test (BST)	C7	JESD22-B117 AEC-Q003 C_{PK} >1.67 20 bumps/pillars from a minimum of 5 devices	1921	5/0	
TEST GROUP D – DIE FABRICATION RELIABILITY TESTS					
Test	**#**	**Test Condition**	**Lot# or Date Code**	**Test Results (S.S./Rej)**	**Comment**
Electromigration (EM)	D1	JESD61 JP001	—	—	Pass
Time Dependent Dielectric Breakdown (TDDB)	D2	JESD36 JP001	—	—	Pass
Hot Carrier Injection (HCI)	D3	JESD60 and 28 JP001	—	—	Pass
Negative Bias Temperature Instability (NBTI)	D4	JESD90 JP001	—	—	Pass
Stress Migration (SM)	D5	JESD61,87 and 202 JP001	—	—	Pass
TEST GROUP E – ELECTRICAL VERIFICATION TESTS					
Test	**#**	**Test Condition**	**Lot# or Date Code**	**Test Results (S.S./Rej)**	**Comment**
ESD: Human Body Model (HBM)	E2	AEC-Q100-002	SJD1281	3/0	>2000V
ESD: Device Charged Model (CDM)	E3	AEC-Q100-011	SJD1281	3/0	>750V
Latch-up	E4	AEC-Q100-004	SJD1281	6/0	>+/-100mA & >1.5Vccmax

5. Failure Rate Calculation

Sample Size:	4250
Rejects:	0
Activation Energy (eV):	0.7
Equivalent Device Hours:	3.32×10^{8} Hours
Failure Rate (FIT@60%CL):	2.8 FIT
MTBF (years):	41,358 Years

Revision / Update History

Revision	Reason for Change	Date	Rel Engineer
1.0	Initial release	October 2020	Ramon Lei

Appendix: Description of Reliability Test and Failure Rate Calculation

High Temperature Operating Life Test

Purpose: This test is used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices operating condition in an accelerated way. The voltage and temperature are used for acceleration of any potential failures over time.
Condition: Tj=150°C @ Vinmax.
Pass Criteria: All units must pass the min/max limits of the datasheet.

ESD Test

Purpose: The purpose of the ESD test is to guarantee that the device can withstand electrostatic voltages during handling.
Condition: Human Body Model and Charged Device Model.
Pass Criteria: ESD Testing on every pin. The device must be fully functional after testing and pass the min/max limits in the datasheet.

IC Latch-Up Test

Purpose: The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up.
Condition: Voltage and current injection.
Pass criteria: All pins with the exception of "no connect" pins and timing related pins, shall be latch-up tested. The device must be fully functional after testing and pass the min/max limits in the datasheet.

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

Purpose: The purpose of this standard is to identify the classification level of nonhermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.
Condition: Bake + moisture sock + 3X reflow at 260°C.
Pass criteria: All units must pass the min/max limits of the datasheet.

Accelerated Moisture Resistance- Unbiased Autoclave/ Unbiased HAST

Purpose: To check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.
Condition: 121°C/100% RH (Unbiased Autoclave), 130°C/85% RH (Unbiased HAST).
Pass Criteria: All units must pass min/max limits of the datasheet.

Temperature Cycle Test

Purpose: This test is conducted to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high- and low-temperature extremes.
Condition: -65°C to 150°C or other conditions.
Pass Criteria: All units must pass min/max limits of the datasheet.

Temperature Humidity Bias(THB)/Biased Highly Accelerated Stress Test (BHAST)

Purpose: This is to evaluate the reliability in humid environments. Temperature, humidity, and bias conditions are applied to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it check the performance of the device in humid environments.
Condition: 85°C/85%RH(THB), 130°C/85% RH (BHAST), with Vin=Vinmax.
Pass Criteria: All units must pass min/max limits of the datasheet.

Power and Temperature Cycling

Purpose: This test method applies to semiconductor devices that are subjected to temperature excursions and required to power on and off during all temperatures. The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed.

Condition: -40°C to 125°C, or other condition, with Vin=Vinmax.

Pass Criteria: All units must pass min/max limits of the datasheet.

High Temperature Storage Life

Purpose: The test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).

Condition: Bake at 150°C/175°C or other conditions.

Pass Criteria: All units must pass min/max limits of the datasheet.

Failure Rate Calculation

The failure rate is gauged by a Failures-In-Time (FIT) based upon accelerated stress data. The unit for FIT is failure per billion device hour.

$$FIT\ Rate = \frac{(\chi^2/2) \times 10^9}{EDH}$$

Where

$\chi 2$ (Chi-Squared) is the goodness-of-fit test statistic at a specified level of confidence;
EDH= Equivalent Device Hours = AF × (Life test sample size) × (test duration);
AF= Acceleration Factor.

High Temperature Operating Life (HTOL) test is usually done under acceleration of temperature and voltage. The total number of failures from the stress test determines the chi-squared factor.

$$AF=AF_T \times AF_V$$

The Temperature Acceleration Factor AF_T:

$$AF_T = \exp\left(\frac{E_a}{K}\left(\frac{1}{T_{J(use)}} - \frac{1}{T_{J(stress)}}\right)\right)$$

T_{Juse} = Junction temp under typical operating conditions;
$T_{Jstress}$ =Junction temp under accelerated test conditions;
Ea is Activation energy=0.7eV;
K=Boltzmann's constant=8.62×10^{-5} eV/K.

The voltage Acceleration Factor AF_V:

$$AF_V = e^{\beta\times[V_{stress}-V_{use}]}$$

V_{use} = Voltage under typical operating conditions;
V_{stress} = Voltage under accelerated stress test conditions;
β = Voltage acceleration factor (in 1/Volts) and specified by technology.
Note: For calculation in the report, AF_V = 1 for simplicity.

MTBF (Mean Time Between Failure) equals to 10^9/FIT (in hours).