



PRODUCT RELIABILITY REPORT

Product: **MPQ2013AGG-AEC1**
MPQ2013AGG-33-AEC1
MPQ2013AGJE-AEC1
MPQ2013AGJE-5-AEC1
MPQ2013AGJE-25-AEC1
MPQ2013AGJE-33-AEC1
MPQ2013AGQ-AEC1
MPQ2013AGQ-5-AEC1
MPQ2013AGQ-25-AEC1
MPQ2013AGQ-33-AEC1
MPQ2013BGQ-33-AEC1
MPQ2013AGQ-18-AEC1

Reliability Department
Monolithic Power Systems
79 Great Oaks Boulevard
San Jose, CA 95119
Tel: 408-826-0600
Fax: 408-826-0601

1. Device Information

Product:	MPQ2013AGG-AEC1/MPQ2013AGG-33-AEC1/MPQ2013AGJE-AEC1/ MPQ2013AGJE-5-AEC1/MPQ2013AGJE-25-AEC1/MPQ2013AGJE-33- AEC1/MPQ2013AGQ-AEC1/MPQ2013AGQ-5-AEC1/MPQ2013AGQ-25- AEC1/MPQ2013AGQ-33-AEC1/ MPQ2013BGQ-33-AEC1/ MPQ2013AGQ-18-AEC1
Package:	QFN2×2-6, QFN3×3-8 and TSOT-4
Process Technology:	BCD
Report Date:	03/11/2019

2. Summary of Test Results

Test	#	Test Condition	Lot# or Date Code	Test Results (S.S./Rej)	Comment
Temperature, Bias, and Operating Life	B1	JESD22-A108, @+125°C for 1000 hours or equivalent	HP3763 DA43773.1 HP376303	80/0 80/0 80/0	
Early Life Failure Rate (ELFR)	B2	AEC-Q100-008, @ +125°C for 48 hours, or equivalent	HP3763 DA43773.1 HP376303	800/0 800/0 800/0	
ESD: Human Body Model (HBM)	E2	AEC-Q100-002	HP376302	3/0	>2000V
ESD: Machine Model (MM)	E2	AEC-Q100-003	HP376302	3/0	>200V
ESD: Device Charged Model (CDM)	E3	AEC-Q100-011	HP376302	3/0	>750V
Latch-up	E4	AEC-Q100-004	HP376302	6/0	>+/-100mA & >1.5Vccmax
Moisture/Reflow Sensitivity	A1	J-STD-020	1525 1527 1529 1309 1402 1406 1526 1528 1529	300/0 300/0 300/0 300/0 300/0 300/0 300/0 300/0 300/0	QFN2×2-6,MSL=1 QFN2×2-6,MSL=1 QFN2×2-6,MSL=1 QFN3×3-8,MSL=1 QFN3×3-8,MSL=1 QFN3×3-8,MSL=1 TSOT-4,MSL=1 TSOT-4,MSL=1 TSOT-4,MSL=1

Steady State Temperature Humidity Bias Life Test	A2	JESD22-A101, @85°C/85%RH static bias at Vinmax for 1000 hours or equivalent	1525	80/0	QFN2×2-6
			1527	80/0	QFN2×2-6
			1529	80/0	QFN2×2-6
			1331	80/0	QFN3×3-8
			1402	80/0	QFN3×3-8
			1406	80/0	QFN3×3-8
			1526	80/0	TSOT-4
			1528	80/0	TSOT-4
			1529	80/0	TSOT-4
Accelerated Moisture Resistance-Unbiased Autoclave	A3	JESD22-A102, @121°C/100%RH for 168 hours or equivalent	1525	80/0	QFN2×2-6
			1527	80/0	QFN2×2-6
			1529	80/0	QFN2×2-6
			1309	80/0	QFN3×3-8
			1402	80/0	QFN3×3-8
			1406	80/0	QFN3×3-8
			1526	80/0	TSOT-4
			1528	80/0	TSOT-4
			1529	80/0	TSOT-4
Temperature Cycling	A4	JESD22-A104, from -65°C to 150°C for 1000 cycles or equivalent	1525	80/0	QFN2×2-6
			1527	80/0	QFN2×2-6
			1529	80/0	QFN2×2-6
			1309	80/0	QFN3×3-8
			1402	80/0	QFN3×3-8
			1406	80/0	QFN3×3-8
			1526	80/0	TSOT-4
			1528	80/0	TSOT-4
			1529	80/0	TSOT-4
Power Temperature Cycling	A5	JESD22-A105, from -40°C to 125°C for 1000 cycles.	HP376303	45/0	
High Temperature Storage Life	A6	JESD22-A103, @150°C for 1000 hours	1525	50/0	QFN2×2-6
			1527	50/0	QFN2×2-6
			1529	50/0	QFN2×2-6
			1309	50/0	QFN3×3-8
			1402	50/0	QFN3×3-8
			1406	50/0	QFN3×3-8
			1526	50/0	TSOT-4
			1528	50/0	TSOT-4
			1529	50/0	TSOT-4

3. Failure Rate Calculation

Sample Size:	5350
Rejects:	0
Activation Energy (eV):	0.7
Equivalent Device Hours:	4.17×10^8 Hours
Failure Rate (FIT@60%CL):	2.2 FIT
MTBF (years):	52,062 Years

Revision / Update History

<u>Revision</u>	<u>Reason for Change</u>	<u>Date</u>	<u>Rel Engineer</u>
1.0	Initial release	July 2014	Ramon Lei
2.0	Update	February 2015	Ramon Lei
3.0	Update	September 2015	Ramon Lei
4.0	Update	March 2016	Ramon Lei
5.0	Update	June 2017	Ramon Lei
6.0	Update	December 2017	Ramon Lei
7.0	Update	March 2019	Ramon Lei

Appendix: Description of Reliability Test and Failure Rate Calculation

High Temperature Operating Life Test

Purpose: This test is a worst-case life test that checks the integrity of the product. The high temperature testing is use for acceleration of any potential failures over time. The calculation for failure rate (FIT) using the operating ambient temperature is done using the Arrhenius equation.

Condition: 125C @ Vccmax

Pass Criteria: All units must pass the min/max limits of the datasheet.

ESD Test

Purpose: The purpose of the ESD test is to guarantee that the device can withstand electrostatic voltages during handling.

Condition: Human Body Model, Machine Model and Charged Device Model

Pass Criteria: ESD Testing on every pin. The device must be fully functional after testing and pass the min/max limits in the datasheet.

IC Latch-Up Test

Purpose: The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up.

Condition: Voltage and current injection

Pass criteria: All pins with the exception of “no connect” pins and timing related pins, shall be latch-up tested. The device must be fully functional after testing and pass the min/max limits in the datasheet.

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

Purpose: The purpose of this standard is to identify the classification level of nonhermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.

Condition: Bake + moisture sock + 3X reflow at 260C

Pass criteria: All units must pass the min/max limits of the datasheet

Steady State Temperature Humidity Bias Life Test

Purpose: This is to check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 85%RH at 85C with $V_{in}=V_{inmax}$

Pass Criteria: All units must pass min/max limits of the datasheet

Highly Accelerated Temperature and Humidity Stress Test

Purpose: This is an equivalent test to Steady State Temperature Humidity Bias Life test with different (higher) temperature stress condition.

Condition: 85%RH at 130C with $V_{in}=V_{inmax}$

Pass Criteria: All units must pass min/max limits of the datasheet

Accelerated Moisture Resistance- Unbiased Autoclave

Purpose: To check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

Condition: 121C/15psig/100% RH (no bias)

Pass Criteria: All units must pass min/max limits of the datasheet

Temperature Cycle Test

- Purpose:** This test is used to evaluate the die attach integrity and bond integrity. This is similar to the Thermal Shock test, but can generate different failure modes due to the longer dwell time and gradual temperature change.
- Condition:** -65C to 150C
- Pass Criteria:** All units must pass min/max limits of the datasheet

High Temperature Storage Life

- Purpose:** The test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).
- Condition:** Bake at 150C
- Pass Criteria:** All units must pass min/max limits of the datasheet

Failure Rate Calculation

The failure rate is gauged by a Failures-In-Time (FIT) based upon accelerated stress data. The unit for FIT is failure per billion device hour.

$$FIT\ Rate = \frac{(\chi^2/2) \times 10^9}{EDH}$$

Where

χ^2 (Chi-Squared) is the goodness-of-fit test statistic at a specified level of confidence;

EDH= Equivalent Device Hours = AF \times (Life test sample size) \times (test duration);

AF= Acceleration Factor.

High Temperature Operating Life (HTOL) test is usually done under acceleration of temperature and voltage. The total number of failures from the stress test determines the chi-squared factor.

$$AF = AF_T \times AF_V$$

The Temperature Acceleration Factor AF_T :

$$AF_T = \exp\left(\frac{E_a}{K} \left(\frac{1}{T_{J(Use)}} - \frac{1}{T_{J(stress)}} \right)\right)$$

$T_{J(Use)}$ = Junction temp under typical operating conditions;

$T_{J(stress)}$ = Junction temp under accelerated test conditions;

E_a is Activation energy=0.7eV;

K =Boltzmann's constant= 8.62×10^{-5} eV/K.

The voltage Acceleration Factor AF_V :

$$AF_V = e^{\beta \times [V_{stress} - V_{use}]}$$

V_{use} = Gate voltage under typical operating conditions;

V_{stress} = Gate voltage under accelerated test conditions;

β = Voltage acceleration factor (in 1/Volts) and specified by technology.

Note: For calculation in the report, $AF_V = 1$ for simplicity.

MTBF (Mean Time Between Failure) equals to $10^9/FIT$ (in hours).