# PRODUCT RELIABILITY REPORT

## Product: MPC22164

**Reliability Department**
**Monolithic Power Systems**
**79 Great Oaks Boulevard**
**San Jose, CA 95119**
**Tel: 408-826-0600**
**Fax: 408-826-0601**

Monolithic Power Systems, Inc.

# 1. Device Information

| | |
|---|---|
| Product: | MPC22164 |
| Report Date: | 11/17/2022 |

# 2. Summary of Test Results

| Test | Test Condition | Lot# or Date Code | Test Results (S.S./Rej) | Comment |
|---|---|---|---|---|
| Solder Attachment | IPC9701, -40°C to 125°C, dwell time=15mins, ramp time=15mins, 1hour/cycle, for 1000 cycles.<br>12 layer board.<br>• 1oz for top/2/3/4 layer.<br>• 2oz for 5/6/7/8 layer.<br>• 1oz for 9/10/11/bottom layer. | N23E113.8Y<br>N23E113.8X<br>N53R068.8Q | 15/0<br>15/0<br>15/0 | |
| Temperature, Bias, and Operating Life | JESD22-A108, @+125°C for 1000 hours | N23E113.8Y<br>N23E113.8X<br>N53R068.8Q | 40/0<br>40/0<br>40/0 | |
| Power Temperature Cycling | IPC9592, from -40°C to 125°C for 1000 cycles. | N23E113.8Y<br>N23E113.8X<br>N53R068.8Q | 15/0<br>15/0<br>15/0 | |
| Electrostatic Discharge Human Body Model (HBM) | ANSI/ESDA/JEDEC JS-001 | N43N559.8A | 3/0 | >2000V |
| Electrostatic Discharge Charged Device Model (CDM) | ANSI/ESDA/JEDEC JS-002 | N43N559.8A | 3/0 | >750V |
| Latch-up (LU) | EIA/JESD78 | N43N559.8A | 6/0 | >+/-100mA & >1.5Vccmax |
| Moisture/Reflow Sensitivity, prior to HTSL, LTSL, TC and THB | J-STD-020 | 2145<br>2148<br>2151 | 36/0<br>36/0<br>36/0 | MSL = 3 |
| High Temperature Storage Life | JESD22-A103, @150°C for 1000 hours | 2145<br>2148<br>2151 | 3/0<br>3/0<br>3/0 | |
| Low Temperature Storage Life | JESD22-A119, @-65°C for 1000 hours | 2145<br>2148<br>2151 | 3/0<br>3/0<br>3/0 | |

| | | | | |
|---|---|---|---|---|
| Temperature Cycling | IPC9592, -40°C to 125°C, dwell time=15mins, ramp time=15mins, 1hour/cycle, for 2000 cycles. | 2145<br>2148<br>2151 | 15/0<br>15/0<br>15/0 | |
| Steady State Temperature Humidity Bias Life Test | IPC9592, @85°C/85%RH static bias at Vinmax for 1000 hours | 2145<br>2148<br>2151 | 15/0<br>15/0<br>15/0 | |

## 3. Failure Rate Calculation

Failure Rate (FIT@60%CL): 7.2 FIT
MTBF (years): 15,854 Years

**Revision / Update History**

| Revision | Reason for Change | Date | Rel Engineer |
|---|---|---|---|
| 1.0 | Initial release | November 2022 | Ramon Lei |

## Appendix: Description of Reliability Test and Failure Rate Calculation

**High Temperature Operating Life Test**

**Purpose:** This test is a worst-case life test that checks the integrity of the product. The high temperature testing is for acceleration of any potential failures over time. The calculation for failure rate (FIT) is completed using the Arrhenius equation.
**Condition:** 125°C @ Vinmax
**Pass Criteria:** All units must pass the min/max limits of the datasheet.

**Power Temperature Cycle Test**

**Purpose:** This test is used to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed. It is intended to simulate worst case conditions encountered in typical applications.
**Condition:** -45°C to 125°C
**Pass Criteria:** All units must pass min/max limits of the datasheet

**ESD Test**

**Purpose:** The purpose of the ESD test is to guarantee that the device can withstand electrostatic voltages during handling.
**Condition:** Human Body Model and Charged Device Model
**Pass Criteria:** ESD Testing on every pin. The device must be fully functional after testing and pass the min/max limits in the datasheet.

**IC Latch-Up Test**

**Purpose:** The purpose of this specification is to establish a method for determining IC latch-up characteristics and to define latch-up failure criteria. Latch-up characteristics are extremely important in determining product reliability and minimizing No Trouble Found (NTF) and Electrical Overstress (EOS) failures due to latch-up.
**Condition:** Voltage and current injection
**Pass criteria:** All pins with the exception of "no connect" pins and timing related pins, shall be latch-up tested. The device must be fully functional after testing and pass the min/max limits in the datasheet.

**Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices**

**Purpose:** The purpose of this standard is to identify the classification level of nonhermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.
**Condition:** Bake + moisture sock + 3X reflow at 260°C
**Pass criteria:** All units must pass the min/max limits of the datasheet

**High Temperature Storage Life**

**Purpose:** The test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).
**Condition:** Bake at 150°C
**Pass Criteria:** All units must pass min/max limits of the datasheet

**Low Temperature Storage Life**

**Purpose:** The test is typically used to determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms and time-to-failure distributions of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms).
**Condition:** Bake at -65°C
**Pass Criteria:** All units must pass min/max limits of the datasheet

**Temperature Cycle Test**

**Purpose:** This test is used to evaluate the die attach integrity and bond integrity. This is similar to the Thermal Shock test, but can generate different failure modes due to the longer dwell time and gradual temperature change.

**Condition:** -45°C to 125°C

**Pass Criteria:** All units must pass min/max limits of the datasheet

**Steady State Temperature Humidity Bias Life Test**

**Purpose:** This is to check the performance of the device in humid environments. This test checks the integrity of the passivation, poor metal to plastic seal and contamination level during assembly and material compatibility.

**Condition:** 85%RH at 85°C with Vin=Vinmax

**Pass Criteria:** All units must pass min/max limits of the datasheet

**Failure Rate Calculation**

The failure rate is gauged by a Failures-In-Time (FIT) based upon accelerated stress data. The unit for FIT is failure per billion device hour.

$$FIT\ Rate = \frac{(\chi^2/2) \times 10^9}{EDH}$$

Where

$\chi 2$ (Chi-Squared) is the goodness-of-fit test statistic at a specified level of confidence;
EDH= Equivalent Device Hours = AF × (Life test sample size) × (test duration);
AF= Acceleration Factor.

High Temperature Operating Life (HTOL) test is usually done under acceleration of temperature and voltage. The total number of failures from the stress test determines the chi-squared factor.

$$AF=AF_T \times AF_V$$

The Temperature Acceleration Factor $AF_T$:

$$AF_T = \exp\left(\frac{E_a}{K}\left(\frac{1}{T_{J(use)}} - \frac{1}{T_{J(stress)}}\right)\right)$$

$T_{Juse}$ = Junction temp under typical operating conditions;
$T_{Jstress}$ =Junction temp under accelerated test conditions;
Ea is Activation energy=0.7eV;
K=Boltzmann's constant=$8.62\times10^{-5}$ eV/K.

The voltage Acceleration Factor $AF_V$:

$$AF_V = e^{\beta \times [V_{stress} - V_{use}]}$$

$V_{use}$ = Gate voltage under typical operating conditions;
$V_{stress}$ = Gate voltage under accelerated test conditions;
β = Voltage acceleration factor (in 1/Volts) and specified by technology.
Note: For calculation in the report, $AF_V$ = 1 for simplicity.

MTBF (Mean Time Between Failure) equals to $10^9$/FIT (in hours).