MP2731 USB PD Reference Design

4.5A, NVDC Single-Cell Charger with OTG

Contents

1 Overview

1.1 Description

The MP2731 USB power delivery (PD) reference design provides a complete solution for USB PD applications that comply with USB PD3.0 specifications. The major components of this reference design include the MP2731 — a 4.5A, narrow voltage DC (NVDC) single-cell Li-ion battery charger — and a CCG3PA (USB PD controller).

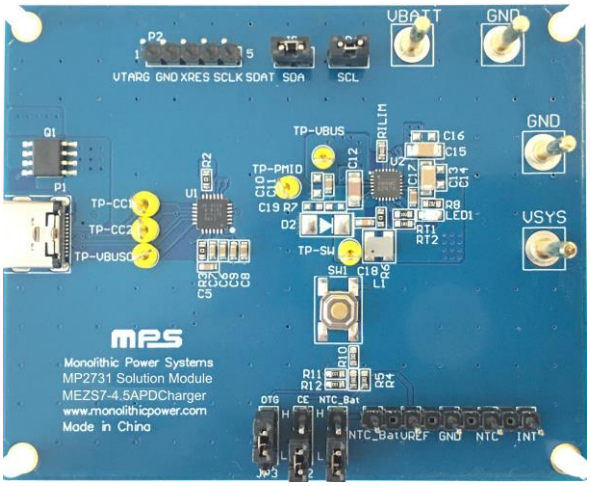
The reference design offers a bidirectional DRP Type-C port. When a USB input is present, the port functions as an upstream-facing port (UFP) to charge the battery. When a USB PD sink is connected to the Type-C port, the reference design functions as a downstream-facing port (DFP), and can provide a 5V USB On-the-Go (OTG) for the sink device. This reference design provides NVDC architecture with power path management functionality, which makes the solution well-suited for smartphones, tablets, and various portable charging applications.

1.2 Features

- 5V to 16V Operating Input Voltage Range Supporting Common Fixed PDO Voltages
- Up to 22V Maximum Sustainable Voltage
- High-Efficiency, 4.5A, 1.35MHz Buck Charger
- Support USB PD 3.0 and BC 1.2 Protocols
- USB On-the-Go (OTG) Function to Power USB Port from Battery Power
- Up to 9A Battery Discharge Current
- Narrow Voltage DC (NVDC) Power Path Management Functionality
- I²C Interface for Configurable System Parameter Settings
- High-Accuracy: ±0.5% Charge Voltage Regulation, ±5% Charge Current Regulation
- Configurable JEITA Thresholds for Battery Temperature Protection
- Provide Thermal Regulation Loop and Thermal Shutdown Protection
- Input and System Over-Voltage Protection (OVP)

1.3 Applications

- Tablets
- Smartphones
- Mobile Devices



(LxWxH) 7.8cmx6.3cmx1.3cm

Figure 1: Solution Module

High Voltage

Warning: Although this board is designed to satisfy safety requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

2 Reference Design

2.1 Block Diagram

The MP2731 USB PD reference design offers a cost-effective solution to achieve up to 18W PD fast charging by pairing a highly integrated MP2731 charger with a universal PD controller (CCG3A). A universally available Type-C connector on the board serves as a bidirectional input. The back-to-back input FET configuration is optional because the MP2731 also provides an internal input-blocking FET, which helps to further reduce PCB size and BOM cost (see Figure 2).

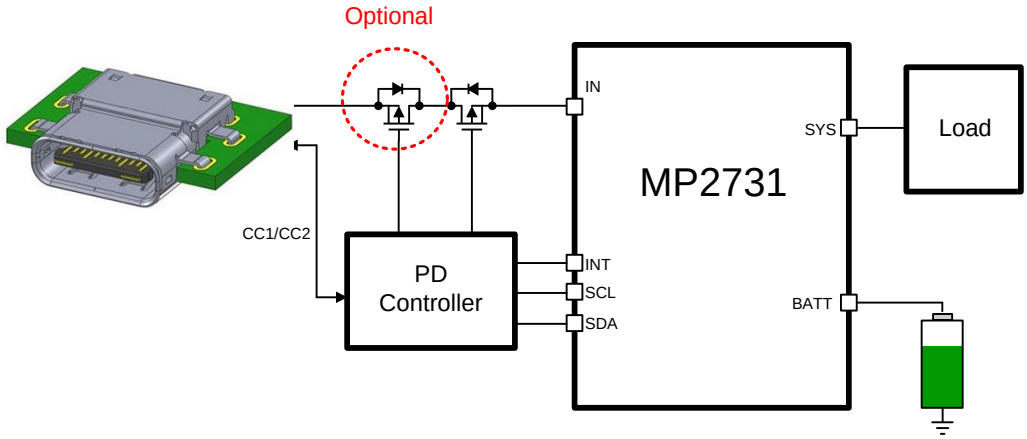


Figure 2: MP2731 USB PD Charger System Block Diagram

2.2 Related Solutions

This reference design is based on the following MPS solution:

Table 1: System Specifications

MPS Integrated Circuit	Description
MP2731GQC-0000	4.5A, NVDC single-cell charger with USB On-the-Go (OTG)

2.3 System Specifications

Table 2: System Specifications

Parameter	Specification
Input voltage range	5 to 16V
Charge-full voltage	4.2V, I²C-configurable
Charge current	3.0A, I²C-configurable
Input voltage regulation	4.6V, I²C-configurable
Input current regulation	0.5A, I²C-configurable
OTG voltage regulation	5.1V, I²C-configurable
OTG current limit	2.4A, I²C-configurable
Board form factor	78mmx63mmx12mm
Efficiency	>90%

3 Design

3.1 Parameter Design

The MP2731 is a 4.5A, highly integrated, switch-mode battery charger with NVDC power path management for a single-cell Li-ion or Li-polymer battery.

3.1.1 Inductor Selection

Inductor selection is a tradeoff between cost, size, and efficiency. From a practical standpoint, the inductor ripple current should not exceed 30% of the maximum load current under the worst-case conditions. The maximum inductor current ripple occurs when V_{BATT} is below V_{SYS_MIN}. The inductance can be estimated with Equation (1):

$$L=\frac{V_{IN}-V_{SYS}}{\Delta I_{L\_MAX}}\frac{V_{SYS}}{V_{IN}\times f_{SW}(MHz)}(\mu H) \quad (1)$$

Where V_{IN} is the input voltage, V_{SYS} is the system voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum inductor ripple current, which is about 30% of the constant current (CC) charge current.

The peak current can be calculated with Equation (2):

$$I_{PEAK}=I_{LOAD(MAX)}\times(1+\frac{\%ripple}{2})(A) \quad (2)$$

The MP2731 has a maximum charge current of 4.5A, but it is important to note that the actual charge current cannot reach this value due to the input current limit. For most applications, the maximum inductor current ripple is set to 0.5A with a 5V input voltage, which corresponds with a 1.5µH inductor. For applications that are a smaller size, select a 1.0µH inductor with a low DC resistance to optimize efficiency.

3.1.2 Input Capacitor Selection

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended, but tantalum or low-ESR electrolytic capacitors can be sufficient.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be calculated with Equation (3):

$$I_{CIN}=I_{LOAD}\times\sqrt{\frac{V_{SYS}}{V_{IN}}\times\left(1-\frac{V_{SYS}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{SYS}$, where $I_{CIN} = I_{SYS} / 2$. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

For the MP2731, the connection between PMID and GND forms the RMS current in the input capacitor. Place a small (e.g. 10µF), high-quality ceramic capacitor as close to the IC as possible between PMID and PGND. Place the remaining capacitor between VIN and GND.

When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input.

3.1.3 System Capacitor Selection

Select a ceramic capacitor with a lower ESR to ignore the equivalent series resistance (ESR) of the output capacitor.

The output voltage ripple can be estimated with Equation (4):

$$\Delta r = \frac{\Delta V_{SYS}}{V_{SYS}} = \frac{1-\frac{V_{SYS}}{V_{IN}}}{8\times C_{SYS}\times f_{SW}{}^{2}\times L}\% \quad (4)$$

To guarantee the ±0.5% system voltage accuracy, the maximum output voltage ripple must not exceed 0.5% (e.g. 0.1%). The maximum output voltage ripple occurs at the minimum system voltage and the maximum input voltage.

If V_{IN} = 5V, V_{SYS} = 3.7V, L = 1µH, f_{SW} = 1.35MHz, and Δr = 0.1%, the output capacitor can be calculated with Equation (5):

$$C_{SYS} = \frac{1-\frac{V_{SYS}}{V_{IN}}}{8\times f_{SW}{}^{2}\times L\times \Delta r} \quad (5)$$

In this example, it is recommended to choose a 22µF ceramic capacitor.

3.1.4 NTC Resistor Selection

Figure 3 shows an external resistor divider reference circuit that limits the low temperature threshold and high temperature threshold at V_{COLD} and V_{HOT}, respectively.

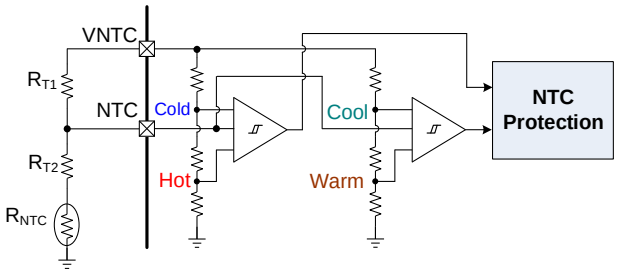


Figure 3: NTC Protection Circuit

For a given NTC thermistor, select R_{T2} and R_{T1} to set the NTC window. R_{T2} and R_{T1} can be calculated with Equation (6) and Equation (7), respectively:

$$R_{T2} = \frac{R_{NTC\_HOT}\times V_{COLD}\times(1\text{-}V_{HOT})\text{-}R_{NTC\_COLD}\times V_{HOT}\times(1-V_{COLD})}{V_{HOT}-V_{COLD}} \quad (6)$$

$$R_{T1} = \frac{(1\text{-}V_{COLD})\times(R_{NTC\_COLD}+R_{T2})}{V_{COLD}} \quad (7)$$

Where R_{NTC_HOT} is the value of the NTC resistor at the high temperature of the required temperature operation range, and R_{NTC_COLD} is the value of the NTC resistor at the low temperature.

The two resistors (R_{T1} and R_{T2}) allow the high temperature limit and low temperature limit to be configured independently. With this feature, the MP2731 can be used with most types of NTC resistors, as well as different temperature operation range requirements.

The R_{T1} and R_{T2} values depend on the type of the NTC resistor.

For example, a 103AT thermistor has the following electrical characteristics:

- At 0°C, R_{NTC_COLD} = 27.28kΩ
- At 60°C, R_{NTC_HOT} = 3.02kΩ

According to Equation (6) and (7) and the V_{HOT} and V_{COLD} values from the MP2731's datasheet, R_{T1} = 11.8kΩ and R_{T2} = 3.06kΩ.

In this solution board, R_{T1} and R_{T2} are fixed at 10kΩ. JP1 can be pulled to GND to set a fixed 50% NTC divider ratio. To connect a real NTC thermistor to the system, pull JP1 to NTC_Bat. If a real NTC thermistor is connected, the values of R_{T1} and R_{T2} should be recalculated with Equation (6) and Equation (7).

3.2 Schematic

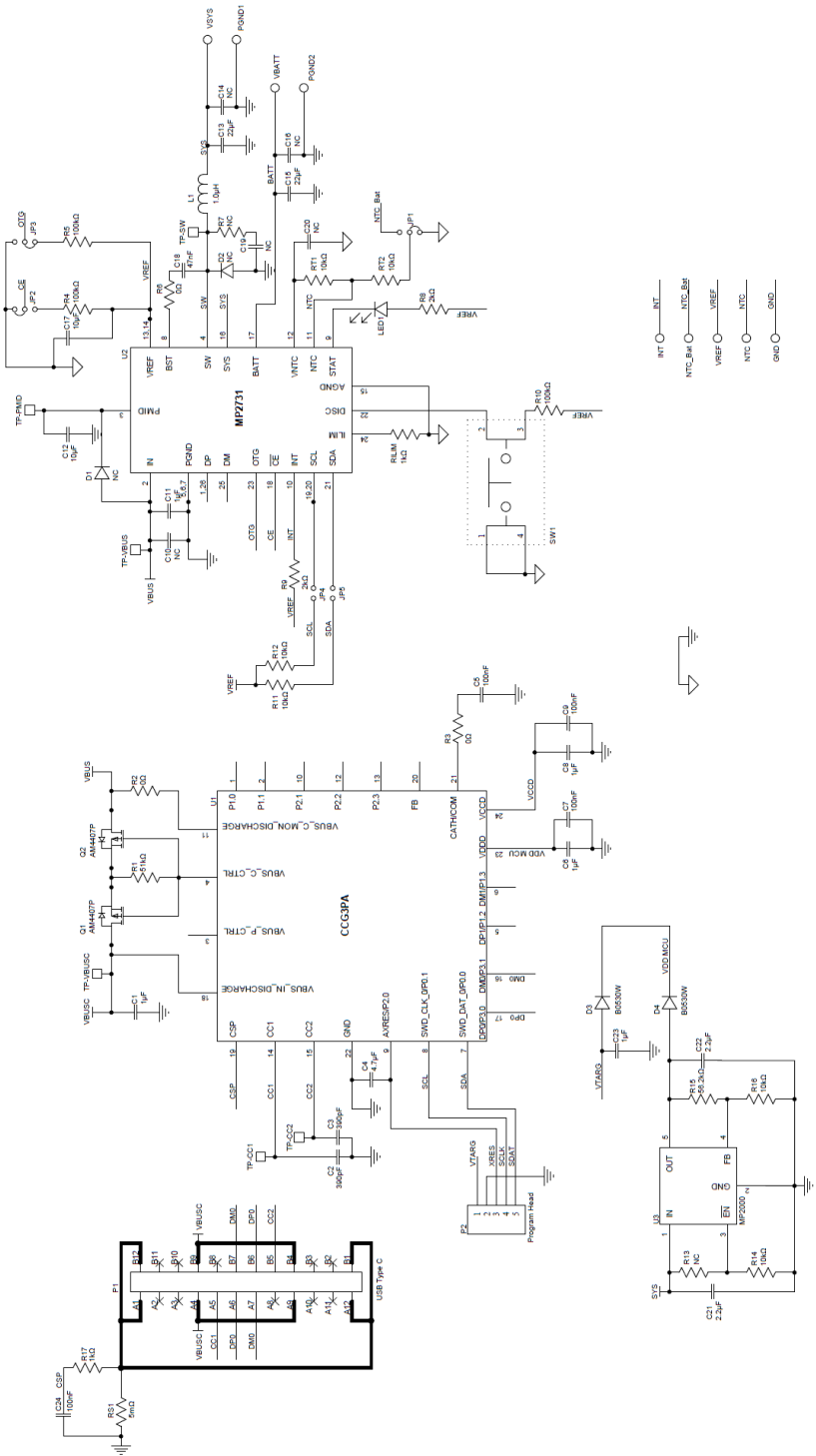


Figure 4: USB PD Charger with the MP2731

3.3 BOM

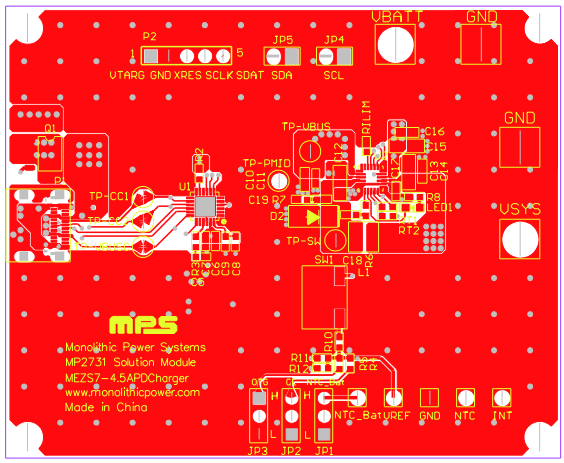
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
1	C1	1μF	Ceramic capacitor, 50V, X7R, 0805	0805	Murata	GRM21BR71H105KA12L
2	C2, C3	390pF	Ceramic capacitor, 50V, C0G, 0603	0603	Murata	GRM1885C1H391JA01D
1	C4	4.7μF	Ceramic capacitor, 25V, X5R, 0805	0805	Murata	GRM21BR61E475KA12L
4	C5, C7, C9, C24	100nF	Ceramic capacitor, 16V, X7R, 0603	0603	Murata	GRM188R71C104KA01D
4	C6, C8, C11, C23	1μF	Ceramic capacitor, 25V, X7R, 0603	0603	Murata	GRM188R71E105KA12D
1	C10	NC	Ceramic capacitor, 50V, X5R, 1206	1206	Murata	
1	C12	10μF	Ceramic capacitor, 50V, X5R, 1206	1206	Murata	GRM31CR61H106KA12L
2	C13, C15	22μF	Ceramic capacitor, 16V, X5R, 1206	1206	Murata	GRM31CR61C226KE15L
2	C14, C16	NC	Ceramic capacitor, 16V, X5R, 0805	0805	Murata	
1	C17	10μF	Ceramic capacitor, 16V, X5R, 0603	0603	Murata	GRM188R61C106KAALD
1	C18	47nF	Ceramic capacitor, 50V, X7R, 0603	0603	Murata	GRM188R71H473KA61D
2	C19, C20	NC	Ceramic capacitor, 16V, X5R, 0603	0603	Murata	
2	C21, C22	2.2μF	Ceramic capacitor, 10V, X7R, 0603	0603	Murata	GRM188R71A225KE15D
2	D1, D2	NC	Diode, 50V, 3A	SMA	Any	
2	D3, D4	B0530W	Schottky diode, 30V, 0.5A	SOD-123	Diodes Inc.	B0530W
1	L1	1.0μH	Inductor, 1.0μH	SMD	Cyntec	HTEP32251B-1R0MIR-89
1	LED1	Red	Red LED	0805	Bright LED	BL-HUF35A-TRB
1	R1	51kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0751KL
3	R2, R3, R6	0Ω	Film resistor, 1%	0603	Yageo	RC0603FR-070RL
3	R4, R5, R10	100kΩ	Film resistor, 5%	0603	Yageo	RC0603JR-07100KL
2	R7, R13	NC	Film resistor, 1%	0603	Yageo	
2	R8, R9	2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-072KL
6	R11, R12, R14, R16, RT1, RT2	10kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0710KL
1	R15	56.2kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-0756K2L
2	R17, RILIM	1kΩ	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
1	RS1	5mΩ	Film resistor, 1%	1206	Yageo	PA1206FRF070R005L
2	Q1, Q2	AM4407P	P-channel MOSFET, -30V, 15A	SO-8	Analog Power	AM4407P

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
4	INT, NTC, NTC_BAT, VREF		2.54mm connector			
3	JP1, JP2, JP3		2.54mm connector			
2	JP4, JP5		2.54mm connector			
5	JP1, JP2, JP3, JP4, JP5		2.54mm connector, shorter			
1	SW1	Push button	Button, SM 4mmx10mm, 1.5mm height			
1	P1	Type-C	Type-C receptacle	DIP	JAE	DX07S024JJ2R1300
1	P2		5-pin header,			
4	VBATT, VSYS, PGND, PGND		2mm			
6	TP-CC1, TP-CC2, TP-PMID, TP-SW, TP-VBUS, TP-VBUSC		Test point			
1	U1	CCG3PA	USB Type-C PD controller	QFN-24 (4mmx 4mm)	Cypress	CYPD3171-24LQXQ
1	U2	MP2731	4.5A, I^2C-controlled SW charger	QFN-26 (3.5mmx 3.5mm)	MPS	MP2731GQC-0000
1	U3	MP2000	Low input voltage, 150mA linear regulator	SOT23-5	MPS	MP2000DJ-ADJ

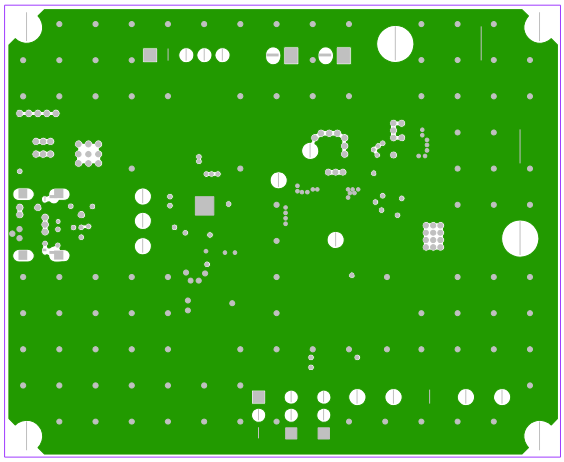
3.4 PCB Layout

PCB layout is critical for stable operation. For the best results when designing the general switching design, refer to Figure 5 and follow the guidelines below:

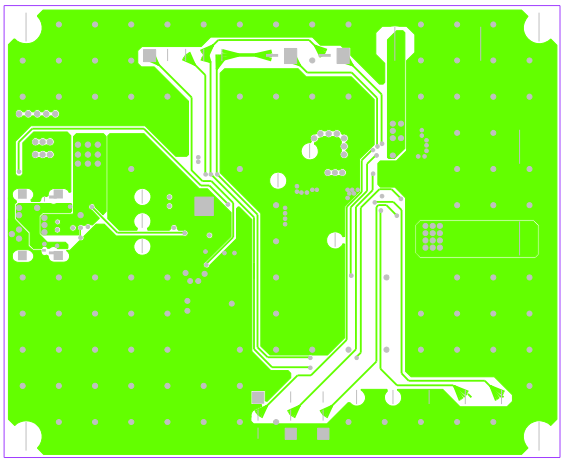
1. Route the power stage adjacent to PGND.
2. Minimize the high-side switching node (e.g. SW and inductor) trace lengths in the high-current path.
3. Keep the switching node short, and route it away from all small control signals.
4. Place the input capacitor as close as possible to the PMID and PGND pins.
5. Place the output inductor close to the IC, and connect the output capacitor between the inductor and PGND of the IC.
6. For high-current applications, the pins for the power pads (IN, SW, SYS, BATT, and PGND) should be connected to as much copper on the board as possible. This improves thermal performance because the board conducts heat away from the IC.
7. Place via holes inside the PGND pads for the IC if applicable.
8. It is recommended to use a star ground design to keep the circuit block currents (high-power/low-power, small signal) isolated. This reduces noise coupling and ground bounce events. It is recommended to use a single ground plane for this design. With a small layout and a single ground plane, ground bounces events are mitigated. Segregating the components minimizes coupling between signals and stability requirements.
9. Pull the connection wire from the MCU (I^2C) far from the SW node and copper areas.



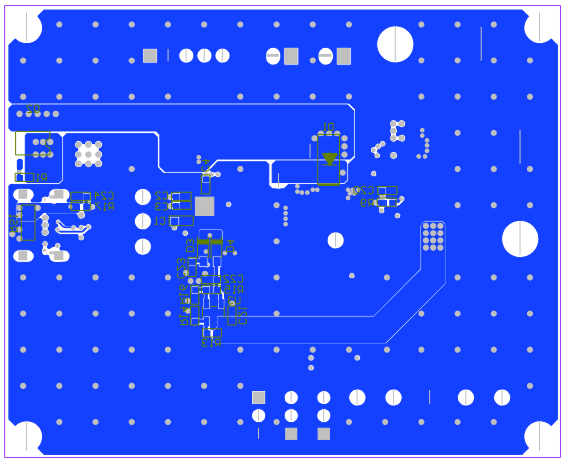
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

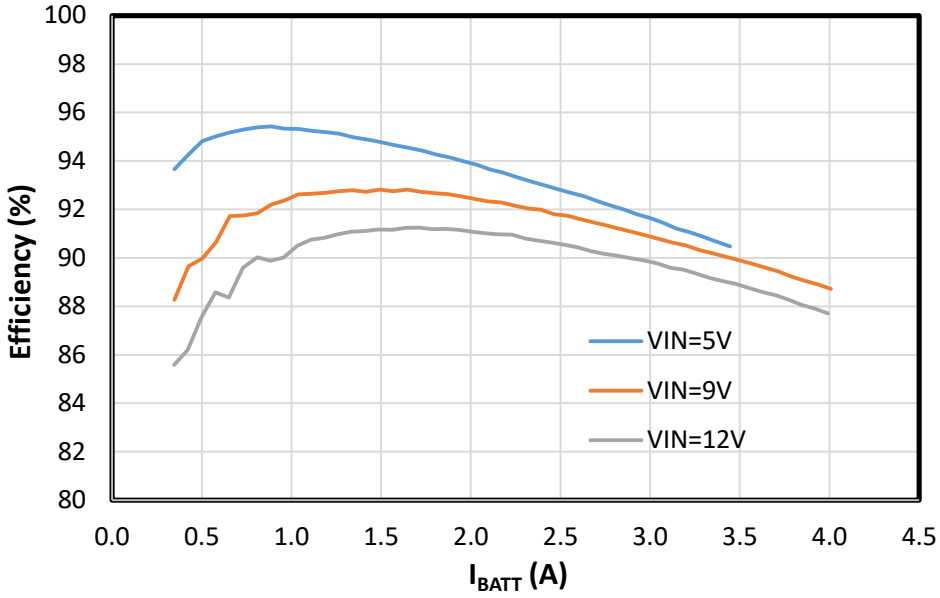
Figure 5: Recommended PCB Layout

4 Test Results

4.1 Charge Efficiency

Efficiency vs. Charge Current

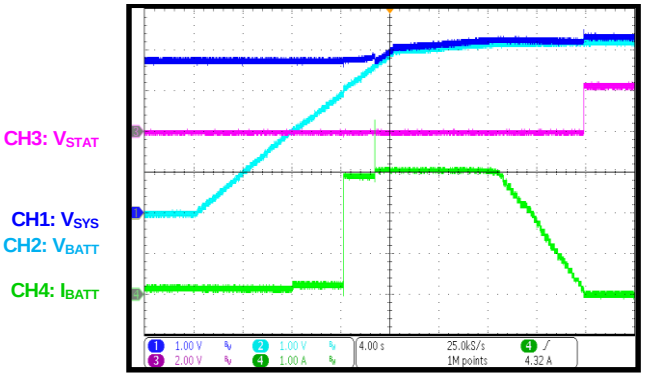
V_{IN} = 5V, 9V, or 12V, V_{BATT} = 3.8V, R_{L_DCR} = 21mΩ, not including the external blocking FET (Q1, Q2)



4.2 Time Domain Waveforms

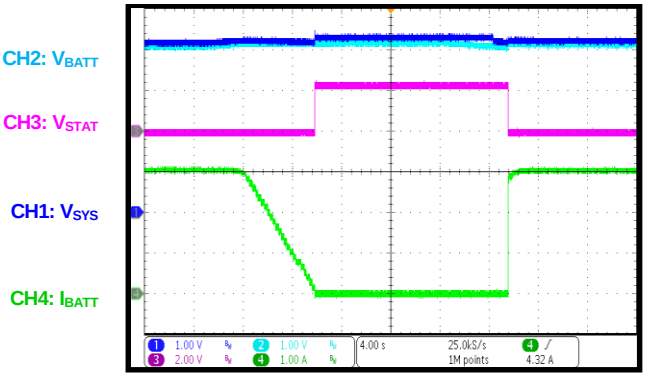
Battery Charge Curve

V_{IN} = 9V, I_{IN_LIM} = 2A, V_{BATT_REG} = 4.2V, I_{SYS} = 0A



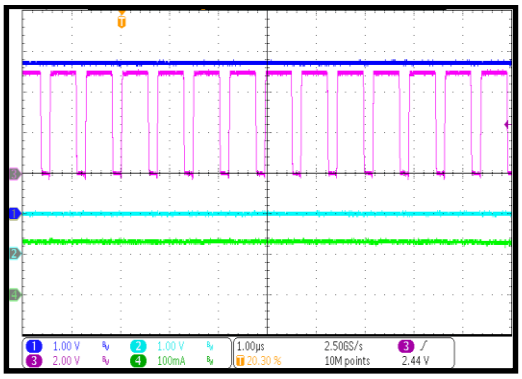
Auto-Recharge

V_{IN} = 9V, I_{IN_LIM} = 2A, V_{BATT_REG} = 4.2V, I_{SYS} = 0A



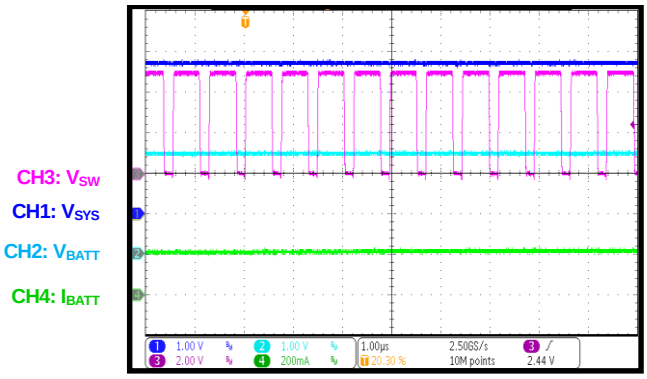
Trickle Charge

V_{IN} = 5V, V_{BATT} = 1.0V, I_{SYS} = 500mA



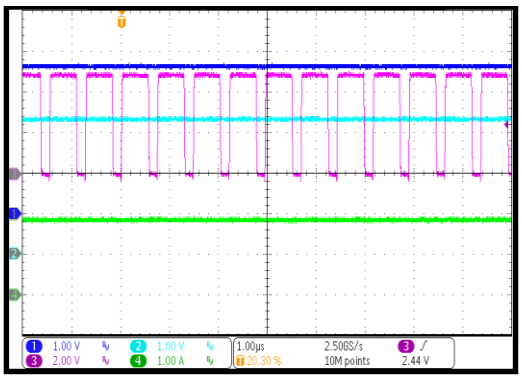
Pre-Charge

V_{IN} = 5V, V_{BATT} = 2.5V, I_{SYS} = 500mA



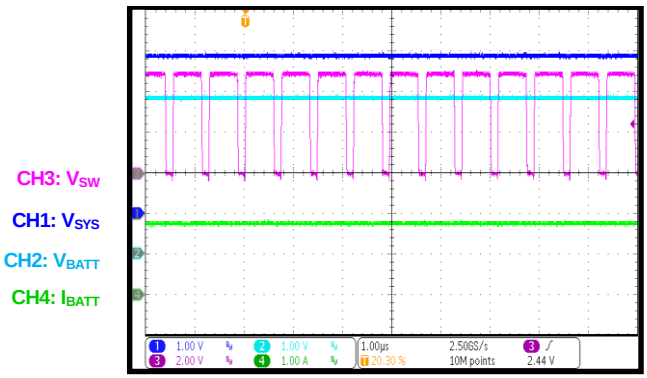
Constant Current Charge

V_{IN} = 5V, I_{IN_LIM} = 1.5A, V_{BATT} = 3.3V, I_{CC} = 3A



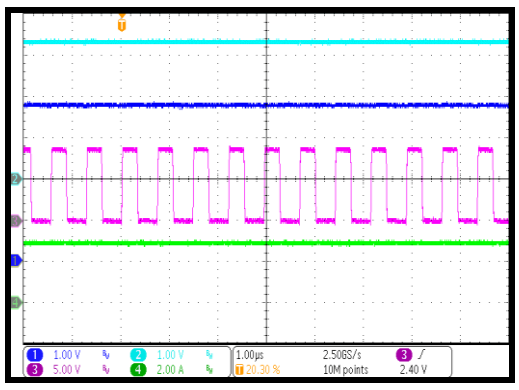
Constant Current Charge

V_{IN} = 5V, I_{IN_LIM} = 1.5A, V_{BATT} = 3.8V, I_{CC} = 3A



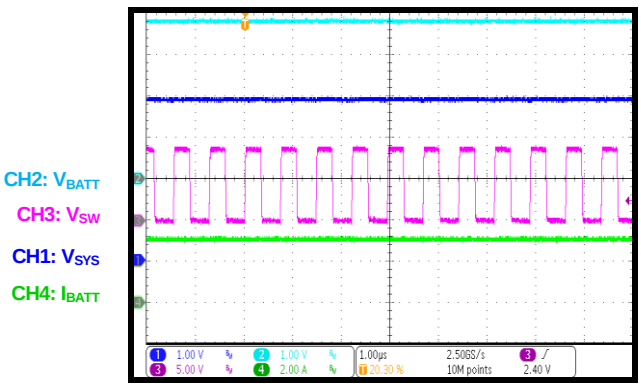
Constant Current Charge

V_{IN} = 9V, I_{IN_LIM} = 2A, V_{BATT} = 3.3V, I_{CC} = 3A



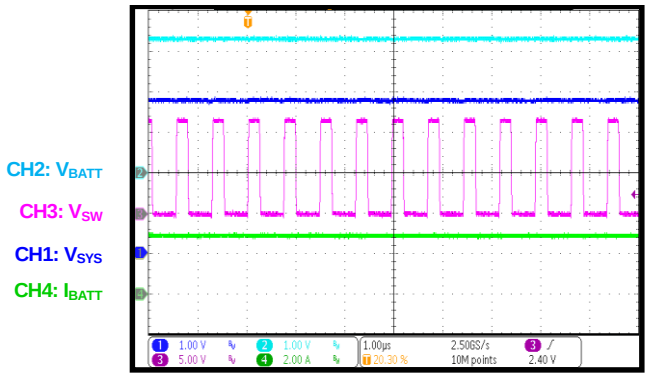
Constant Current Charge

V_{IN} = 9V, I_{IN_LIM} = 2A, V_{BATT} = 3.8V, I_{CC} = 3A



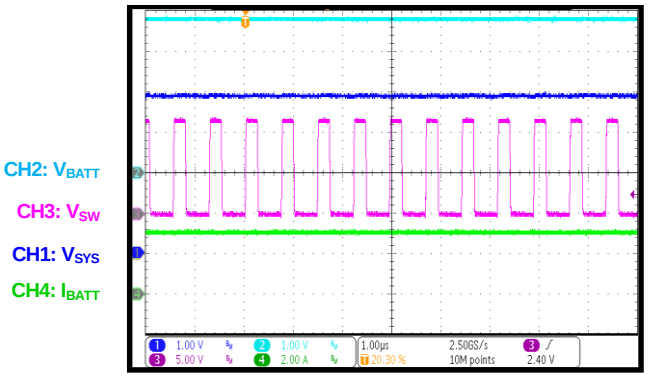
Constant Current Charge

V_{IN} = 12V, I_{IN_LIM} = 2A, V_{BATT} = 3.3V, I_{CC} = 3A



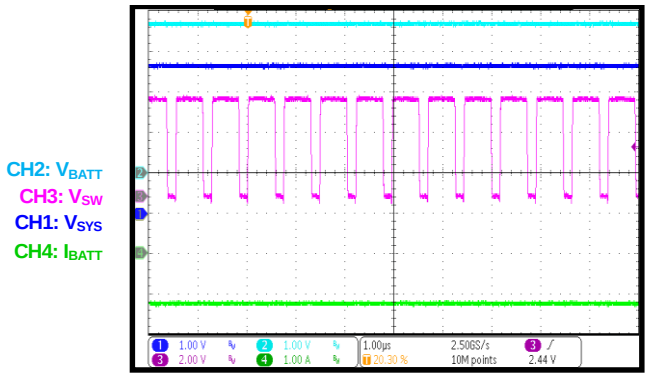
Constant Current Charge

V_{IN} = 12V, I_{IN_LIM} = 2A, V_{BATT} = 3.8V, I_{CC} = 3A



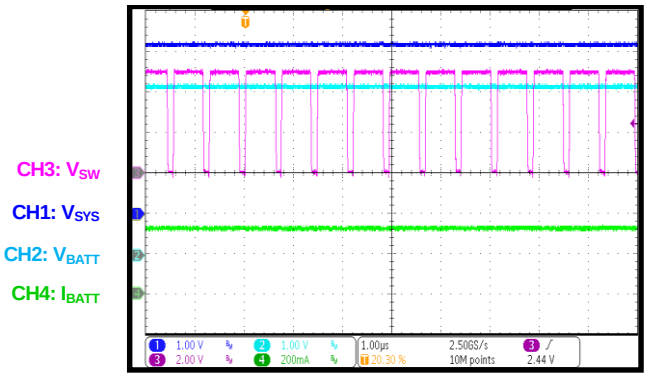
Battery Supplement Mode

V_{IN} = 5V, I_{IN_LIM} = 1.5A, V_{BATT} = 3.8V, I_{SYS} = 3A



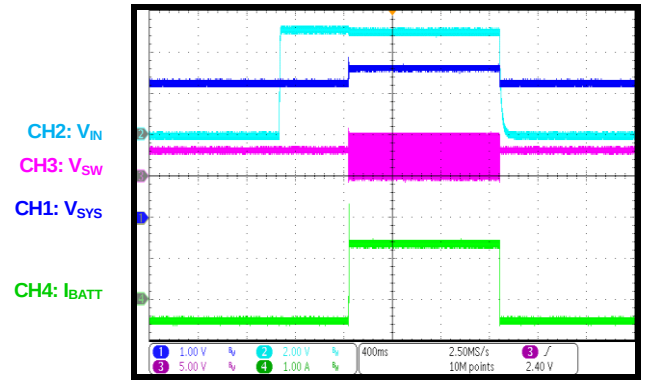
Constant Voltage Charge

V_{IN} = 5V, I_{IN_LIM} = 1.5A, V_{BATT} = 4.19V, I_{SYS} = 0A



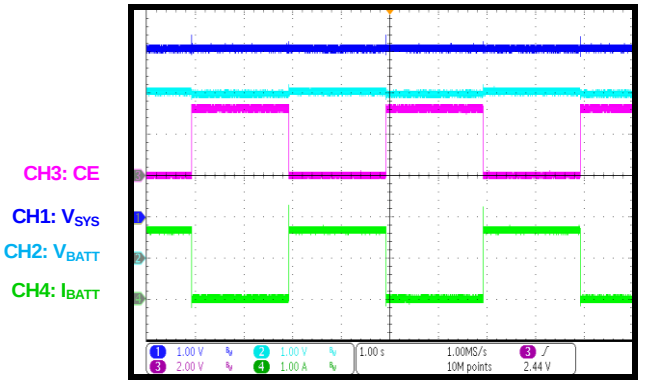
Start-Up/Shutdown Waveform

V_{IN} = 5V, I_{IN_LIM} = 1.5A, V_{BATT} = 3.3V, I_{SYS} = 0.5A



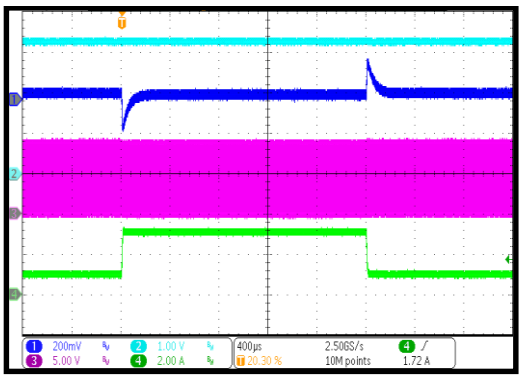
Charge On/Off

V_{IN} = 5V, I_{IN_LIM} = 1.5A, V_{BATT} = 4.0V, I_{SYS} = 0A



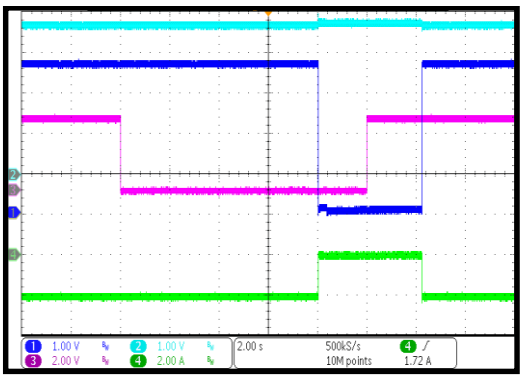
SYS Load Transient

V_{IN} = 9V, V_{BATT} = 3.3V, charging disabled, I_{SYS} = 1A to 3A



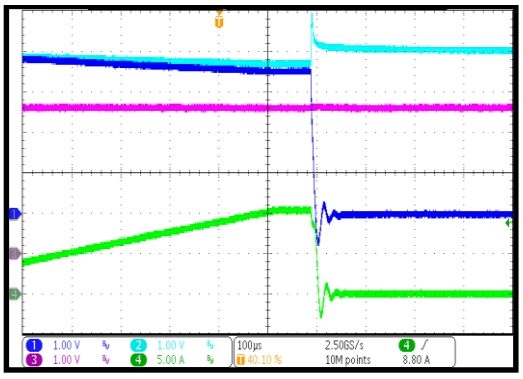
System Reset Mode

VIN floating, V_{BATT} = 3.8V, I_{SYS} = 2A



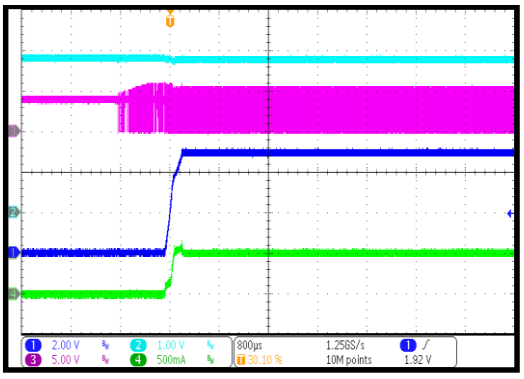
Battery Discharge Current

VIN floating, V_{BATT} = 4.0V, I_{SYS} = up to 10A



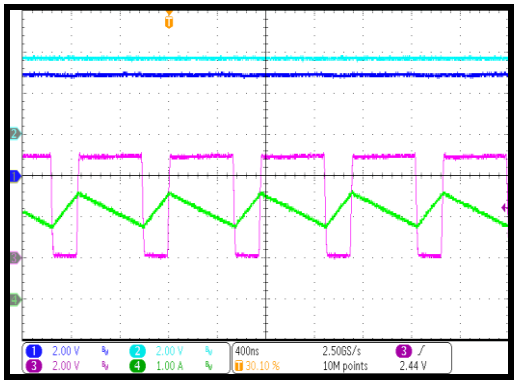
OTG Mode On

VIN floating, OTG mode, V_{BATT} = 3.8V, I_{IN_DSCHG} = 2.4A, I_{OTG} = 0.5A



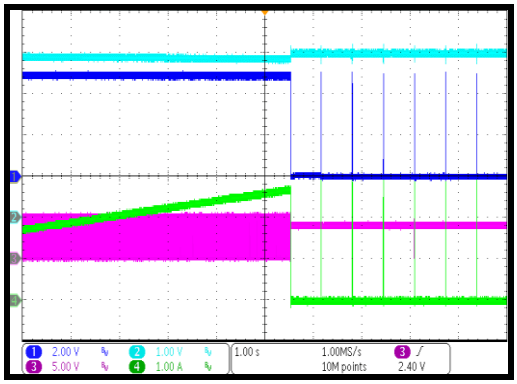
OTG Steady State Operation

VIN floating, OTG mode, V_{BATT} = 3.8V, I_{IN_DSCHG} = 2.4A, I_{OTG} = 1.5A



OTG Voltage Regulation

VIN floating, OTG mode, V_{BATT} = 4.0V, I_{IN_DSCHG} = 2.4A, I_{OTG} = 0-2.4A



4.3 Thermal Measurements

Conditions: V_{IN} = 12V, V_{BATT} = 3.8V, I_{BATT} = 3A, T_A = 24°C.

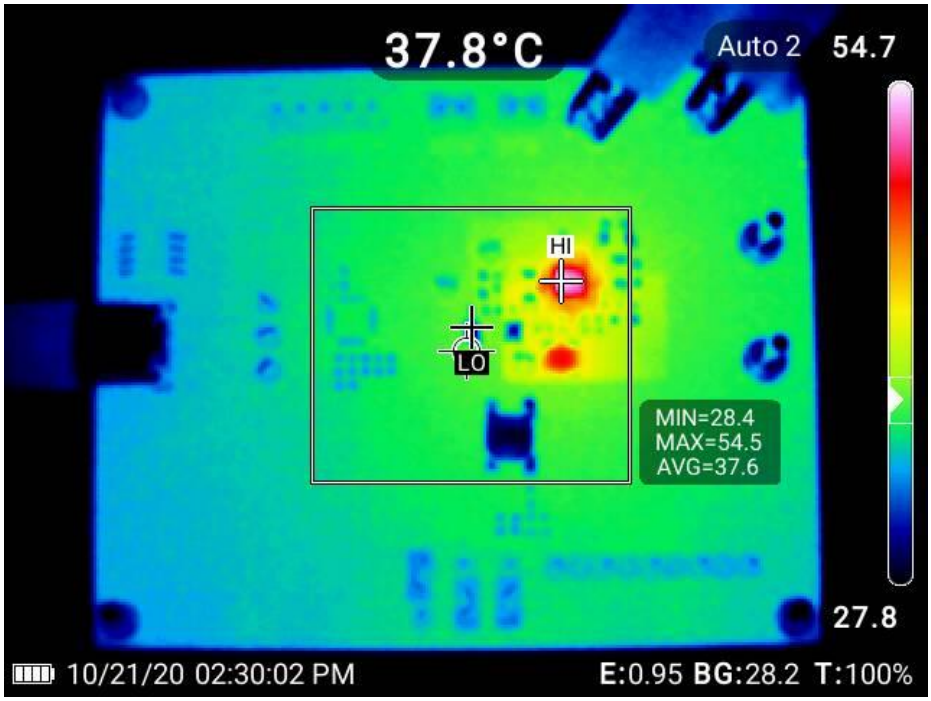


Figure 6: Thermal Performance

5 Start-Up

5.1 Test Procedure

1. Connect the load terminals to:
   a. Positive (+): VSYS
   b. Negative (-): GND
2. Connect the battery terminals to:
   a. Positive (+): VBATT
   b. Negative (-): GND
3. If using a battery simulator, preset the battery voltage between 0V and 4.2V, then turn it off. Connect the battery simulator output terminals to the VBATT and GND pins, respectively.
4. Ensure that the battery voltage is present (if using a battery simulator, turn the battery simulator on). Then connect the board to an adapter with a USB Type-C to Type-C, or Type-A to Type-C cable.
5. Figure 7 shows the original set-up for the MEZS7-4.5APDCharger.

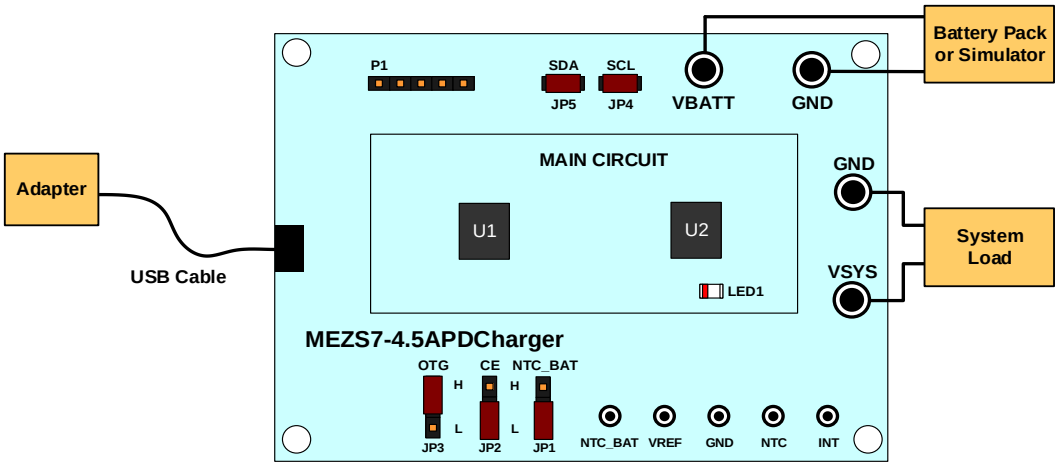


Figure 7: Test Set-Up for the MEZS7-4.5APDCharger

Charge Mode

SCP, CDP, DCP, and PD charge modes can be tested on this board using the steps below. For SCP mode, follow step 1. For CDP or DCP mode, follow step 2. For PD mode, follow step 3.

1. Connect a USB SCP port to the board with a USB Type-A to Type-C cable. There is a 5V input, and the input current limit is set to 500mA.
2. Connect a USB CDP/DCP port to the board with a USB Type-A to Type-C cable. There is a 5V input, and the input current limit is set to 1.5A.
3. Connect a PD adapter to the board with a USB Type-C to Type-C cable. There is a 12V maximum input, and the input current limit is set according to the adapter's output capability.

Discharge Mode

The Type-C port in this board is a DRP port. When a load is attached, it can work as a DFP to power the USB from the battery. The output voltage is 5.1V, and the output current limit is preset to 2.4A. Disconnect the adapter from the board, and connect a smartphone to the board with a USB Type-C to Type-C cable. The board should start outputting 5.1V to charge the phone. When the smartphone is removed, the output of the board should be disabled automatically.

6 Disclaimer

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