MPQ8861

18V, 12A, High-Efficiency, Wide-Input, Synchronous Step-Down Converter with Integrated Telemetry, AEC-Q100 Qualified

DESCRIPTION

The MPQ8861 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. The MPQ8861 offers a fully integrated solution that achieves 12A of continuous output current (I_{OUT}), with excellent load and line regulation across a wide input voltage (V_{IN}) supply range.

The output voltage (V_{OUT}) level can be controlled on-the-fly via the I²C serial interface. The reference voltage (V_{REF}) range can be adjusted from 0.6V to 1.108V in 4mV steps. Functions such as the voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power-save mode are also selectable via the I²C.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates when V_{OUT} is within its nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MPQ8861 is AEC-Q100 qualified, and available in a QFN-14 (3mmx4mm) package with wettable flanks.

FEATURES

- 0.6V to 5.5V Output Voltage (V_{OUT}) Range
- 2.9V to 18V Input Voltage (V_{IN}) Range
- 12A DC Output Current (I_{OUT})
- 1% Internal Reference Accuracy
- 4mV Steps for Dynamic Reference Adjustments with Slew Rate Control
- Up to 1.25MHz Adjustable Frequency via the I²C
- Selectable Pulse-Frequency Modulation (PFM) Mode, Pulse-Width Modulation (PWM) Mode, and Adjustable Current Limit via the I²C
- Four Different Selectable I²C Addresses
- Power Good (PG) Indication Output
- Over-Voltage Protection (OVP), Over-Current Protection (OCP), and Thermal Shutdown Protection
- Available in a QFN-14 (3mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Systems
- Industrial Systems

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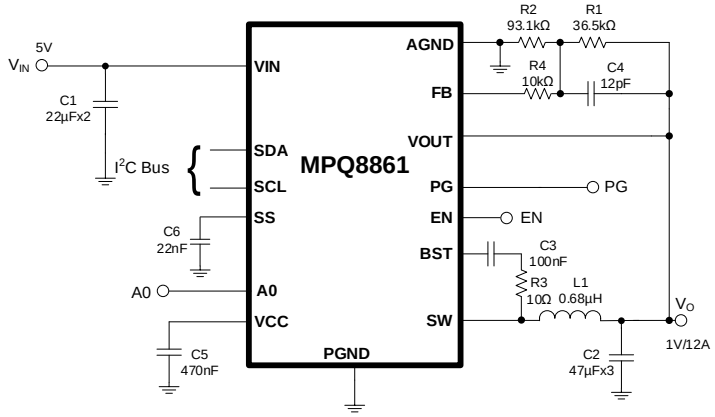
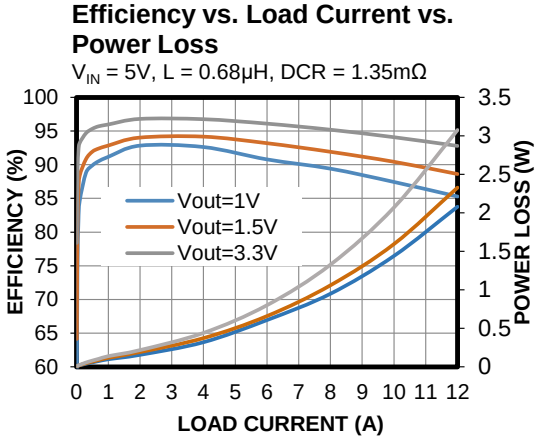
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ8861GLE-AEC1	QFN-14 (3mmx4mm)	*See Below*	1
EVKT-MPQ8861	N/A	N/A	N/A

* For Tape & Reel, add suffix -Z (e.g. MPQ8861GLE-AEC1-Z).

TOP MARKING

MPYW
8861
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
8861: First four digits of the part number
LLL: Lot number
E: Wettable flank

EVALUATION KIT EVKT-MPQ8861

EVKT-MPQ8861 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVQ8861-LE-00A	MPQ8861 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes USB to I²C communication interface, one USB cable, and one ribbon cable	1

Order directly from MonolithicPower.com or our distributors.

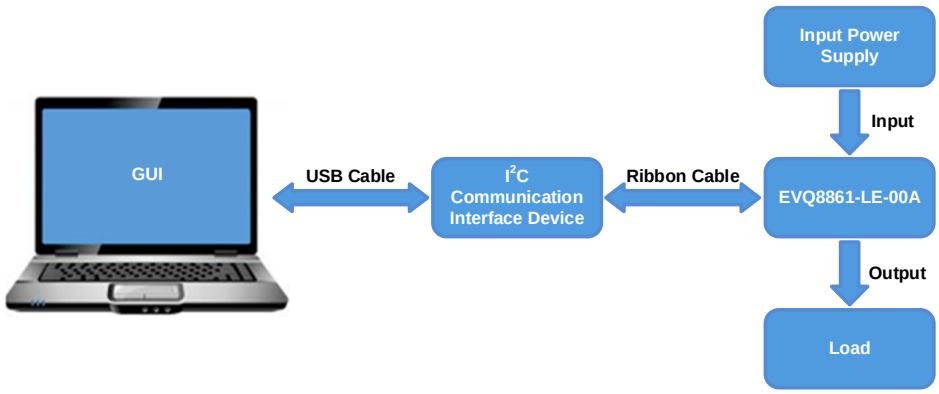

Figure 1: EVKT-MPQ8861 Evaluation Kit Set-Up

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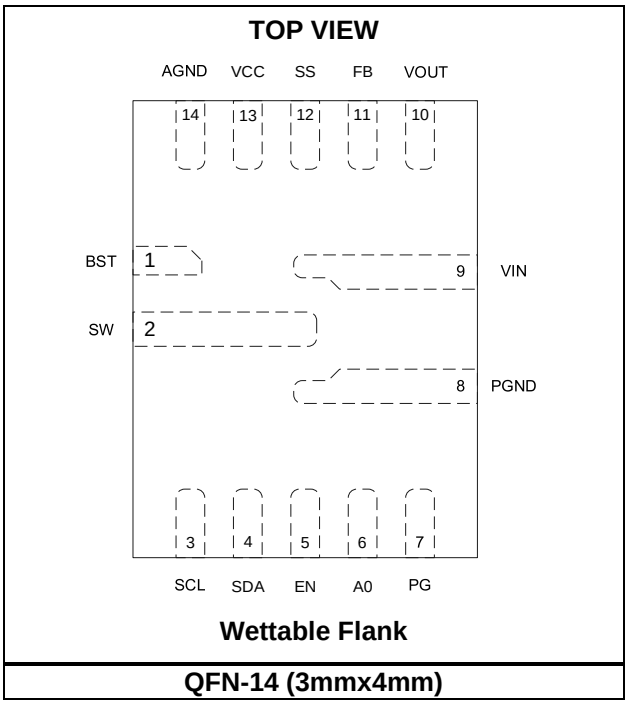
PACKAGE REFERENCE



QFN-14 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** A capacitor is required between the SW and BST pins to form a floating supply across the high-side (HS) switch driver.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	SCL	**I²C serial clock.**
4	SDA	**I²C serial data.**
5	EN	**Enable.** Drive EN high to enable the MPQ8861. EN has a 1.6MΩ internal pull-down resistor to GND. EN is a high-voltage pin; connect EN to VIN directly for automatic start-up.
6	A0	**I²C address set-up.** Connect a resistor divider from VCC to A0 to set up different I²C addresses.
7	PG	**Power good indication.** PG is an open-drain structure. PG becomes de-asserted if the output voltage (V_{OUT}) is out of the regulation window.
8	PGND	**System power ground.** PGND is the regulated V_{OUT} reference ground, and requires special consideration during PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MPQ8861 operates on a 2.9V to 18V input rail. To decouple the input rail with a ceramic capacitor, connect VIN to an input capacitor using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the positive load terminal.
11	FB	**Feedback.** To set V_{OUT}, connect FB to the tap of an external resistor divider, placed between output and GND.
12	SS	**Soft start set-up.** Connect a capacitor from SS to ground to set the soft-start time (t_{SS}).
13	VCC	**Internal low-dropout (LDO) regulator output.** Decouple VCC with a 0.47µF capacitor.
14	AGND	**Analog ground.** Connect AGND to PGND through low-impedance routing or a ground plane.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +19V
V_{SW} ..... -0.6V (-7V for <10ns) to ..... V_{IN} + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
V_{OUT} 7V
All other pins ..... -0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (5) 4.3W
Junction temperature ..... Thermal shutdown
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (3)

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 2.9V to 18V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
Operating junction temp (T_J) ..... -40°C to thermal shutdown

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (3mmx4mm)		
EVQ8861-LE-00A (5)	29	3°C/W
JESD51-7 (6)	48	11°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. The JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. The JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a 4-layer PCB (85.5mmx63.5mm).
6) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply shutdown current	I_{IN}	V_{EN} = 0V		2.1	8	μA
Supply quiescent current	I_Q	No switching, feedback (FB) = 105% V_{REF}, pulse-frequency modulation (PFM) mode		420	620	μA
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN hysteresis threshold	V_{EN_HYS}			110		mV
EN to GND pull-down resistor	R_{EN}		1	1.6	2.2	MΩ
VCC voltage	V_{CC}	I_{CC} = 0mA to 20mA	-5%	3.53	+5%	V
VIN under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_R}$		2.45	2.65	2.85	V
VIN UVLO falling threshold	$V_{IN_UVLO_F}$		2.3	2.5	2.7	V
High-side (HS) switch-on resistance	$R_{DS(ON)_HS}$	V_{BST} - V_{SW} = 3.3V		15	30	mΩ
Low-side (LS) switch-on resistance	$R_{DS(ON)_LS}$	V_{CC} = 3.3V		4.5	10	mΩ
Switch leakage	SW_{LKG1}	V_{EN} = 0V, V_{SW} = 18V, T_J = 25°C			1	μA
	SW_{LKG2}	V_{EN} = 0V, V_{SW} = 18V, T_J = 125°C			14	μA
LS valley-current limit	I_{LIMIT_L}	D[2:0] = 010		14		A
LS negative current limit	I_{LIMIT_LN}	In forced pulse-width modulation (PWM) mode or over-voltage protection (OVP) state		-3.5	-2	A
Switching frequency	f_{SW1}	V_{IN} = 12V, V_{OUT} = 1V, T_J = 25°C		500		kHz
	f_{SW2}	V_{IN} = 12V, V_{OUT} = 5V, T_J = 25°C		500		kHz
Minimum off time (7)	t_{OFF_MIN}			185		ns
Minimum on time (7)	t_{ON_MIN}	V_{OUT} = 0.6V		50		ns
Reference voltage	V_{REF}	T_J = 25°C	-1%	720	+1%	mV
		T_J = -40°C to +125°C	-2.1%	720	+2.1%	mV
FB current	I_{FB}	V_{FB} = 740mV		10	80	nA
Power good (PG) under-voltage (UV) rising threshold	PGV_{TH-HI}	Good	0.86	0.9	0.94	V_{REF}
PG UV falling threshold	PGV_{TH-LO}	Fault	0.81	0.85	0.89	V_{REF}
PG over-voltage (OV) rising threshold	PGV_{TH-HI}	Fault	1.11	1.15	1.19	V_{REF}
PG OV falling threshold	PGV_{TH-LO}	Good	1.01	1.05	1.09	V_{REF}
PG deglitch time	PG_t_D	I^2C-configurable	20	30	45	μs
PG sink current capability	V_{PG}	Sink 1mA			0.15	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{OUT} OVP rising threshold	V_{OVP_RISING}		121%	125%	129%	V_{REF}
V_{OUT} OVP falling threshold	$V_{OVP_FALLING}$		106%	110%	114%	V_{REF}
V_{OUT} OVP delay	t_{OVP}		2.3	5.3	8.3	µs
Output pin absolute OV	V_{OVP2}		6	6.5	7	V
V_{OUT} under-voltage protection (UVP) threshold	$V_{FB_UV_TH}$	Hiccup entry	55%	60%	65%	V_{REF}
Soft-start current	I_{SS}		4	7	10	µA
Thermal shutdown (7)	T_{TSD}			150		°C
Thermal hysteresis (7)	T_{TSD_HYS}			20		°C
I²C Specifications						
I²C slave address 1	ADD_1	A0 pin float		61h		
I²C slave address 2	ADD_2	Resistance accuracy = 1%, R_{A0_UP} = 100kΩ, R_{A0_DOWN} = 60.4kΩ		63h		
I²C slave address 3	ADD_3	Resistance accuracy = 1%, R_{A0_UP} = 60.4kΩ, R_{A0_DOWN} = 100kΩ		65h		
I²C slave address 4	ADD_4	R_{A0_UP} = 100kΩ		67h		
A0 to GND pull-down resistor	R_{A0_PD}		1.5	2	2.5	MΩ
High input logic	V_{IH}	I²C pull-up VDD can be 1.8V to 3.6V	1.4			V
Low input logic	V_{IL}				0.4	V
Low V_{OUT} logic	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$		0	60		ns
Set-up time for a (repeated) start condition	$t_{SU.STA}$		160			ns
Hold time for a (repeated) start condition	$t_{HD.STA}$		160			ns
Bus free time between a start condition and a stop condition	t_{BUF}		160			ns
Set-up time for a stop condition	$t_{SU.STO}$		160			ns
SCL and SDA rise time	t_R		10		300	ns
SCL and SDA fall time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF

Note:

7) Guaranteed by engineering sample characterization.

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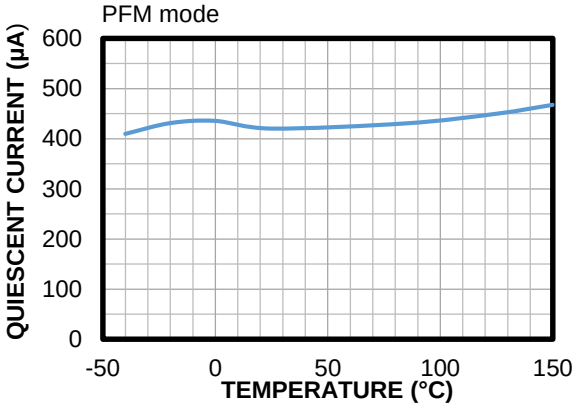
TYPICAL PERFORMANCE CHARACTERISTICS

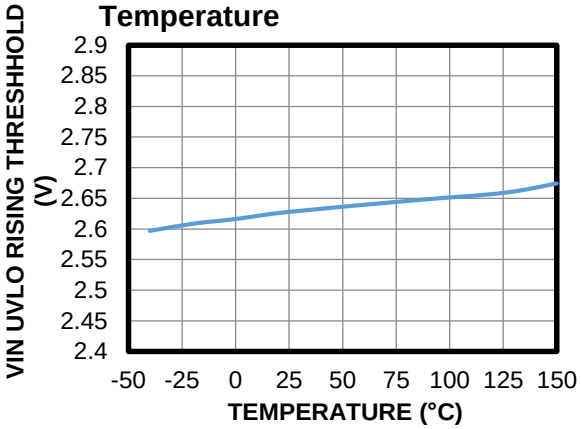
Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Temperature

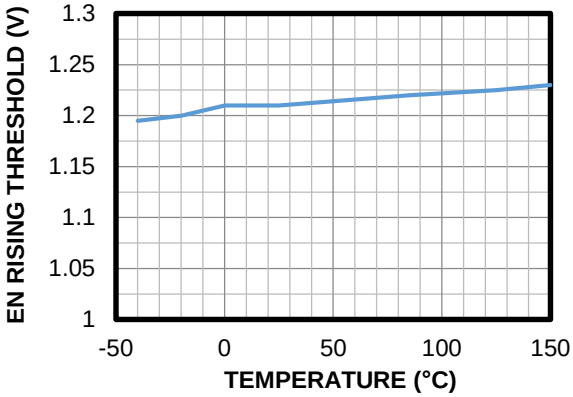
No switching, FB = 105% V_{REF}, PFM mode



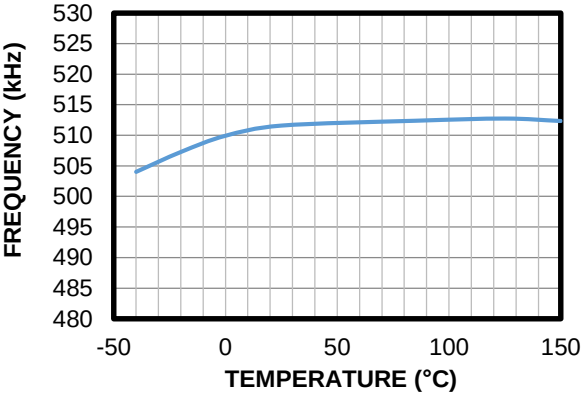
VIN UVLO Rising Threshold vs. Temperature



EN Rising Threshold vs. Temperature

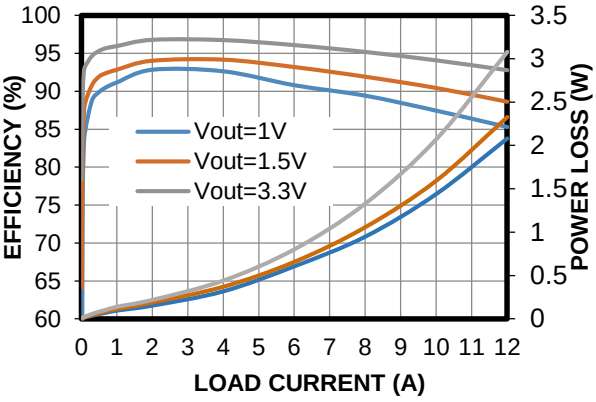


Frequency vs. Temperature



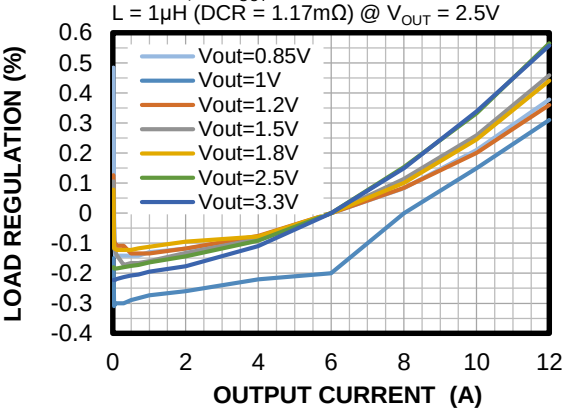
Efficiency vs. Load Current vs. Power Loss

V_{IN} = 5V, L = 0.68µH, DCR = 1.35mΩ



Load Regulation vs. I_{OUT}

V_{IN} = 5V, L = 0.68µH (DCR = 1.35mΩ) at V_{OUT} = 1V/1.2V/1.8V/3.3V, L = 0.47µH (DCR = 1.53mΩ) at V_{OUT} = 0.85V, L = 1µH (DCR = 1.17mΩ) @ V_{OUT} = 2.5V



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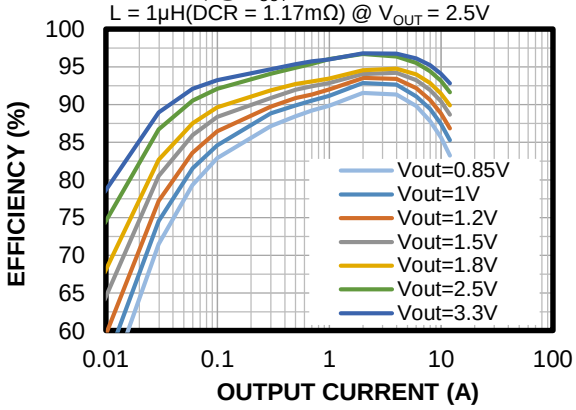
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

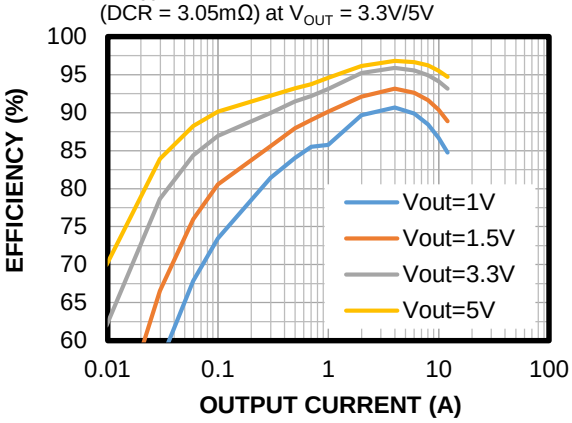
Efficiency vs. Output Current

V_{IN} = 5V, L = 0.68µH (DCR = 1.35mΩ)
@ V_{OUT} = 1V/1.2V/1.8V/3.3V, L = 0.47µH (DCR = 1.53mΩ) @ V_{OUT} = 0.85V,
L = 1µH(DCR = 1.17mΩ) @ V_{OUT} = 2.5V



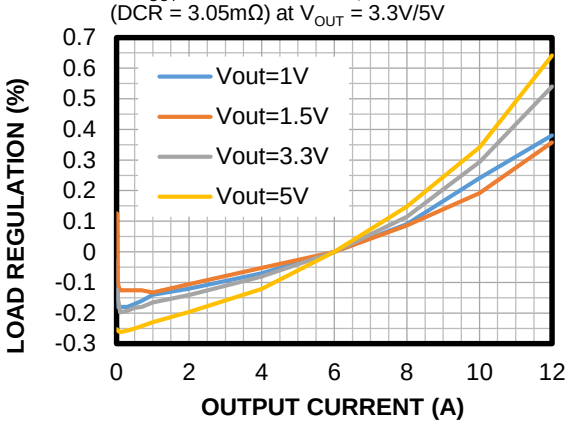
Efficiency vs. Output Current

V_{IN} = 12V, L = 1µH (DCR = 1.17mΩ)
at V_{OUT} = 1V/1.5V, L = 2.2µH
(DCR = 3.05mΩ) at V_{OUT} = 3.3V/5V



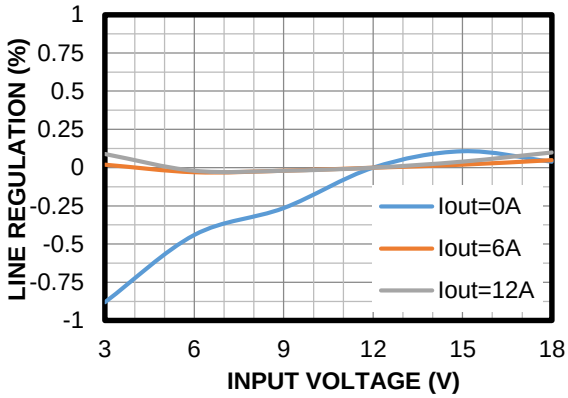
Load Regulation vs. I_{OUT}

V_{IN} = 12V, L = 1µH (DCR = 1.17mΩ)
at V_{OUT} = 1V/1.5V, L = 2.2µH
(DCR = 3.05mΩ) at V_{OUT} = 3.3V/5V



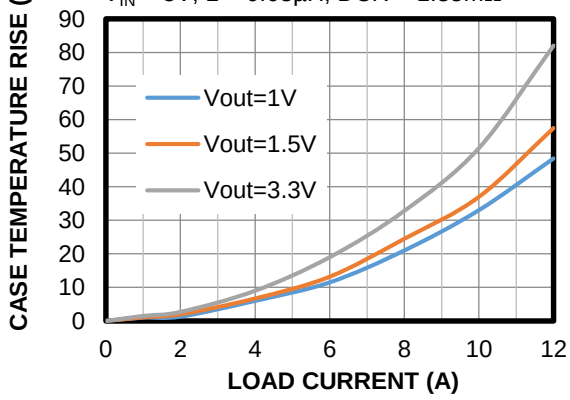
Line Regulation vs. Input Voltage

L = 0.68µH, DCR = 1.35mΩ



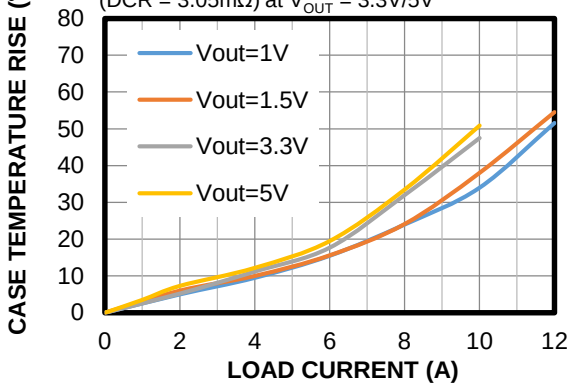
Case Temperature Rise vs. Load Current

V_{IN} = 5V, L = 0.68µH, DCR = 1.35mΩ



Case Temperature Rise vs. Load Current

V_{IN} = 12V, L = 1µH (DCR = 1.35mΩ)
at V_{OUT} = 1V/1.5V, L = 2.2µH
(DCR = 3.05mΩ) at V_{OUT} = 3.3V/5V



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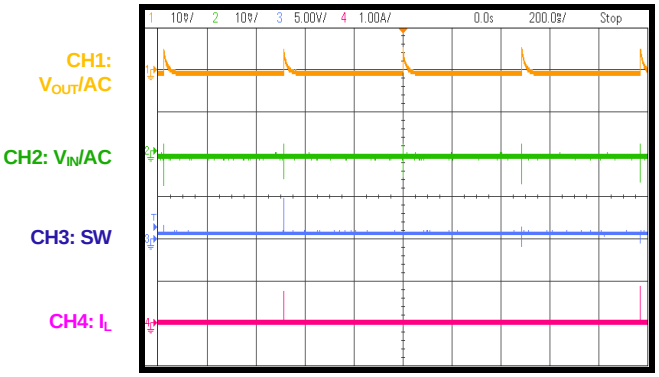
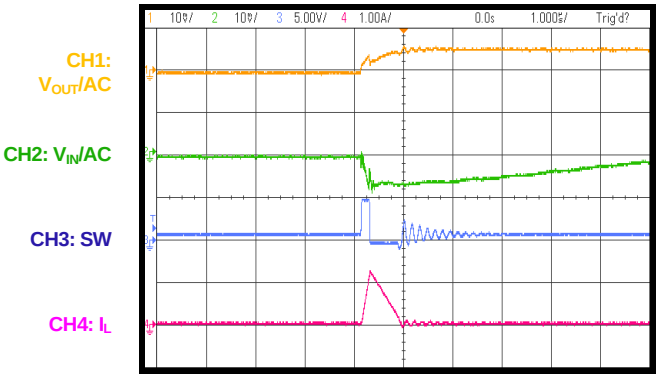
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

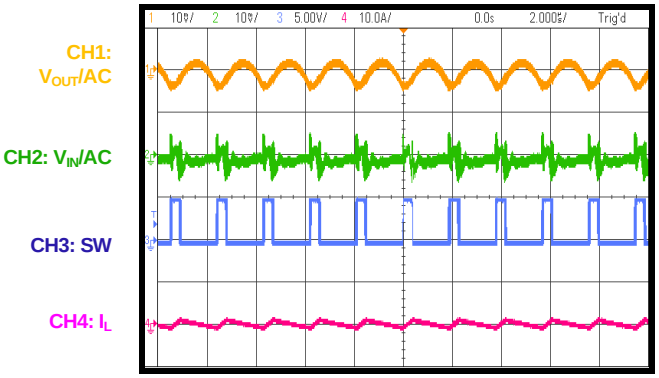
Steady State
Auto-PFM/PWM mode, I_{OUT} = 0A



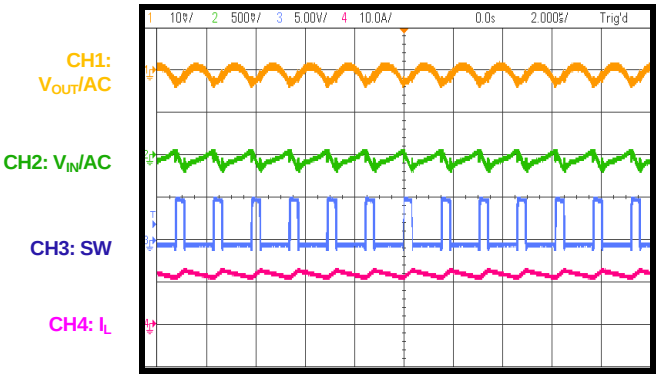
Steady State
Auto-PFM/PWM mode, I_{OUT} = 0A



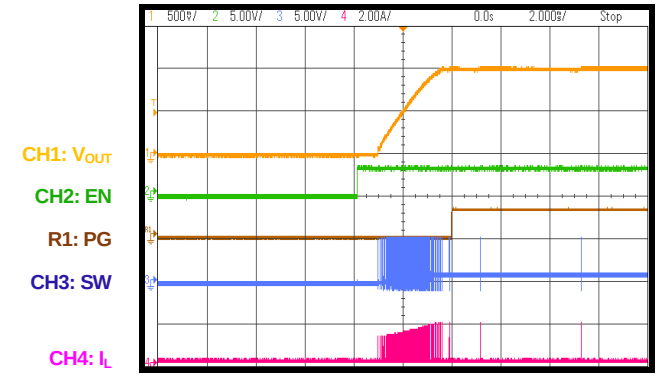
Steady State
Forced PWM mode, I_{OUT} = 0A



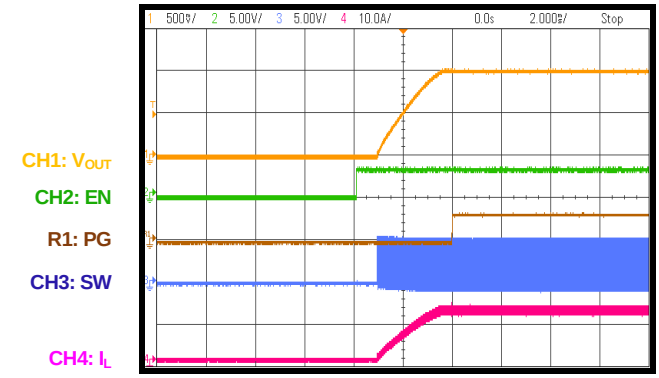
Steady State
I_{OUT} = 12A



Start-Up through EN
I_{OUT} = 0A



Start-Up through EN
I_{OUT} = 12A



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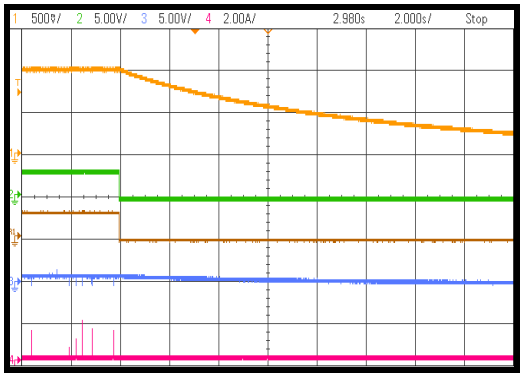
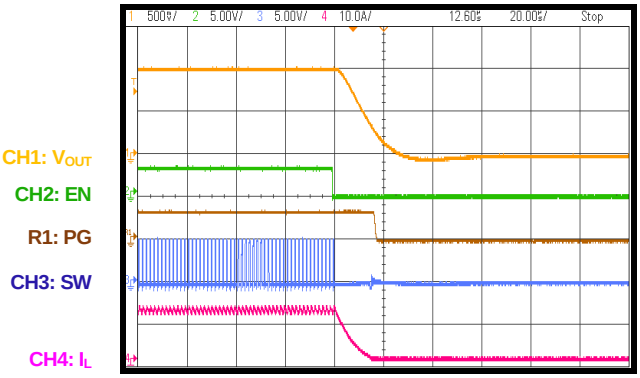
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

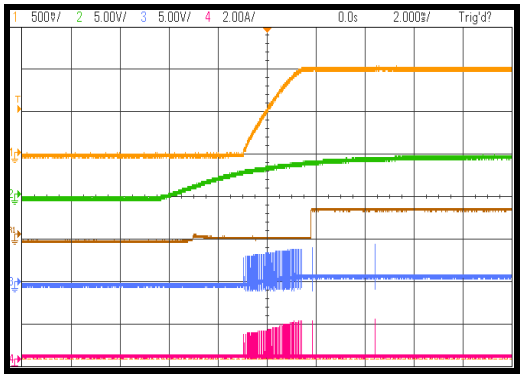
Shutdown through EN
I_{OUT} = 0A



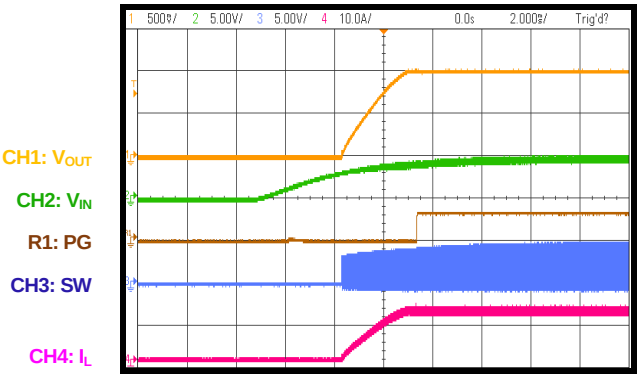
Shutdown through EN
I_{OUT} = 12A



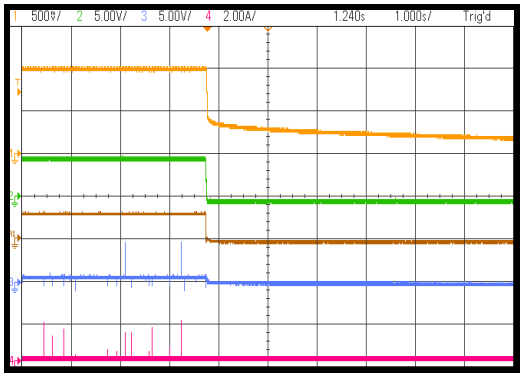
Start-Up
I_{OUT} = 0A



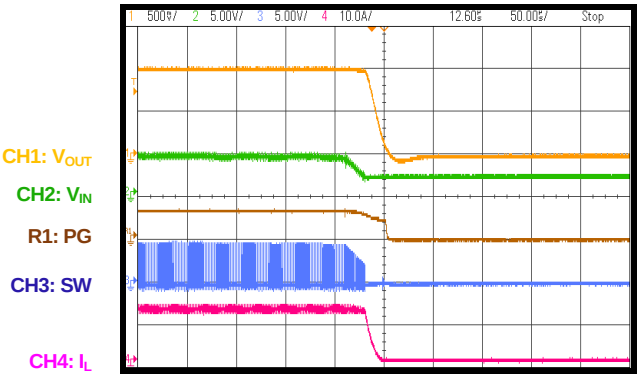
Start-Up
I_{OUT} = 12A



Shutdown
I_{OUT} = 0A



Shutdown
I_{OUT} = 12A



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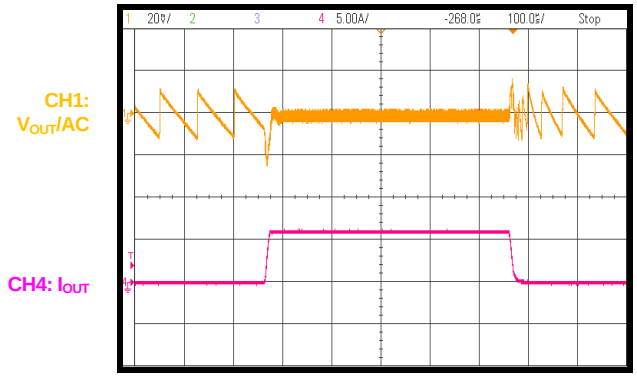
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1V, L = 0.68µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

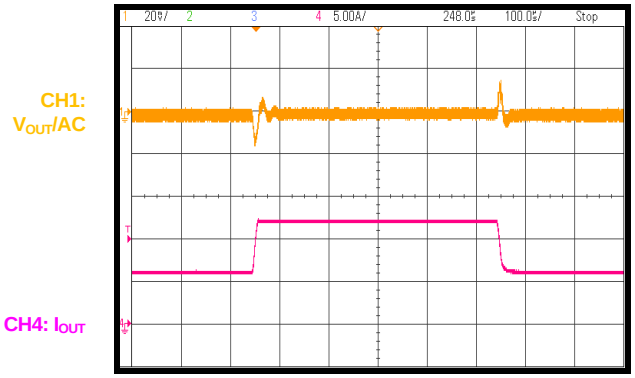
Load Transient

I_{OUT} = 0A to 6A, slew rate = 0.6A/µs



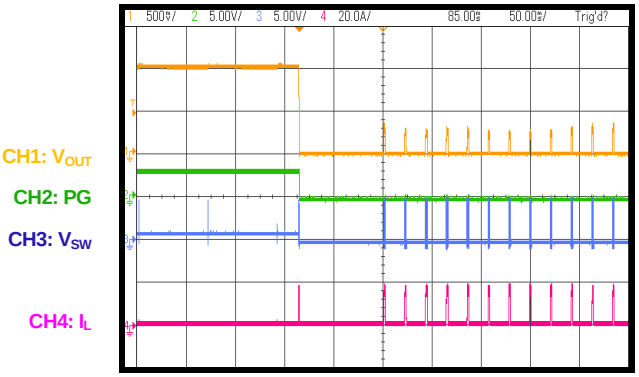
Load Transient

I_{OUT} = 6A to 12A, slew rate = 0.6A/µs



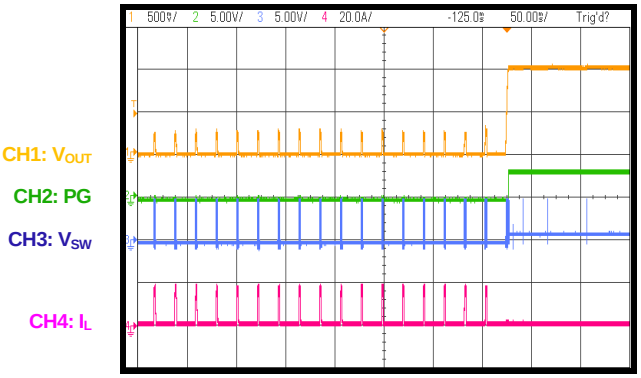
SCP Entry, Hiccup Mode

I_{OUT} = 0A



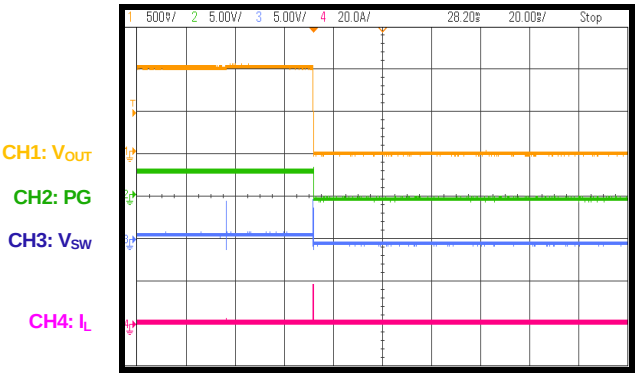
SCP Recovery, Hiccup Mode

I_{OUT} = 0A



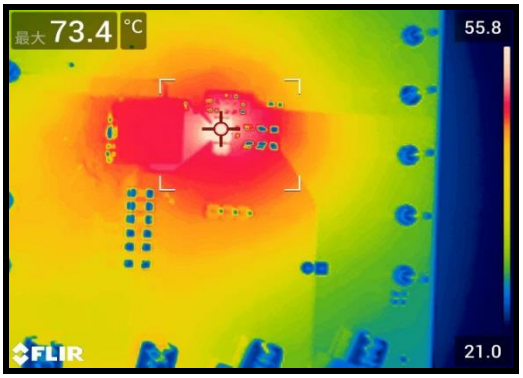
SCP Entry, Latch-Off Mode

I_{OUT} = 0A



Thermal Image

V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 12A, measured on 4-layer PCB (85.5mmx63.5mm), top/bottom layers: 2oz, mid-layers 1 and 2: 1oz, T_A = 25°C



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FUNCTIONAL BLOCK DIAGRAM

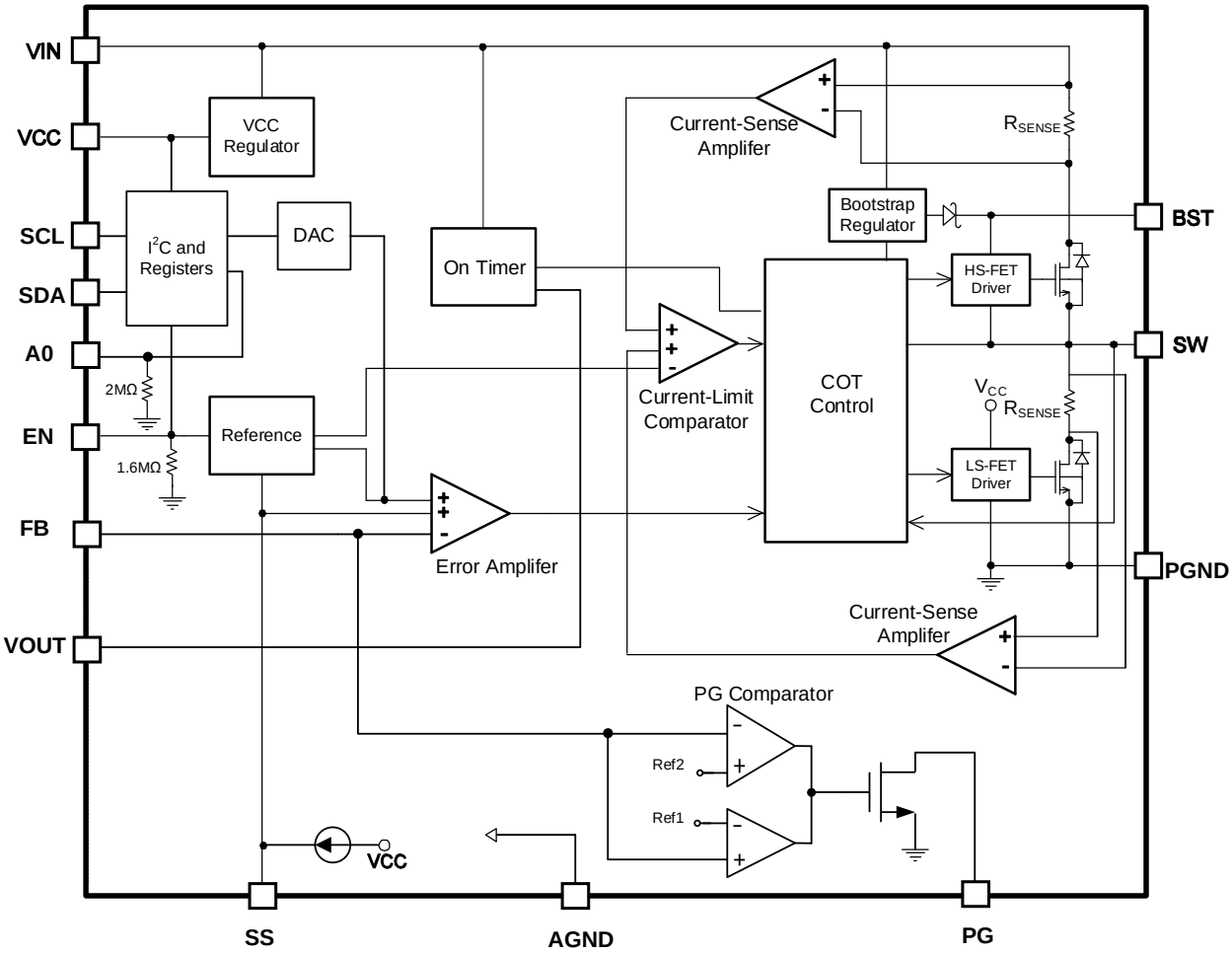

Figure 2: Functional Block Diagram

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OPERATION

Pulse-Width Modulation (PWM)

The MPQ8861 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The MPQ8861 uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization. Figure 3 shows the simplified ramp compensation block.

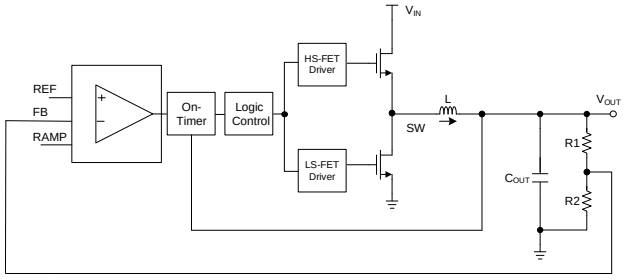

Figure 3: Simplified Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on once the ramp voltage (V_{RAMP}) drops below the error amplifier (EA) output voltage (V_{EAO}), which indicates an insufficient output voltage. The on period is determined by both the output voltage (V_{OUT}) and input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the entire V_{IN} range.

After the on period elapses, the HS-FET turns off. By cycling the HS-FET on and off, the converter regulates V_{OUT}. To minimize conduction loss, the integrated low-side MOSFET (LS-FET) turns on once the HS-FET turns off.

A dead short between input and GND occurs when both the HS-FET and LS-FET are on at the same time, reducing efficiency drastically. This is called shoot-through. The MPQ8861 prevents shoot-through by internally generating a dead time (DT) between the HS-FET off period and LS-FET on period, and vice versa. The MPQ8861 enters either heavy-load operation or light-load operation depending on the output current (I_{OUT}) amplitude.

Switching Frequency (f_{SW})

The MPQ8861 uses COT control without a dedicated oscillator in the IC. V_{IN} is fed into the one-shot on-timer through the internal frequency resistor. The duty ratio is V_{OUT} / V_{IN}, and f_{SW} is fairly constant across the entire V_{IN} range.

The MPQ8861's f_{SW} can be adjusted by setting the bits D[5:4] in register 0x02 via the I^2C. When the V_{OUT} setting is low and V_{IN} is high, the switching on time is limited by the internal minimum on time limit, and f_{SW} decreases. Table 1 shows the maximum f_{SW} compared to V_{OUT} when V_{IN} = 12V and when V_{IN} = 5V.

Table 1: Selecting the Maximum f_{SW} vs. V_{OUT}

V_{OUT}	Maximum Switching Frequency	
-	V_{IN} = 12V	V_{IN} = 5V
5V	1.25MHz	-
3.3V	1.25MHz	1.25MHz
2.5V	1.25MHz	1.25MHz
1.8V	1.25MHz	1.25MHz
1.5V	1.25MHz	1.25MHz
1.2V	1MHz	1.25MHz
1V	750kHz	1.25MHz
0.9V	750kHz	1.25MHz
0.6V	500kHz	1.25MHz

Forced PWM Operation

When the MPQ8861 works in forced PWM mode, the device enters continuous conduction mode (CCM), during which the HS-FET and LS-FET repeat the on/off operation, even if the inductor current (I_L) is at 0A or a negative value. f_{SW} is fairly constant (see Figure 4).

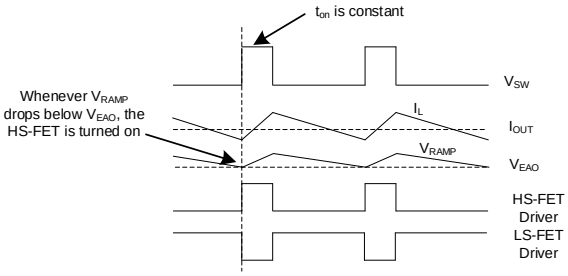

Figure 4: Forced PWM Operation

Light-Load Operation

When the MPQ8861 works in auto-PWM mode, auto-pulse-frequency modulation (PFM) mode, or light-load operation, the MPQ8861 automatically reduces f_{SW} to maintain high efficiency, and I_L drops almost to zero. When I_L reaches 0A, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 5 on page 15).

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The output capacitors discharge slowly to GND through R1 and R2. This operation significantly improves device efficiency when I_{OUT} is low.

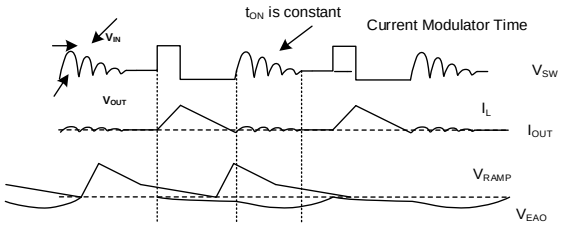

Figure 5: Light-Load Operation

Light-load operation is also called skip mode since the HS-FET does not turn on as frequently compared to during heavy-load operation. The frequency at which the HS-FET turns on is a function of I_{OUT}. As I_{OUT} increases, the current modulator regulation period becomes shorter. Therefore, the HS-FET turns on more frequently and f_{SW} increases. I_{OUT} reaches critical levels when the current modulator time is zero, which can be calculated using Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The MPQ8861 reverts to PWM mode once I_{OUT} exceeds its critical level. f_{SW} then remains fairly constant across the entire I_{OUT} range.

The MPQ8861 can operate in PFM mode under light loads to improve efficiency in low-power mode. The MPQ8861 can also operate in forced PWM mode at any load condition. This mode is selectable via the I^2C. To enable low-power mode, set the MODE bit to 0. To disable low-power mode, set the MODE bit to 1, and the converter operates in forced PWM mode. The MODE bit is set to 0 (PFM) by default.

Operating without an External Ramp

The traditional COT control scheme is intrinsically unstable if the output capacitor's equivalent series resistance (ESR) is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot typically be used as output capacitors. The MPQ8861 includes built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. This pure ceramic capacitor solution can significantly reduce the output ripple, total BOM cost, and board area.

VCC Regulator

A 3.5V internal VCC regulator powers most of the internal circuitries. A 0.47µF decoupling capacitor is required to stabilize the regulator and reduce ripple. This regulator takes the VIN input and operates in the full V_{IN} range. If EN is pulled high and V_{IN} exceeds 3.5V, the regulator's output is in full regulation. If V_{IN} falls below 3.5V, V_{OUT} decreases and follows V_{IN}. A 0.47µF ceramic capacitor is required for decoupling.

Enable (EN)

EN is a digital control pin that turns the regulator on and off, including the I^2C block. Drive EN high to turn the regulator on; drive EN low to turn it off. An internal 1.6MΩ resistor is connected from EN to ground. EN can operate with an 18V V_{IN}, which allows EN to be connected directly to VIN for automatic start-up. When the external EN is high, set the EN bit to 0 in register 0x01 to prevent the HS-FET and LS-FET from switching. The MPQ8861 resumes switching once the EN bit is set to 1.

Under-Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. The MPQ8861's UVLO comparator monitors the VCC regulator's V_{IN} and V_{OUT}. The MPQ8861 is active once these voltages exceed their respective UVLO rising thresholds.

Soft Start (SS) and Pre-Biased Start-Up

Soft start (SS) prevents the converter V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start current (I_{SS}) to charge the SS capacitor (C_{SS}) from 0V to V_{CC}. When the VSS voltage (V_{SS}) is below the reference voltage (V_{REF}), the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

The typical soft-start time (t_{SS}) can be calculated using Equation (2):

$$t_{SS}(ms) = \frac{V_{REF}(V) \times C_{SS}(nF)}{7\mu A} \quad (2)$$

Where V_{REF} is the reference voltage.

If MPQ8861's output is pre-biased to a certain voltage during start-up, then the IC disables the switching of both the HS-FET and LS-FET until

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the voltage on the C_{SS} exceeds the sensed V_{OUT} at the FB pin.

The MPQ8861 also provides a selectable soft shutdown function that defines the output discharge behavior after an EN shutdown. By default, the output is not controlled after EN shutdown. If the soft shutdown control bit (SOFT_STOP, D[3] in register 0x02) is set to 1, the output is discharged linearly to zero in 1/4 of the total t_{SS}.

Over-Current Protection (OCP)

The MPQ8861 features default hiccup, cycle-by-cycle, over-current limit control. The current-limit circuit employs both a high-side (HS) current limit and a low-side (LS) valley current-sensing algorithm. The MPQ8861 uses the LS-FET's $R_{DS(ON)}$ as a current-sensing element for the valley current limit. If the magnitude of the HS current-sense signal is above the current limit threshold, the PWM on pulse is terminated and the LS-FET turns on. Subsequently, I_L is monitored by the voltage between GND and SW. GND is used as the positive current-sensing node, so GND should be connected to the bottom MOSFET's source terminal. PWM cannot initiate a new cycle before I_L drops to the valley threshold.

After the over-current (OC) limit is reached, V_{OUT} drops until it is below the under-voltage (UV) threshold (typically 60% below V_{REF}). Once under-voltage protection (UVP) is triggered, the MPQ8861 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground by significantly reducing the average short-circuit current to alleviate thermal issues and protect the regulator. Once the OC condition is removed, the MPQ8861 exits hiccup mode and resumes normal operation.

Short the output to ground first, then power on the MPQ8861. The I^2C is disabled in this condition, and resumes operation once the short circuit is removed. If the hiccup OCP bit (HICCUP_OCP, D[1] in register 0x01) is set to 0 and OCP is triggered or FB UVP is triggered, then the MPQ8861 latches off.

Power Good (PG)

The PG pin indicates whether V_{OUT} is in the normal range compared to the internal V_{REF}. PG is an open-drain structure. An external pull-up supply is required. During start-up, the PG output is pulled low. This indicates to the system to remain turned off while minimizing the load on the output, which helps reduce inrush current at start-up.

Once V_{OUT} is above 90% and below 115% of the internal V_{REF} and SS completes, then the PG signal is pulled high. If V_{OUT} is below 85% after SS finishes, the PG signal remains low. If V_{OUT} is above 115% of the internal V_{REF}, PG is switched low. The PG signal goes high again after V_{OUT} drops below 105% of the internal V_{REF}.

PG implements an adjustable deglitch time via the I^2C whenever V_{OUT} crosses the under-voltage (UV) and over-voltage (OV) rising and falling thresholds. This guarantees the correct indication when V_{OUT} is scaled via the I^2C.

If EN UVLO, input UVLO, OCP, or over-temperature protection (OTP) are triggered, then PG output is pulled low immediately.

Input Over-Voltage Protection (OVP)

The MPQ8861 monitors VIN to detect an input over-voltage (OV) event. This function is active only when the output is in an OV or soft shutdown condition. When the output is in the OVP state or soft shutdown is enabled, output discharge is enabled to charge V_{IN} high. When V_{IN} exceeds the input OVP threshold (typically 18V), both the HS-FET and LS-FET stop switching.

Output OVP

The MPQ8861 monitors both FB and VOUT to detect an OV event. If the FB voltage (V_{FB}) exceeds 125% of the internal V_{REF}, an internal comparator monitors FB, and the controller enters dynamic regulation mode. V_{IN} may be charged up during this time. If input OVP is triggered, the IC stops switching. If OVP mode is set to auto-retry via the I^2C, then the IC begins switching once V_{IN} drops below the V_{IN} OVP recovery threshold. Otherwise, the MPQ8861 latches off. OVP auto-retry or latch-off occur only if SS has finished.

Dynamic regulation mode can be operated by turning on the LS-FET until the LS negative current limit is triggered. Then the body diode of the HS-FET freewheels the current.

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The output power (P_{OUT}) charges the input capacitor, which may trigger the V_{IN} OVP function. In V_{IN} OVP, neither the HS-FET nor LS-FET turn on and stop charging V_{IN}. Repeat the operation if the output is still over-voltage and V_{IN} drops below the V_{IN} OVP threshold. If V_{OUT} is below 110% of the internal V_{REF}, then the device exits output OVP.

Output Absolute OVP

The MPQ8861's V_{OUT} can be adjusted by the FB V_{REF} and the external resistor dividers. However, the MPQ8861's V_{OUT} must be set below the absolute OVP threshold (typically 6.5V).

The MPQ8861 monitors V_{OUT} to detect absolute OVP. If V_{OUT} exceeds 6.5V and the OVP retry bit (in register 0x01) is set to 1, then the controller enters dynamic regulation mode (for details, see the Output OVP section on page 16). Otherwise, the MPQ8861 latches off anytime output OVP and input OVP are both triggered. Absolute OVP works once both the V_{IN} and EN exceed their rising thresholds. This means that this function can work even during SS.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 160°C, the entire chip shuts down. Once the temperature is below its lower threshold (typically 140°C), the chip is enabled again.

The D[1] and D[2] bits in register 0x06 can be monitored for more information about the IC's silicon temperature.

Floating Driver and Bootstrap (BST) Charging

An external BST capacitor (C_{BST}) powers the floating power MOSFET driver, which has its own UVLO protection. The UVLO rising threshold is 2.4V, with a 150mV hysteresis. The C_{BST} voltage is internally regulated by VIN through D1, M1, C4, L1, and C2 (see Figure 6). If V_{BST} - V_{SW} exceeds 3.3V, then U1 regulates M1 to maintain a 3.3V BST voltage (V_{BST}) across C4.

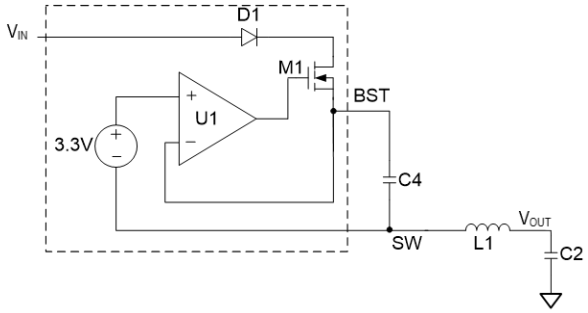

Figure 6: Internal BST Charging Circuit

Start-Up and Shutdown

If VIN, VCC, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, VCC low, thermal shutdown, OVP latch, and OCP latch. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{EAO} and the internal supply rail are then pulled down.

I²C Control and Default V_{OUT}

When the MPQ8861 is enabled, V_{OUT} is determined by the FB resistors with a programmed soft-start time (t_{SS}). The I²C bus can subsequently communicate with the master. If the chip does not receive a continuous I²C communication signal, it can work through FB and perform similarly to a traditional non-I²C part. V_{OUT} is determined by the resistor dividers, R1 and R2, and FB V_{REF}. V_{OUT} can be calculated using Equation (3):

$$V_{OUT} = V_{REF} \times (\frac{R1+R2}{R2}) \quad (3)$$

Note that V_{OUT} cannot be set above the absolute OVP threshold (typically 6.5V).

I²C Slave Address

To support multiple devices used on the same I²C bus, A0 can be used to select any of four different addresses. A resistor divider from VCC to GND can achieve an accurate V_{REF}. Connect A0 to this V_{REF} to set a different I²C slave address (see Figure 7 on page 18).

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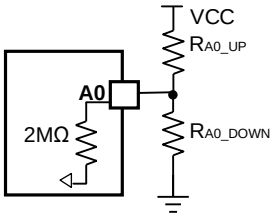

Figure 7: I²C Slave Address Selection Set-Up

The internal circuit changes the I²C address accordingly. When the master sends an 8-bit address value, the 7-bit I²C address should be followed by 0/1 to indicate a read/write (R/W) operation. Table 2 shows the recommended I²C address selection based on the A0 voltage.

Table 2: Selection by A0 Resistor Divider

A0 Upper Resistor R_{A0_UP} (kΩ)	A0 Lower Resistor R_{A0_DOWN} (kΩ)	I²C Slave Address	
		Binary	Hex
Not connected	Not connected	110 0001	61h
100	60.4	110 0011	63h
60.4	100	110 0101	65h
100	Not connected	110 0111	67h

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I²C INTERFACE

I²C Serial Interface

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. When connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPQ8861 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. Parameters such as V_{OUT} and the transition slew rate can be controlled in real time via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the clock's high period. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 8).

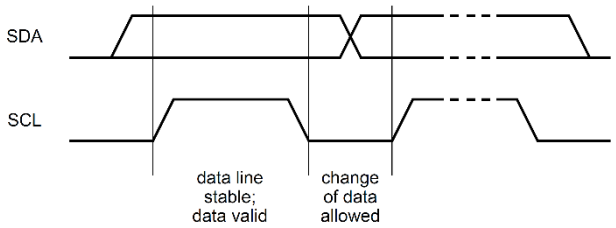

Figure 8: Bit Transfer on the I²C Bus

Start (S) conditions and stop (P) conditions are signaled by the master device, which signifies the beginning and the end of the I²C transfer. A start condition is defined as the SDA signal transitioning from high to low while the SCL line is high. A stop condition is defined as the SDA signal transitioning from low to high while the SCL line is high (see Figure 9).

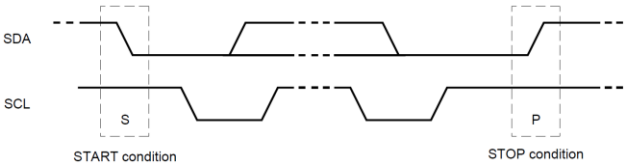

Figure 9: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is busy after a start condition is sent, and is free again a minimum of 4.7μs after a stop condition. The bus remains busy if a repeated start (Sr) condition is generated instead of a stop condition. The S and Sr conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains at stable low during the high period of this clock pulse.

Figure 10 shows the format of data transfers. After the start condition, a slave address is sent. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop condition generated by the master. However, if the master still wishes to communicate on the bus, it can generate a repeated start condition and address another slave without first generating a stop condition.

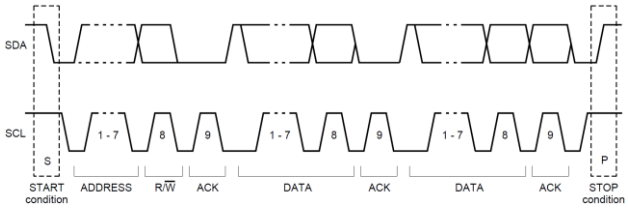

Figure 10: Complete Data Transfer

The MPQ8861 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ8861 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ8861. The MPQ8861 performs an update on the falling edge of the least significant bit (LSB).

The MPQ8861 contains seven read or write (R/W) registers. Register 00 is the feedback (FB) reference voltage (V_{REF}) selection register. Register 0x01 is the first system control register and can be used to set the slew rate, hiccup over-current protection (OCP), etc. Register 0x02 is the second system control register, and

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can be used to set f_{SW}, the current limit, etc.

Register 0x03 and register 0x04 are reserved for future use. Register 0x05 is the IC ID register. Register 0x06 is the IC status indication register, and can be used to check whether the IC is in OCP, over-temperature protection (OTP) status, etc.

Figure 11 shows an example of an I^2C write command. Figure 12 shows an example of an I^2C read command.

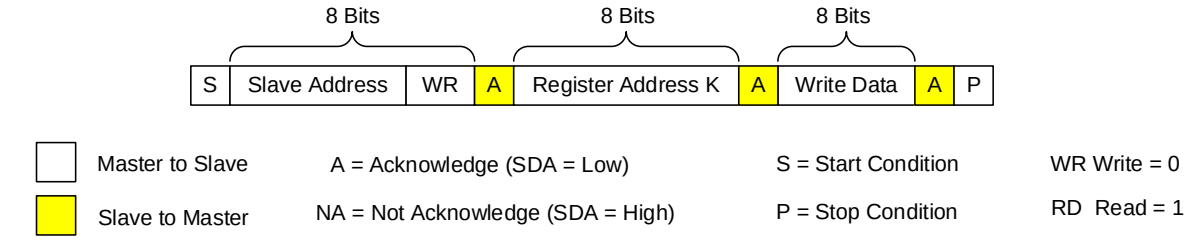

Figure 11: I^2C Write Single Register Example

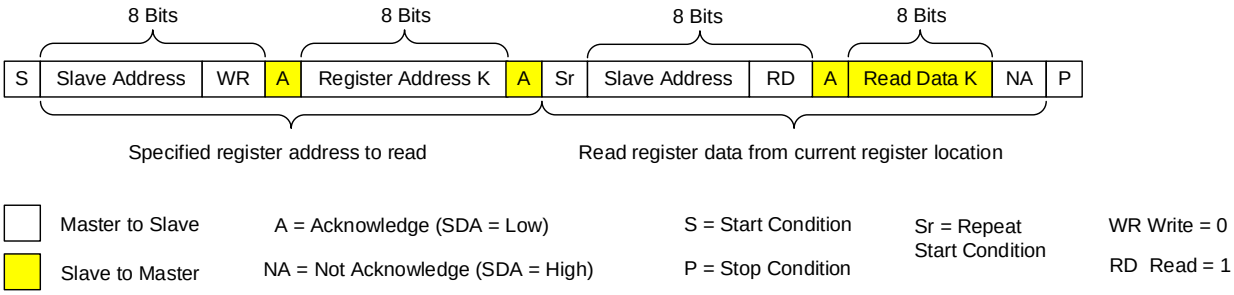

Figure 12: I^2C Read Single Register Example

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REGISTER DESCRIPTION

Register Map

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x00	VSEL	R/W	RESERVED	FB_REF						
0x01	SYSCNTL REG1	R/W	EN	GO_BIT	SLEW_RATE			RETRY _OVP	HICCUP _OCP	MODE
0x02	SYSCNTL REG2	R/W	PG_DEGLITCH_TIME		FSW		SOFT_ STOP	CURRENT_LIMIT_ ADJUST		
0x03	RESERVED	-	RESERVED							
0x04	RESERVED	-	RESERVED							
0x05	ID1	R	VENDOR_ID				IC_REVISION_ID			
0x06	STATUS	R	RESERVED				OC	OTEW	OT	PG

REG0x00: VSEL

Register 0x00 is the FB_REF voltage selection register. The MPQ8861 default FB_REF voltage is 0.72V, so the MPQ8861's default V_{OUT} is determined by the FB resistor divider and 0.72V default reference after power start-up or EN start-up. V_{REF} is adjustable from 0.6V to 1.108V. Before adjusting the FB_REF voltage, GO_BIT in register 0x01 should be set to 1, and then V_{REF} can be adjusted by the lower 7 bits of register 0x00.

When the FB_REF voltage setting command is finished, GO_BIT auto-resets to 0 to prevent false V_{OUT} scaling operation. GO_BIT should be set to 1 before adjusting the FB_REF voltage via the I^2C.

Table 3 on page 22 shows the FB_REF voltage selection chart from 0.6V to 1.108V via the I^2C.

Name	Bits	Default Value	Description
RESERVED	D[7]	1	Reserved for future use.
FB_REF	D[6:0]	001 1110	Sets the FB_REF voltage between 0.6V and 1.108V (see Table 3 on page 22). The default value is 0.72V.

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Table 3: FB_REF Voltage Selection Chart

D[6:0]	V_{REF} (V)	D[6:0]	V_{REF} (V)	D[6:0]	V_{REF} (V)	D[6:0]	V_{REF} (V)
000 0000	0.6	010 0000	0.728	100 0000	0.856	110 0000	0.984
000 0001	0.604	010 0001	0.732	100 0001	0.86	110 0001	0.988
000 0010	0.608	010 0010	0.736	100 0010	0.864	110 0010	0.992
000 0011	0.612	010 0011	0.74	100 0011	0.868	110 0011	0.996
000 0100	0.616	010 0100	0.744	100 0100	0.872	110 0100	1
000 0101	0.62	010 0101	0.748	100 0101	0.876	110 0101	1.004
000 0110	0.624	010 0110	0.752	100 0110	0.88	110 0110	1.008
000 0111	0.628	010 0111	0.756	100 0111	0.884	110 0111	1.012
000 1000	0.632	010 1000	0.76	100 1000	0.888	110 1000	1.016
000 1001	0.636	010 1001	0.764	100 1001	0.892	110 1001	1.02
000 1010	0.64	010 1010	0.768	100 1010	0.896	110 1010	1.024
000 1011	0.644	010 1011	0.772	100 1011	0.9	110 1011	1.028
000 1100	0.648	010 1100	0.776	100 1100	0.904	110 1100	1.032
000 1101	0.652	010 1101	0.78	100 1101	0.908	110 1101	1.036
000 1110	0.656	010 1110	0.784	100 1110	0.912	110 1110	1.04
000 1111	0.66	010 1111	0.788	100 1111	0.916	110 1111	1.044
001 0000	0.664	011 0000	0.792	101 0000	0.92	111 0000	1.048
001 0001	0.668	011 0001	0.796	101 0001	0.924	111 0001	1.052
001 0010	0.672	011 0010	0.8	101 0010	0.928	111 0010	1.056
001 0011	0.676	011 0011	0.804	101 0011	0.932	111 0011	1.06
001 0100	0.68	011 0100	0.808	101 0100	0.936	111 0100	1.064
001 0101	0.684	011 0101	0.812	101 0101	0.94	111 0101	1.068
001 0110	0.688	011 0110	0.816	101 0110	0.944	111 0110	1.072
001 0111	0.692	011 0111	0.82	101 0111	0.948	111 0111	1.076
001 1000	0.696	011 1000	0.824	101 1000	0.952	111 1000	1.08
001 1001	0.7	011 1001	0.828	101 1001	0.956	111 1001	1.084
001 1010	0.704	011 1010	0.832	101 1010	0.96	111 1010	1.088
001 1011	0.708	011 1011	0.836	101 1011	0.964	111 1011	1.092
001 1100	0.712	011 1100	0.84	101 1100	0.968	111 1100	1.096
001 1101	0.716	011 1101	0.844	101 1101	0.972	111 1101	1.1
001 1110	0.72	011 1110	0.848	101 1110	0.976	111 1110	1.104
001 1111	0.724	011 1111	0.852	101 1111	0.98	111 1111	1.108

REG0x01: SYSCNTLREG1

Register 0x01 is the first system control register.

The highest bit, EN, turns the MPQ8861 on and off when the external EN is high. When the external EN is high, the MPQ8861 shuts down by setting the EN bit to 0, and then the HS-FET and LS-FET stop switching. The MPQ8861 resumes switching by setting the EN bit to 1 again. When the external EN is low, the converter is off and the I^2C shuts down.

Set GO_BIT to 1 to enable the I^2C to write FB_REF. When the command is finished, GO_BIT auto-resets to 0 to prevent false V_{OUT} scaling operation.

The IC switches to forced PWM mode when GO_BIT is set to 1 to achieve a smooth output waveform during output dynamic scaling. After output scaling is complete, GO_BIT auto-resets to 0, and the IC operation mode switches to the original mode set by the MODE bit.

The 3-bit SLEW RATE command (D[5:3]) selects the V_{OUT} slew rate during V_{OUT} dynamic scaling. A proper slew rate reduces the inrush current, as well as voltage overshoot and undershoot. Eight different slew rate levels can be selected.

The RETRY_OVP bit defines the protection mode when OVP is triggered. If RETRY_OVP is set to 1, then the part enters auto-recovery once OVP is removed. If RETRY_OVP is set to 0, then the MPQ8861 latches off once output OVP occurs, and VIN OVP is triggered until VIN or EN are toggled.

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The HICCUP_OCP bit defines the OCP mode. If HICCUP_OCP is set to 1, then the MPQ8861 enters hiccup mode once OCP and UVP are both triggered. If HICCUP_OCP is set to 0, then the MPQ8861 latches off by simultaneously triggering OCP and UVP.

The lowest bit, MODE, selects forced PWM or auto-PFM/PWM mode at light loads. If MODE is set to 0, auto-PFM/PWM mode is enabled at light loads. If MODE is set to 1, forced PWM mode is enabled at light loads.

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th>Description</th></tr>
<tr><td>EN</td><td>D[7]</td><td>1</td><td>I²C controlled start-up or shutdown. When the external EN is low, the converter is off and the I²C shuts down. When EN is high, the EN bit takes over. The default value for EN is 1.</td></tr>
<tr><td>GO_BIT</td><td>D[6]</td><td>0</td><td>Sets the I²C write capability for the FB reference command. Set GO_BIT = 1 to enable the I²C to write the FB reference. When the command is finished, GO_BIT auto-resets to 0 to prevent false V_{REF} scaling operation.
FB_REF voltage scaling examples:
1. Set GO_BIT = 1.
2. Write register 0x00, and set the FB_REF.
3. Read back the GO_BIT value to see if output scaling is finished. If GO_BIT = 0, the voltage scaling is done. Otherwise, V_{REF} is still in adjustment.
4. Set GO_BIT = 1 if V_{OUT} scaling is needed a second time.
5. Write register 0x00, and set the FB_REF.</td></tr>
<tr><td>SLEW_RATE</td><td>D[5:3]</td><td>100</td><td>The slew rate during I²C-controlled voltage scaling is set by 3 bits. V_{OUT} changes linearly from the previous voltage to the new set voltage with a V_{OUT} slew rate (see the table below). This helps significantly reduce inrush current, voltage overshoot, and voltage undershoot.
<table>
<tr><th>D[5:3]</th><th>Slew Rate</th><th>D[5:3]</th><th>Slew Rate</th></tr>
<tr><td>000</td><td>19mV/µs</td><td>100</td><td>2.5mV/µs</td></tr>
<tr><td>001</td><td>15mV/µs</td><td>101</td><td>1.25mV/µs</td></tr>
<tr><td>010</td><td>10mV/µs</td><td>110</td><td>0.6mV/µs</td></tr>
<tr><td>011</td><td>5mV/µs</td><td>111</td><td>0.3mV/µs</td></tr>
</table></td></tr>
<tr><td>RETRY_OVP</td><td>D[2]</td><td>1</td><td>OVP mode selection bit. If this bit is set to 1, the part auto-recovers when OVP is removed. If this bit is set to 0, the part latches off once output OVP (including absolute OVP) and V_{IN} OVP are both triggered, and remains off until VIN or EN is power reset.</td></tr>
<tr><td>HICCUP_OCP</td><td>D[1]</td><td>1</td><td>Enables OCP mode selection.
1: Hiccup mode OCP
0: Latch-off OCP</td></tr>
<tr><td>MODE</td><td>D[0]</td><td>0</td><td>Set this bit to 0 to enable PFM mode; set it to 1 to disable auto-PFM/PWM mode. The default is auto-PFM/PWM mode for light loads.</td></tr>
</table>

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REG0x02: SYSCNTLREG2

Register 0x02 is the second system control register.

The highest 2 bits of the PG_DEGLITCH_TIME D[7:6] define the PG signal rising and falling edge delay times. If output OVP or UVP is triggered, the PG signal goes low or high after a set delay time. Four PG delay times can be programmed by the I^2C for different conditions.

The 2 FSW bits D[5:4] are used for f_{SW} selection. The MPQ8861 supports a f_{SW} up to 1.25MHz by setting the 2 bits to 11. The MPQ8861 maximum configurable f_{SW} is limited by the internal minimum on time (see Table 1 on page 14).

The SOFT_STOP bit defines the V_{OUT} discharge behavior after EN shutdown. When SOFT_STOP is set to 0, V_{OUT} is not discharged after EN shutdown. When SOFT_STOP is set to 1, V_{OUT} is discharged linearly to 0V with the set soft shutdown time.

The lowest 3 bits, CURRENT_LIMIT_ADJUST D[2:0], are used for peak and valley current limit selection. Eight current limit levels can be selected for different application conditions.

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th>Description</th></tr>
<tr><td>PG_ DEGLITCH_ TIME</td><td>D[7:6]</td><td>11</td><td>Sets the PG signal rising and falling edges' delay time. When FB or VOUT is out of the regulation window, the PG comparator is triggered, but requires a delay time before the PG signal goes high or low.
<table>
<tr><th>D[7:6]</th><th>PG Deglitch Time</th><th>D[7:6]</th><th>PG Deglitch Time</th></tr>
<tr><td>00</td><td><1µs</td><td>10</td><td>12µs</td></tr>
<tr><td>01</td><td>6µs</td><td>11</td><td>30µs</td></tr>
</table></td></tr>
<tr><td>FSW</td><td>D[5:4]</td><td>00</td><td>Sets the switching frequency (f_{SW}). There is no dedicated frequency oscillator inside the part. f_{SW} is kept fairly constant by controlling the t_{ON} timer.
<table>
<tr><th>D[5:4]</th><th>Frequency</th><th>D[5:4]</th><th>Frequency</th></tr>
<tr><td>00</td><td>500kHz</td><td>10</td><td>1MHz</td></tr>
<tr><td>01</td><td>750kHz</td><td>11</td><td>1.25MHz</td></tr>
</table></td></tr>
<tr><td>SOFT_STOP</td><td>D[3]</td><td>0</td><td>Defines the V_{OUT} discharge behavior after EN shutdown.
0: V_{OUT} is not discharged after EN shutdown
1: V_{OUT} is discharged linearly to zero with the set soft shutdown time</td></tr>
<tr><td>CURRENT_ LIMIT_ ADJUST</td><td>D[2:0]</td><td>010</td><td>
<table>
<tr><th>D[2:0]</th><th>Valley Current Limit (A)</th><th>D[2:0]</th><th>Valley Current Limit (A)</th></tr>
<tr><td>000</td><td>19</td><td>100</td><td>10</td></tr>
<tr><td>001</td><td>16</td><td>101</td><td>8.5</td></tr>
<tr><td>010</td><td>14</td><td>110</td><td>7</td></tr>
<tr><td>011</td><td>12</td><td>111</td><td>6</td></tr>
</table></td></tr>
</table>

REG0x03 and REG0x04

Register 0x03 and register 0x04 are reserved for future use.

REG0x05: ID1

Register 0x05 is the IC identification register. The highest 4 bits, VENDOR_ID D[7:4], are set to 1000 internally, and represent the vendor ID.

The lowest 4 bits, IC_REVISION_ID, indicate the IC revision information.

Name	Bits	Description
VENDOR_ID	D[7:4]	1000.
IC_REVISION_ID	D[3:0]	IC revision (0000).

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REG0x06: STATUS

Register 0x06 is a fault condition indication register. The highest 4 bits, D[7:4], are reserved for future use.

The OC bit is the output over-current indicator. When this bit is set to 1, the IC is in hiccup mode or OC latch-off mode.

The OTEW bit is the die temperature early warning indicator. When the bit is set to 1, the IC die temperature is above 120°C.

The PG bit is output power good (PG) indicator. When this bit is set to 1, the output power (P_{OUT}) is normal.

Name	Bits	Description
RESERVED	D[7:4]	Reserved for future use.
OC	D[3]	Output over-current (OC) indicator. When this bit is high, the IC is in hiccup mode or the OC latch-off mode.
OTEW	D[2]	Die temperature early warning bit. When this bit is high, the die temperature is above 120°C. When the die temperature is below 100°C, the bit goes low.
OT	D[1]	Over-temperature (OT) indicator. When this bit is high, the IC is in thermal shutdown.
PG	D[0]	Output power good (PG) indicator. When this bit is high, V_{OUT} power is normal, which means V_{OUT} is above 90% and below 115% of V_{REF}. PG compares FB/VOUT with FB_REF.

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APPLICATION INFORMATION

Setting V_{OUT} via the FB Control Loop

The MPQ8861 can be controlled by the FB loop. V_{OUT} can be set by the external resistor dividers. The FB loop V_{REF} default value is 0.72V, and can be configured by the I^2C. The MPQ8861's V_{OUT} must be below the absolute OVP threshold (typically 6.5V).

Figure 13 shows the FB loop network.

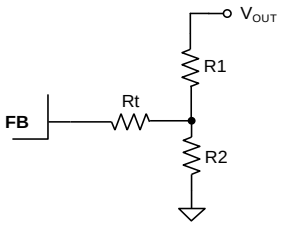

Figure 13: FB Loop Network

Calculate R1 and R2 using Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.72V} - 1} \quad (4)$$

Table 4 shows the recommended FB resistors value for common output voltages. The recommended parameters are based on 3 x 47µF output capacitors (C_{OUT}). Different V_{IN} and C_{OUT} values may affect the selection of R1 and R2. For other component parameters, please see the Typical Application Circuits section on page 30.

Table 4: Resistor Selection for Common Output Voltages

V_{IN} (V)	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)	L (µH)
5	0.85	16.5	90.9	10	0.47
5	1.0	36.5	93.1	10	0.68
5	1.2	36.5	54.9	10	0.68
5	1.5	36.5	33.2	10	0.68
5	1.8	36.5	24.3	10	0.68
5	2.5	36.5	14.7	10	1
5	3.3	36.5	10.2	10	0.68
12	0.85	16.5	90.9	10	1
12	1.0	36.5	93.1	10	1
12	1.2	36.5	56	10	1
12	1.5	36.5	33.2	10	1
12	1.8	80.6	53.6	10	1.5
12	2.5	80.6	32.4	10	1.5
12	3.3	80.6	22.6	10	2.2
12	5	80.6	13.7	10	2.2

V_{OUT} Dynamic Scaling

V_{OUT} dynamic scaling can only be done via the I^2C. See Figure 14 and follow the steps below:

1. Write GO_BIT (REG01, bit[6]) to 1.
2. Write REG0x00 to set V_{REF} by FB_REF (REG0x00, bits[6:0]) simultaneously. When the command is finished, GO_BIT auto-resets to 0 to prevent false V_{OUT} scaling operation.

Repeat the above two steps if V_{OUT} must be changed to a different voltage.

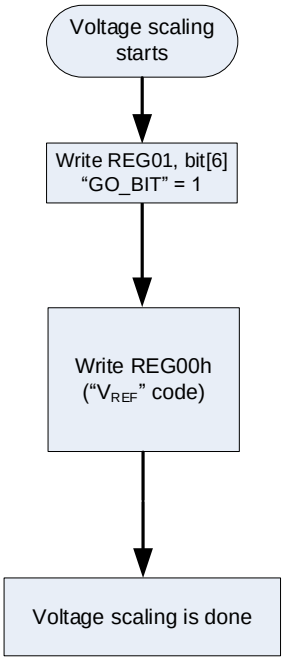

Figure 14: V_{OUT} Dynamic Scale Flowchart

Selecting the Inductor

Use a 0.47µH to 5µH inductor with a DC current rating at least 25% greater than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance below 5mΩ. For most designs, the inductance (L_1) can be derived using Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

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Select the inductor ripple current to be approximately 30% of the maximum load current and below 4A. The maximum inductor peak current ($I_{L(MAX)}$) can be calculated using Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

See Table 4 on page 26 for the recommended inductor values for common output and input voltages.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to use two 22µF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated using Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

The V_{IN} ripple caused by the capacitance can be estimated using Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the V_{OUT} ripple low. The V_{OUT} ripple (ΔV_{OUT}) can be estimated using Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (10)$$

Where L_1 is the inductance, and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of the V_{OUT} ripple. For simplification, the V_{OUT} ripple (ΔV_{OUT}) can be estimated using Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, the output voltage ripple (ΔV_{OUT}) can be approximated using Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ8861 can be optimized for a wide range of capacitance and ESR values.

External BST Diode

An external BST diode can enhance the efficiency of the regulator, given the following conditions:

- V_{OUT} is 5V or 3.3V
- The duty cycle is high (D > 50%)

In these cases, add an external BST diode from VCC to BST (see Figure 15 on page 28).

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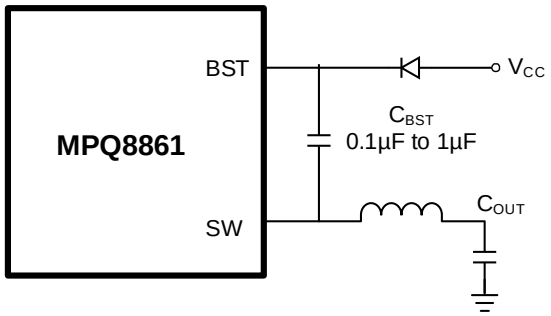

Figure 15: Optional External BST Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended C_{BST} value is 0.1µF to 1µF.

Connect VCC to VIN at a Low V_{IN}

VCC can be connected directly to VIN when V_{IN} is below 3.5V. This helps improve the MPQ8861's efficiency performance.

To use this application set-up, the VIN spike voltage must be limited below 4V, otherwise VCC may be damaged.

Design Example

Table 5 shows a design example following the application guidelines for the specifications below.

Table 5: Design Example

V_{IN}	V_{OUT}	I_{OUT}
5V	1V	12A

Figure 17 through Figure 31 on pages 30–34 show the detailed application schematics. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheet.

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PCB Layout Guidelines [8]

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 16 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SW) as close as possible to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large copper planes.
3. Use at least 2 layers for the VIN and PGND traces to achieve better thermal performance.
4. Add several vias close to the IN and PGND pads to support thermal dissipation. Place more than one via adjacent to the inner edge of PGND pad, which connects to the AGND pad through low-impedance routing or a ground plane.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and PGND as possible.
7. Add several vias close to the AGND pad, then connect to the PGND plane using a Kelvin connection.
8. Place the external FB resistors next to FB.
9. Ensure that there is no via on the FB trace.
10. Keep the switching node (SW) short and away from the feedback network.
11. Keep the BST voltage path (BST, C3, and SW) as short as possible.

Note:

8) The recommended layout is based on the Typical Application Circuits section on page 30.

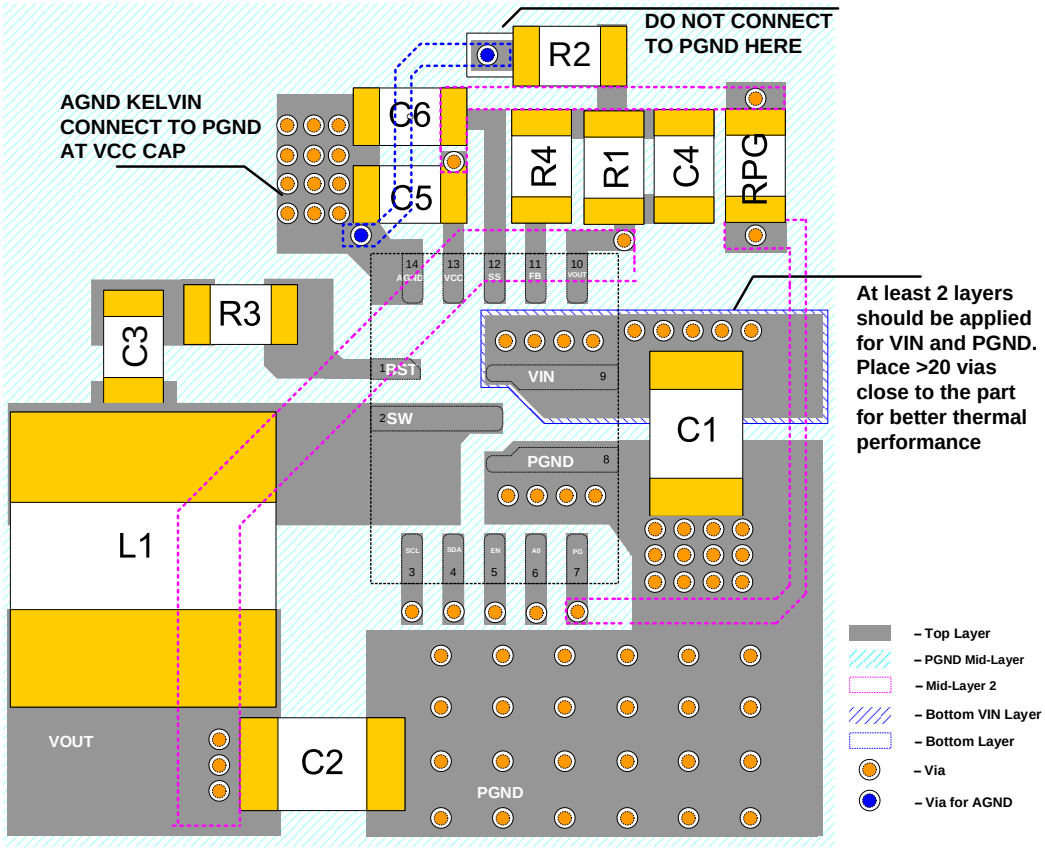

Figure 16: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS (9)

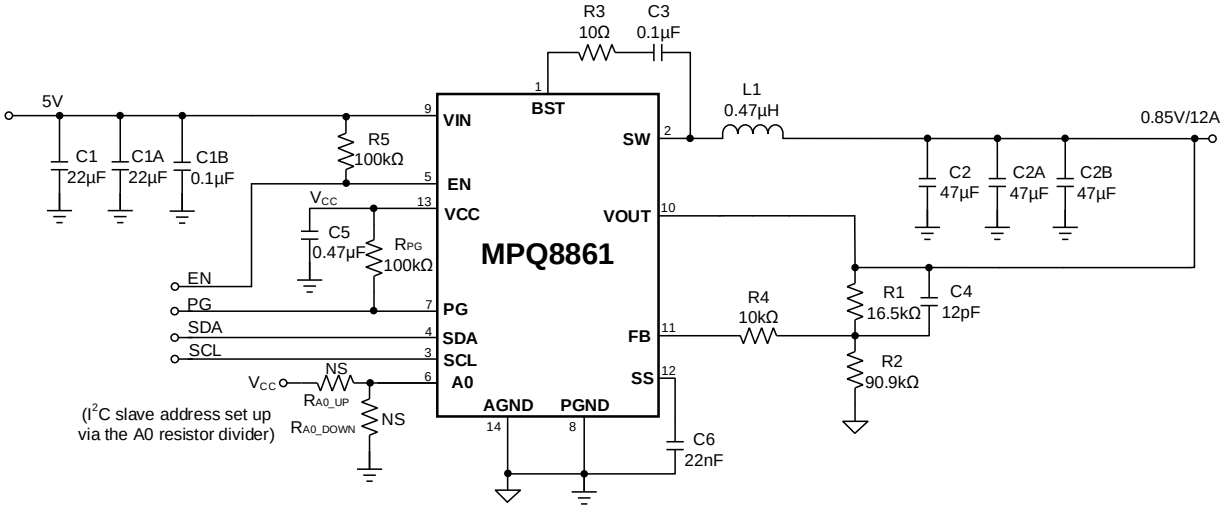

Figure 17: V_{IN} = 5V, V_{OUT} = 0.85V, I_{OUT} = 12A

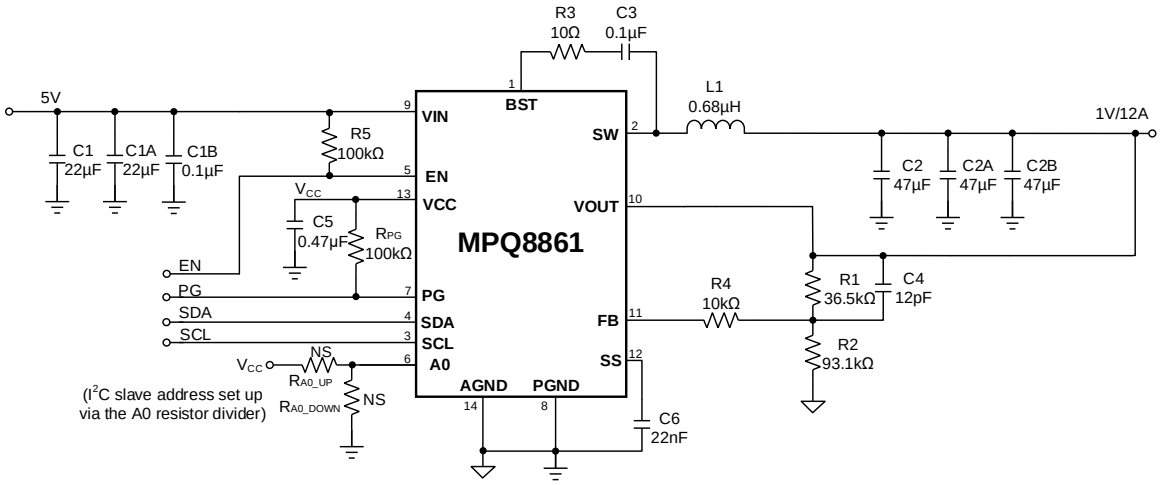

Figure 18: V_{IN} = 5V, V_{OUT} = 1V, I_{OUT} = 12A

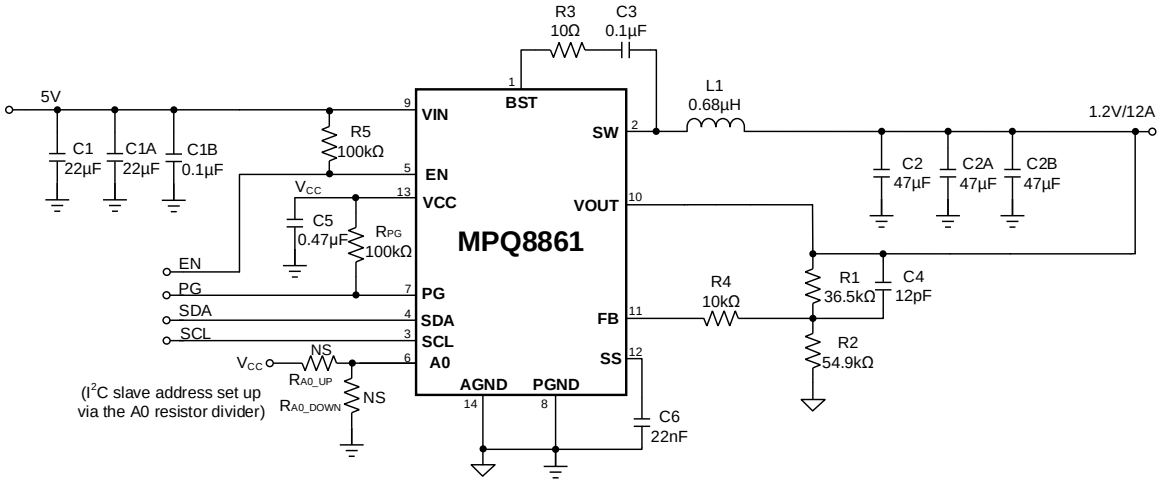

Figure 19: V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 12A

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TYPICAL APPLICATION CIRCUITS *(continued)* (9)

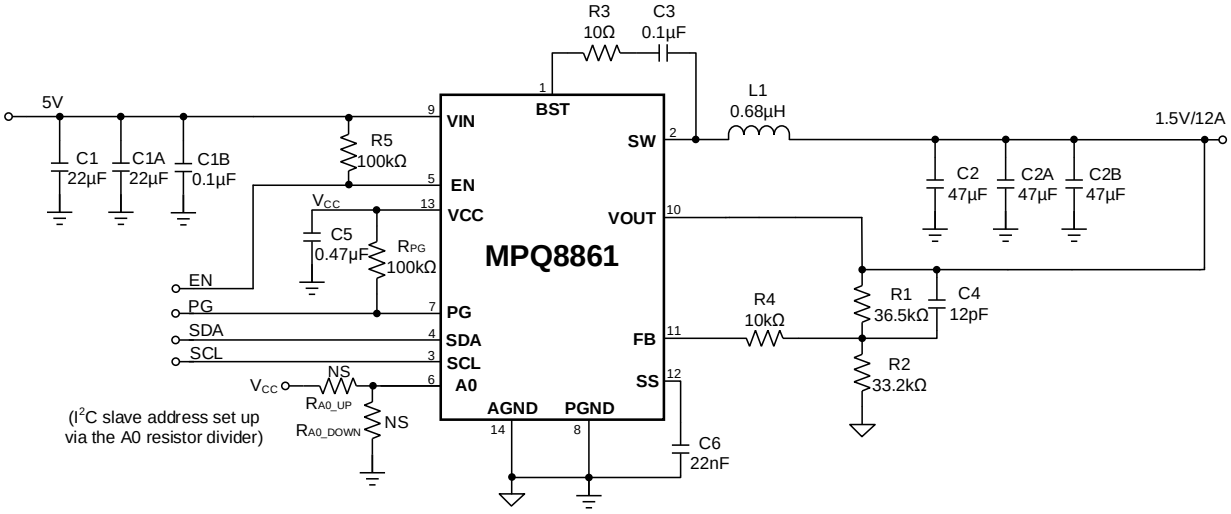

Figure 20: V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 12A

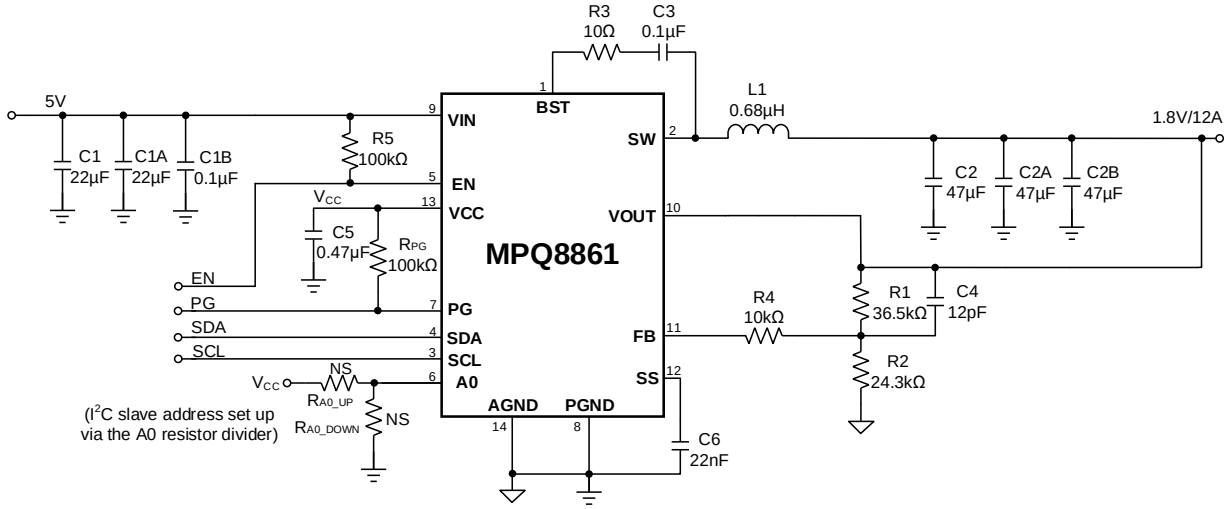

Figure 21: V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 12A

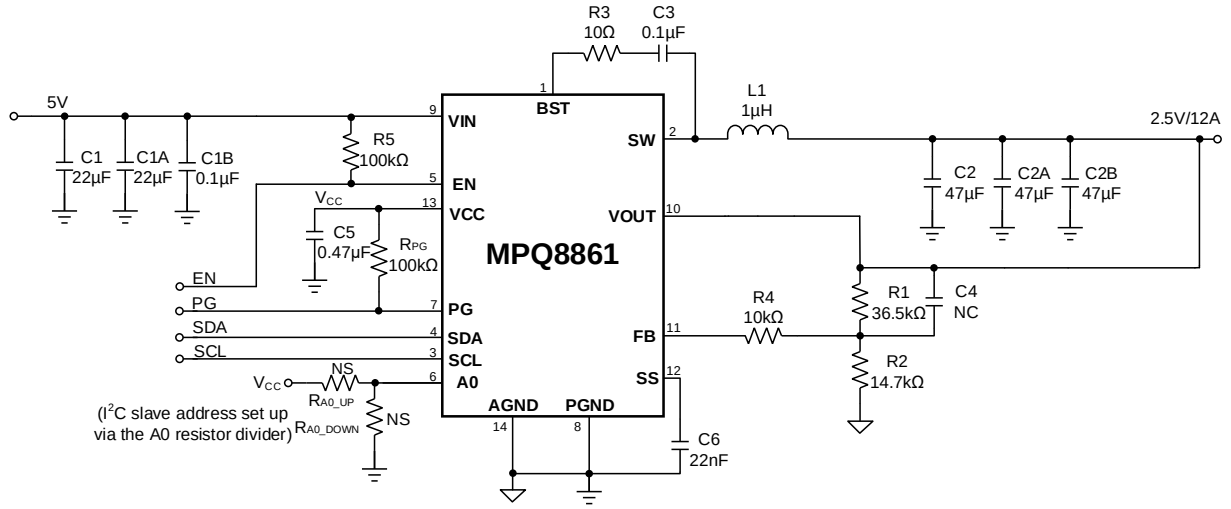

Figure 22: V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 12A

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TYPICAL APPLICATION CIRCUITS *(continued)* (9)

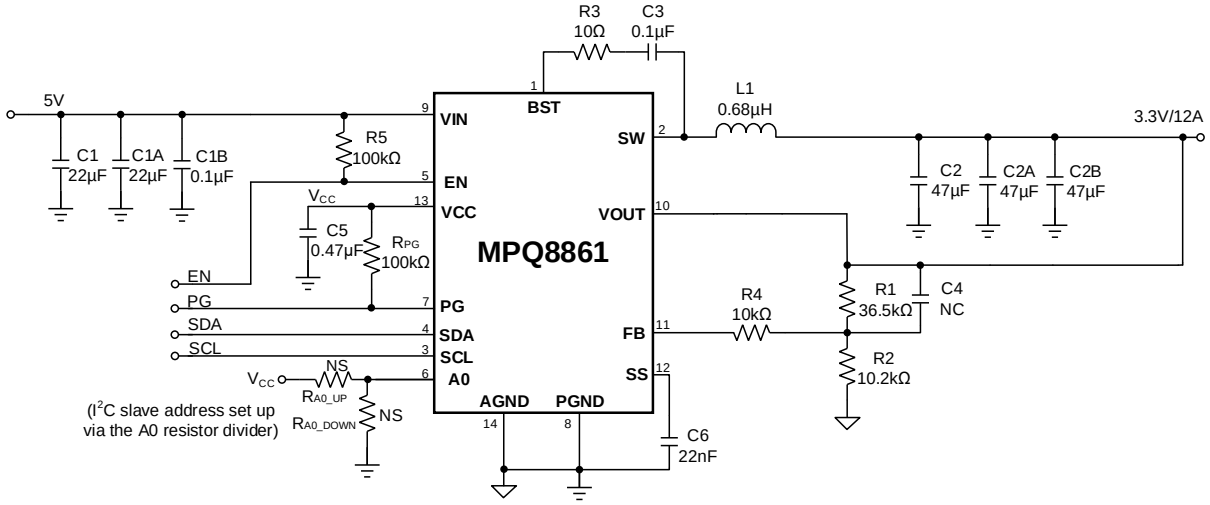

Figure 23: V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 12A

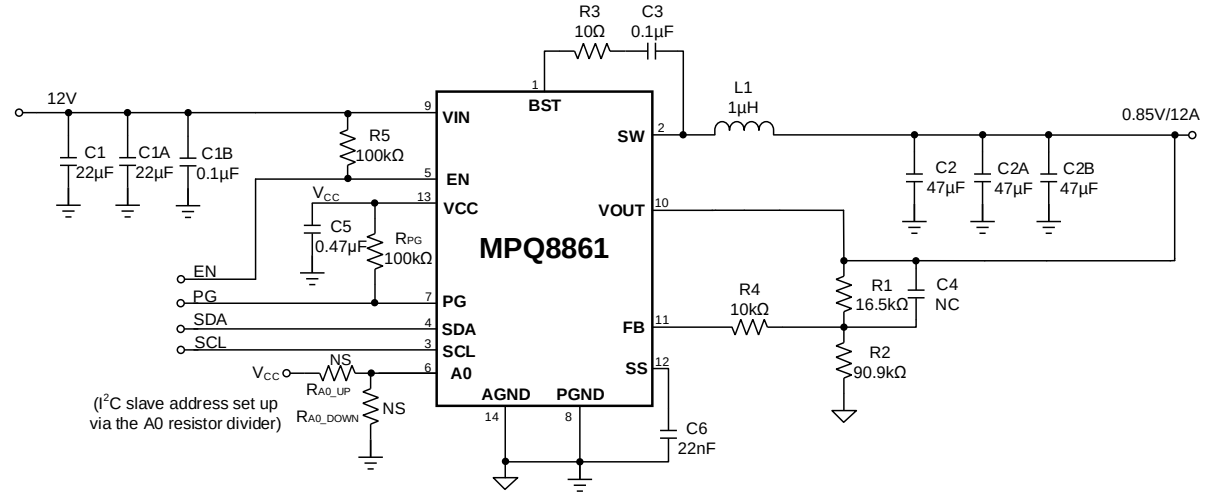

Figure 24: V_{IN} = 12V, V_{OUT} = 0.85V, I_{OUT} = 12A

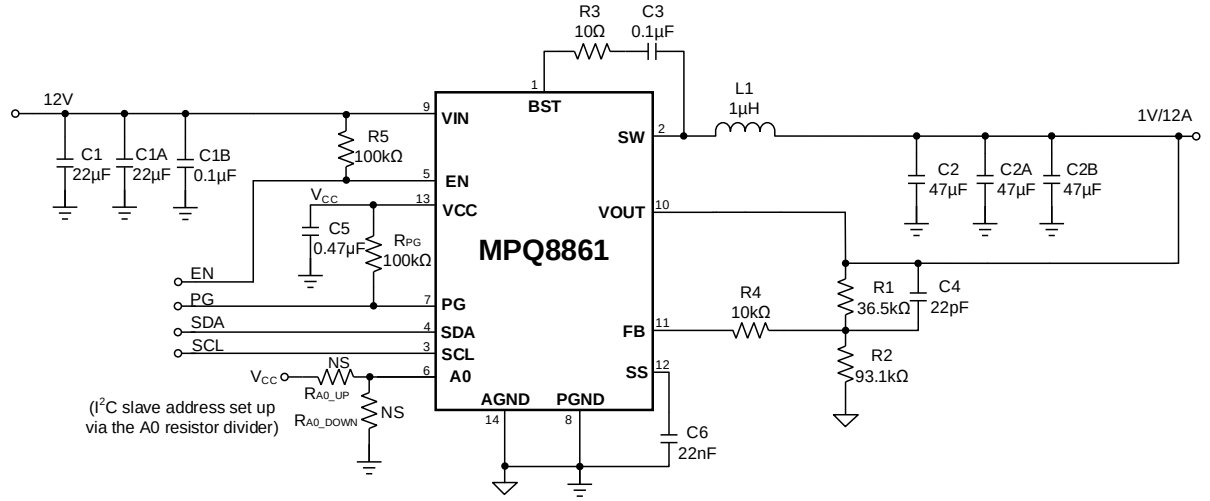

Figure 25: V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A

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TYPICAL APPLICATION CIRCUITS *(continued)* (9)

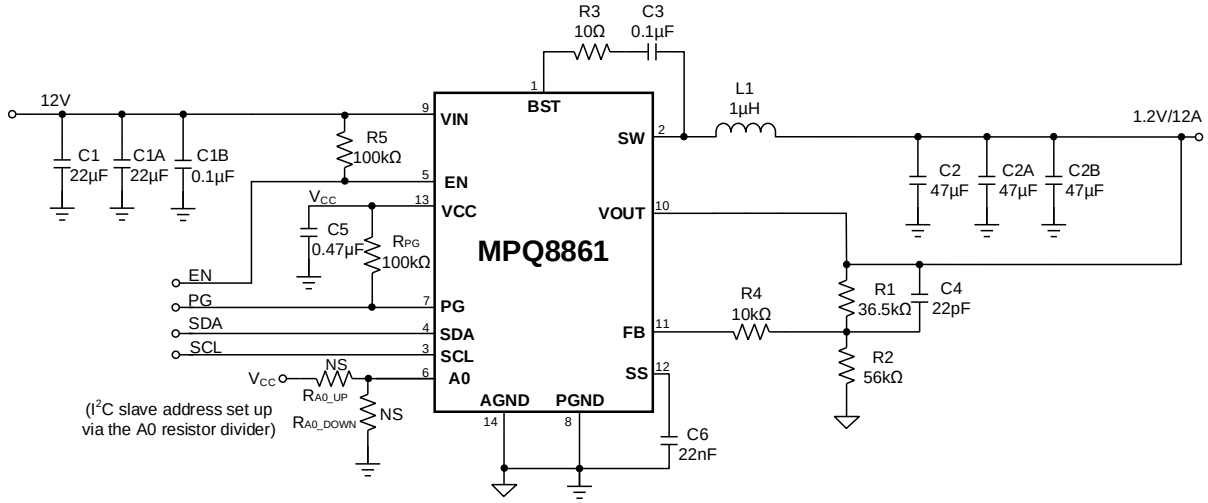

Figure 26: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 12A

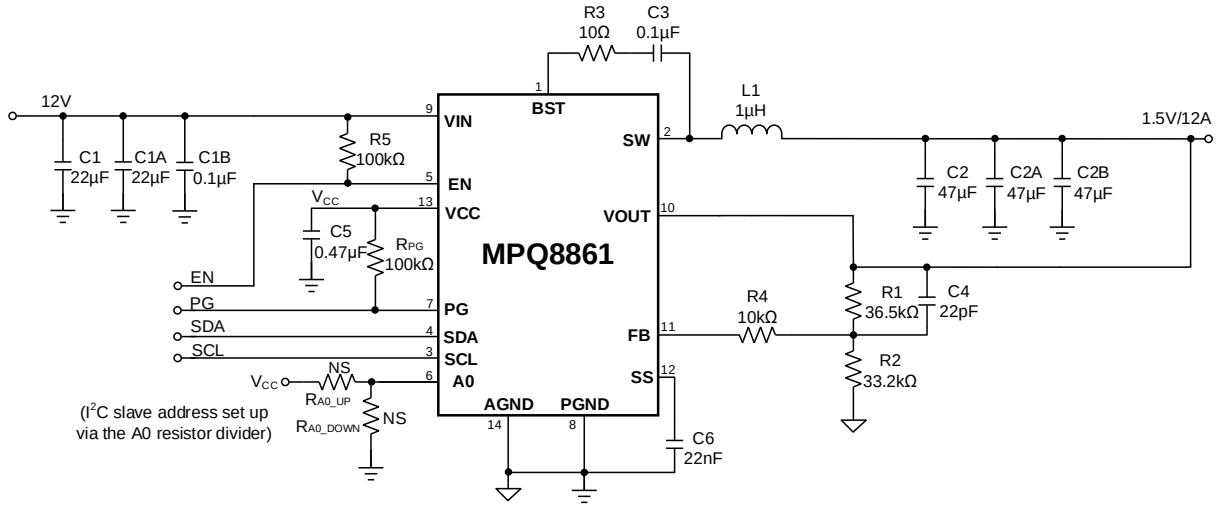

Figure 27: V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A

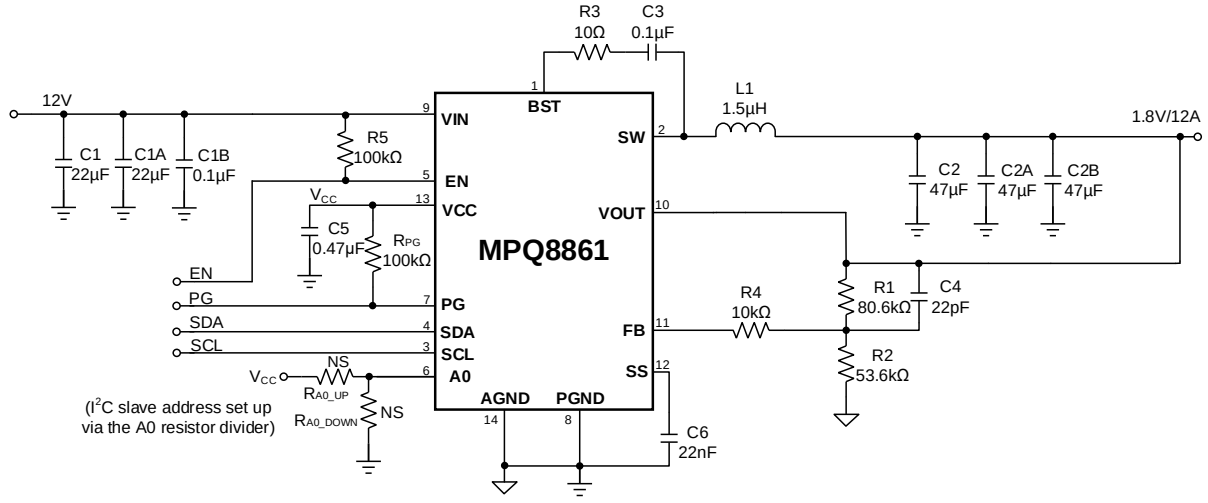

Figure 28: V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 12A

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TYPICAL APPLICATION CIRCUITS *(continued)* (9)

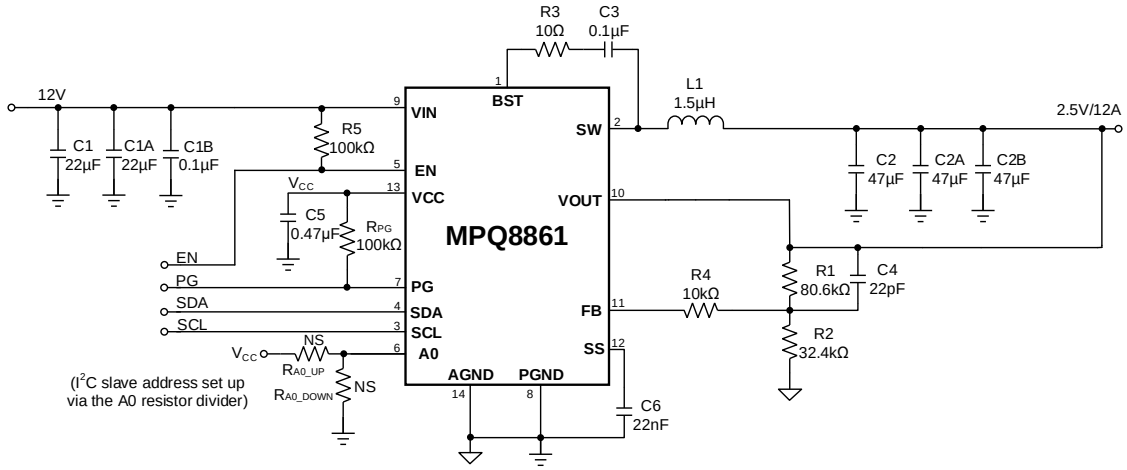

Figure 29: V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 12A

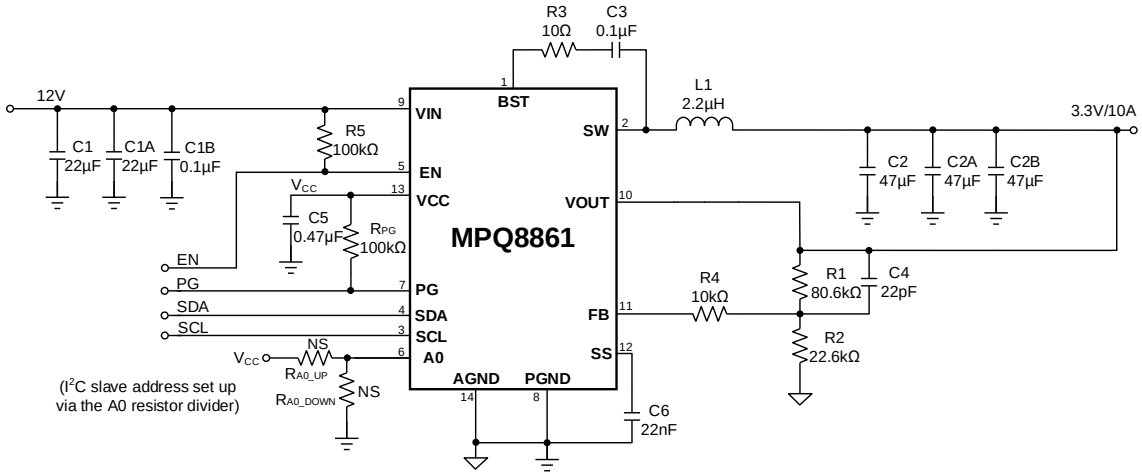

Figure 30: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 10A

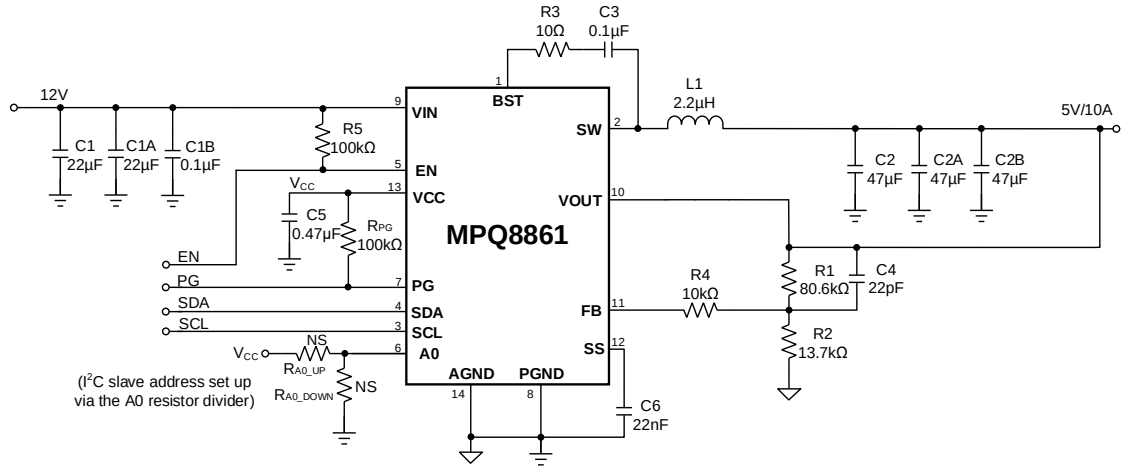

Figure 31: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 10A

Note:

9) All circuits are based on a 0.72V default V_{REF}. The MPQ8861's V_{OUT} can be adjusted by the FB V_{REF} and external resistor dividers. However, the MPQ8861's V_{OUT} must be set below the absolute OVP threshold (typically 6.5V). When the I^2C function is not used, SCL/SDA should be connected to VCC.

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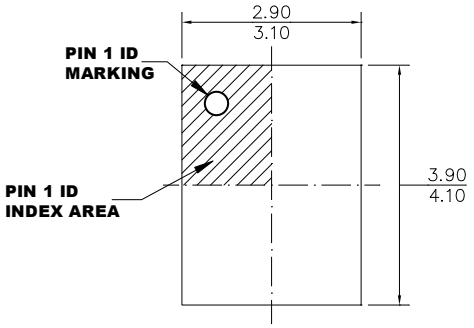
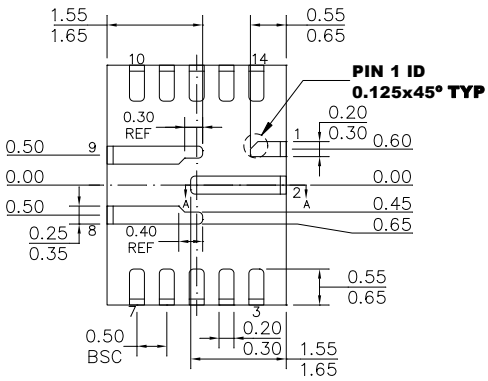
PACKAGE INFORMATION

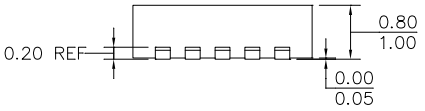
QFN-14 (3mmx4mm)



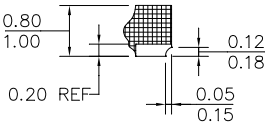
TOP VIEW



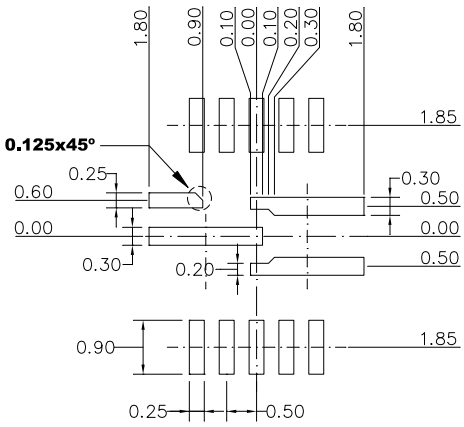
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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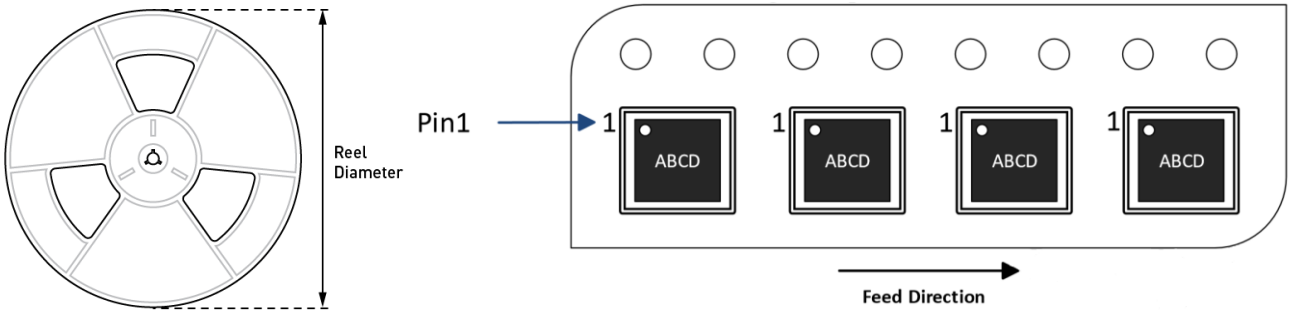
CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ8861GLE-AEC1-Z	QFN-14 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/18/2021	Initial Release	-

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