MPQ86750

50A, Monolithic, Half-Bridge Intelli-Phase™ Solution in LGA-38 (5mmx6mm) Package, AEC-Q100 Qualified

DESCRIPTION

The MPQ86750 is a monolithic, half-bridge Intelli-Phase™ solution with built-in internal power MOSFETs and gate drivers. It can achieve up to 50A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range.

The integrated MOSFETs and drivers achieve high efficiency through an optimized dead time (DT) and reduced parasitic inductance.

This device is compatible with tri-state output controllers. It also includes a general-purpose current sensing and temperature sensing.

The MPQ86750 is ideal for autonomous driving applications, where efficiency and compact size are at a premium. It is available in an LGA-38 (5mmx6mm) package, and is AEC-Q100 qualified.

FEATURES

- Wide Operating Input Voltage (V_{IN}) Range
- 50A Output Current (I_{OUT})
- Accepts Tri-State PWM Signal
- Built-In Switch for Bootstrap (BST)
- Accu-Sense™ Current Sense
- Temperature Sense
- Current-Limit Protection and Fault Flag
- OTP and Fault Flag
- Catastrophic Protection and Fault Flag
- Used for Multi-Phase Operation
- Available in an LGA-38 (5mmx6mm) Package
- Available in AEC-Q100 Grade 1

MPSafe™ Q M — Developed for Functional Safety Applications: ISO 26262 Compliant

APPLICATIONS

- Autonomous Driving System-on-Chips (SoCs)
- Infotainment Systems

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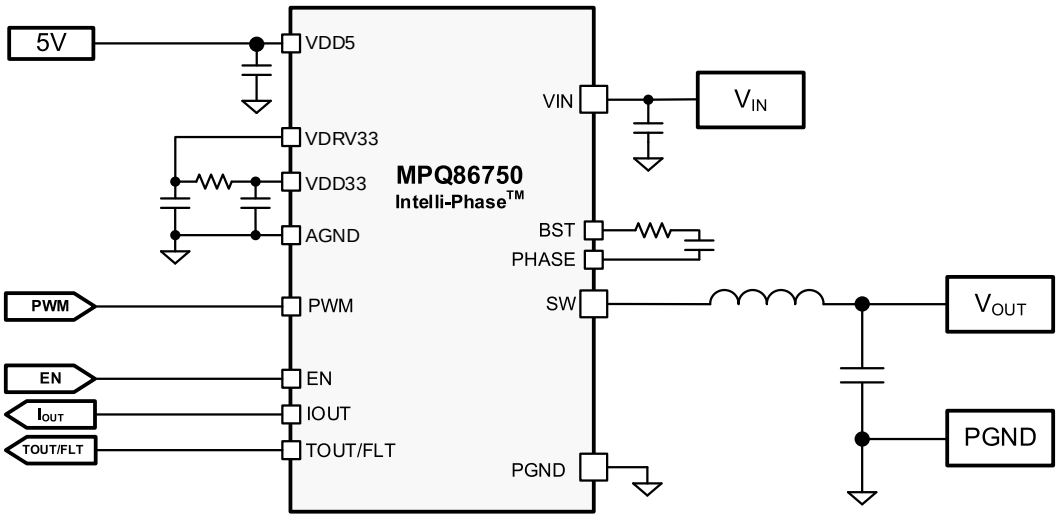
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ86750GMJT-AEC1	LGA-38 (5mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ86750GMJT-AEC1-Z).

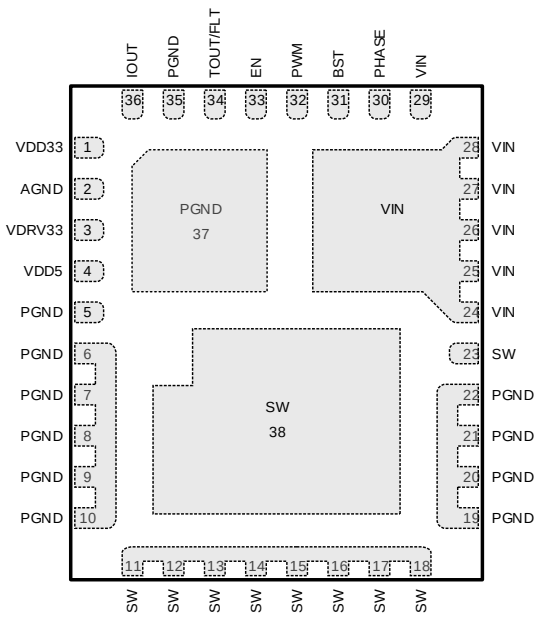
TOP MARKING

MPSYYWW
MP86750
LLLLLLL
T

MP: MPS prefix
YY: Year code
WW: Week code
MP86750: Part number
LLLLLLL: Lot number
T: Thin

PACKAGE REFERENCE

TOP VIEW



LGA-38 (5mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	VDD33	**3.3V power supply for internal logic.** Connect the VDD33 pin to the VDRV33 pin through a 2.2Ω resistor. Decouple the VDD33 pin with a 1µF capacitor connected to AGND. Connect AGND and PGND at the VDD33 capacitor.
2	AGND	**Analog ground.**
3	VDRV33	**Internal LDO output for driver voltage.** Decouple the VDRV33 pin with a 1µF to 4.7µF ceramic capacitor.
4	VDD5	**5V power supply.** Connect the VDD5 pin to a 5V supply, and decouple this pin with a 1µF to 4.7µF ceramic capacitor.
5, 6, 7, 8, 9, 10, 19, 20, 21, 22, 35, 37	PGND	**Power ground.**
11, 12, 13, 14, 15, 16, 17, 18, 23, 38	SW	**Phase node.**
24, 25, 26, 27, 28, 29	VIN	**Input supply voltage.** Place the ceramic input capacitor (C_{IN}) close to the device to support the switching current and minimize parasitic inductance.
30	PHASE	**Switch node for bootstrap capacitor connection.** The PHASE pin is internally connected to the SW pin.
31	BST	**Bootstrap.** The BST pin requires a 0.1µF to 0.47µF capacitor to drive the power MOSFET's gate above the supply voltage. Connect the capacitor between the BST and PHASE pins to form a floating supply across the power MOSFET driver.
32	PWM	**Pulse width modulation input.** Float the PWM pin or drive PWM to a middle-state to force SW into a high-impedance (Hi-Z) state.
33	EN	**Enable.** Pull the EN pin high to enable the device; pull EN low to disable the device and force SW into a high-impedance (Hi-Z) state.
34	TOUT/ FLT	**Single-pin temperature sense and fault reporting.** If a fault occurs, the TOUT/FLT pin is pulled up to the VDD33 pin's voltage (V_{DD33}).
36	IOUT	**Current-sense output.** Connect an external resistor to the IOUT pin to adjust the IOUT voltage (V_{IOUT}), which is proportional to the inductor current (I_L).

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) (DC)..... 26V
V_{IN} (25ns).....-3V to +28V
V_{SW} (DC) .....-0.3V to +24V
V_{SW} (25ns).....-3V to +28V
V_{BST} (DC) ..... V_{SW} + 4V
V_{BST} to V_{SW} (25ns) (2) 5V
V_{DD5}.....-0.3V to +6.5V
V_{DD33}, V_{DRV33}.....-0.3V to +4V
AGND, PGND .....-0.3V to +0.3V
Instantaneous current $I_{INSTANTANEOUS}$ (20ms)……
…… 60A
Instantaneous current $I_{INSTANTANEOUS}$ (10µs)…….
……...100A
All other pins .....-0.3V to +4V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (3)

Human body model (HBM) .....Class 2
Charged-device model (CDM) ..... Class C2b

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....3V to 22V
Supply voltage (V_{DD5}).....4.5V to 5.5V
Supply voltage (V_{DRV33}) .....3V to 3.6V
Logic voltage (V_{DD33}) .....3V to 3.6V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (5) θ_{JB} θ_{JC_TOP}

LGA-38 (5mmx6mm) ……...2.6…...9.…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For the AMR of a shorter pulse (<25ns), contact an MPS FAE for the related application note.
3) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 22V, V_{DD5} = 5V, EN = 3.3V, T_A = 25°C for typical value and T_A = -40°C to +150°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold			2.4	2.6	2.95	V
V_{IN} UVLO threshold hysteresis				240		mV
VDRV33 regulator output voltage	V_{DRV33}	I_{VDRV33} = 0mA	3.3	3.45	3.6	V
VDRV33 regulator load capability	V_{DRV33}	I_{VDRV33} = 40mA	3			V
V_{IN} quiescent current in standby mode	I_{IN_STBY}	PWM = low, EN = low, V_{IN} = 22V, T_A = 25°C		5	10	µA
V_{IN} quiescent current in active mode	$I_{IN_QUIESCENT}$	PWM = low, EN = high, V_{IN} = 22V, T_A = 25°C		20	40	µA
VDD5 standby current	I_{VDD5_STBY}	VDRV33 and VDD33 supplied by the internal LDO, EN = low, PWM = low		300	500	µA
VDD5 quiescent current	$I_{VDD5_QUIESCENT}$	VDRV33 and VDD33 supplied by the internal LDO, EN = high, PWM = low		3.1	5	mA
VDD5 voltage UVLO rising threshold			2.4	2.75	2.95	V
VDD5 voltage UVLO hysteresis				270		mV
VDD33 voltage UVLO rising threshold			2.4	2.75	2.95	V
VDD33 voltage UVLO threshold hysteresis				270		mV
VDRV33 voltage UVLO rising threshold			2.4	2.75	2.95	V
VDRV33 voltage UVLO threshold hysteresis				270		mV
High-side current limit				100		A
Low-side current limit				-25		A
Dead time when SW is rising (6)				2.5		ns
Dead time when SW is falling (6)		Positive inductor current (I_L)		10		ns
		Negative I_L		20		ns
EN input high threshold voltage			1.3			V
EN input low threshold voltage					0.9	V
EN turn-on delay time (6)		V_{IN} = 5V, PWM = high		30		µs
PWM high to SW rising delay (6)	t_{RISING}			20		ns
PWM low to SW falling delay (6)	$t_{FALLING}$			20		ns
PWM tri-state to SW Hi-Z delay (6)	t_{LT}			50		ns
	t_{TL}			25		ns
	t_{HT}			50		ns
	t_{TH}			20		ns
Minimum PWM pulse width (6)				30		ns
IOUT sense gain				5		µA/A
IOUT sense gain accuracy		20A ≤ I_{SW} ≤ 40A	-5	0	+5	%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 22V, V_{DD5} = 5V, EN = 3.3V, T_A = 25°C for typical value and T_A = -40°C to +150°C for max and min values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IOUT sense offset		I_{SW} = 0A, V_{IOUT} = 1.2V	-10	0	+10	µA
		PWM = Hi-Z, V_{IOUT} = 1.2V	-2	0	+2	µA
IOUT pin voltage range	V_{IOUT}		0.8		2	V
TOUT/FLT sense gain (6)				8		mV/°C
TOUT/FLT voltage		T_J = 25°C		800		mV
Over-temperature (OT) fault latch-off (6)				170		°C
TOUT/FLT when a fault occurs		I_{FAULT} = 0.5mA	3			V
PWM resistance		Pull up, EN = high		6		kΩ
		Pull down		5		kΩ
PWM logic high voltage			2.3			V
PWM tri-state region			1.1		2	V
PWM logic low voltage					0.8	V

Note:

6) Guaranteed by design. Not tested in production.

PWM TIMING DIAGRAM

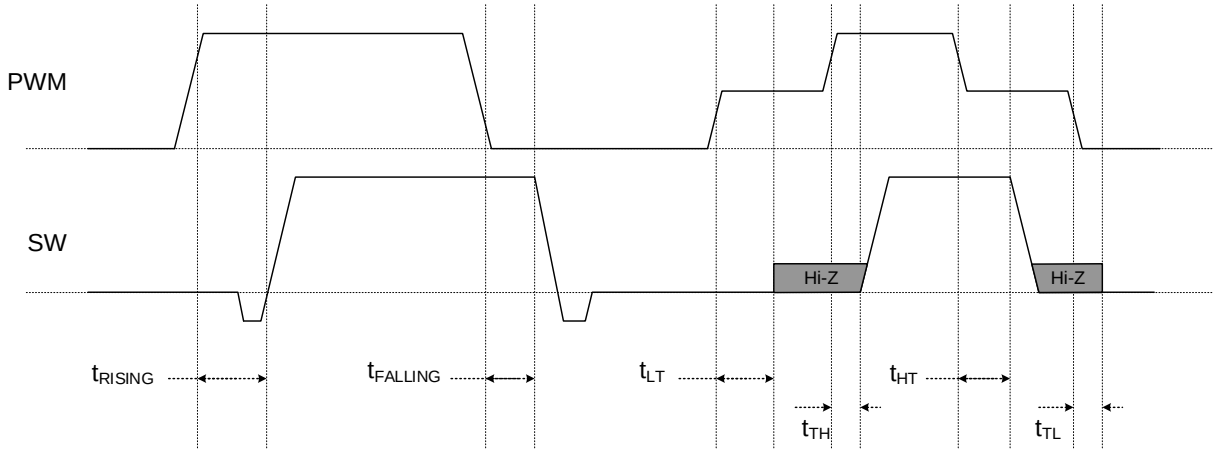

Figure 1: PWM Timing Diagram

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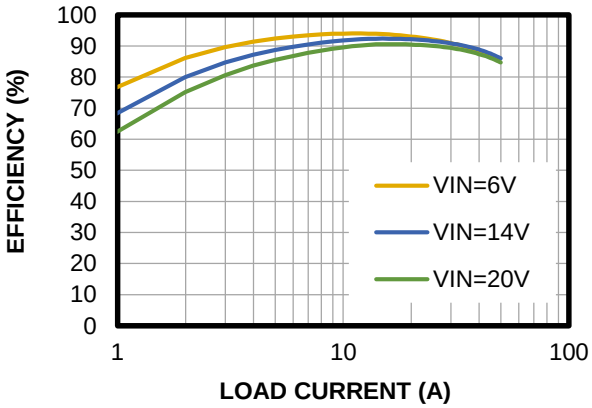
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs. Load Current

V_{OUT} = 0.85V, f_{SW} = 450kHz, L = 220nH



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FUNCTIONAL BLOCK DIAGRAM

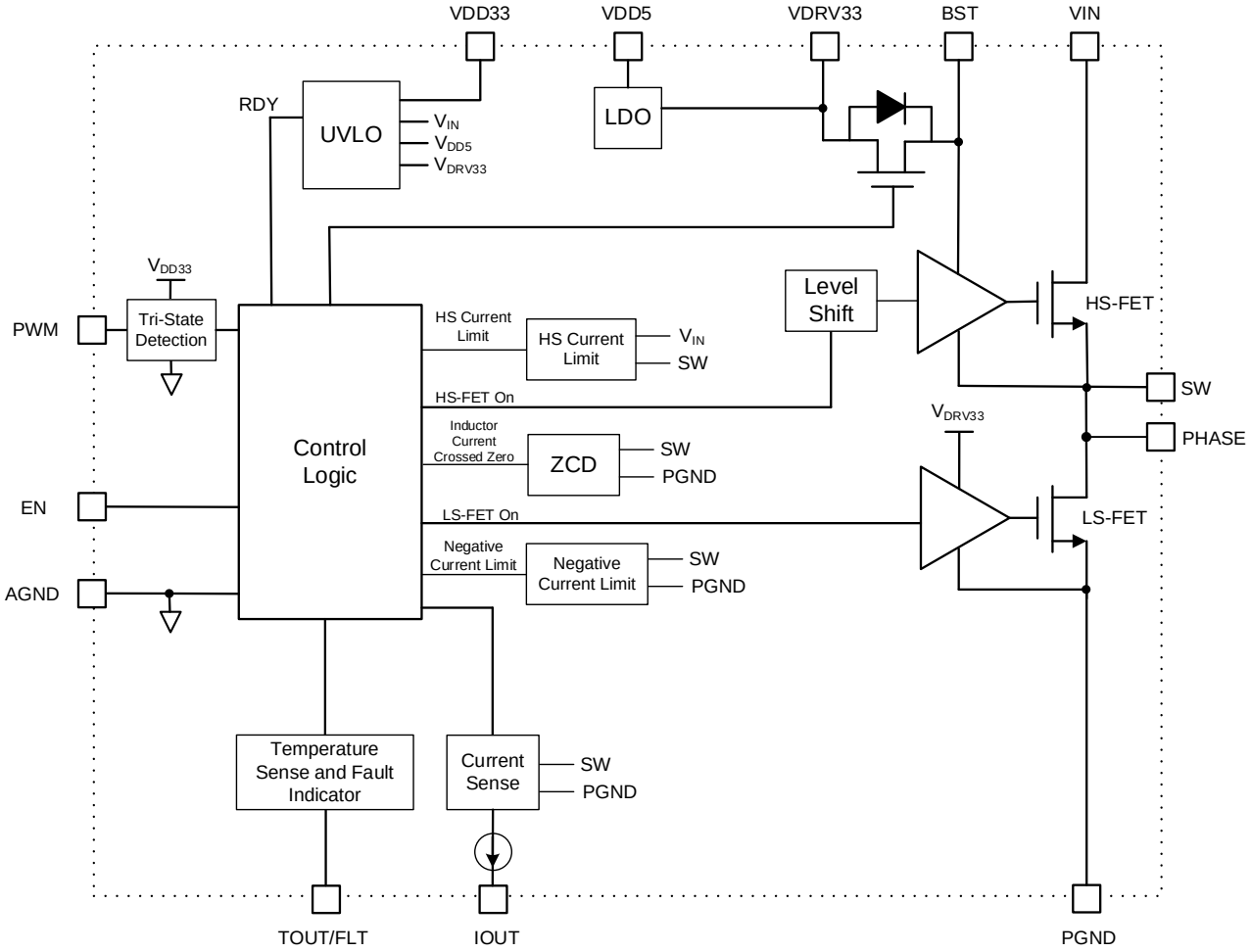

Figure 2: Functional Block Diagram

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OPERATION

The MPQ86750 is a 50A, monolithic, half-bridge Intelli-Phase™ driver with integrated MOSFETs. It is well-suited for multi-phase buck regulators.

If the VIN, VDD5, VDRV33, VDD33, and VBST signals are sufficiently high, the device begins operating.

Pulse-Width Modulation (PWM)

The PWM pin can operate with a tri-state input. If the pulse-width modulation (PWM) input signal is within the tri-state threshold window for 50ns (t_{HT} to t_{LT}), the high-side MOSFET (HS-FET) turns off immediately and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET remains in diode emulation mode until zero-current detection (ZCD).

The tri-state PWM input can come from a forced middle-voltage PWM signal, or it can be made by floating the PWM input so that the internal current source charges the signal to a middle voltage. See Figure 1 on page 6 for the PWM to SW node propagation delay definition.

Standby Mode

When the EN pin is pulled low, the MPQ86750 enters standby mode. In standby mode, the device shuts down, and both the IOUT and TOUT/FLT outputs are disabled. The fault latch cannot be reset by entering standby mode.

Diode Emulation Mode

When PWM is in tri-state, the MPQ86750 enters diode emulation mode. If the inductor current (I_L) is positive, the LS-FET turns on. If I_L crosses the zero-current detection (ZCD) threshold, the LS-FET turns off. Float PWM or force PWM to a middle voltage to enter diode emulation mode.

Current Sense (IOUT)

The current-sense pin (IOUT) is a bidirectional current source that is proportional to I_L. The current-sense gain is 5μA/A. Use a resistor to convert the current-sense gain into a volt-per-ampere gain to report the inductor current.

The IOUT output has two states (see Table 1). In standby mode, the IOUT circuit is disabled. It takes 20μs for the device to wake up and enter active mode.

Table 1: IOUT Output States

EN	IOUT
Low	Standby
High	Active

The voltage on the IOUT pin (V_{IOUT}) must be between 0.8V and 2V to obtain an accurate IOUT current output (I_{OUT}), up to +500μA/-125μA (e.g. +100A/-25A). Typically, there is a resistor (R_{IOUT}) connected from IOUT to an external voltage, which can sink a small current. This provides enough voltage to meet the required operating voltage range.

Figure 3 shows the typical circuit diagram for the IOUT connection to achieve a differential voltage source proportional to I_L.

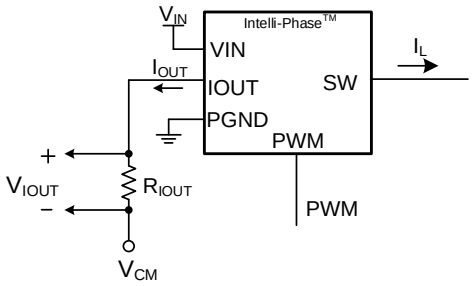

Figure 3: Typical Circuit Diagram for IOUT Pin Connection

To maintain V_{IOUT} within its operating range, calculate R_{IOUT} with Equation (1):

$$0.8V < I_{OUT} \times R_{IOUT} + V_{CM} < 2.0V \quad (1)$$

Where V_{CM} is the reference voltage connected to R_{IOUT}.

The IOUT current (I_{OUT}) can be calculated with Equation (2):

$$I_{OUT} = I_L \times G_{IOUT} \quad (2)$$

Where G_{IOUT} is the current-sense gain.

V_{CM} can be obtained using a voltage divider from 3.3V (e.g. V_{DD33}) (see Figure 4 on page 10).

To minimize V_{CM} variation across I_{IOUT}, R_{IOUT} should exceed the equivalent resistance of R_1 in parallel with R_2 (R_{IOUT} >> R_1 || R_2).

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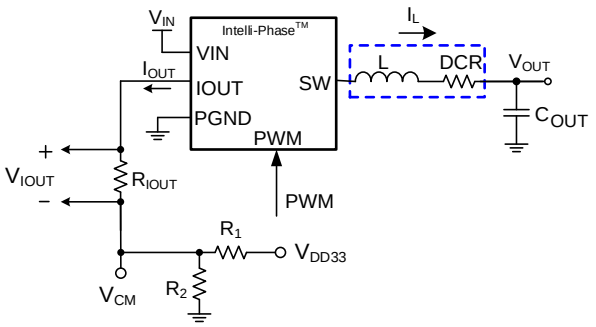

Figure 4: V_{CM} Voltage for IOUT Signal from V_{DD33}

Positive and Negative Inductor Current Limit

If an over-current (OC) condition is detected on the HS-FET, the MPQ86750 immediately turns off the HS-FET and turns on the LS-FET.

If an over-current condition is detected on the LS-FET, the MPQ86750 turns off the LS-FET and turns on the HS-FET for 120ns to limit the negative current.

Over-Temperature Protection (OTP)

If the junction temperature (T_J) reaches the over-temperature (OT) threshold, the HS-FET latches off, and TOUT/FLT is pulled to V_{DD33}. The LS-FET turns on and stays on until ZCD.

Temperature-Sense Output with Fault Indication (TOUT/FLT)

The TOUT/FLT pin has two functions: junction temperature sense and fault indication. Each function is described below .

Junction Temperature Sense

TOUT/FLT is a voltage output that is proportional to T_J when the MPQ86750 is in active mode. The temperature-sense gain is 8mV/°C, with a 600mV offset. For example, the voltage gain is 0.8V when T_J = 25°C, and 1.6V when T_J = 125°C.

Fault Indication

If an OT fault occurs (T_J reaches the OT threshold), TOUT/FLT is pulled to V_{DD33} to report the fault event. Then the MPQ86750 latches off to turn off the HS-FET. The LS-FET turns on and remains on until I_L reaches 0A.

The fault latch cannot be reset by entering standby mode. The fault latch can only be released by cycling the power on VIN or VDD5.

For multi-phase operation, connect all of the Intelli-Phase™ devices' TOUT/FLT pins together (see Figure 5).

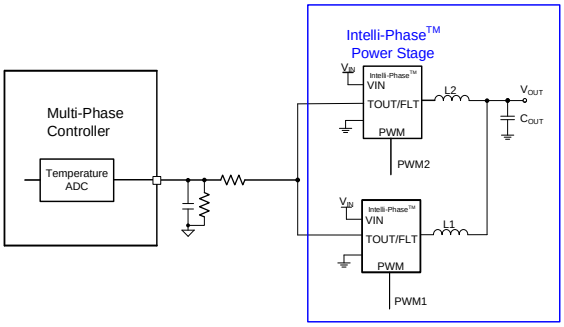

Figure 5: Temperature Sense during Multi-Phase Operation

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APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the input MLCC capacitors as close as possible to the VIN and PGND pins.
2. Place the major MLCC capacitors on the same layer as the Intelli-Phase™.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Place as many PGND vias as possible near the PGND plane to minimize parasitic impedance and thermal resistance.
5. Place the VDD5 decoupling capacitor close to the VDD5 pin.
6. Place the VDD33 decoupling capacitor close to the VDD33 pin.
7. Place the VDRV33 decoupling capacitor close to the VDRV33 pin.
8. Ensure that the VDRV33 capacitance exceeds the bootstrap (BST) capacitance (C_{BST}). For example, use a 1µF capacitor for the VDRV33 pin and a 0.22µF capacitor for the BST pin.
9. Connect AGND and PGND at the point of the VDD33 capacitor's ground connection.
10. Place C_{BST} as close as possible to the BST and PHASE pins.
11. Use an RC snubber circuit placeholder to tune the switching spike if required.
12. Route the BST path with a trace width that is at least 10mil.
13. C_{BST} should be between 0.1µF and 1µF.
14. Route the IOUT signal with a 10mil trace width.
15. Route the IOUT signal trace away from high-current paths, such as SW and PWM.
16. Keep a 40mil distance between IOUT and any noisy signals.
17. Route the IOUT signal and the noisy signals in two different layers. Place a solid GND layer between these layers.
18. Route the PWM signal with a 10mil trace width.

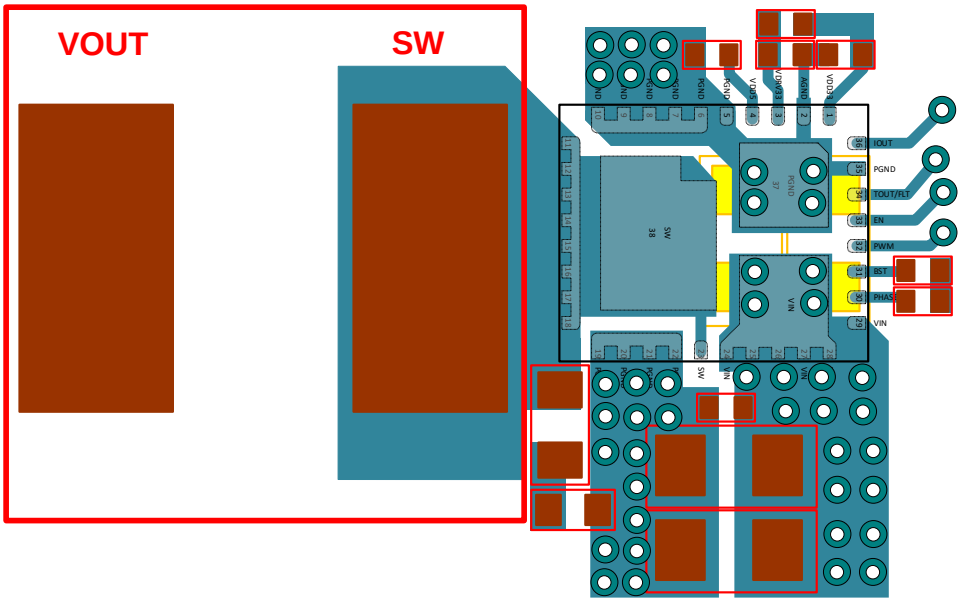

Figure 6: Recommended PCB Layout (Placement and Top Layer PCB)

Input Capacitor: 1206 Package (Top Side and Bottom Side) and 0402 Package (Top Side)

VDD5/VDRV33/VDD33/BST Capacitor: 0402 Package

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TYPICAL APPLICATION CIRCUIT

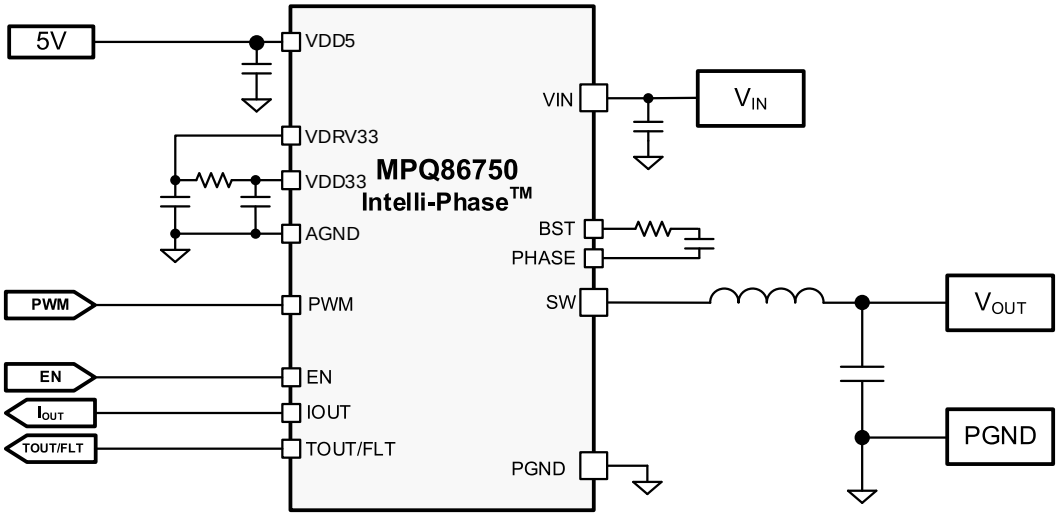

Figure 7: Typical Application Circuit

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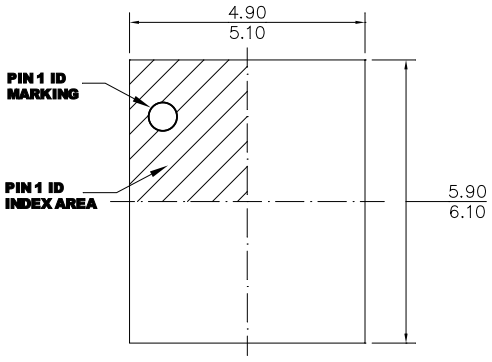
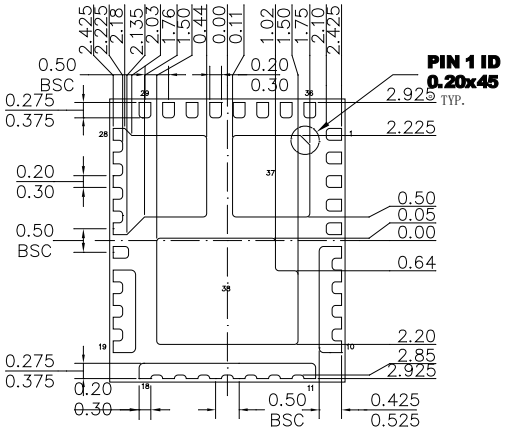
PACKAGE INFORMATION

LGA-38 (5mmx6mm)

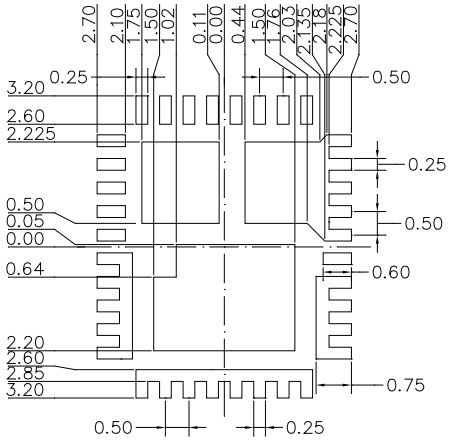


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) REFERENCEIS MO-303.
4) DRAWING IS NOT TO SCALE.

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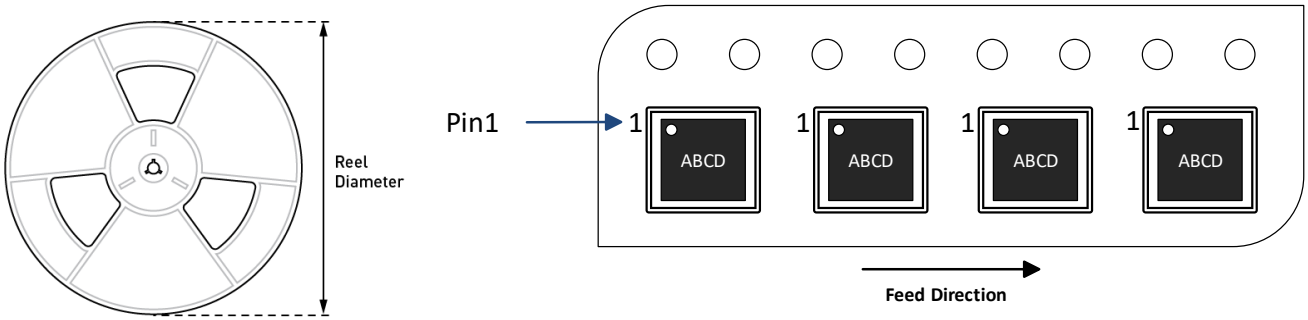
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ86750GMJT-AEC1-Z	LGA-38 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/9/2024	Initial Release	-
1.01	10/6/2026	Updated POD package image in the Package Information section.	13

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