MPQ7232

36V, 6A, Synchronous Buck Infrared LED Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ7232 is a synchronous, step-down, constant-current, infrared (IR) LED driver. It features a compact solution that achieves up to 6A of peak LED current (I_{LED}). An ideal configuration is to drive 1 or 2 IR LEDs. Peak LED current control mode provides fast transient response and eases loop stabilization.

The MPQ7232 supports a 10Hz to 2kHZ pulse-width modulation (PWM) dimming frequency range. It is compatible with IR LED applications that require 30fps, 60fps, or 120fps dimming.

The MPQ7232 also supports analog dimming. It applies a DC voltage between 0.2V and 1.6V on the ADIM pin to linearly adjust the internal LED current reference voltage (V_{REF}) from 25mV to 200mV. Frequency spread spectrum (FSS) modulation improves EMC performance.

Full protection features include LED short to GND, LED open, thermal shutdown (TSD), and a dedicated fault pin.

The MPQ7232 requires a minimal number of readily available, standard external components. It is available in a space-saving QFN-15 (3mmx4mm) package, and is AEC-Q100 qualified.

FEATURES

- Designed for Automotive Applications
  - 4.5V to 36V Input Voltage (V_{IN}) Range
  - -40°C to +150°C Junction Temperature (T_J) Rating
- Built for IR LED Applications
  - Up to 6A of Peak LED Current (I_{LED})
  - Configurable LED Current
  - 10Hz to 2kHz Pulse-Width Modulation (PWM) Dimming Frequency
  - Compatible with 30fps, 60fps, and 120fps Dimming
  - Analog Dimming
- Improved Efficiency and Thermals
  - 45mΩ/30mΩ On Resistance ($R_{DS(ON)}$) Internal MOSFETs
  - High-Efficiency Synchronous Driver
- Optimized for EMC and EMI
  - 2.25MHz Switching Frequency (f_{SW})
  - Frequency Spread Spectrum (FSS)
- Full Protection Features
  - Fault Indication for LED Short to GND, Open
  - Thermal Shutdown (TSD)
- Additional Features
  - Available in a QFN-15 (3mmx4mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Infrared (IR) LED Drivers for Driver Monitoring Systems (DMS)
- Surveillance Systems

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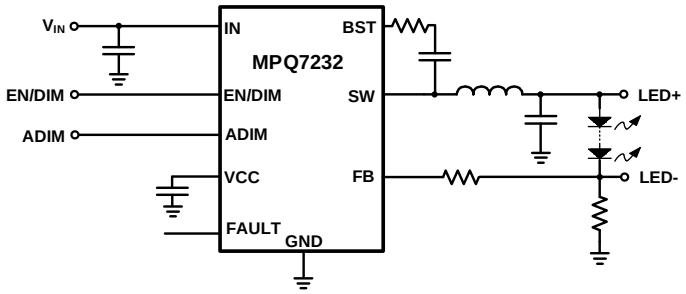
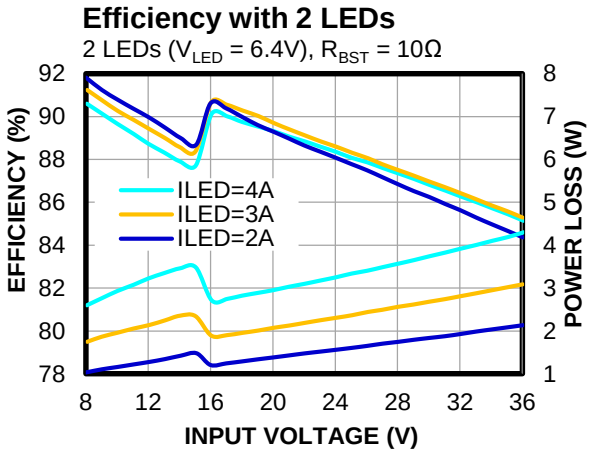
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ7232GLE-AEC1***	QFN-15 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ7232GLE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable Flank

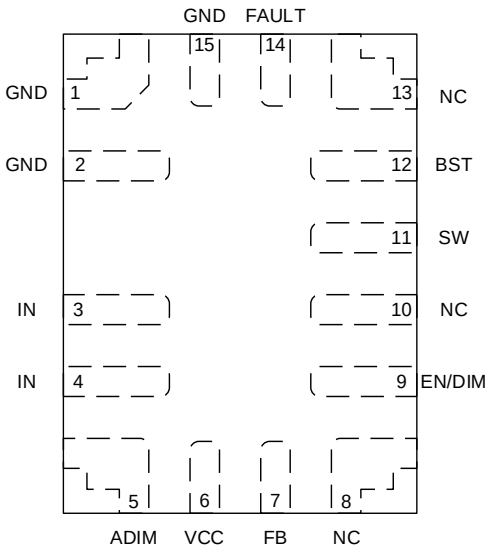
TOP MARKING

MPYW
7232
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
7232: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-15 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 15	GND	**Power ground.**
3, 4	IN	**Supply voltage.** The MPQ7232 operates from a 4.5V to 36V input rail, and requires an input capacitor (C_{IN}) to decouple the input rail. Connect the IN pin to the input rail using a wide PCB trace.
5	ADIM	**Analog dimming input.** Connect this pin to an external reference voltage to adjust the analog dimming V_{REF} or tie it to the VCC pin to achieve 100% LED current (I_{LED}) if analog dimming is not used. The analog input can vary between 200mV and 1.6V to set the current reference voltage (V_{REF}) from 25mV to 200mV, providing between 0.75A and 6A of peak I_{LED}. Pull the ADIM pin above the specified threshold (typically 1.68V) to exit the analog dimming adjustment mode.
6	VCC	**Internal bias supply.** The VCC pin supplies power to the internal control circuitry and gate drivers. It is recommended to place a 1µF, 10V, or 16V X7R capacitor as close to the VCC pin as possible.
7	FB	**LED current feedback input.** Connect a current-sense (CS) resistor between the FB and GND pins to set I_{LED}.
8, 10, 13	NC	**No connection.** Connect the NC pin to GND externally on the board to simplify the layout. This pin can also be left floating.
9	EN/DIM	**Enable/dimming control.** Pull the EN pin above 1.65V to turn on the MPQ7232; pull the EN pin below 1.05V for longer than 600ms to turn off the MPQ7232. Apply a 10Hz to 2kHz external clock to the EN/DIM pin for pulse-width modulation (PWM) dimming. The dimming time can be as long as 100ms to support low-to-10Hz dimming frequencies, which can cover the 30Hz IR LED driver.
11	SW	**Switching node.** The SW pin is the middle point of the high-side and low-side MOSFETs (HS-FET and LS-FET, respectively). Use a wide trace and small-sized SW node to reduce noise coupling and improve EMI during PCB layout.
12	BST	**Bootstrap.** The BST pin requires a 0.1µF (typical) capacitor connected between the SW and BST pins to form a floating supply across the HS-FET driver. Place a 10Ω resistor between the SW and BST capacitor to reduce SW spike voltage and improve EMI performance.
14	FAULT	**Fault indicator.** The FAULT pin is an open-drain output. This pin is pulled toward the VCC pin or an external source with a resistor to indicate a fault condition. This pin is pulled low if any of the following occurs: LED short to GND, LED open, or thermal shutdown. The FAULT pin can be connected to the input voltage (V_{IN}) using a pull-up resistor.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +40V
V_{SW}.....-0.3V (-5V for < 10ns) to V_{IN} + 0.3V (43V for < 10ns)
V_{FAULT} .....-0.3V to +40V
V_{BST} ..... V_{SW} + 5.5V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-15 (3mmx4mm) 3.8W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (3)
Charged-device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Operating input voltage (V_{IN}) range..4.5V to 36V
LED current (I_{LED})..... 6A
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-15 (3mmx4mm)			
JESD51-7	49.4	5.9	°C/W (5)
EVQ7232-L-00A	32.9	3.9	°C/W (6)

Notes:

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on a standard EVB for the MPQ7232, 63.5mmx63.5mm, 4-layer PCB, 2oz. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage (V_{IN})						
Shutdown supply current	I_{SD}	V_{EN} = 0V, T_J = 25°C			1	µA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 220mV, no switching		600	900	µA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$		3.6	4	4.4	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_FALLING}$		3.1	3.5	3.9	V
V_{IN} UVLO hysteresis threshold	$V_{IN_UVLO_HYS}$			500		mV
MOSFETs and Frequency						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST_SW} = 5.5V		45	90	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 5V		30	60	mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	µA
Oscillator frequency	f_{SW}	V_{FB} = 200mV	1900	2250	2600	kHz
Frequency spread spectrum (FSS) (7)				9		kHz
FSS range (7)	f_{SS}			±5% x f_{SW}		kHz
Maximum duty cycle (7)	D_{MAX}			96		%
Minimum on time (7)	t_{ON_MIN}			60		ns
Feedback (FB)						
FB voltage	V_{FB}	T_J = 25°C	192	200	208	mV
		T_J = -40°C to +150°C	185	200	215	
FB current	I_{FB}	V_{FB} = 200mV	-75	0	+75	nA
Enable (EN)						
EN rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN_FALLING}$		1.05	1.25	1.45	V
EN hysteresis threshold	V_{EN_HYS}			150		mV
EN input current	I_{EN}	V_{EN} = 2V		4	10	µA
		V_{EN} = 0V		0	0.2	µA
EN turn-off delay	$t_{EN_D_OFF}$		360	600	1000	ms
Soft Start (SS) and VCC						
Soft-start time (7)	t_{SS}	After start-up, I_{LED} = 6A, L = 2.2µH, load = 2 series LEDs, I_L increasing from 10% to 90%		90		µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC regulator	V_{CC}	I_{CC} = 0mA		5		V
VCC load regulation		I_{CC} = 5mA		1.5	4	%
LDO drop voltage	V_{LDO_DROP}	V_{IN} < 5V		200		mV
Analog Dimming						
LED current derating (percentage of nominal value)	I_{LED_ANA}	V_{ADIM} = 1.6V	95	100	105	%
		V_{ADIM} = 1.2V	70	75	80	
		V_{ADIM} = 0.8V	45	50	55	
Analog dimming voltage (V_{ADIM}) UVLO rising threshold	$V_{ADIM_UVLO_RISING}$		160	200	240	mV
V_{ADIM} UVLO falling threshold	$V_{ADIM_UVLO_FALLING}$		60	100	140	mV
Protections						
Current limit (7)	I_{LIMIT}		7	10.5	14	A
LED open protection disabled V_{IN} rising threshold		V_{IN} rising		7.2		V
LED open protection disabled V_{IN} falling threshold		V_{IN} falling		7		V
V_{ADIM} UVLO detection time		After start-up, V_{ADIM} < 100mV		1.5		µs
Over-voltage detection time		After start-up, V_{COMP} > 2V		1.5		µs
FAULT sink current capability	V_{FT}	Sink 1mA			0.5	V
FAULT leakage current	I_{FT_LEAK}				200	nA
Thermal shutdown (7)	T_{SD}			165		°C
Thermal hysteresis (7)	T_{SD_HYS}			20		°C

Note:

7) Not tested in production. Guaranteed by design and characterization.

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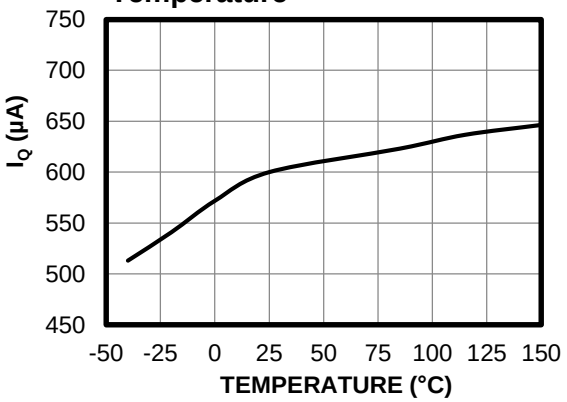
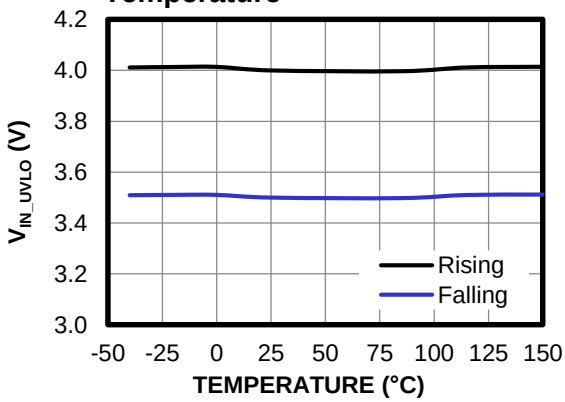
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

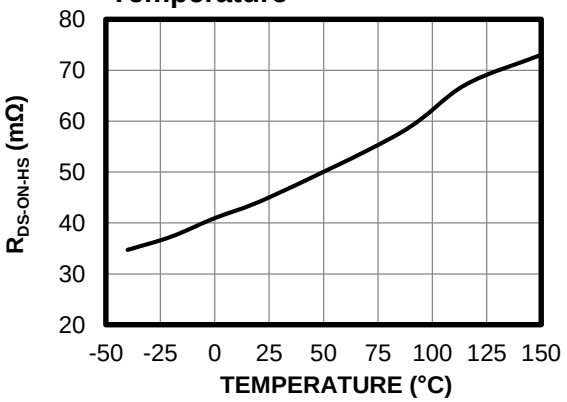
Quiescent Current vs. Temperature



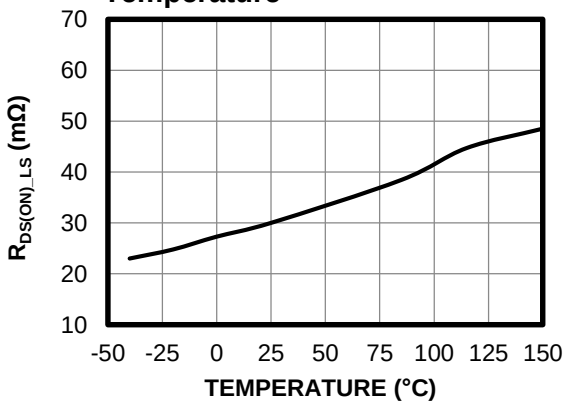
V_{IN} UVLO Threshold vs. Temperature



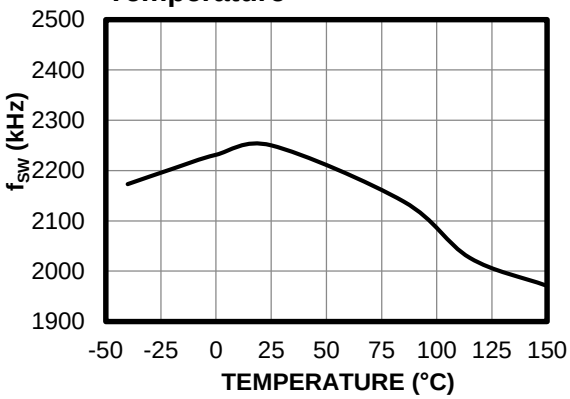
HS switch-on Resistance vs. Temperature



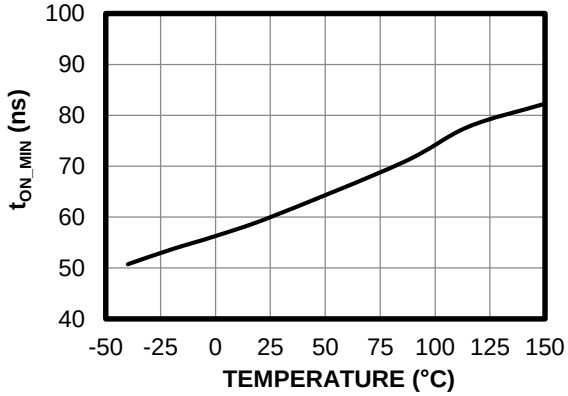
LS-FET On Resistance vs. Temperature



Switching Frequency vs. Temperature



Minimum On Time vs. Temperature



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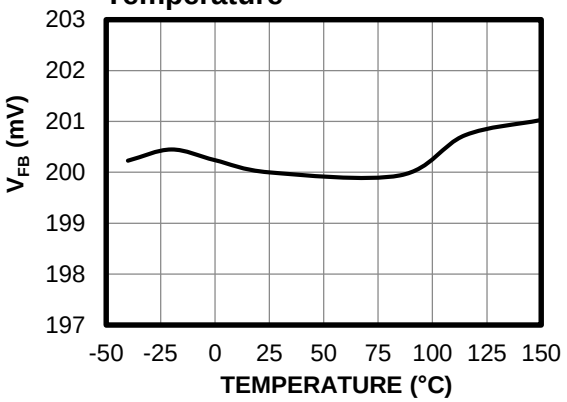
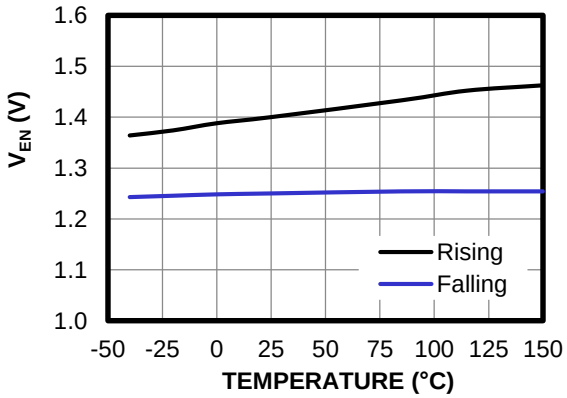
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

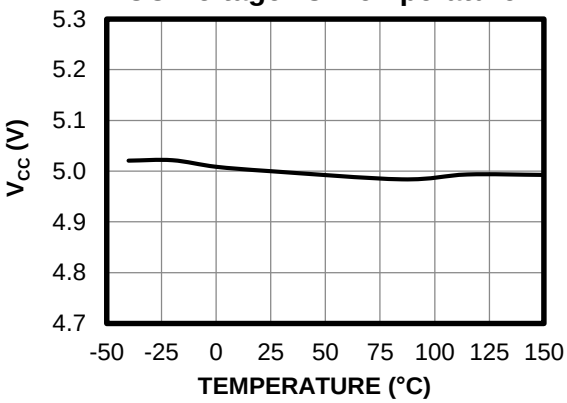
Feedback Voltage vs. Temperature



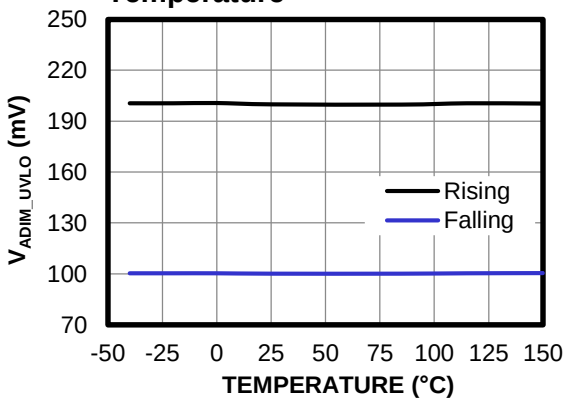
EN Threshold vs. Temperature



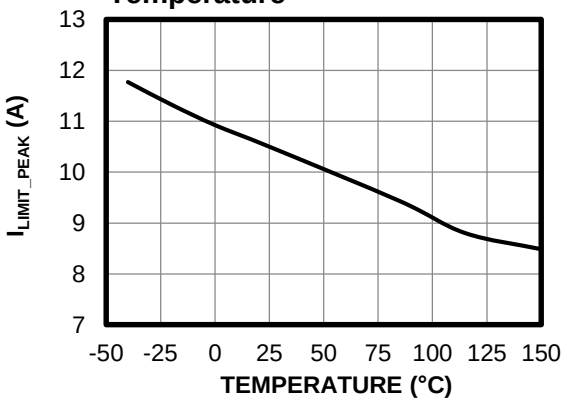
VCC Voltage vs. Temperature



ADIM UVLO Threshold vs. Temperature



Peak Current Limt vs. Temperature



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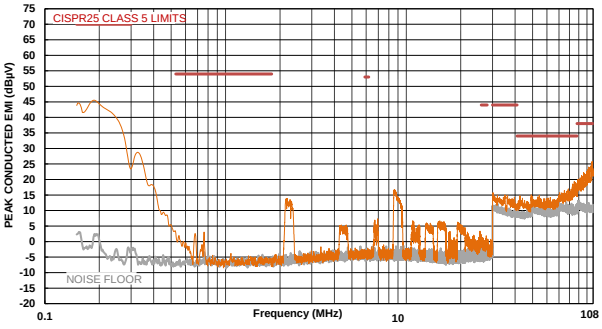
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6.4V) at I_{LED_PEAK} = 6A, with PWM dimming = 30Hz/5ms, f_{SW} = 2.25MHz, L = 2.2µH, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

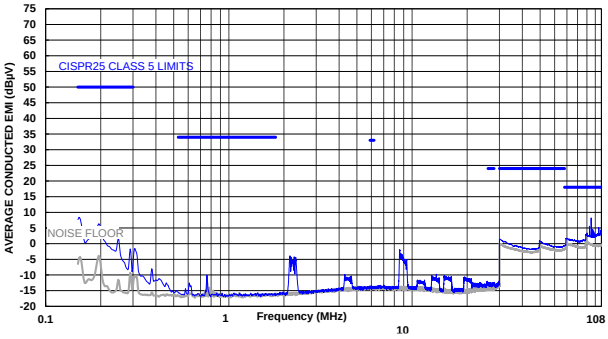
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



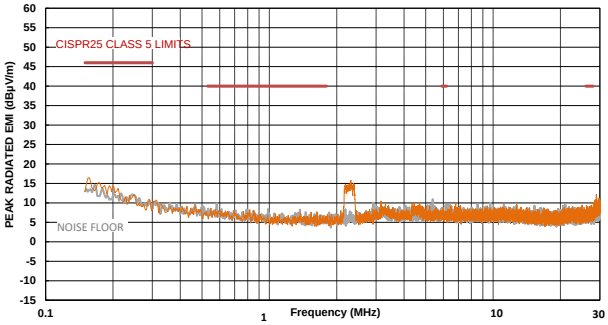
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



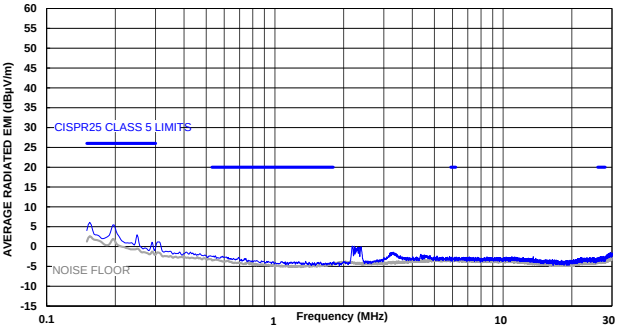
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



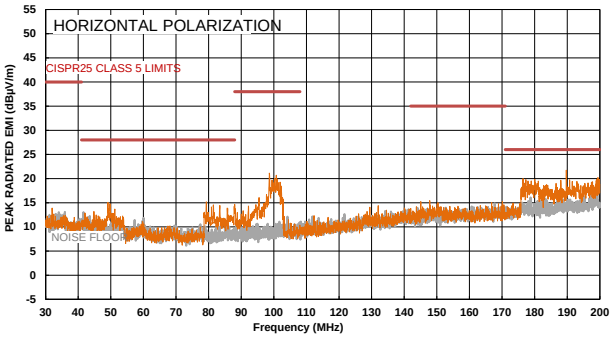
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



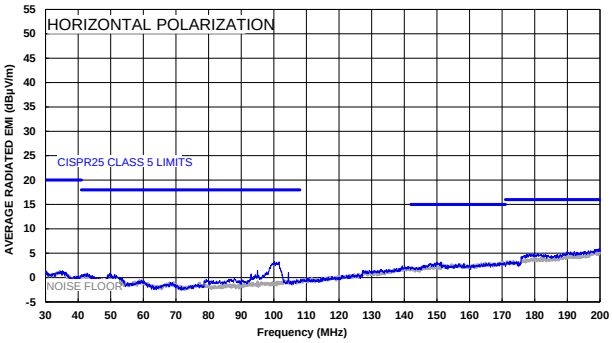
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



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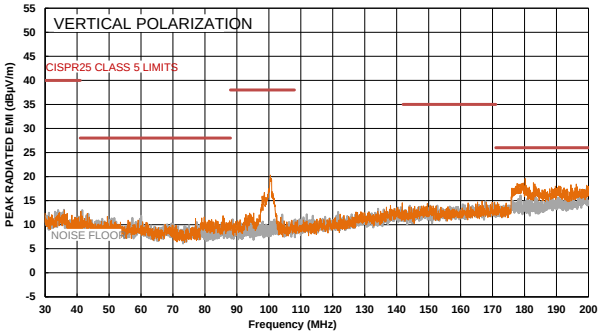
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6.4V) at I_{LED_PEAK} = 6A, with PWM dimming = 30Hz/5ms, f_{SW} = 2.25MHz, L = 2.2µH, with EMI filters, T_A = 25°C, unless otherwise noted. (8)

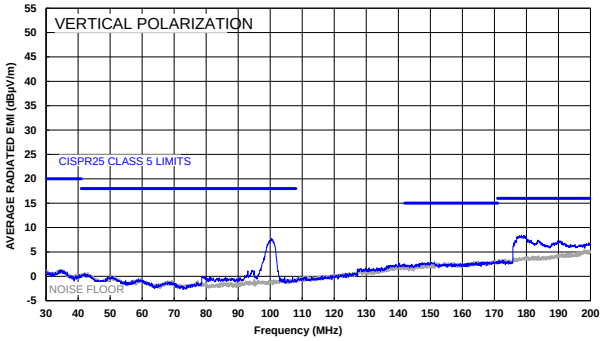
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



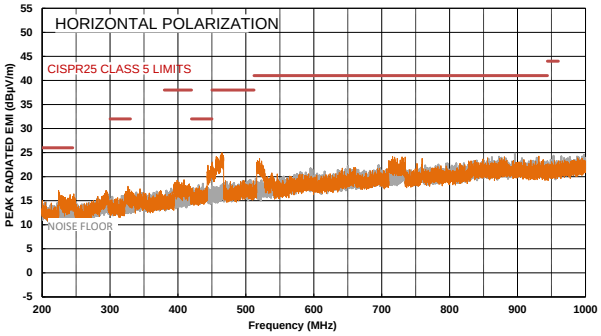
CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



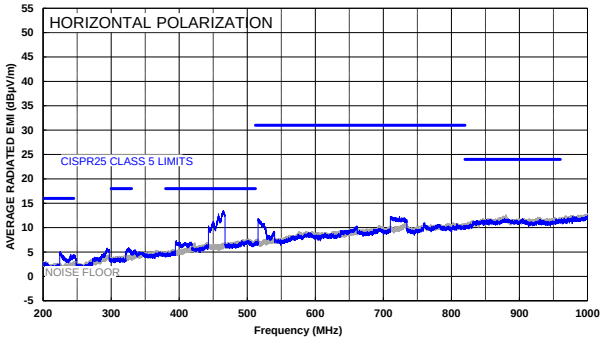
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



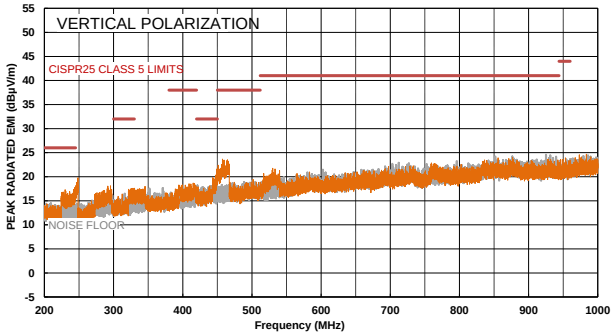
CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



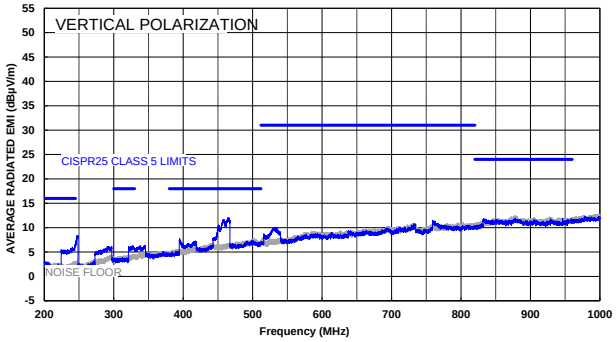
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

8) EMI test results are based on the typical application circuit with EMI filters (see Figure 12 on page 25).

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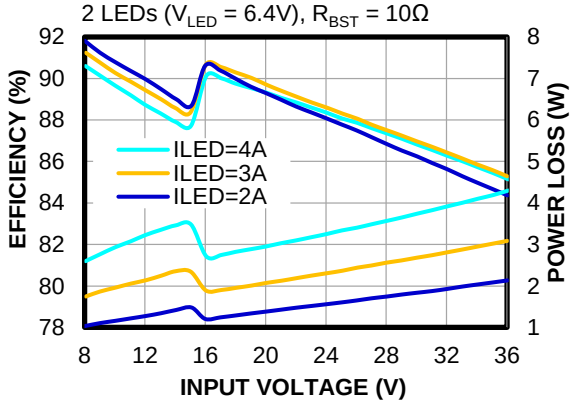
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6.4V), f_{SW} = 2.25MHz, L = 2.2µH, T_A = 25°C, unless otherwise noted. (9)

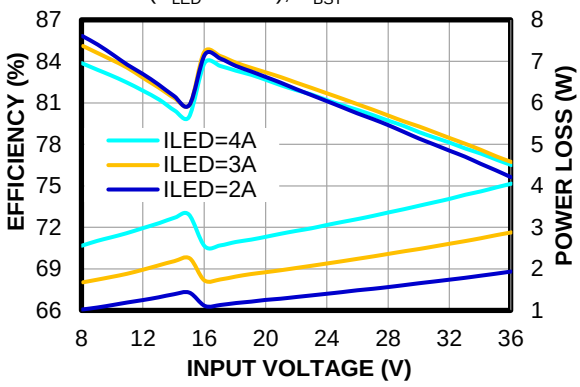
Efficiency with 2 LEDs

2 LEDs (V_{LED} = 6.4V), R_{BST} = 10Ω



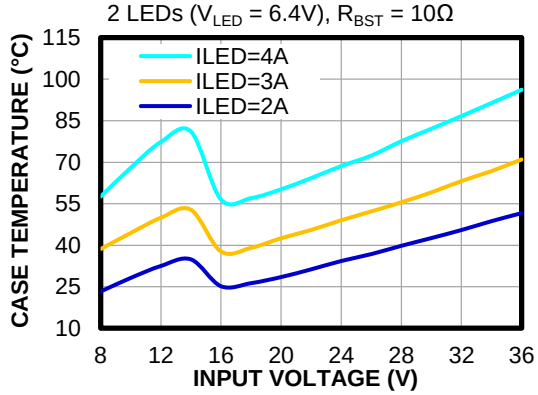
Efficiency with 1 LED

1 LED (V_{LED} = 3.2V), R_{BST} = 10Ω



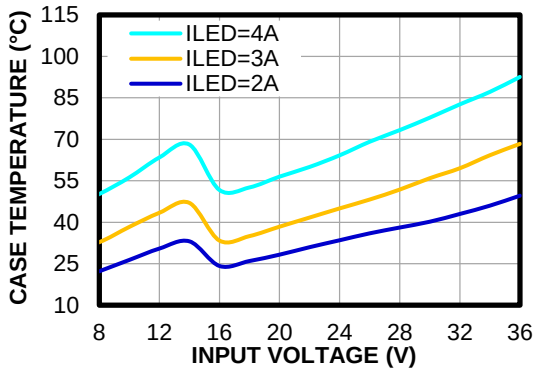
Case Temperature Rise with 2 LEDs

2 LEDs (V_{LED} = 6.4V), R_{BST} = 10Ω



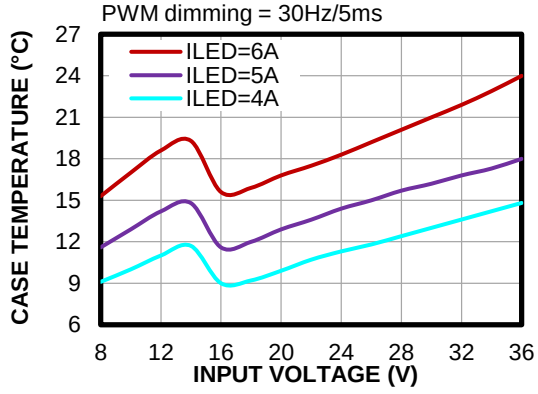
Case Temperature Rise with 1 LED

1 LED (V_{LED} = 3.2V), R_{BST} = 10Ω



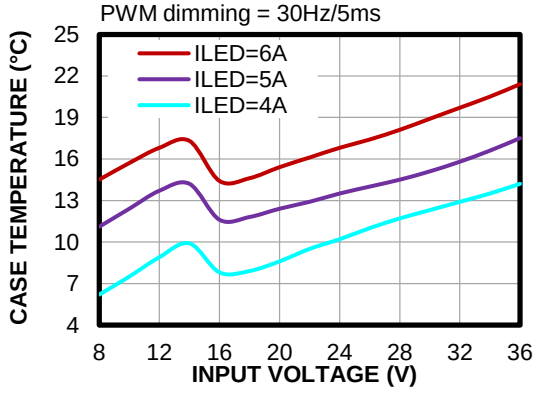
Case Temperature Rise with 2 LEDs

PWM dimming = 30Hz/5ms



Case Temperature Rise with 1 LED

PWM dimming = 30Hz/5ms



Note:

9) Efficiency and thermal curves are based on Figure 12 on page 25, with the output and input filters removed. L = 2.2µH (XEL5030-222MEB).

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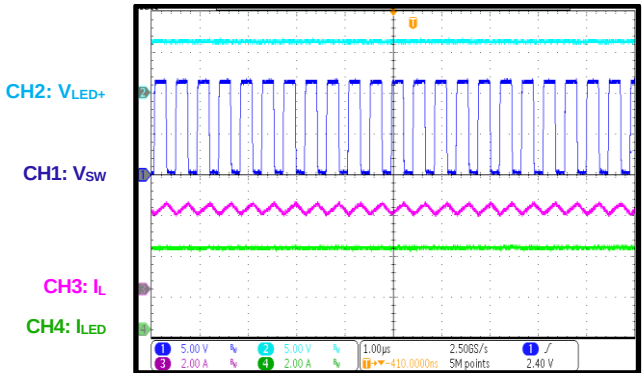
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6.4V), f_{SW} = 2.25MHz, L = 2.2µH, T_A = 25°C, unless otherwise noted.

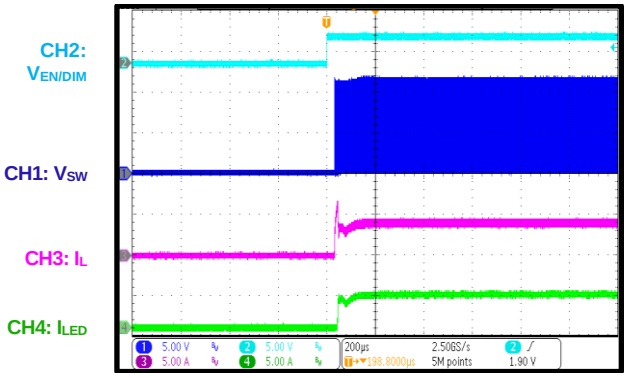
Steady State

I_{LED} = 4A



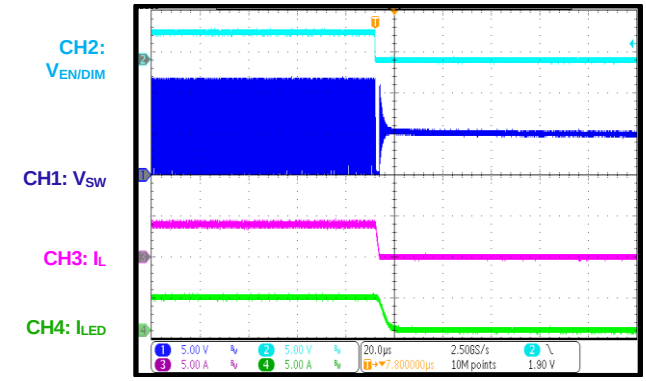
Start-Up through EN

I_{LED} = 4A



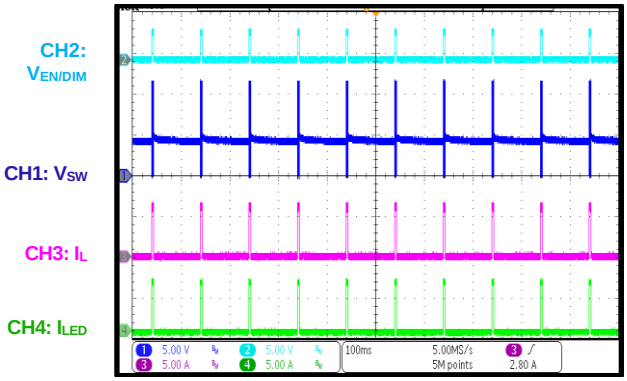
Shutdown through EN

I_{LED} = 4A



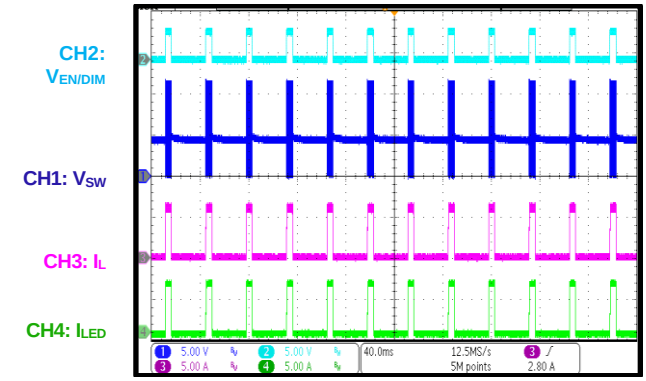
PWM Dimming Steady State

Dimming frequency = 10Hz/5ms, I_{LED_PEAK} = 6A



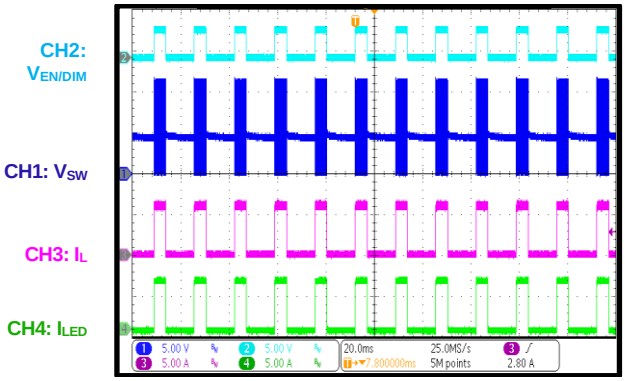
PWM Dimming Steady State

Dimming frequency = 30Hz/5ms, I_{LED_PEAK} = 6A



PWM Dimming Steady State

Dimming frequency = 60Hz/5ms, I_{LED_PEAK} = 6A



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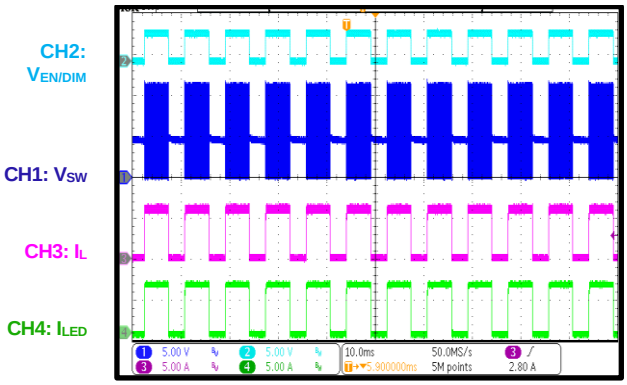
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6.4V), f_{SW} = 2.25MHz, L = 2.2µH, T_A = 25°C, unless otherwise noted.

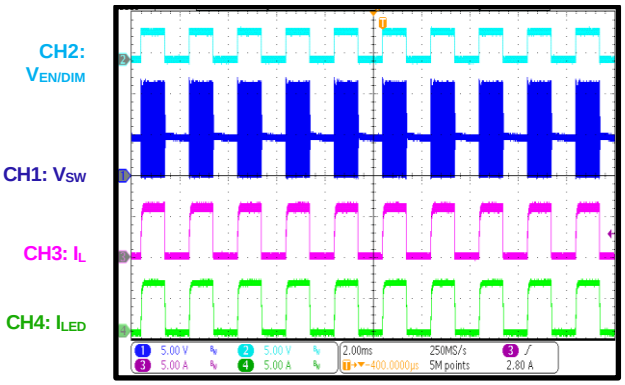
PWM Dimming Steady State

Dimming frequency = 120Hz/5ms,
I_{LED_PEAK} = 6A



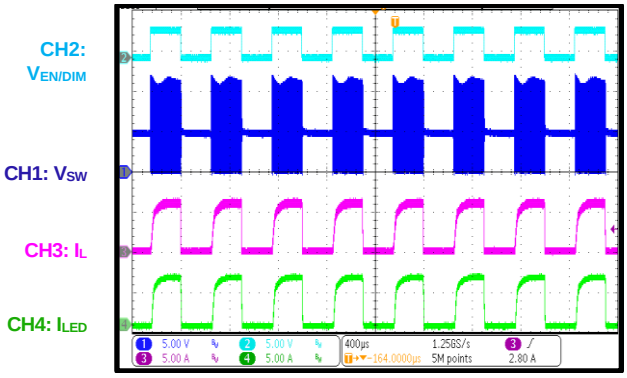
PWM Dimming Steady State

Dimming frequency = 500Hz,
dimming duty = 50%, I_{LED_PEAK} = 6A



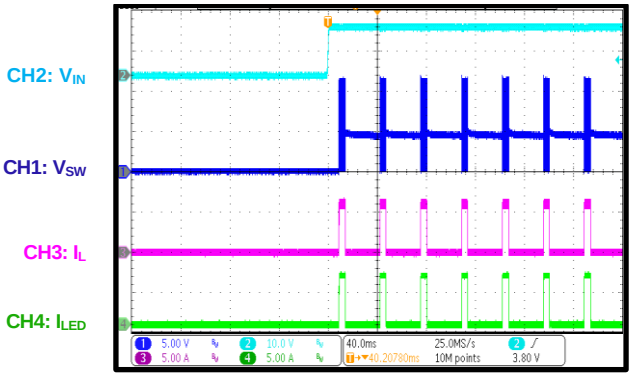
PWM Dimming Steady State

Dimming frequency = 2kHz,
dimming duty = 50%, I_{LED_PEAK} = 6A



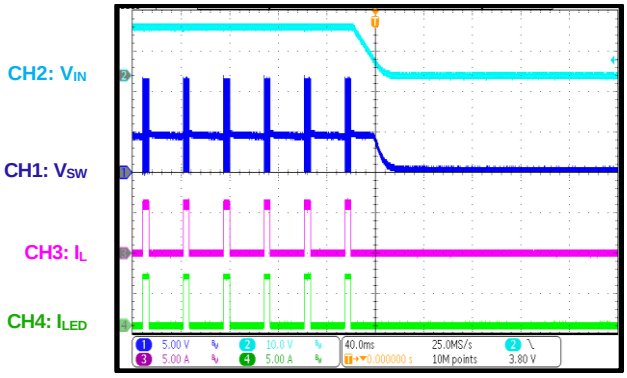
PWM Dimming

Start-up through VIN, I_{LED_PEAK} = 6A



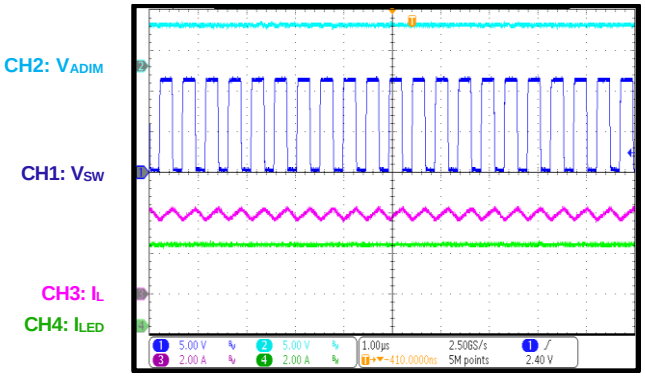
PWM Dimming

Shutdown through VIN, I_{LED_PEAK} = 6A



Analog Dimming Steady State

V_{ADIM} = 5V



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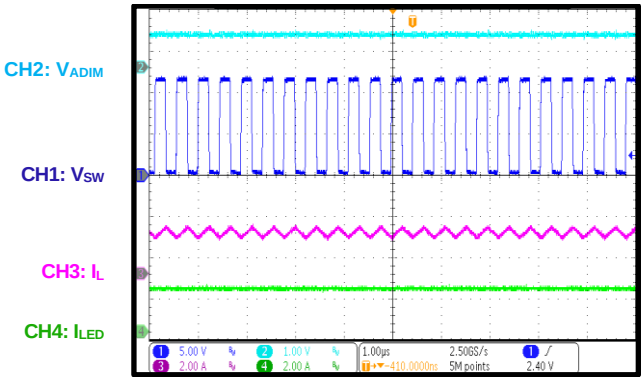
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6.4V), f_{SW} = 2.25MHz, L = 2.2µH, T_A = 25°C, unless otherwise noted.

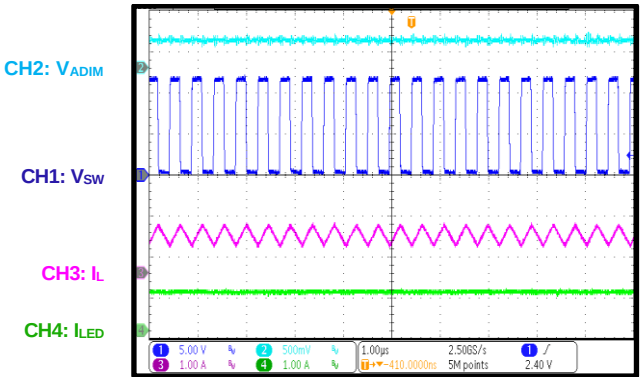
Analog Dimming Steady State

V_{ADIM} = 0.8V



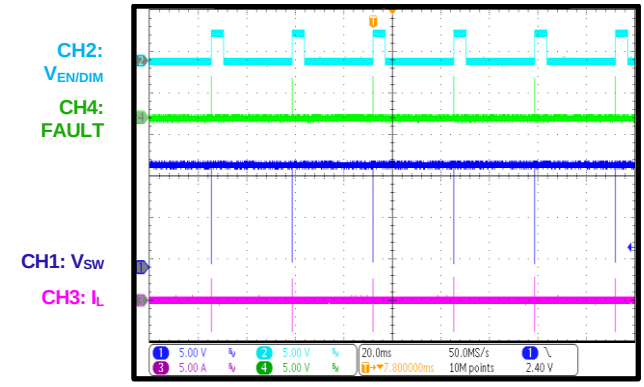
Analog Dimming Steady State

V_{ADIM} = 0.4V



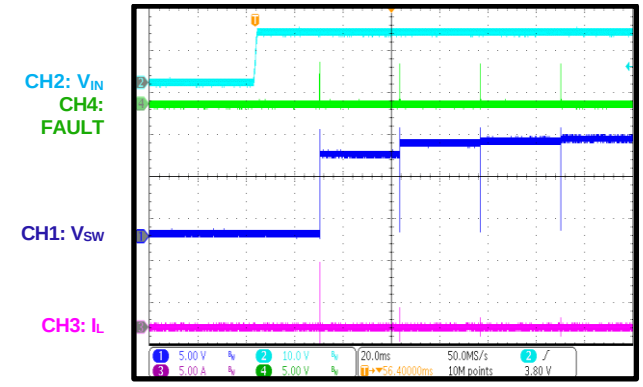
PWM Dimming

LED open steady state



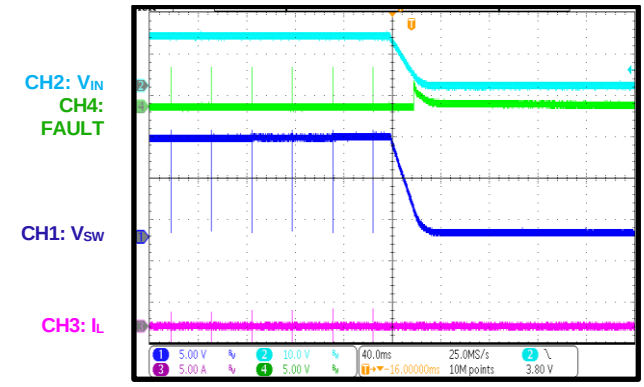
PWM Dimming

LED open input start-up



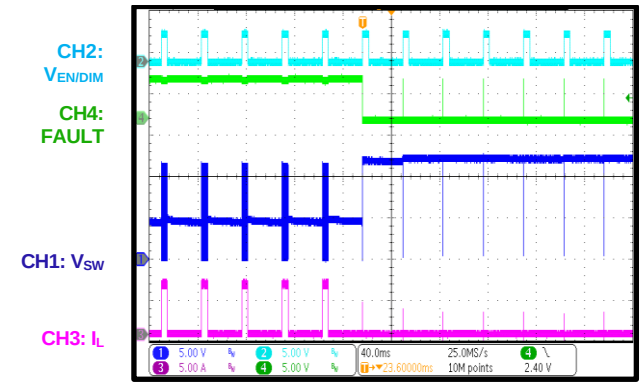
PWM Dimming

LED open input shutdown



PWM Dimming

LED open entry, I_{LED_PEAK} = 6A



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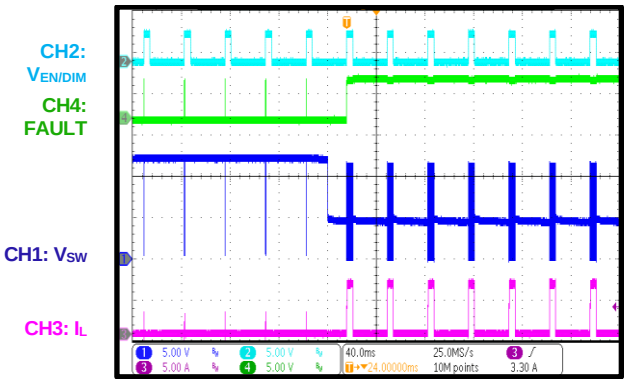
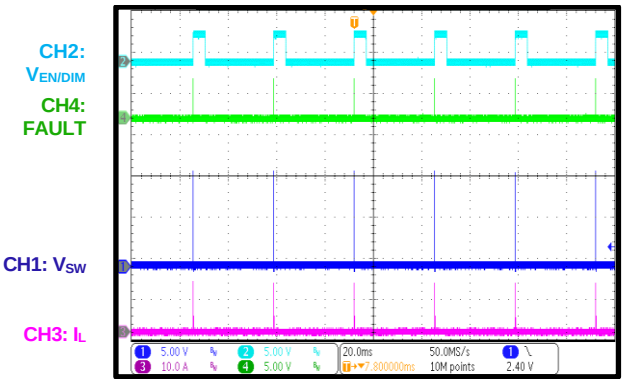
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 2 LEDs in series (V_{LED} = 6.4V), f_{SW} = 2.25MHz, L = 2.2µH, T_A = 25°C, unless otherwise noted.

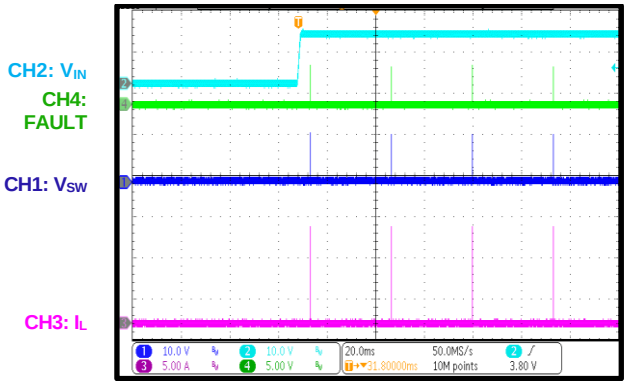
PWM Dimming
LED open recovery, I_{LED_PEAK} = 6A



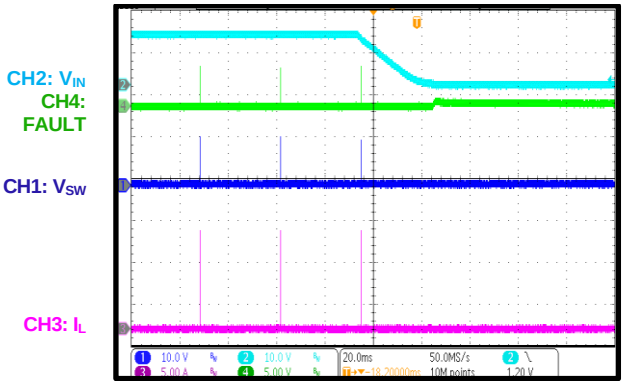
PWM Dimming
LED+ short to GND steady state, I_{LED_PEAK} = 6A



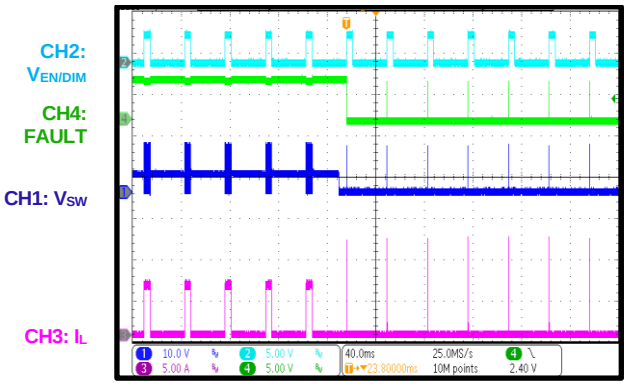
PWM Dimming
LED short to GND input start-up



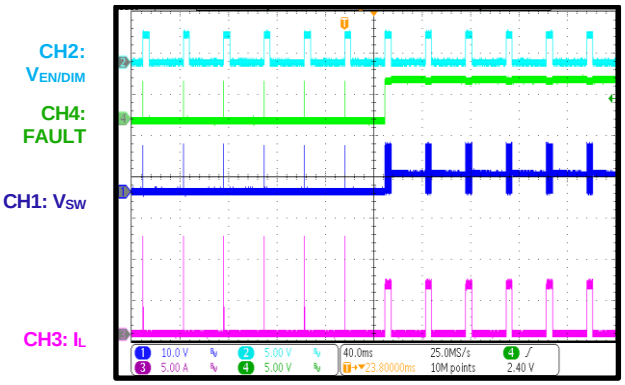
PWM Dimming
LED short to GND input shutdown



PWM Dimming
LED+ short to GND entry, I_{LED_PEAK} = 6A



PWM Dimming
LED+ short to GND recovery, I_{LED_PEAK} = 6A



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FUNCTIONAL BLOCK DIAGRAM

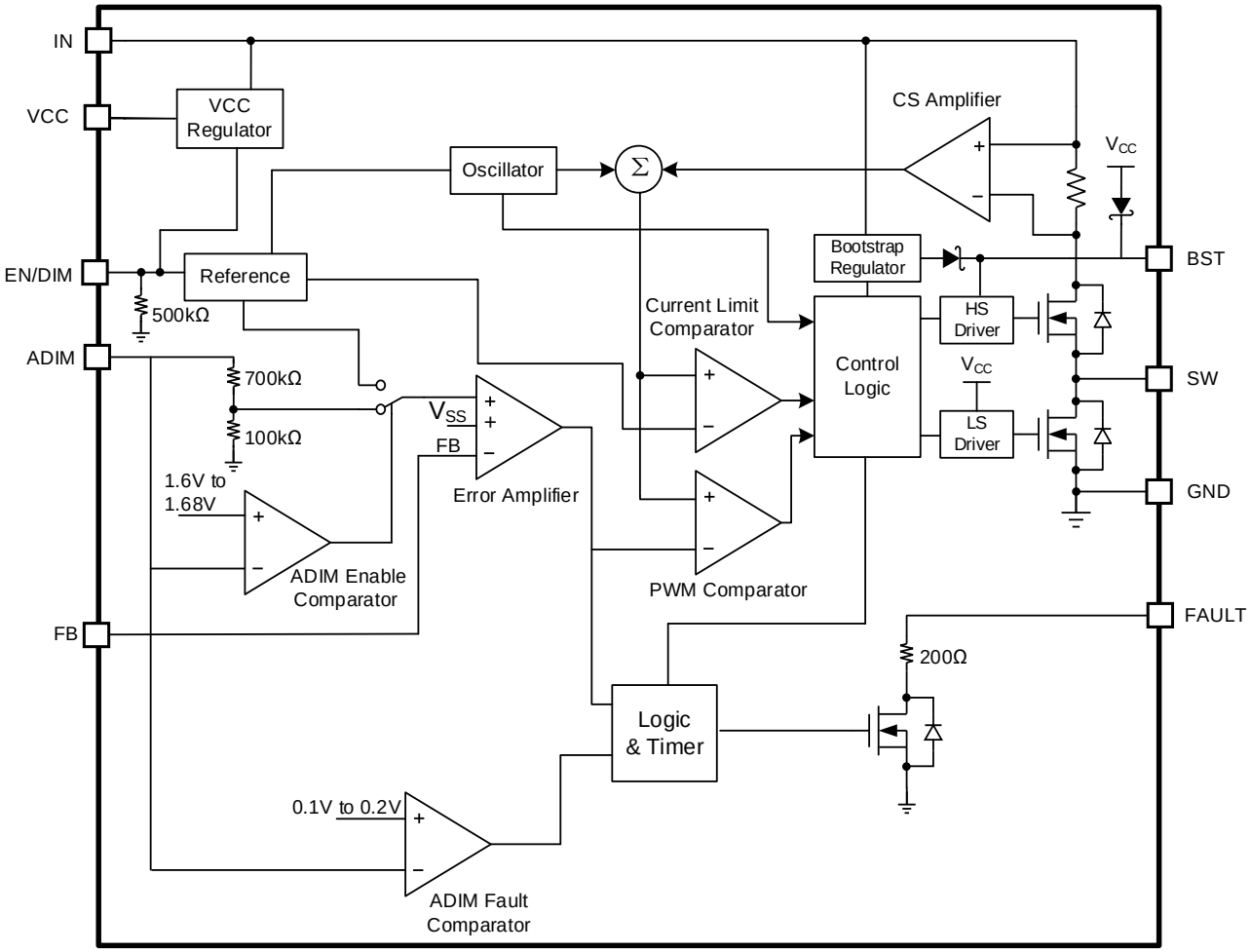

Figure 1: Functional Block Diagram

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OPERATION

The MPQ7232 is a high-frequency, synchronous, rectified, step-down, switch-mode IR LED driver with built-in power MOSFETs. It offers a compact solution that achieves up to 6A of peak LED current (I_{LED}) across a wide input supply voltage (V_{IN}) range, with excellent load and line regulation.

The MPQ7232 operates in fixed-frequency, peak current control mode to regulate the output current (I_{OUT}). An internal clock initiates a PWM cycle. The integrated high-side power MOSFET (HS-FET) turns on and remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the HS-FET turns off, it remains off until the next clock cycle starts. If the current in the HS-FET does not reach the current value set by V_{COMP} within 96% of one PWM period (switching frequency [f_{SW}] = 2.25MHz), the HS-FET is forced to turn off.

Error Amplifier (EA)

The EA compares the feedback (FB) voltage (V_{FB}) to the internal 0.2V reference voltage (V_{REF}) and outputs a current proportional to the difference between the two. I_{OUT} then charges or discharges the internal compensation network to form V_{COMP}, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal VCC Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator uses V_{IN} across the full V_{IN} range. When V_{IN} exceeds 5V, the regulator's output is in full regulation. If V_{IN} is below 5V, the output decreases with V_{IN}. The drop between V_{IN} and the VCC voltage (V_{CC}) is about 200mV. The VCC pin requires an external 0.22µF to 1µF ceramic decoupling capacitor.

Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM)

The MPQ7232 uses continuous conduction mode (CCM) under heavy loads to ensure the part operates with a fixed frequency. The advantage of CCM is its controllable frequency and lower output ripple. Under light-load conditions, if the inductor's valley current is below 0A, the MPQ7232 enters discontinuous conduction mode (DCM), and the LS-FET acts as an ideal diode. Choose a larger value inductor to ensure the part does not enter DCM during light loads. Otherwise, the LED current ripple will be too large, and decrease the lifetime of the LED.

Frequency Foldback

When V_{IN} exceeds 16V, the MPQ7232 enters frequency foldback. Then, f_{SW} decreases to half the nominal value and changes to 1.13MHz. If V_{IN} is below 15.6V, the frequency foldback is disabled and f_{SW} changes back to 2.25MHz.

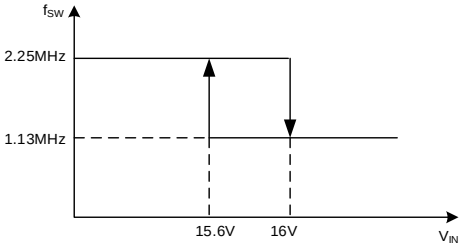

Figure 2: Frequency Foldback

EN/DIM Control

The EN/DIM control pin turns the regulator on and off. Drive the pin high to turn the regulator on; drive the pin low to turn the regulator off. An internal 500kΩ resistor placed between the EN/DIM and GND pins allows the EN/DIM pin to be floated to shut down the chip.

The EN/DIM pin is clamped internally with a 6.5V series Zener diode (see Figure 3). Use a pull-up resistor (R_{PULL_UP}) to connect the EN/DIM input and V_{IN} to limit the EN input current to less than 100µA. For example, with 12V connected to V_{IN}, R_{PULL_UP} ≥ (12V - 6.5V) / 100µA = 55kΩ.

To connect the EN/DIM pin to a voltage source via R_{PULL_UP}, limit the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

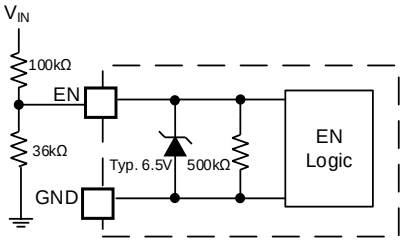

Figure 3: 6.5V Zener Diode Connection

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Driving EN/DIM low for more than 600ms typically shuts down the IC.

If the EN/DIM pin is needed to turn the IC on and off, the time (several seconds depending on the output capacitor (C_{OUT}) and VLED+) between EN turning off and on should be long enough to ensure the VLED+ voltage (V_{LED+}) drops below 2.7V, or an LED open fault will be triggered the next time EN is on. Unexpectedly triggering the LED open protection only happens when the IC shuts down for a long time (several seconds) and the IC needs to turn on for a short time. To avoid unexpectedly triggering LED open protection, it is recommended to place a 1kΩ dummy load in parallel with C_{OUT} to discharge V_{LED+} low. Using a PWM dimming frequency between 10Hz and 2kHz has no such limitation.

PWM Dimming

Apply an external 10Hz to 2kHz PWM signal to the EN/DIM pin for PWM dimming. The average I_{LED} is proportional to the PWM duty cycle. The minimum amplitude of the PWM signal is 1.65V. If the dimming signal is applied before the chip starts up, the first dimming signal's on time must be longer than 140µs for the part to fully reach the setting value (initial time is about 50µs and soft start is about 90µs). After 140µs, I_{LED} can reach the setting value. If the dimming signal is applied after soft start (SS) finishes, there is a 90µs delay to launch SS again. If the first pulse time is less than 50µs for start-up, The IC needs another 50µs to restart and another 90µs for SS.

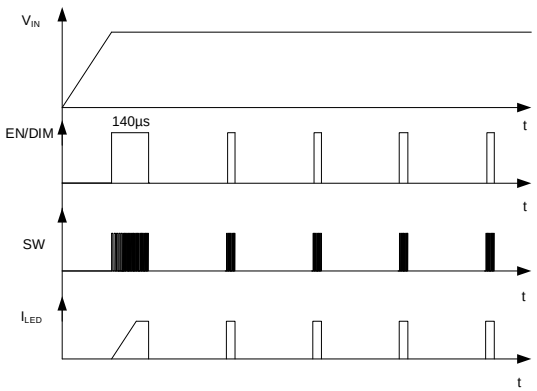

Figure 4: Timing with Active PWM Dimming

Analog Dimming

The MPQ7232 supports analog dimming by applying a 200mV to 1.6V DC voltage on the ADIM pin to linearly adjust the internal LED current V_{REF} from 25mV to 200mV. The DC voltage on the ADIM pin can be set at any time, even before EN rising edge/start-up.

Figure 5 shows the analog dimming curve. If the ADIM voltage (V_{ADIM}) drops below 100mV, the IC stops switching and the FAULT pin is pulled low to indicate a short-to-GND condition. When V_{ADIM} exceeds 200mV, the IC restarts and the I_{LED} amplitude is equal to (V_{ADIM} / 1.6 x I_{LED}), where I_{LED} is the LED current set by the resistor connected to the FB pin. The internal LED current V_{REF} can increase to 210mV when V_{ADIM} rises to 1.68V. If V_{ADIM} exceeds 1.68V, the part exits analog dimming and the internal LED current V_{REF} immediately decreases to 200mV. When V_{ADIM} decreases from a high voltage to 1.6V, the part can enter analog dimming. To avoid exceeding the max V_{REF} (typically 200mV), it is recommended to set V_{ADIM} between 1.6V and 1.68V.

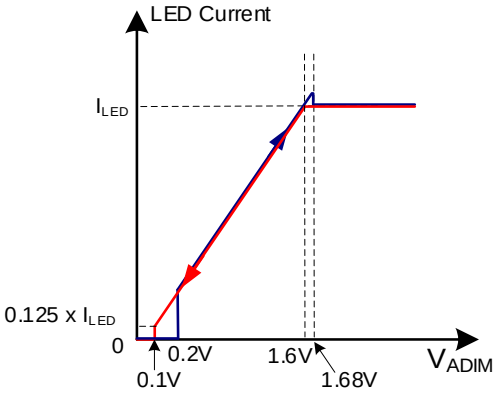

Figure 5: Analog Dimming

If analog dimming is not used, pull the ADIM pin to VCC. If the ADIM pin is floating, the internal pull-down resistor (R_{PULL_DOWN}) pulls the pin low and asserts FAULT low.

The IC requires a long time, at most 18 seconds, for ADIM short/open recovery before V_{LED+} decreases to 2.7V, otherwise there is a risk of mistriggering an LED open fault. To avoid unexpectedly triggering LED open protection, it is recommened to place a 1kΩ dummy load in parallel with C_{OUT} to discharge V_{LED+} low.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the VCC pin's output voltage. The V_{IN} UVLO rising threshold is 4V; its falling threshold is 3.5V.

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Internal Soft Start (SS)

SS prevents V_{OUT} from overshooting during start-up. When the chip starts up or restarts after a DIM_OFF period (at each EN/DIM rising edge), the internal circuitry generates an SS voltage (V_{SS}). The EA references V_{SS} for about 90µs. After 90µs, the EA uses V_{REF} as the reference.

Over-Current Protection (OCP)

The MPQ7232 features cycle-by-cycle peak current limit protection with valley-current detection. The inductor current (I_L) is monitored during the high-side MOSFET (HS-FET) on-state. If I_L exceeds the current-limit value set by the COMP high-clamp voltage, the HS-FET turns off immediately. Then the low-side MOSFET (LS-FET) turns on to discharge the energy, and I_L decreases.

The HS-FET remains off unless the inductor valley current falls below the valley current limit, even though the internal clock pulses high. If I_L does not drop below the valley current limit when the internal clock pulses high, the HS-FET misses the clock. Once I_L exceeds the current-limit value twice in the same dimming period (EN to level high), the MPQ7232 stops switching for the rest of the dimming pulse.

The over-current (OC) counter only resets after the EN/DIM falling edge. This over-current protection (OCP) is especially useful when the LED+ or LED- is shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. If OCP occurs, the MPQ7232 will not exit latch mode until V_{IN} power reset (POR) or the EN/DIM pin is pulled low.

LED Open Protection

The MPQ7232 monitors the internal EA output to detect whether the output circuit is open. If the LED is open, the internal EA output exceeds the over-voltage (OV) threshold and the part stops switching for the rest of the dimming pulse. Reset the part by power-on reset (POR) or pulling EN/DIM low. Under warm-crank conditions, V_{IN} goes low (as low as V_{OUT}). In this case, the duty cycle increases and may reach its maximum value, which can cause the internal compensation to exceed the EA's output OV threshold. To avoid an incorrect LED open detection, this protection is disabled anytime V_{IN} is below 7V.

Thermal Shutdown (TSD)

TSD prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 165°C, the entire chip shuts downs and the FAULT pin is pulled low. Once the temperature falls below its lower threshold (typically 145°C), the chip starts up again immediately with SS and the FAULT pin is pulled high.

Fault Indicator

The MPQ7232 has fault indication. The FAULT pin is the open drain of a MOSFET, and should be connected to VCC or another voltage source through a resistor (e.g. 100kΩ). The FAULT pin is pulled high during normal operation. If an OCP, LED short to GND, open, TSD, or ADIM short/open fault occurs, this pin is pulled low to indicate a fault. However, the FAULT pin does not assert during SS unless TSD or ADIM short/open is triggered.

If an LED short to GND, LED open, or OCP condition is detected, FAULT asserts until the next EN/DIM rising edge. If an ADIM short to GND/open condition is detected, FAULT asserts until ADIM exceeds 200mV. If TSD occurs, FAULT asserts until the temperature falls below its lower threshold (typically 145°C). The FAULT pin is pulled high after the part is disabled.

Figure 6 and Table 1 on page 21 summarize the device behavior under various fault conditions.

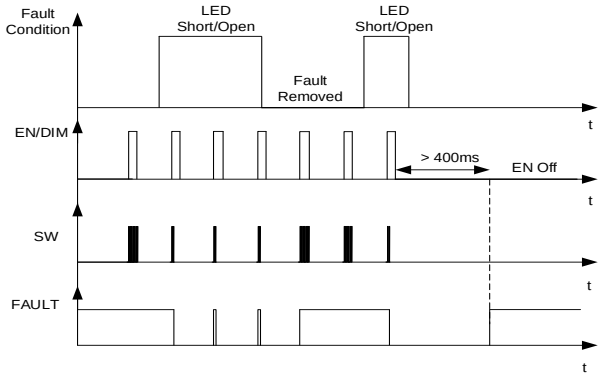

Figure 6: Fault Indication

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Table 1: Fault Detection

Fault Condition	Detection
ADIM short to GND	V_{ADIM} < 100mV
ADIM open	
LED+ short to GND	Current limit triggered 2 times
LED- short to GND	
LED open	V_{COMP} > 2V
TSD	T_J > 165°C

Frequency Spread Spectrum (FSS)

Frequency spread spectrum (FSS) minimizes peak emissions at a specific frequency.

The MPQ7232 uses a 9kHz triangle wave (55.5µs rising and falling) to modulate the internal oscillator. The FSS span is ±5% (see Figure 7). The same ±5% range also applies during frequency foldback when V_{IN} exceeds 16V.

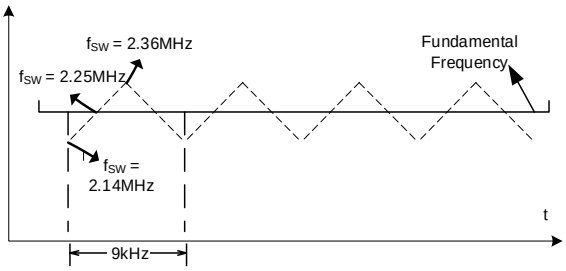

Figure 7: Frequency Spread Spectrum

Floating Driver and Bootstrap Charging

An external bootstrap (BST) capacitor (C_{BST}) powers the MOSFET's floating driver. This floating driver has its own UVLO protection. The UVLO rising threshold is 2.2V, with a 150mV hysteresis. The C_{BST} voltage is internally regulated by V_{IN} and V_{CC} through D1, D2, M1, R1, C1, L1, and C2 (see Figure 8). The C_{BST} voltage charges quickly via V_{CC} through M1. The 1µA input to BST current source also charges C_{BST} when the LS-FET does not turn on.

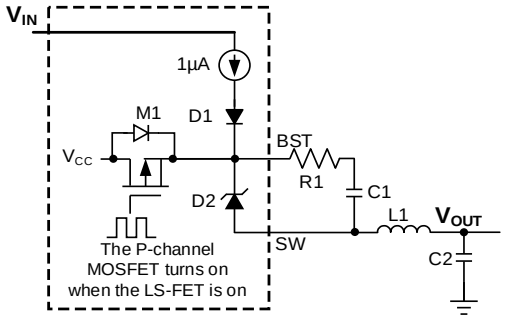

Figure 8: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceeds their appropriate thresholds, the MPQ7232 starts up. The reference block starts generating a stable V_{REF} and currents, then enables the internal regulator. The regulator provides a stable supply for the remaining circuitry. This takes about 50µs before the part enters internal SS.

Two events can shut down the chip: pulling the EN pin low for more than 600ms, or V_{IN} going low. During shutdown, the signaling path is blocked to avoid any fault triggering. V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Current

The external feedback (FB) resistor (R_{FB}) sets I_{OUT} (see Figure 9).

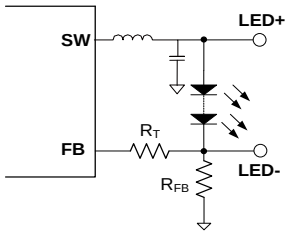

Figure 9: Feedback Network

The feedback V_{REF} is 0.2V, and I_{LED} can be calculated with Equation (1):

$$I_{LED} = \frac{0.2V}{R_{FB}} \quad (1)$$

R_T sets the loop bandwidth. The lower the value of R_T, the higher the bandwidth. A higher bandwidth may cause insufficient phase margin, resulting in loop instability. A proper R_T value must make a tradeoff between the bandwidth and phase margin. Table 2 lists the recommended R_{FB} and R_T values for common outputs with 1 or 2 series LEDs.

Table 2: Resistor Values for Common Outputs

I_{LED} (A)	R_{FB} (mΩ)	R_T (kΩ)
1	200 (1%)	150 (1%)
2	100 (1%)	100 (1%)
4	50 (1%)	100 (1%)
6	33.3 (1%)	100 (1%)

For example, choose R_{FB} to be 50mΩ for a 4A I_{LED}. A 2A I_{LED} can be achieved if V_{ADIM} = 800mV.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. For best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the small capacitor as close to the IN and GND pins as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor (I_{CIN}) can be estimated with Equation (2):

$$I_{CIN} = I_{LED} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case scenario occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (3):

$$I_{CIN} = \frac{I_{LED}}{2} \quad (3)$$

Choose an input capacitor (C_{IN}) with an RMS current rating that exceeds half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC pin as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The V_{IN} ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LED}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep a low V_{OUT} ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (5)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW}, and causes the majority of the output voltage ripple.

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ΔV_{OUT} can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. ΔV_{OUT} can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (7)$$

The characteristics of C_{OUT} also affect the stability of the regulation system. The MPQ7232 can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating that is 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower ΔV_{OUT}. However, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance (L) is to allow the inductor ripple current to be approximately 30% of the maximum load current. L can be calculated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum peak inductor current (I_{LP}) can be calculated with Equation (9):

$$I_{LP} = I_{LED} + \frac{V_{OUT}}{2 f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

BST Resistor and Capacitor

A 10Ω resistor in series with C_{BST} is required to reduce the SW spike voltage. A higher resistance leads to better SW spike reduction, but decreases efficiency. If C_{BST} or the BST resistor is disconnected, the HS-FET cannot turn on. In this case, V_{COMP} increases and the part detects an error amplifier output (EAO) OV. This triggers LED open protection, and the FAULT pin is pulled low.

The recommended C_{BST} is between 0.1µF and 1µF (See Figure 10).

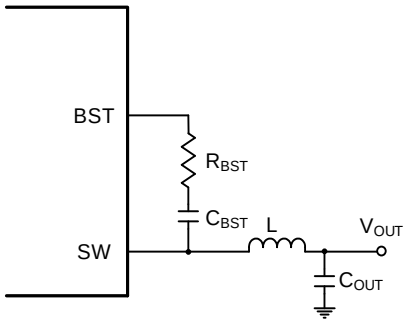

Figure 10: Recommended BST Circuit

Low Dimming Frequency Application

For applications with low PWM dimming frequencies at small dimming duty cycles, the EA's V_{OUT} (V_{COMP}) may be discharged by the leakage if the dimming off time is too long. The minimum dimming frequency should not be below 10Hz.

Note that driving the EN/DIM pin low for longer than 600ms (typical) shuts down the IC.

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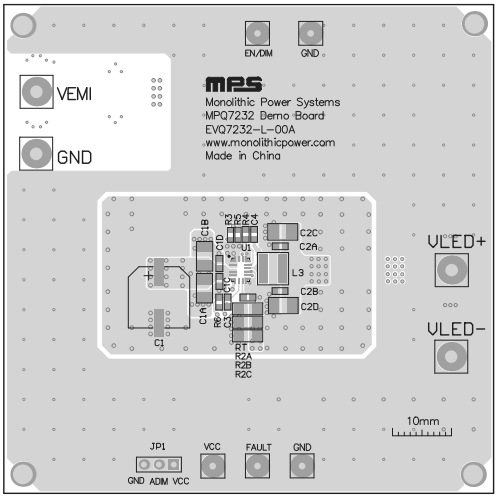
PCB Layout Guidelines (10)

Efficient PCB layout is critical for stable operation and thermal dissipation. To ensure an effective layout design, refer to Figure 9 and follow the guidelines below:

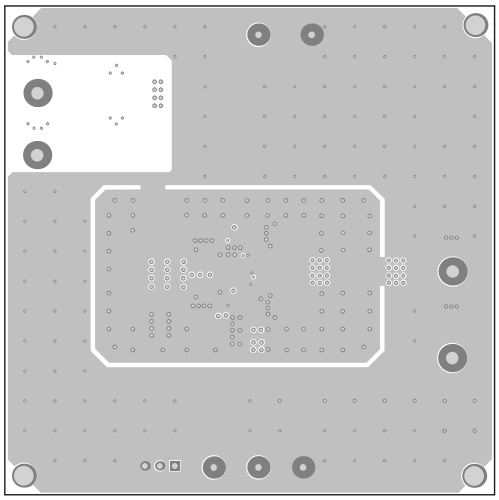
1. Connect a large ground plane directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
2. Ensure the high-current paths at PGND and IN have short, direct, and wide traces.
3. Place the ceramic input capacitor, especially the small package (0603) input bypass capacitor, as close to IN and PGND as possible to minimize high-frequency noise.
4. Keep the connection between the input capacitor and the IN pin as short and wide as possible.
5. Place the VCC capacitor as close to the VCC and GND pins as possible.
6. Route SW and BST away from sensitive analog areas, such as FB.
7. Place the feedback (FB) resistors close to the chip to make the trace connected to FB as short as possible.
8. Use multiple vias to connect the power planes to the internal layers.

Note:

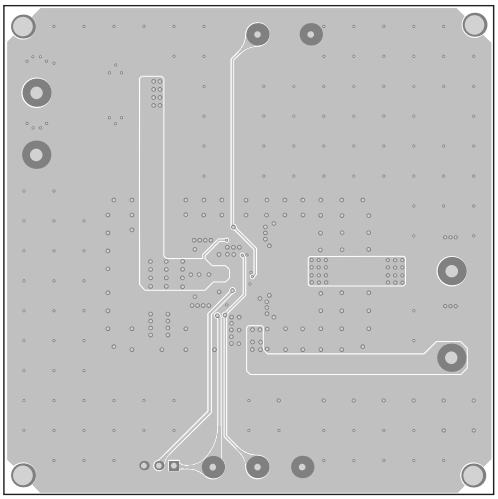
10) The recommended layout is based on the typical application circuit on page 25 (see Figure 12).



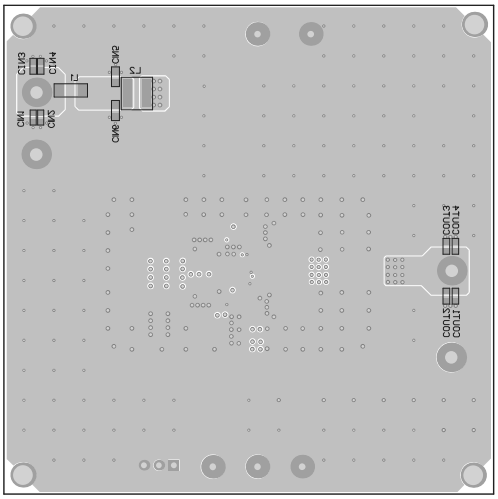
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 11: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

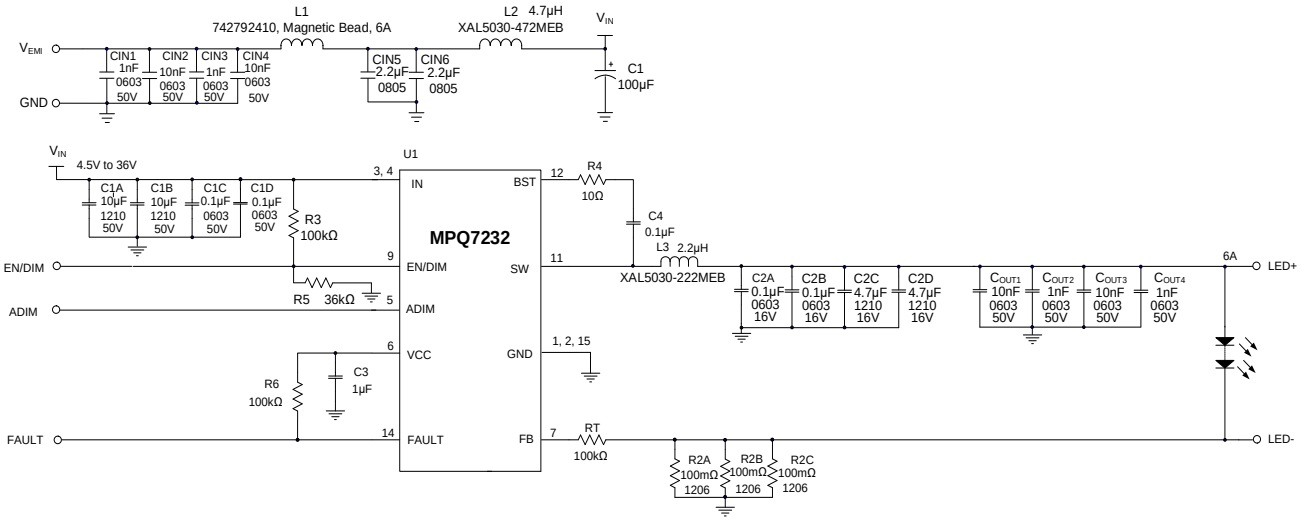

Figure 12: Typical Application Circuit with EMI Filters (I_{LED} = 6A)

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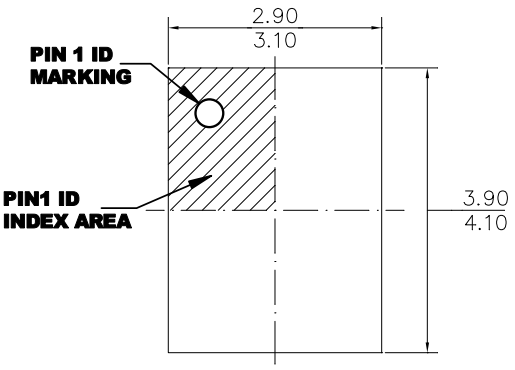
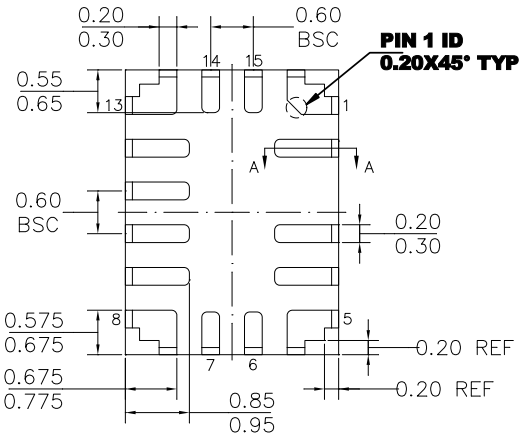
PACKAGE INFORMATION

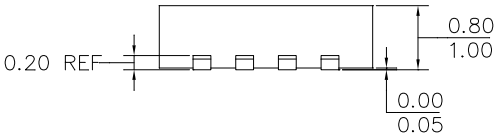
QFN-15 (3mmx4mm)
Wettable Flank



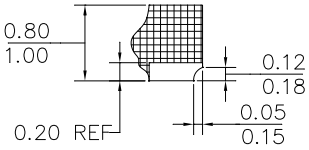
TOP VIEW



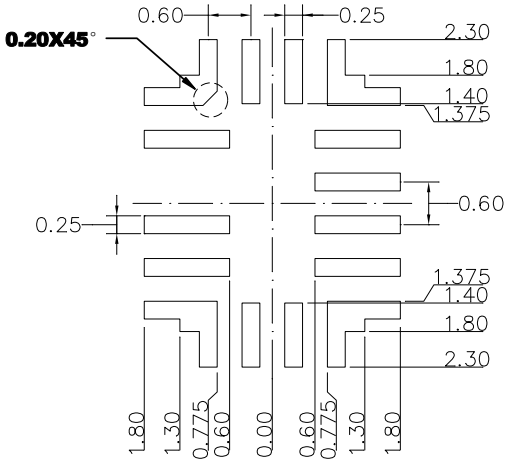
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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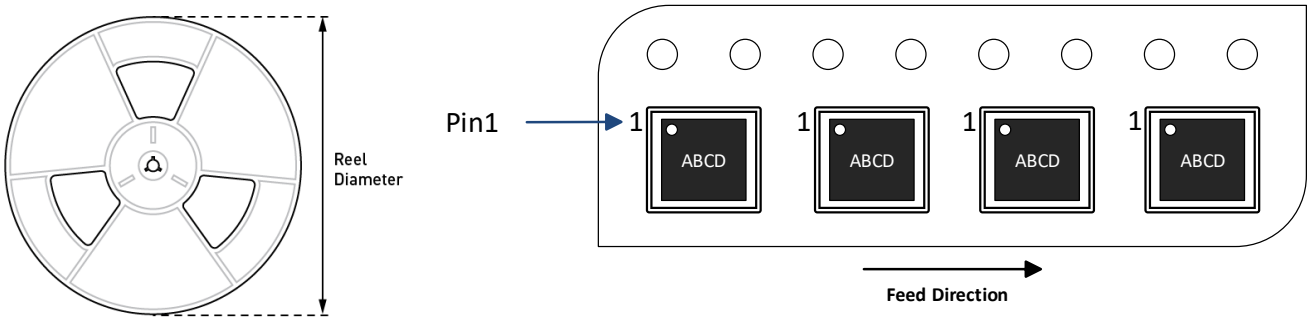
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7232GLE-AEC1-Z	QFN-15 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/1/2024	Initial Release	-

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