MPQ7224

16-Channel Current Sink LED Driver with Pre-Programmed Animations, AEC-Q100 Qualified

DESCRIPTION

The MPQ7224 is a 16-channel current sink LED driver. Each channel is rated for up to 200mA of current, and 16 ICs can be cascaded together to create a 256-channel solution.

The MPQ7224 is optimized for animated or dynamic lighting applications. It employs a 12-bit pulse-width modulation (PWM) dimming and 6-bit analog dimming register per channel, with individual control of each channel.

The MPQ7224 features adaptive feedback control (AFC) to maximize system efficiency. The pre-regulator (e.g. buck voltage regulator) output voltage (V_{OUT}) is adjusted in real time so that the voltage across the channels is kept at a minimum value.

Frequency spread spectrum (FSS) optimizes EMC performance. The LED current's ramping rate and phase shift between channels can be digitally configured as well.

The MPQ7224 can output a signal via its READYOUT pin to delay the start-up of one or more ICs in the system, allowing for proper sequencing in animated applications.

The MPQ7224 can aid a system design for functional safety with a failsafe (FS) indicator. Protection features include LED open/short protection, ISET pin open/short protection, and thermal shutdown. If a fault occurs, the fault indicator pulls low.

The MPQ7224 is available in a QFN-32 (5mmx6mm) package. It is AEC-Q100 qualified.

FEATURES

- Scalability
  - 16 Channels, 200mA/Channel (Max Current)
  - Cascade up to 16 ICs for Up to 256 Channels
  - Pin-Configurable Device Address
- Designed for Automotive Applications
  - Supports 2.5V Cold Crank

FEATURES *(continued)*

  - -40°C to +150°C Operating Junction Temperature (T_J)
- Cooler Thermals and Optimized Efficiency
  - Adaptive Feedback Control (AFC) Dynamically Optimizes Pre-Regulator Output
  - 300mV Current Sink Headroom at 200mA
  - Headroom Optimization for Multiple ICs
- Selectable Built-In Animations
  - Immediate Animation
  - Sequential Animation
  - Breathing Animation
- Optimized for EMI/EMC Reduction
  - Configurable Phase Shift and Slew Rate
  - FSS (Internal Clock)
  - Selectable PWM Dimming Frequency
  - CISPR25 Class 5 Compliant
- Additional Features
  - Functional Safety System Design Capable MPSafe™ Compatible – Functional Safety Supporting Document Available
  - Failsafe (FS) Pin for System Protection and Diagnostics
    - LED Short (to GND and Battery)
    - LED Open
    - Thermal Warning and Shutdown
    - ISET Pin Open/Short
- One-Time Programmable (OTP) Memory
- Available in a QFN-32 (5mmx6mm) Package with Wettable Flank
- Available in AEC-Q100 Grade 1

MPSafe™ FuSa Compatible

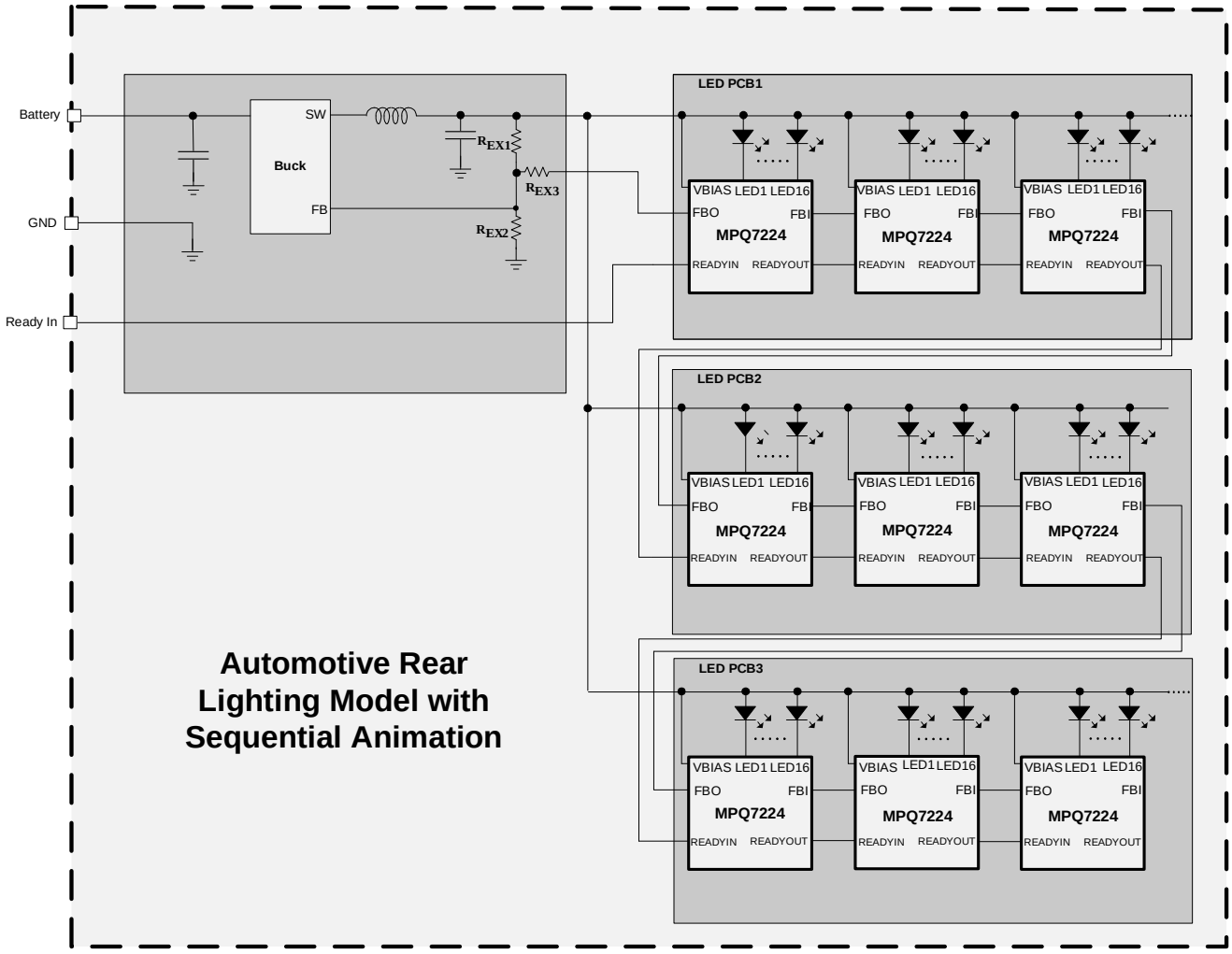
APPLICATIONS

- Dynamic/Animated Tail Lights
- Daytime Running Lights (DRLs)
- Turn Signals
- Puddle Lights

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ7224GQJE-xxxx-AEC1***, ****	QFN-32 (5mmx6mm)	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MPQ7224GQJE-xxxx-AEC1-Z).

** Moisture Sensitivity Level Rating

*** “xxxx” is the configuration code identifier for the register settings stored in the OTP register. Each “x” can be a hexadecimal value between 0 and F. The default code is “0000”. Contact an MPS FAE to create this unique number.

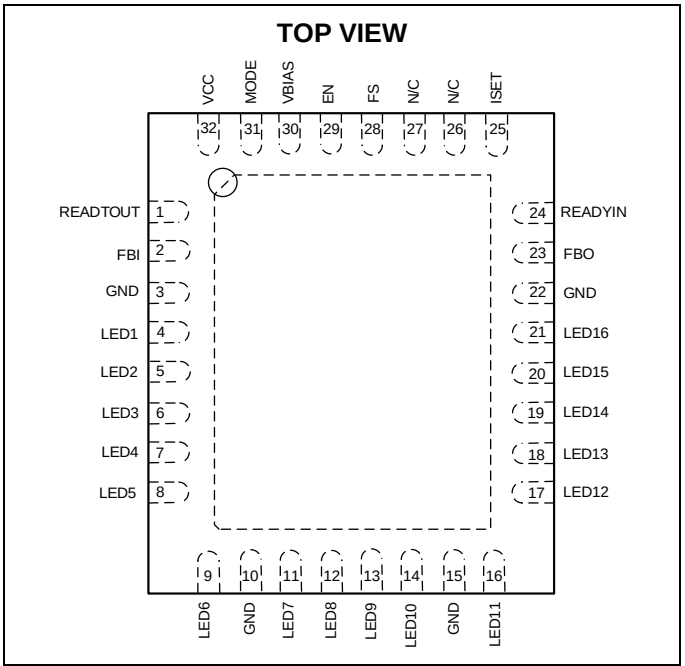
**** Wettable flank

TOP MARKING

MPSYYWW
MP7224
LLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP7224: Part number
LLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-32 (5mmx6mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	READYOUT	**Ready output.** The READYOUT pin is a synchronous open-drain output pin that supports the delay between multiple devices for sequential animation. READYOUT is pulled up to VCC using a 100kΩ resistor. For immediate animation or breathing animation, pull READYOUT low.
2	FBI	**Feedback input.** The FBI pin indicates the current sink headroom information input between multiple MPQ7224 devices. Connect the master device's FBI pin and GND pins. Connect to the slave device's FBI and FBO pins. If adaptive feedback control (AFC) is not used, connect to FBI to GND.
3, 10, 15, 22	GND	**Ground.** GND is the reference ground of the power device, and requires careful consideration during PCB layout.
4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21	LED1–LED16	**LED channel 1–16 current inputs**. Connect the cathodes of LED channels 1–16 to these pins.
23	FBO	**Feedback output.** Connect to the FBO pin to the DC/DC converter's feedback pin through a resistor divider network. FBO is the current sink headroom information output between multiple MPQ7224 devices. Float FBO if AFC is not used.
24	READYIN	**Ready input.** After the VCC, EN, and VBIAS pins reach their respective UVLO rising thresholds and the READYIN pin is pulled high, the IC starts up with the built-in animation. READYIN is a synchronous input that supports the delay between multiple devices for sequential animation. READYIN cannot be controlled by READYOUT for immediate animation or breathing animation.
25	ISET	**LED current setting.** Connect an external resistor between the ISET and GND pins to set the average LED current (I_{LED}). (I_{LED} for each channel (mA) = 600 / R_{ISET}(kΩ).) If ISET is shorted to ground or an open condition is detected, the device latches off and asserts FS.
26, 27	N/C	**Not connected.**
28	FS	**Failsafe output.** The FS pin is an active-low, open-drain output. FS pulls low if any of the following occur: LED short, LED open, thermal shutdown, ISET pin open, or ISET pin short. The FS pin can support a continuous connection to VBIAS or VCC through a pull-up resistor. Float FS if it is not used.
29	EN	**Enable input.** Pull EN above 2.2V to turn the device on; pull EN below 0.8V to turn it off. Don't float EN pin is not used.
30	VBIAS	**Bias supply.** The MPQ7224 operates from a 2.5V to 18V input rail. Decouple the input rail using an input capacitor (C_{IN}). The VBIAS pin is also the power supply for VCC.
31	MODE	**Mode selection.** The MODE pin is used for master/slave mode selection. Tie MODE to GND to configure the master mode, or tie MODE to VCC to configure the slave mode.
32	VCC	**Internal bias supply.** The VCC pin is powered from VBIAS, and it supplies power to the internal control circuitry and gate drivers. Connect a ≥10μF decoupling capacitor and 1kΩ to 10kΩ resistor from VCC to ground. Place this capacitor close to the VCC pin. VCC requires power from an external source if the VBIAS voltage (V_{BIAS}) is below 3.5V.
-	Exposed pad	**Exposed thermal pad.** The exposed pad has no internal electrical connection to GND. Connect the exposed pad to the external GND plane on the board for optimal thermal performance.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

VBIAS voltage (V_{BIAS}).....-0.3V to +20V
LEDx voltage (V_{LEDx}) .....-0.3V to +20V
FBO, EN, FS, READYIN, READYOUT……
……..-0.3V to +20V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-32 (5mmx6mm)..... 5.9W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (3)
Charged-device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

V_{CC} (if supplied externally) .....3.1V to 3.5V
V_{BIAS} .....2.5V to 18V
LED current (I_{LED})..... 200mA/ch
Operating T_J..... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-32 (5mmx6mm)			
JESD51-7	23.8	1.4	°C/W (5)
EVQ7224-QJ-00A	21.2	0.93	°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-5,7, 4-layer PCB, where a thermal via array under the exposed pad. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-5,7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on the MPQ7224 standard EVB, a 83.5mmx83.5mm, 4-layer PCB, 2oz. And the value of θ_{JC} shows the thermal resistance from junction-to-case top.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Bias supply current	I_{BIAS}	Disabled, EN pin is low (shutdown)		0.5	2.5	µA
		Enabled, no LED load (EN pin is high, EN_ANA bit = 0, quiescent current), VCC is supplied externally, V_{BIAS} = 6.5V		0.6	1	mA
		Enabled, no LED load (EN pin is high, EN_ANA bit = 0, quiescent current), VCC is supplied externally, V_{BIAS} = 14V		1.4	2.1	mA
		Enabled, no LED load (EN pin is high. EN_ANA bit = 0, quiescent current), VCC supplied internally, V_{BIAS} = 6.5V		7	12	mA
		Enabled, no LED load (EN pin is high, EN_ANA bit = 0, quiescent current) VCC internally supplied, V_{BIAS} = 14V		8	13	mA
VBIAS under-voltage lockout (UVLO) threshold	V_{BIAS_UVLO}	Rising edge		1.8		V
		Falling edge		1.6		V
VCC supply current	I_{CC}	Only required if VCC is supplied externally; Disabled, EN pin is low (shutdown), V_{CC} = 3.5V		0.05	60	µA
		Only required if VCC is supplied externally; V_{CC} = 3.5V, enabled, no LED load (EN pin is high, quiescent current)		6.5	13	mA
		Only required if VCC is supplied externally; V_{CC} = 3.5V, 16 LED channels are enabled (EN pin is high, EN_ANA bit = 1, PWM duty = 100%, R_{ISET} = 6.04kΩ, I_{LED} = 100mA)		12	20	mA
Internal VCC regulator voltage	V_{CC}	I_{VCC} = 0mA	3.1	3.3	3.5	V
V_{CC} under-voltage lockout (UVLO) threshold	V_{CC_UVLO}	Rising edge	2.8	3	3.2	V
		Falling edge	2.6	2.8	3	V
LED Current						
LED current (channel output to ideal current error)	I_{LED}	R_{ISET} = 3.01kΩ, T_J = 25°C	194.35	199.34	204.32	mA
		R_{ISET} = 3.01kΩ, T_J = -40°C to +150°C	189.37	199.34	209.3	mA
		R_{ISET} = 6.04kΩ, T_J = 25°C	96.85	99.34	101.82	mA
		R_{ISET} = 6.04kΩ, T_J = -40°C to +150°C	94.37	99.34	104.3	mA
Current sink headroom		I_{LED} = 200mA		300	400	mV
		I_{LED} = 100mA		150	250	mV
		I_{LED} = 50mA		75	125	mV
ISET voltage	V_{ISET}	R_{ISET} = 3.01kΩ (or I_{ISET} = 200µA)	0.57	0.60	0.63	V
Channel output leakage current	I_{LKG}	PWM duty = 0% (a single channel), T_J = -40°C to +150°C			2	µA
		PWM duty = 0% (all 16 channels), T_J = -40°C to +150°C			32	µA

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Channel-to-channel current error	I_{EER_CC}	I_{ERR_CC} = (I_{OUTI} - I_{AVE}) / I_{AVE} x 100%, 100mA, 200mA	-5%		+5%	
Dimming						
Pulse-width modulation (PWM) dimming frequency	f_{PWM}	Default setting	225	250	275	Hz
f_{PWM} range		Configuration range	250		1000	Hz
PWM duty slew rate	t_{PWM}	12-bit resolution, f_{PWM} = 250Hz	0.8	1	1.2	µs
Phase shift delay	t_{DELAY}	PHASE_SHIFT= 11	16	20	24	µs
I_{LED} slew rate during PWM dimming		SLEW_RATE = 01, rising edge, R_{ISET} = 6.04kΩ	2	5	10	µs
		SLEW_RATE = 11, rising edge	8	20	32	µs
READYIN high to LED on delay	t_{ON_DELAY}	Immediate animation, no phase shift		10		µs
READYIN low to LED off delay	t_{OFF_DELAY}	Immediate animation, no phase shift		2		µs
Protection (Selectable Latch-Off or Hiccup Mode)						
LED short protection threshold	V_{LED_S}	LED_SHORT_THR = 00	1.8	2.1	2.3	V
LED short protection time	t_{LED_S}	V_{LEDx} > V_{LED_S}	3.6	4	4.4	ms
LED open protection threshold	V_{LED_O}	At LED on, real-time monitoring (cover pin short-to-GND)	50	100	150	mV
LED open protection time	t_{LED_O}	V_{LEDx} < 100mV	3.6	4	4.4	ms
ISET pin short current threshold (FS, latch)	I_{ISET_STH}		0.7	1	1.3	mA
ISET pin open current threshold (FS, latch)	I_{ISET_OTH}		2	4.5	7	µA
Thermal warning threshold (7)	T_{WARN}		135	150	165	°C
Thermal warning hysteresis (7)	T_{WARN_HYS}			20		°C
Thermal shutdown threshold (7)	T_{SD}		155	170	185	°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C
Failsafe Output (FS) (Open Drain)						
Failsafe low-level output voltage	V_{FS_OL}	I_{FS_OL} = 2mA, active	0.15	0.33	0.5	V
Failsafe input current leakage	I_{FS_LKG}	Inactive			1	µA
Failsafe assertion deglitch time	t_{FS_TD}		5	20	40	µs
Ready Input (READYIN)						
READYIN threshold	V_{RI_H}	V_{RI} - V_{GND}	2			V
	V_{RI_L}	V_{RI} - V_{GND}			0.8	V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN threshold	V_{EN_R}	V_{EN} - V_{GND}	2.2			V
	V_{EN_F}	V_{EN} - V_{GND}			0.8	V

Note:

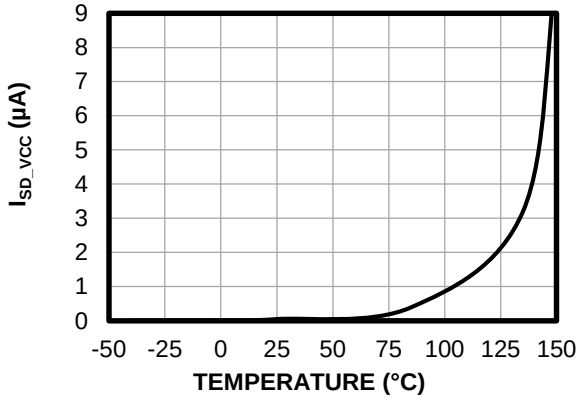
7) Guaranteed by design and characterization. Not tested in production.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

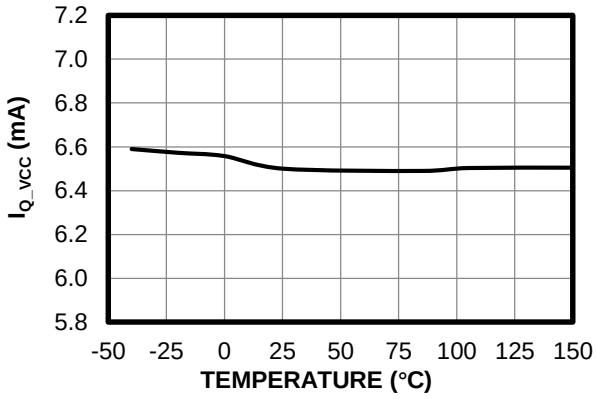
TYPICAL CHARACTERISTICS

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, unless otherwise noted.

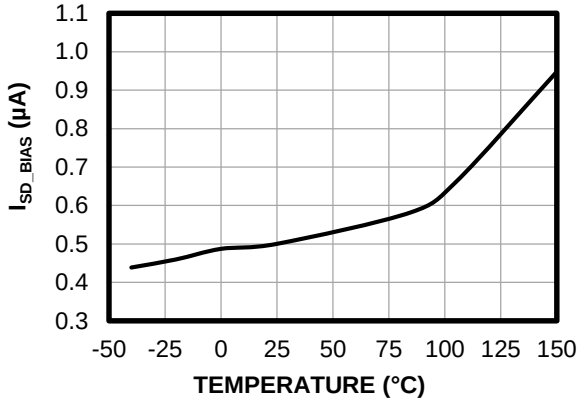
VCC Shutdown Current vs. Temperature



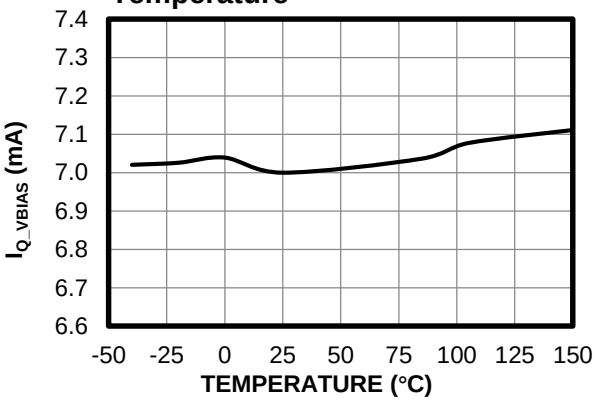
VCC Quiescent Current vs. Temperature



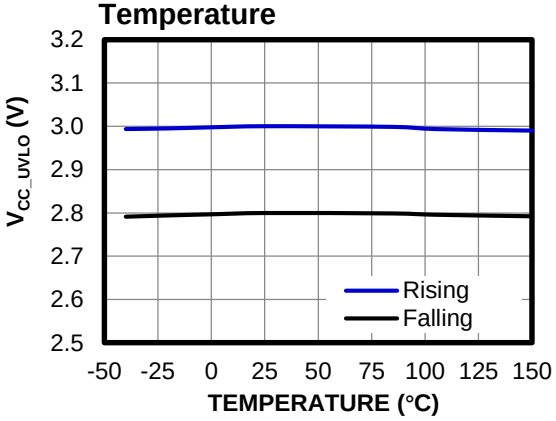
VBIAS Shutdowon Current vs. Temperature



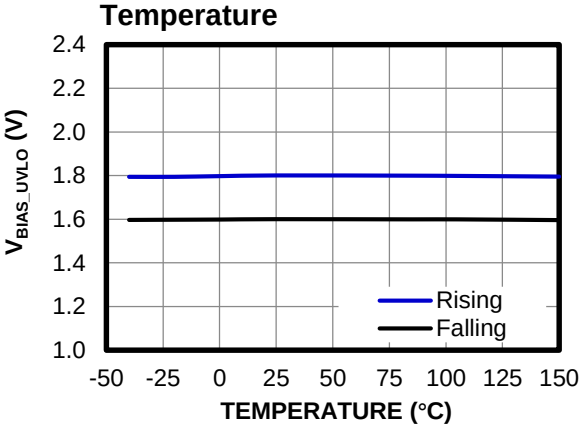
VBIAS Quiescent Current vs. Temperature



V_{CC} UVLO Threshold vs. Temperature



VBIAS UVLO Threshold vs. Temperature

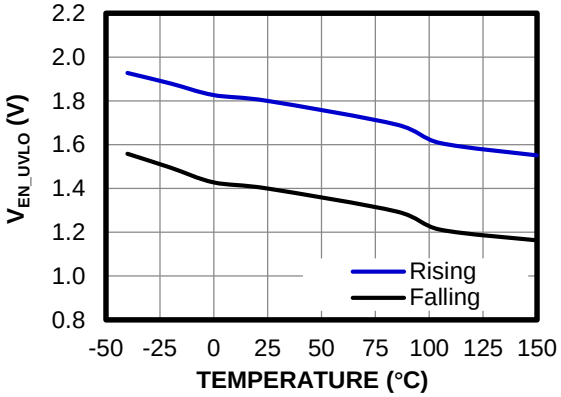


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

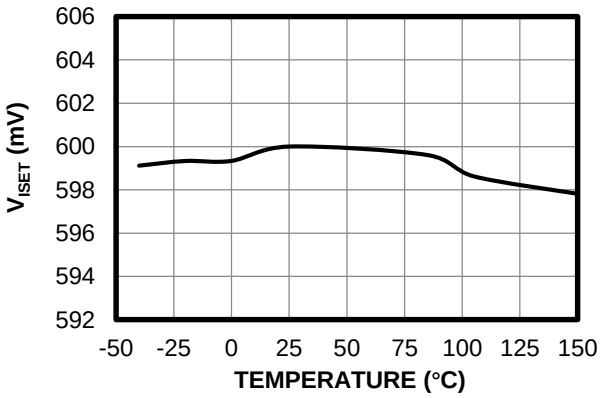
TYPICAL CHARACTERISTICS *(continued)*

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, unless otherwise noted.

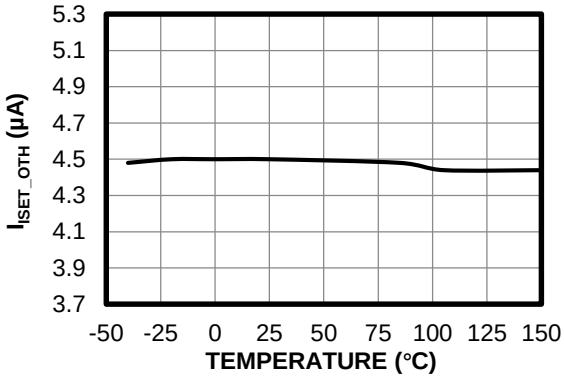
EN UVLO Threshold vs. Temperature



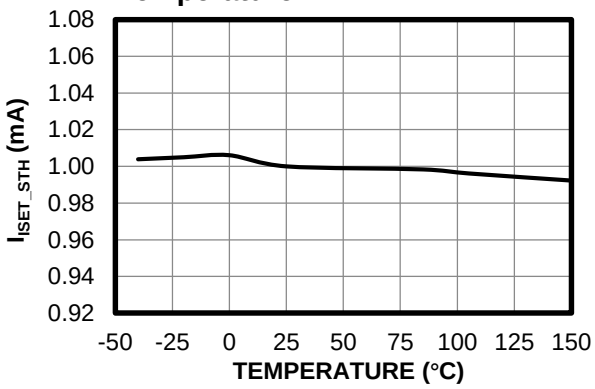
ISET Voltage vs. Temperature



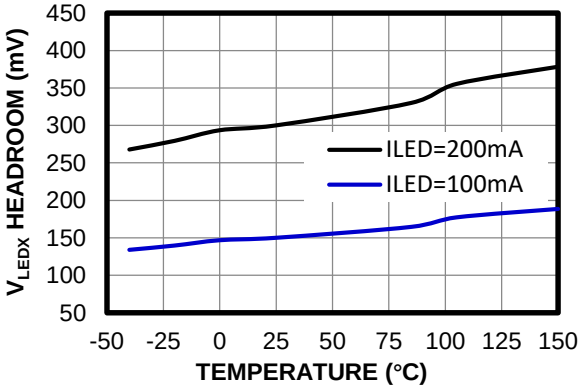
ISET Open Threshold vs. Temperature



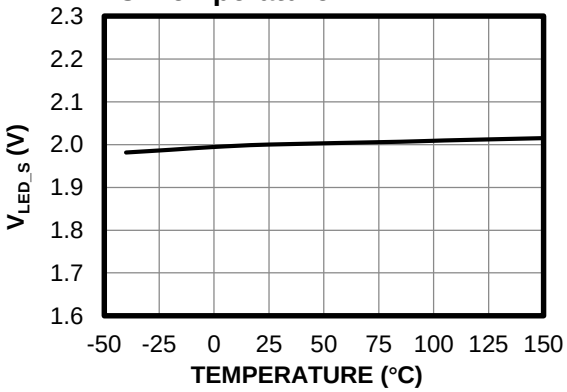
ISET Short Threshold vs. Temperature



LEDx Voltage Headroom vs. Temperature



LED Short Protection Threshold vs. Temperature

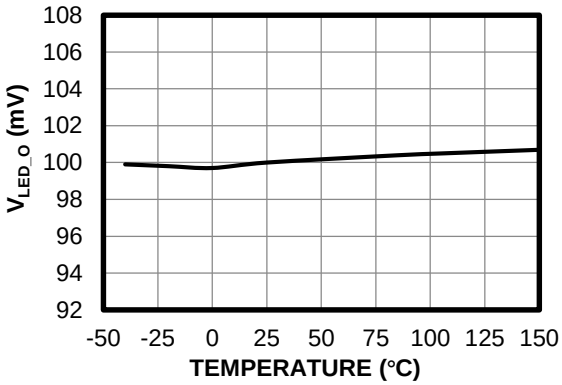


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

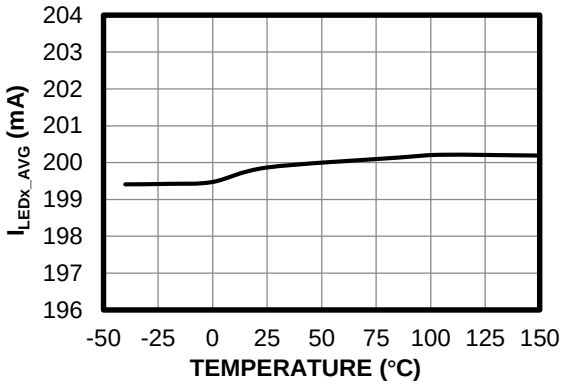
TYPICAL CHARACTERISTICS *(continued)*

V_{BIAS} = 6.5V, T_J = -40°C to +150°C, unless otherwise noted.

LED Open Protection Threshold vs. Temperature



LEDx Average vs. Temperature



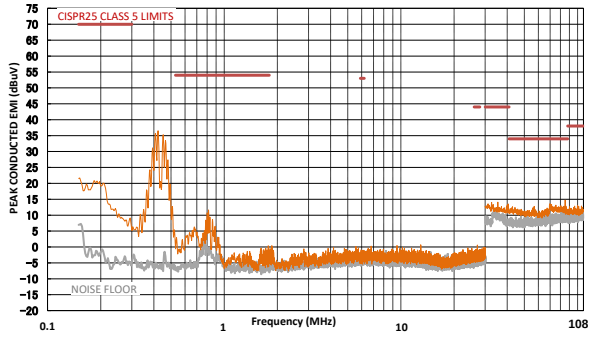
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

2 LEDs in series (V_{LEDx} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (8)

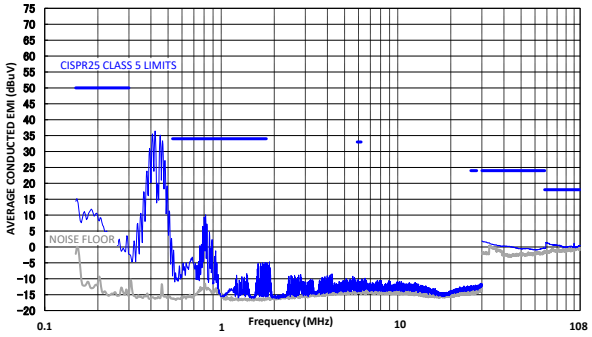
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



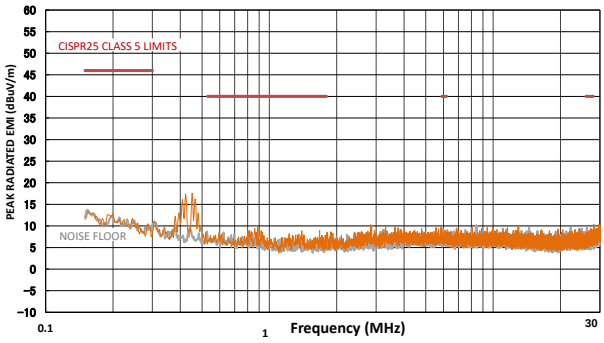
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



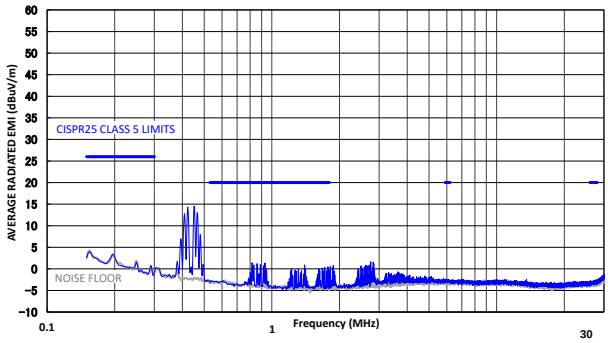
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



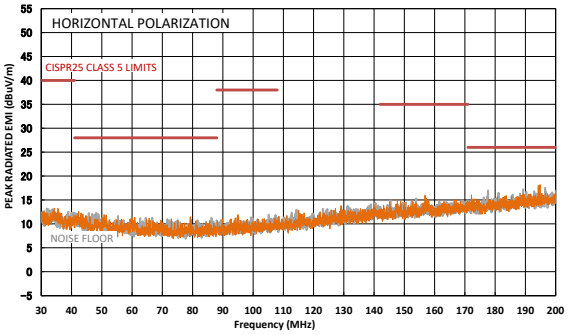
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



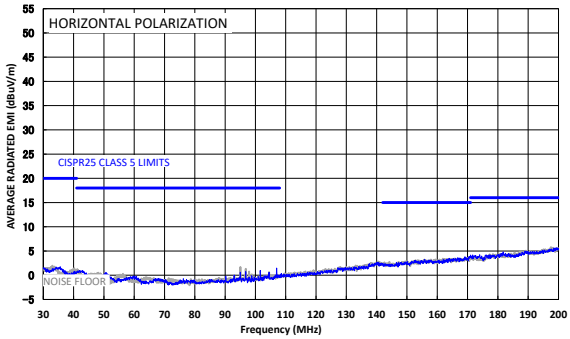
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



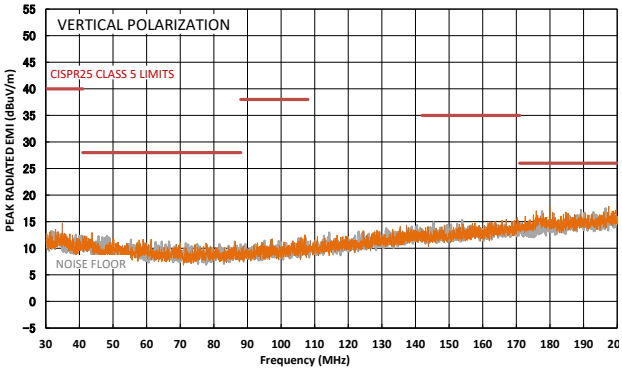
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LEDx} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (8)

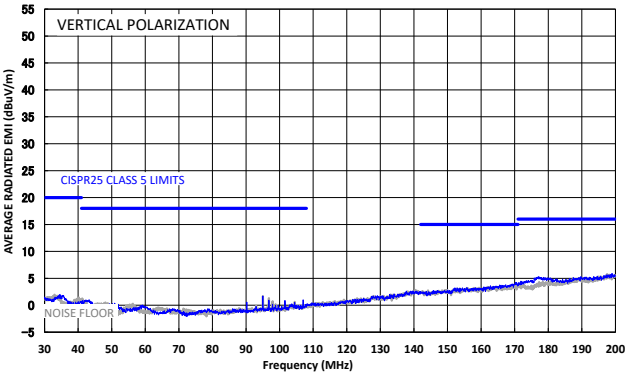
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



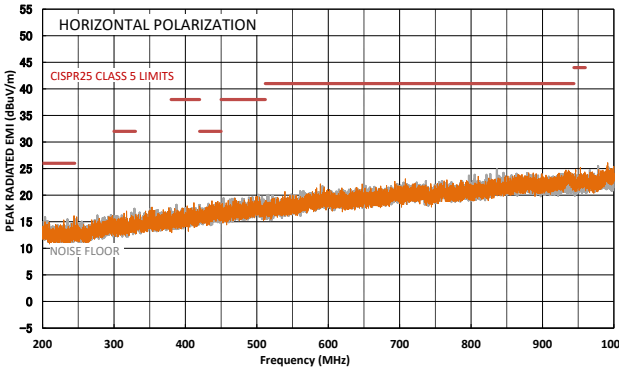
CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



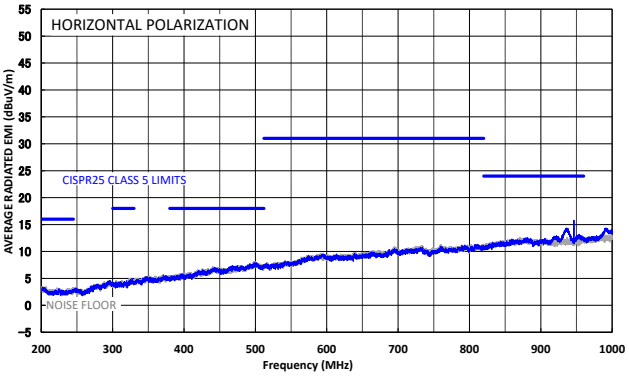
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



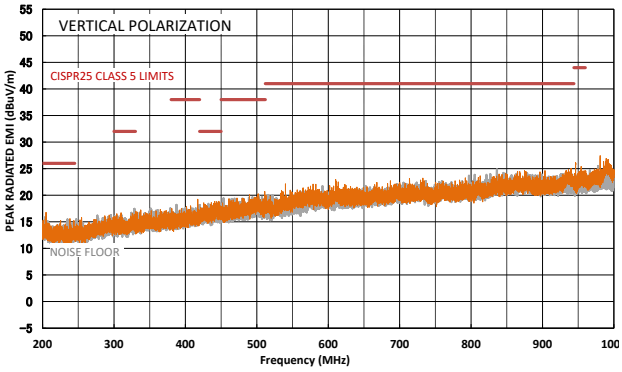
CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



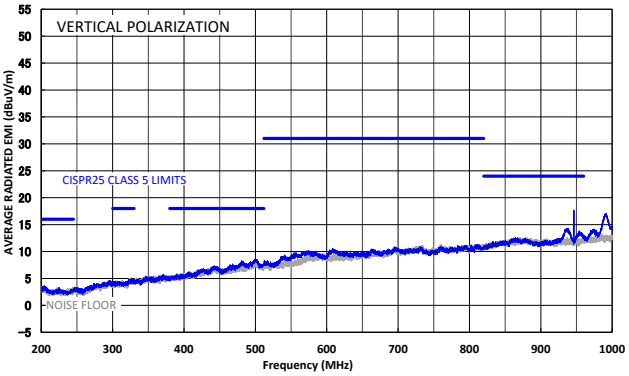
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

8) The EMC test results are based on Figure 15 on page 34.

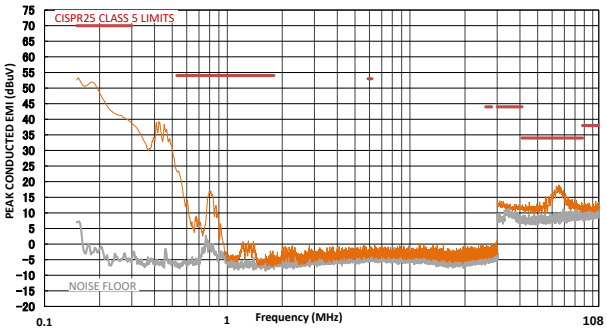
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LEDx} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (9)

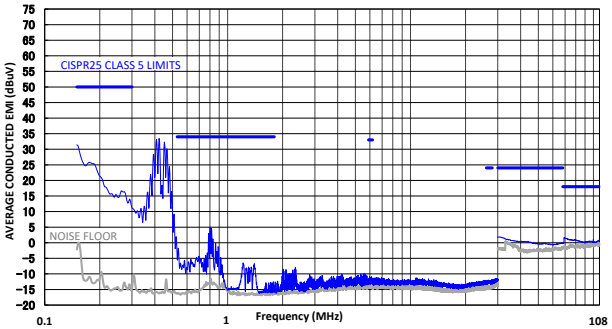
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



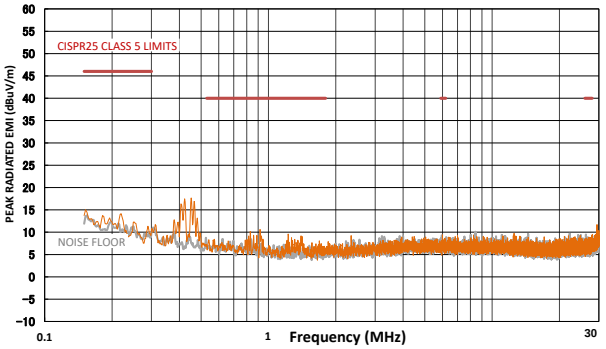
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



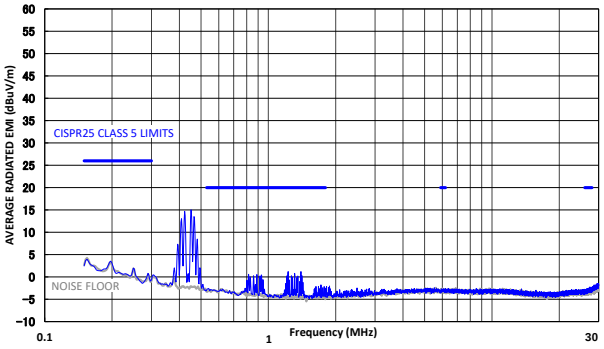
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



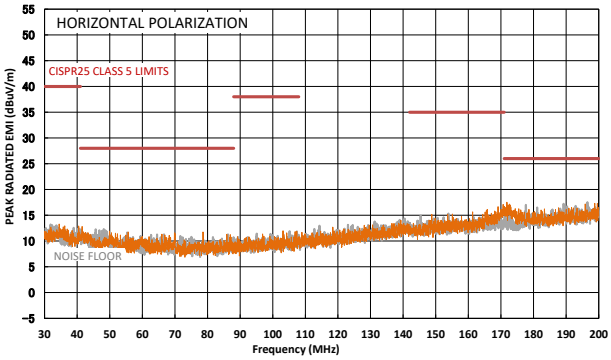
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



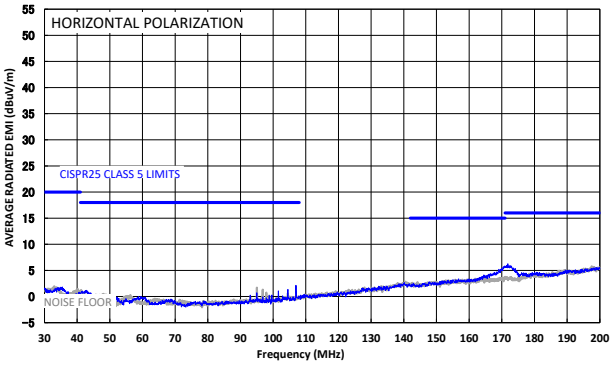
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz



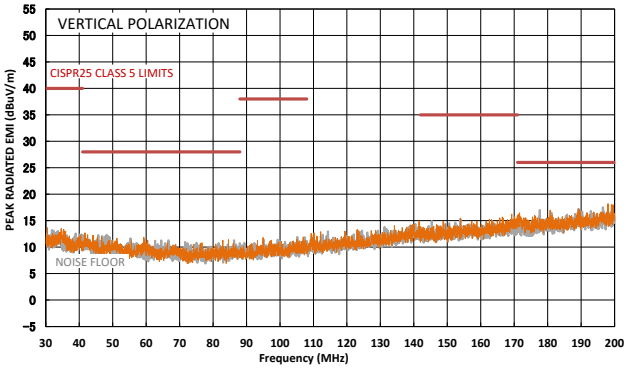
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LEDx} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted. (9)

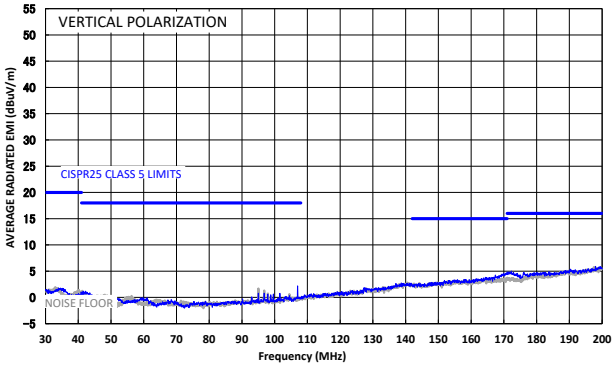
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



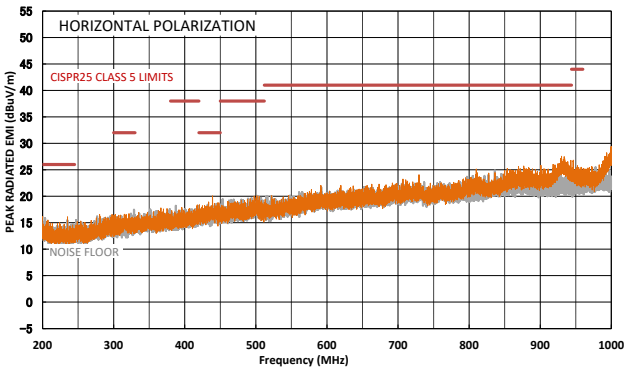
CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



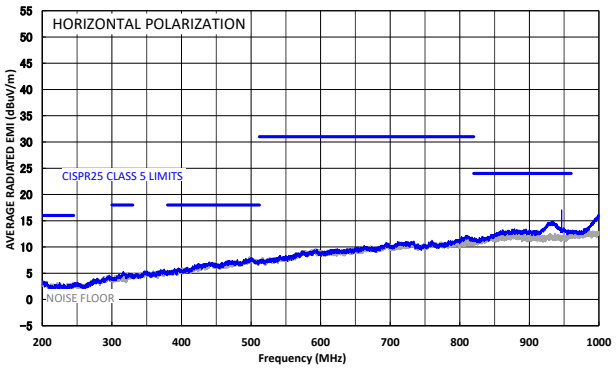
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



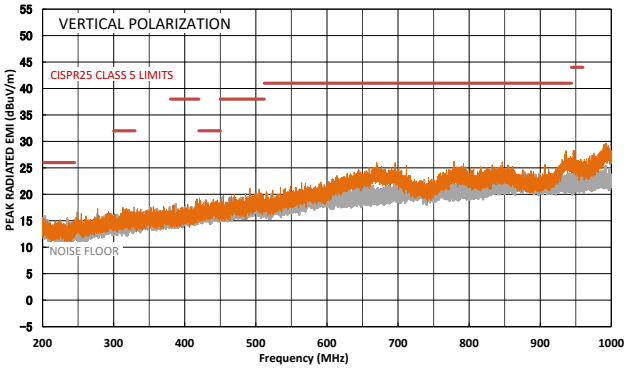
CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



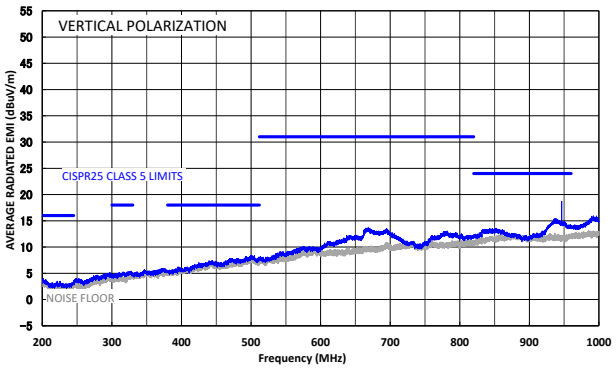
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



Note:

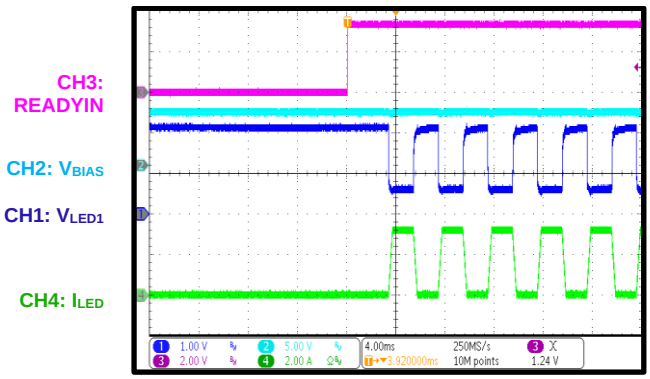
9) The EMC test results are based on Figure 15 on page 34. f_{PWM} = 250Hz, PWM duty = 50%, phase shift = 1µs, slew rate = 5µs.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

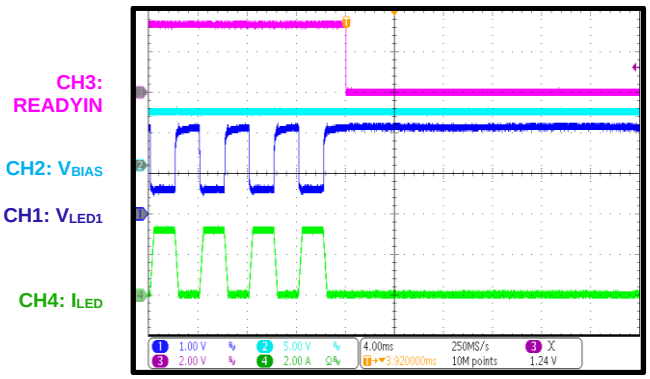
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

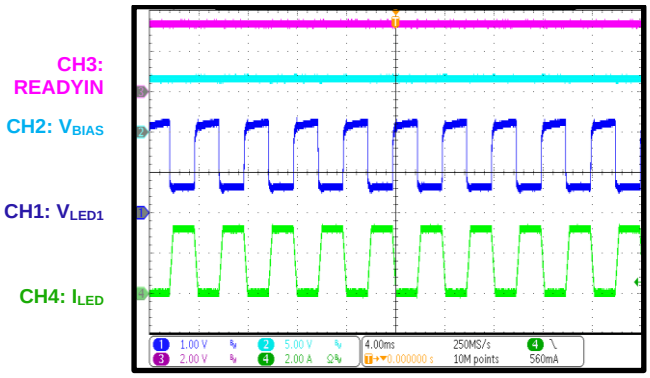
Immediate Animation
READYIN is on



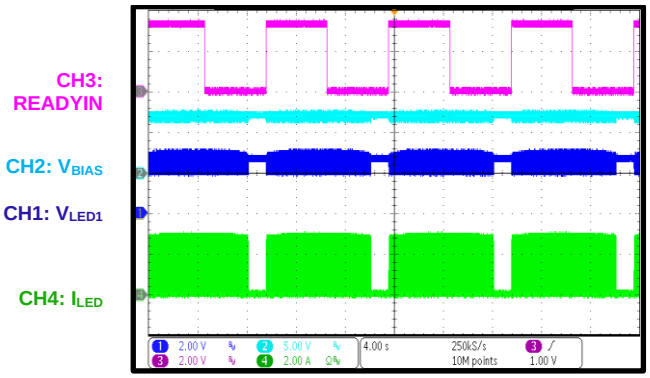
Immediate Animation
READYIN is off



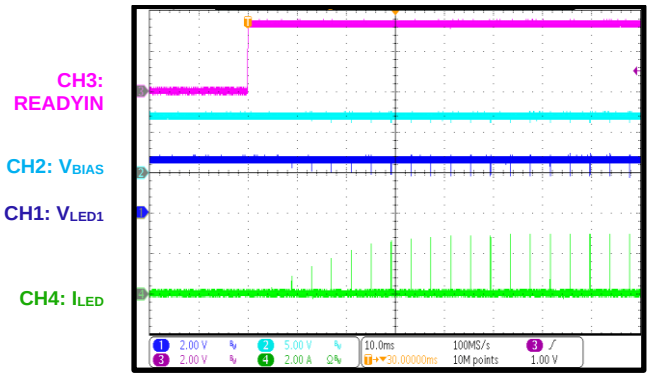
Immediate Animation
Steady state



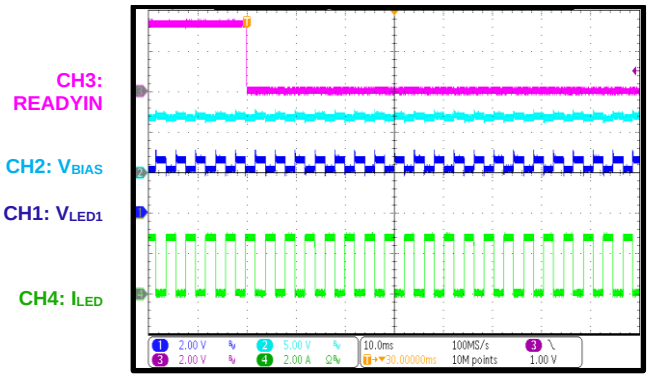
Breathing Animation



Breathing Animation
READYIN is on



Breathing Animation
READYIN is off

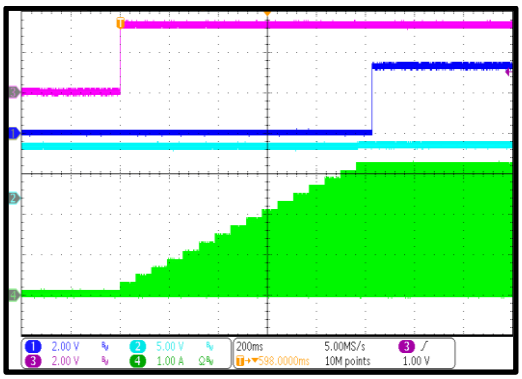


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

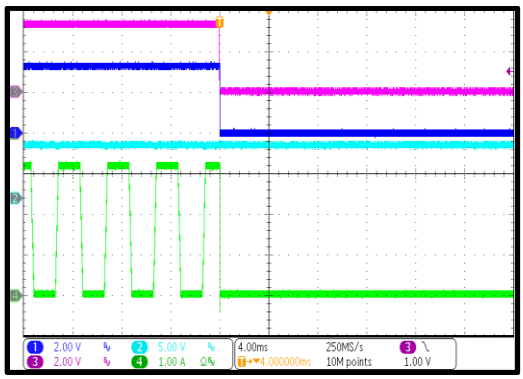
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

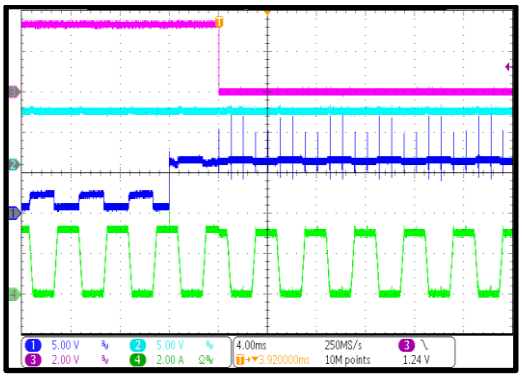
Sequential Animation
READYIN is on



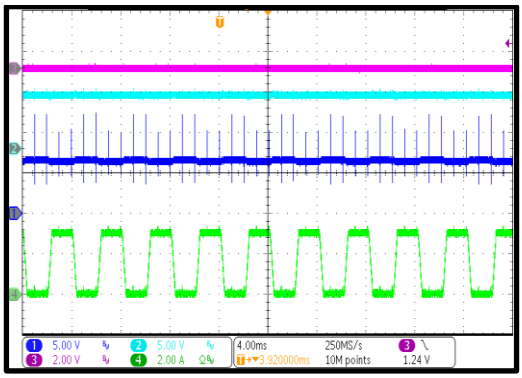
Sequential Animation
READYIN is off



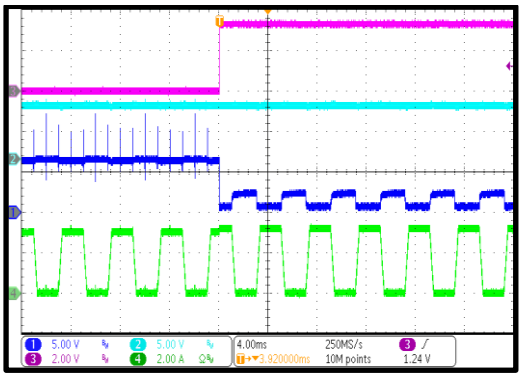
VBIAS Short to LED1 Entry



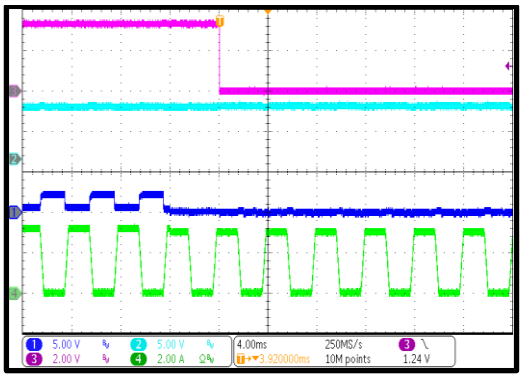
VBIAS Short to LED1 Steady State



VBIAS Short to LED1 Recovery



LED Open Entry

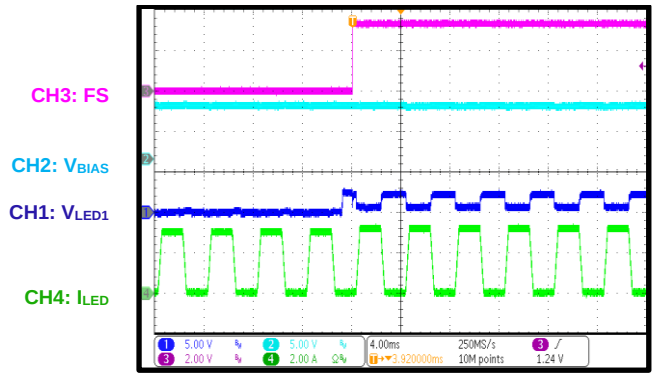


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

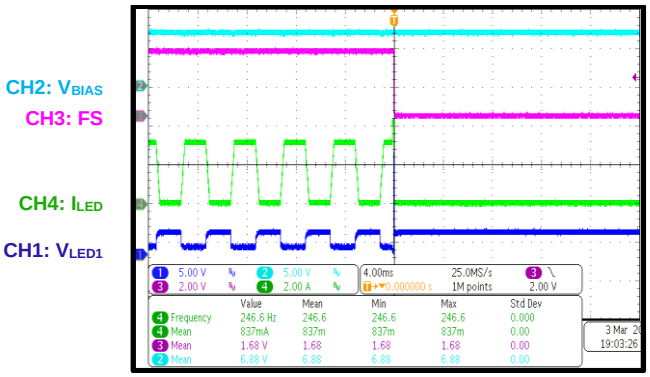
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

2 LEDs in series (V_{LED} = 6V), I_{LED}/channel = 200mA, T_A = 25°C, unless otherwise noted.

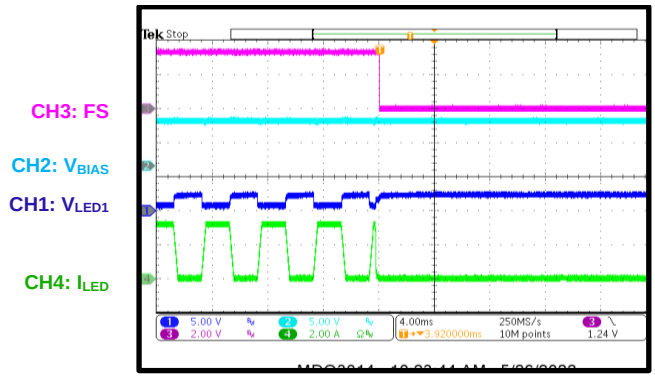
LED Open Recovery



ISET Pin Short

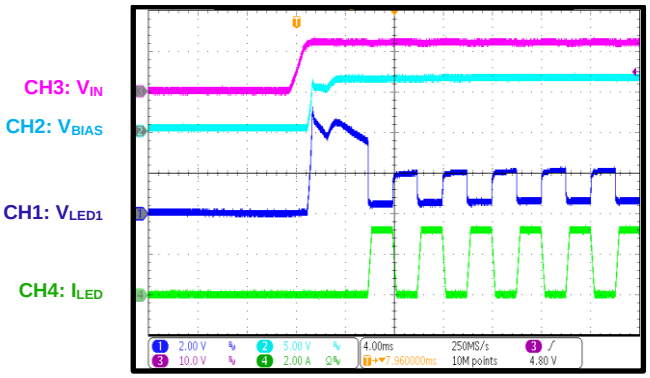


ISET Pin Open



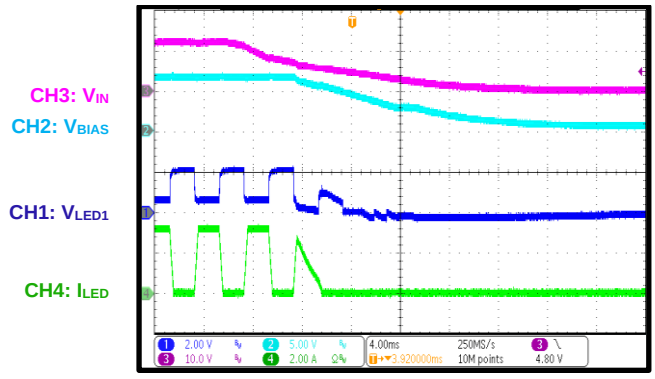
Start-Up

READYIN is connected to VBIAS



Shutdown

READYIN is connected to VBIAS



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

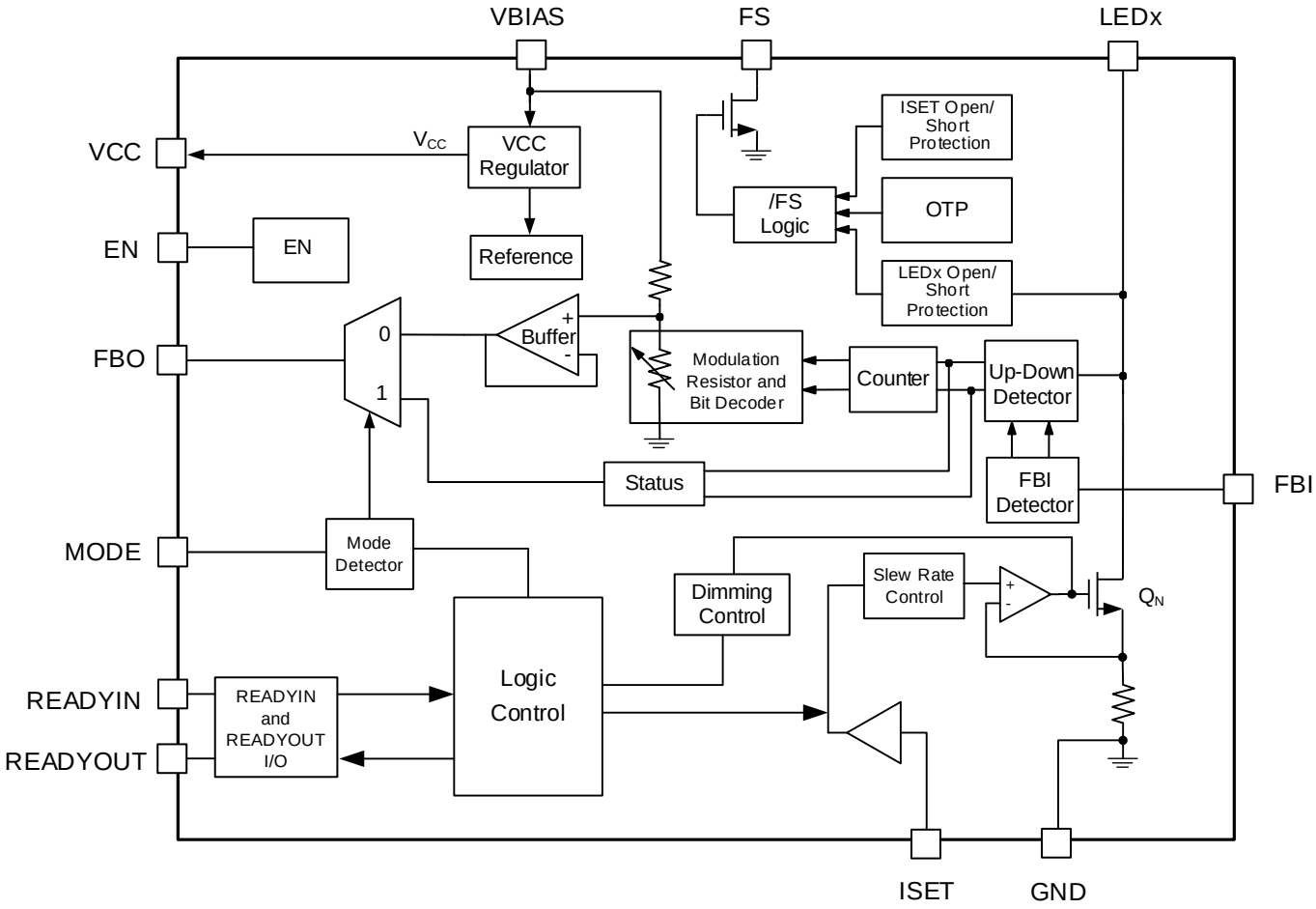


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

OPERATION

LED Current Sinks

The current sink regulators (16 channels) embedded in the MPQ7224 can be individually configured to provide up to 200mA of maximum current for each channel. These 16 specialized current sinks are accurate to within ±5% for currents at 200mA across the full temperature range, with a string-to-string difference of ±5%.

Pre-Regulator Adaptive Feedback Control (AFC)

The MPQ7224 features adaptive feedback control (AFC) for the external pre-regulator. The output voltage (V_{BIAS}) of the pre-regulator (e.g. the buck) is always self-adjusted based on the LED string with the lowest headroom voltage. This minimizes the LEDx pin voltage (V_{LEDx}) and maintains the target LED current (I_{LED}) for the 16 channels. Overall efficiency is maximized when the MPQ7224's current sinks operate with the minimum headroom voltage.

The number of LED outputs used is detected automatically, and only the active LED outputs are monitored for AFC. If any LED strings are not used, they can be disabled via the one-time programmable (OTP) memory using CHx_EN (0x03).

V_{LEDx} is periodically monitored by the control loop. If any of the LED outputs fall below the low-band threshold (0.45V), the external pre-regulator's output voltage increases. If all LED outputs exceed the high-band threshold (0.55V), the external pre-regulator's output decreases.

V_{LEDx} should remain between the low band and high band. The band can be configured via register 0x27 based on I_{LED}. The high-band voltage can be set between 0.25V and 0.6V, while the low-band voltage can be set between 0.2V and 0.55V. If 150mA < I_{LED} ≤ 200mA, it is recommended to set the overall band between 0.45V and 0.55V. If I_{LED} ≤150mA, it is recommended to set the overall band between 0.3V and 0.4V to improve efficiency.

The initial VBIAS voltage (V_{BIAS}) can also be configured via the OTP. The internal resistor divider (R1 and R2) defines both the minimum and maximum adaptive V_{BIAS} levels (see Figure 2 on page 21).

Choose the maximum V_{BIAS} based on the maximum (V_{BIAS} - V_{LEDx}) specification. Before the LED drivers are active, the initial V_{BIAS} exceeds the maximum LED string voltage by about 0.3V.

One of the MPQ7224's key benefits is that its dropout information can be transferred to the DC/DC converter's feedback pin via the FBO pin to optimize system efficiency in real time. This information sharing is also available between multiple MPQ7224 devices via the FBI and FBO pins. The channel with the lowest V_{LEDx} uses its V_{LEDx} to determine the DC/DC converter's power supply output. AFC also works if multiple MPQ7224 devices are connected in parallel.

If AFC is not used, float the MPQ7224's FBO pin, and connect the FBI and MODE pins to GND.

Multiple Devices

The MPQ7224 can also support several devices in parallel by setting the part to master mode or slave mode via the MODE pin. If the MODE pin is connected to GND, the part is configured as the master. The slave device's FBO pin should be connected to the master's FBI pin. If the MODE pin is connected to VCC, the part is configured as a slave. The FBO pin of the master is connected to the pre-regulator's FB resistor divider (see Figure 2 on page 21). Only the master device can directly adjust V_{BIAS}; the slave device can only deliver the VBIAS information to master device via the FBI pin.

For the master device, the FBI pin voltage (V_{FBI}) and V_{LEDx} determine how to adjust V_{BIAS}. If the high band is set to 0.55V, the low band is set to 0.45V, and V_{FBI} is between 0.75V and 1.2V (or any of the master devices' V_{LEDx} is below 0.45V), the device decreases R2. This decreases the FBO voltage (V_{FBO}), which regulates V_{BIAS} to high by the pre-regulator. If V_{FBI} is below 0.3V and all of the masters' V_{LEDx} exceeds 0.55V, the device increases R2. This increases V_{FBO}, which regulates V_{BIAS} to low by the pre-regulator. For other conditions, V_{BIAS} is maintained as normal.

See the FBI detector in Figure 2 on page 21. When V_{FBI} is between 0.75V and 1.2V, UP_S = 1 and DOWN_S = 0. This means that V_{BIAS} is not sufficient for the slave device, so V_{BIAS} must be

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

increased. When V_{FBI} is below 0.3V, slave device, so V_{BIAS} must be increased. When V_{FBI} is below 0.3V, DOWN_S = 1 and UP_S = 0. This means that V_{BIAS} is too high for the slave device, so V_{BIAS} must be decreased. When V_{FBI} is between 0.3V and 0.75V, UP_S = 0 and DOWN_S = 0. This means that V_{BIAS} must stay the same for the slave device.

For any slave device, if V_{LEDx} is below 0.45V, or V_{FBI} is between 0.75 and 1.2V, then V_{FBO} is 1V (V_{BIAS} is not sufficient, and should be increased for the slave device). If all V_{LEDx} exceed 0.55V and V_{FBI} is below 0.3V, then V_{FBO} is 0V (V_{BIAS} is too high, and should be decreased for the slave device). For other conditions, V_{FBO} is 0.5V (maintain V_{BIAS} for the slave device).

In summary, if V_{LEDx} is below 0.45V, then V_{BIAS} increases. V_{BIAS} only decreases when each V_{LEDx} exceeds 0.55V. For other conditions, V_{BIAS} stays the same. Table 1 summarizes these relationships.

Table 1: Relationship between FBI, FBO, V_{BIAS}, and V_{LEDx}

Slave Device			
Condition	Any V_{LEDx} < 0.45 or 0.75 < V_{FBI} < 1.2V	All V_{LEDx} > 0.55V and V_{FBI} < 0.3V	Other condition
V_{FBO}	1V	0V	0.5V
Master Device			
Condition	Any V_{LEDx} < 0.45 or 0.75 < V_{FBI} < 1.2V	All V_{LEDx} > 0.55V and V_{FBI} < 0.3V	Other condition
V_{FBO}	Decreases	Increases	Stays the same
V_{BIAS}	Increases	Decreases	Stays the same

Figure 2 shows how to set up the master and slave modes.

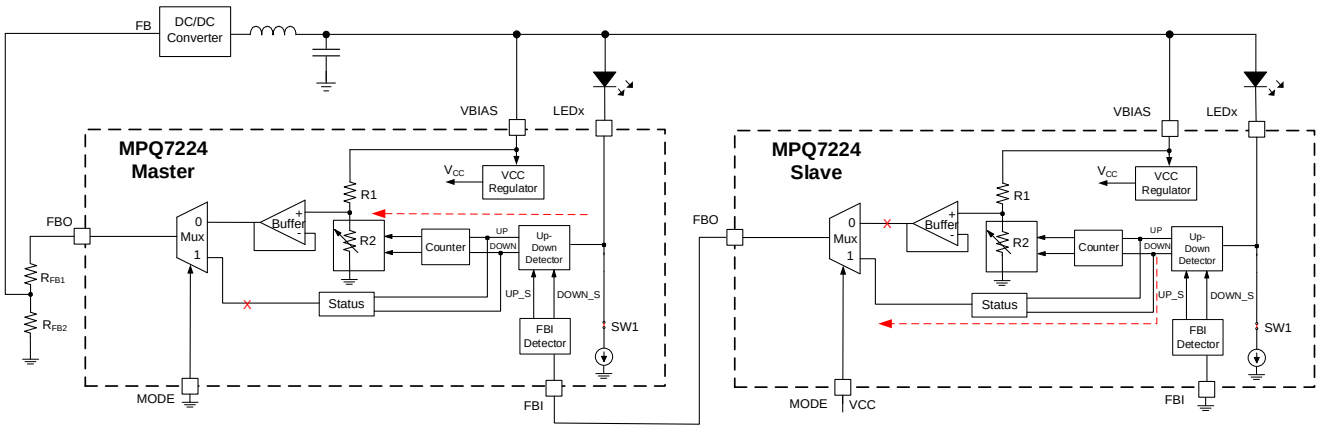


Figure 2: Master and Slave Mode Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Enable and Start-Up

The EN pin can be connected to VBIAS through a resistor divider, or it can be supplied externally.

VCC is powered by the VBIAS pin or an external DC source (if V_{BIAS} is not high enough to support VCC). When both EN and VBIAS are high, V_{CC} ramps up, and the internal logic circuitry (including the differential interface) is active. The start-up sequence is as follows:

- V_{BIAS} and EN pull high.
- V_{CC} exceeds its under-voltage lockout (UVLO) threshold.
- The internal logic circuitry is active.
- READIN pulls high.
- I_{LED} ramps up.

Each channel can be enabled or disabled individually by setting the corresponding bit ChxEN (where x = 1, 2...16) (register address: 0x03) to “disabled.”

Figure 3 shows the start-up sequence. This sequence is described in greater detail below.

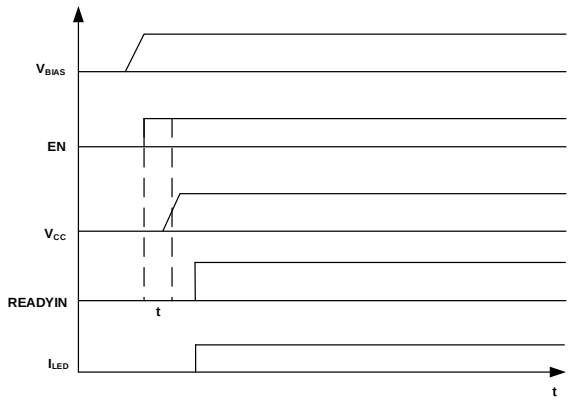


Figure 3: Start-Up Sequence

The delay time from EN going high to V_{CC} > V_{CC_UVLO} is about 200µs, which is based on the 10µF VCC capacitor.

If V_{BIAS} is below 3.5V, another external LDO is required to power VCC. Set the external LDO voltage to 3.3V and with a current capability greater than (n20mA + 50mA), where n is the number of MPQ7224 devices in the system. VCC should be on before VBIAS and EN turn on.

If VBIAS is disconnected from the pre-regulator, or the FBO pin is disconnected from the FB divider, then the pre-regulator works at a maximum duty cycle, and V_{BIAS} is regulated to the input voltage (V_{IN}). Then all the LEDx pins detect an LED short after 4ms, and all the LEDx pins turn off.

LED Current Setting

The LED currents of all channels are set by an external ISET resistor (R_{ISET}). I_{LED} can be calculated with Equation (1):

$$I_{LED}(mA) = \frac{600}{R_{ISET}(k\Omega)} \quad (1)$$

The nominal ISET voltage (V_{ISET}) is 0.6V. When the ISET current (I_{ISET}) exceeds a specific value, it is be detected as an ISET pin short to ground. The ISET short detection threshold is 1mA (corresponding to a 0.6kΩ R_{ISET}, or 1000mA I_{LED}). When I_{ISET} is below 5µA (corresponding to a 120kΩ R_{ISET}, or 5mA I_{LED}), an ISET pin open is detected.

If an open or short condition is detected, the device latches off and asserts the FS pin.

EMI Reduction

The MPQ7224 features three EMI reduction methods. The first method requires configuring the I_{LED} rising/falling slew rates during pulse-width modulation (PWM) dimming, as this can sufficiently optimize EMI performance. The I_{LED} rising/falling slew rates are controlled via register 0x01, bits[13:12]. The slew rates can be set to no slew rate, 5µs, 10µs, and 20µs. The default value is 5µs.

The second method requires configuring the I_{LED} phase-shift function. This function is controlled via register 0x01, bits[11:10]. When the phase-shift function is enabled, the channel x + 1 (where x = 1, 2...13) LED current phase shift is 1µs, 5µs, or 20µs after channel x’s LED current rising edge.

The third EMI reduction method is frequency spread spectrum (FSS). The FSS function reduces EMI noise around the internal clock frequency and its harmonic frequencies. This method deliberately spreads the frequency of the clock waveform and widens the bandwidth of the switching waveform, which ultimately reduces its EMI spectral density. The spread spectrum

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

function modulates the internal clock frequency within ±10% from the central frequency, with a 15.6 kHz modulation frequency (f_M) (see Figure 4). The FSS function can disabled via register 0x01, bit[0].

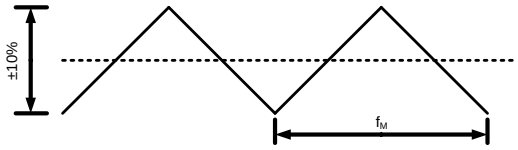


Figure 4: Frequency Spread Spectrum (FSS)

Dimming

Each channel has its own 6-bit analog dimming and 12-bit PWM dimming register, which can independently control the dimming functions for each channel.

Analog Dimming

During analog dimming, the I_{LED} amplitude changes when the analog dimming register changes. Change the value of the analog dimming register for the corresponding channel via 0x17~0x26, bits[5:0]. The initial analog dimming register value is 0x20, though it can be set between 0x00 and 0x3F. When the register increases by 1 bit, the I_{LED} amplitude increases by 0.5%. When the register decreases by 1 bit, the I_{LED} amplitude decreases by 0.5%. I_{LED} can be adjusted between 84% and 115.5% of the normal value. This function can be used in the applications that require different currents for the different channels.

Pulse-Width Modulation (PWM) Dimming

During PWM dimming, I_{LED} is chopped. This means that the I_{LED} amplitude stays the same, and the I_{LED} duty varies with the PWM dimming register.

The PWM dimming duty cycle is set via the PWM dimming registers 0x07~0x26, bits[11:0].

The duty cycle (D) can be estimated with Equation (2):

$$D = \frac{PWMx}{2^{12}-1} = \frac{PWMx}{4095} \quad (2)$$

Where PWMx is the PWM dimming register for channel x (x = 1, 2...16). When PWMx, bits [11:0] = 0x000, the corresponding I_{LED} is 0A.

The PWM dimming frequency can be set to 250Hz, 500Hz, or 1kHz. The PWM dimming duty can be set between 2% to 100%.

The MPQ7224 supports three kinds of built-in dimming patterns. The desired dimming and configuration settings are preconfigured at the factory, and are stored in the OTP (see Table 2). The MPQ7224 can also be configured by the user via the OTP.

Table 2: OTP Memory Default Settings

Effect	Sequential Animation	Breathing Animation	Immediate Animation
Sequential	64ms/ch	N/A	N/A
Breathing	N/A	4s	N/A
PWM dimming duty	100%	100%	100%
Analog dimming	100%	100%	100%
Slew rate	5µs	5µs	5µs
Phase shift	No phase shift	No phase shift	No phase shift
PWM frequency	250Hz	250Hz	250Hz
Fault mode	Hiccup	Hiccup	Hiccup
Channel number	16	16	16
Initial V_{BIAS}	6.6V (for 2 LEDs in series)	6.6V (for 2 LEDs in series)	6.6V (for 2 LEDs in series)

Immediate Animation

During immediate animation, all LEDx channels turn on immediately (according to the preconfigured dimming value) once the READYIN pin is pulled high. The dimming duty can be configured via the OTP memory. When the duty is configured to 100%, the READYIN pin can also act as the PWM dimming input pin. The typical delay time between READYIN high/low and LED on/off is 10/2µs.

Note that READYOUT is always low during immediate animation. If there are multiple devices connected in parallel, connect all of the READYIN pins together, and connect them to the control signal.

Figure 5 on page 24 shows immediate animation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

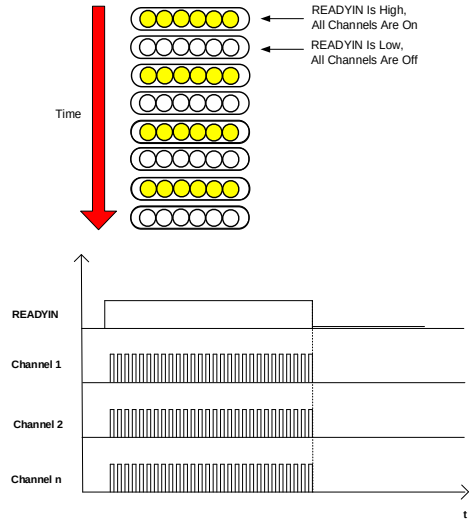


Figure 5: Immediate Animation

Sequential Animation

During sequential animation, the LEDx channels turn on sequentially starting when the master device's READYIN pin is pulled high. When READYIN is high, LED channel 1 turns on after a configured time (typically 64ms) with a configured duty. Then LED channel 2 turns on, followed by LED channels 3 through 16. The delay time between channels can be set to between 1ms and 64ms. Once channel 16 is on for 64ms, the READYOUT pin pulls high to start up the next MPQ7224 device.

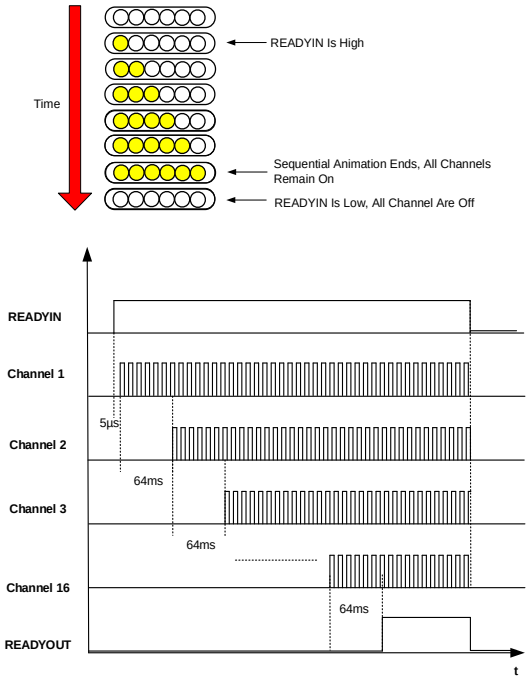


Figure 6: Sequential Animation

Breathing Animation

Breathing animation is on for all channels once READYIN is high. When READYIN is high, the LED PWM dimming duty takes 4s to change from 0% to 100% with a certain logarithmic curve (see Figure 7). Then the PWM dimming duty remains at 100% until READYIN pulls low, and the LED breathing tuns off. If multiple devices are connected in parallel, connect all of the READYIN pins together, and connect them to the control signal.

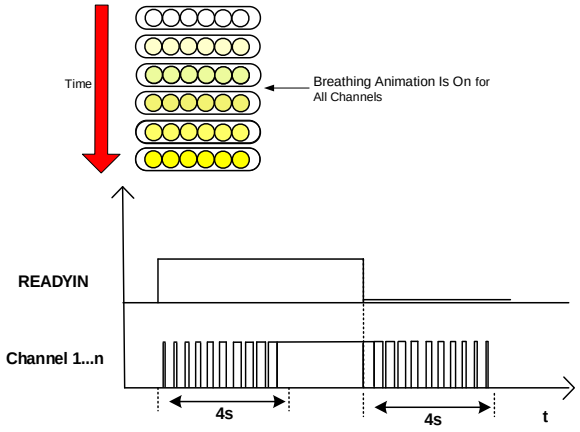


Figure 7: Breathing Animation

Automatic Logarithmic Curve

To reduce the burden on the communication bus during breathing animation, the MPQ7224 provides imbedded, automatic logarithmic dimming based on a fixed 64-point look-up table. Assume there are a total of 4096 steps between when the duty cycle = 0% and duty cycle = 100%. For a fixed constant (*k*), the logarithmic curve can be fixed, so the duty cycle value for the 4096 points can be calculated via software and solidified in a digital circuity.

Figure 8: Logarithmic Dimming Curve

If the configurable duty cycle is not equal to the duty cycle on the curve, one more step is

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

required to change the configured duty cycle. This function is primarily used for breathing animation.

Diagnostic and Fault Indications

The MPQ7224 supports a variety of diagnostic features, including the following:

- VCC UVLO
- LED short protection
- LED open protection
- ISET pin open/short
- Thermal warning and shutdown

The FS pin is an active-low open drain that is pulled high to an external voltage source via a 100kΩ resistor. If a protection is triggered, the FS pin is pulled low.

The LATCH_EN bit determines the channel behavior and pin behavior. Fault channels should latch off or hiccup if LED open or short protection occurs (not including V_{CC} UVLO, ISET pin open/short protection, thermal warning, and thermal shutdown).

If LATCH_EN = 1 (latch-off mode) and the fault is triggered, the fault channel remains off until a power-on reset (POR) or until EN turns off to reset the channel. Meanwhile, the other channels operate normally. The FS pin is pulled low.

If LATCH_EN = 0 (hiccup mode), the fault channel tries to conduct 32μs every 1ms to detect whether the fault is cleared. FS is released once the fault condition is removed.

FS being pulled low can be masked by OTP.

V_{CC} Under-Voltage Lockout (UVLO)

UVLO protects the device from operating at an insufficient supply voltage. V_{CC} UVLO does not trigger the FS pin. If V_{CC} UVLO is triggered, the IC stops working, and all the registers are reset.

LED Open Protection

The MPQ7224 features integrated LED open diagnostics. If V_{LEDx} drops below the LED open protection threshold (V_{LED_O}) (about 100mV) for longer than 4ms, an open load condition is detected. If there is an open load on one of the outputs, the output turns off and FS pulls low.

If LATCH_EN = 1 (latch-off mode), the fault channel stays off until POR or until EN turns off to reset the channel. Meanwhile, the other channels operate normally. FS is released high after the fault bit is read-cleared by the MCU.

If LATCH_EN = 0 (hiccup mode), the LED open is not latched, and the fault channel tries to conduct for 32μs every 1ms to detect whether the fault is cleared. As soon as the open load condition is no longer present, the channel turns on again. FS releases high once the fault condition is removed.

LED Short Protection

During an LED short condition, (V_{BIAS} - V_{LEDx}) drops low. If V_{LEDx} exceeds the LED short protection threshold (V_{LED_S}) for 4ms, LED short protection is triggered. The shorted channel turns off, the corresponding fault bit (CHx_SHORT) is set, and FS pulls low.

If LATCH_EN = 1 (latch-off mode), the fault channel stays off until VCC or EN go low to reset the channel. Meanwhile, the other channels operate normally. FS is released high after the fault bit is read-cleared by the MCU.

If LATCH_EN = 0 (hiccup mode), the LED short is not latched, and the fault channel tries to conduct for 32μs every 1ms to detect whether the fault has cleared. As soon as the short load condition is removed, the channel turns on again. FS releases high once the fault condition is removed.

V_{LED_S} can be configured via LED_SHORT_THR, bits[1:0]. There are four potential thresholds:

- If LED_SHORT_THR = 00, V_{LED_S} is 2V.
- If LED_SHORT_THR = 01, V_{LED_S} is 3V.
- If LED_SHORT_THR = 10, V_{LED_S} is 4V.
- If LED_SHORT_THR = 11, V_{LED_S} is 5V.

ISET Pin Open/Short Protection

The MPQ7224 implements a current monitor for R_{ISET} to provide open and short diagnostics and protection. The device monitors I_{ISET} flowing out of the ISET pin. If I_{ISET} exceeds the ISET pin short current threshold (I_{ISET_STH}) (1mA), a short condition asserts. If I_{ISET} falls below I_{ISET_OTH} (5μA), an ISET pin open condition asserts.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ISET open or short protection is a latch-off protection. If an open or short is detected, the MPQ7224 latches off and asserts FS.

The FS pin does not release high until POR or until EN goes high.

Thermal Warning

If the junction temperature (T_J) exceeds 150°C, the FS pin asserts. The MPQ7224 continues working. FS releases high once the thermal warning condition is removed.

Thermal warning can be individually masked via OT_WARN_MASK to prevent the FS open-drain output from pulling low.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. If T_J exceeds 170°C, all output channels turn off, the OT_STD bit is set, and FS asserts. FS releases high when the MPQ7224 recovers from thermal shutdown.

Thermal shutdown is a non-latch protection. If T_J drops at least 20°C below the thermal shutdown threshold, the MPQ7224 recovers, and the channels turn on using the previous settings without re-initialization.

One-Time Programmable (OTP) Memory

The MPQ7224 provides a one-time programmable (OTP) memory to permanently store the user's desired settings. An OTP cell is used instead of a single-ended cell for long-term reliability, and data is stored on two floating gate avalanche injection metal oxide semiconductors (FAMOS). The MPQ7224 has three type of OTP effects (see Table 1 on page 21). The parameters can be flexibly configured via the OTP memory (see Register Description section on page 27).

Table 3: OTP Memory Overview

Register Name	Address	Default
DEV_CFG_1	0x01	0x1200
DEV_CFG_2	0x02	0x6003
CH_EN	0x03	0xFFFF
PWM dimming duty (Ch1–CH16)	0x07-0x16	0x07FF
PRE-VBIAS	0x27	0x6464
DROP_ BAND	0x28	0x21B9

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER DESCRIPTION

DEV_CFG_1 (0x01)

POR: Load from the OTP.

The DEV_CFG_1 command configures the LED short protection threshold, PWM dimming frequency, I_{LED} slew rate, and phase shift during PWM dimming. It also enables FSS control.

Bits	Bit Name	Description
D[15:14]	LED_SHORT_TH	Sets the LED short threshold. 00: 2V 01: 3V 10: 4V 11: 5V
D[13:12]	SLEW_RATE	Controls the dimming slew rate. 00: No slew rate 01: 5μs 10: 10μs 11: 20μs
D[11:10]	PHASE_SHIFT	Sets the LED short threshold. 00: 2V 01: 3V 10: 4V 11: 5V
D[9:8]	PWM_FREQ	Controls the dimming slew rate. 00: No slew rate 01: 5μs 10: 10μs 11: 20μs
D[7:2]	RESERVED	Reserved.
D1	RESERVED	Reserved.
D0	FSS_EN	Enables frequency spread spectrum (FSS). 0: Disabled 1: Enabled

DEV_CFG_2 (0x02)

POR: Load from the OTP.

The DEV_CFG_2 command configures the LED open/short fault mask and protection behavior, the thermal warning fault mask automatic dimming parameters, logarithmic automatic dimming, AFC, and the analog dimming circuit.

Bits	Bit Name	Description
D15	CH_FS_MASK	Enables the FS mask for LED channel diagnostics. 0: Disabled. FS is pulled down if there is a fault error flag or any channel experiences a short/open fault 1: Enabled. FS is not pulled down if there is a fault error flag or any channel experiences a short/open fault
D14	LATCH_EN	Sets the fault protection mode. 0: Hiccup mode 1: Latch-off mode
D13	CRC_EN	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D12	AUTO_DIM_MODE	Sets the logarithmic automatic dimming mode. 0: Manual mode. The PWM dimming duty cycle changes for the next PWM dimming cycle 1: Automatic diming mode (logarithmic dimming). The duty cycle changes according to the fixed exponential curve with a certain speed setting
D11	AUTO_DIM_HOLD	Holds the current brightness. 0: Normal operation. The dimming duty cycles changes to the setting value 1: Stops all the ongoing automatic dimming ramping, and remains at the current dimming value on the curve regardless of whether the final duty has been reached
D[10:8]	AUTO_DIM_SPEED	Sets the automatic dimming speed for the 64-point logarithmic curve. 000: Normal speed. Jumps 4 points per PWM cycle (0% to 100% in 16 PWM cycles) 001: 2x speed. Jumps 8 points per PWM cycle (0% to 100% in 8 PWM cycles) 010:4x speed. Jumps 16 points per PWM cycle (0% to 100% in 4 PWM cycles) 011: 1/2x speed. Jumps 2 points per PWM cycle (0% to 100% in 32 PWM cycles) 100: 1/4x speed. Jumps 1 point per PWM cycle (0% to 100% in 64 PWM cycles) Others: Reserved, or similar to selecting 000
D7	OT_WARN_FS_MASK	Sets the over-temperature (OT) warning diagnostic mask control. 0: An OT warning signal pulls down the FS pin 1: An OT warning signal does not pull down the FS pin
D[6:2]	RESERVED	Reserved.
D1	MOD_EN	Enables AFC. 0: AFC is disabled. Disables up-down counter and maintains the current modulation bit 1: AFC is enabled. Enables the up-down counter
D0	EN_ANA	Enables the analog circuit. 0: The analog circuit is disabled. When disabled, the device shuts down 1: The analog circuit is enabled. When enabled, the device turns on

CHx_EN (0x03)

POR: Load from the OTP.

The CH_EN command enables channels 1–16.

Bits	Bit Name	Description
D[15:0]	CH_EN	Channel enable bit. Bits[15:0] control channel 16 to channel 1, respectively. If any channel is not used, set the related bit to 0. 0: Disabled 1: Enabled

PWM_DIM (0x07~0x16)

POR: Load from the OTP.

The PWM_DIM command controls the PWM dimming duty for all channels (channels 1–16). Register 0x07 corresponds to channel 1, while register 0x16 corresponds to channel 16.

Bits	Bit Name	Description
D[15:12]	RESERVED	Reserved.
D[11:0]	PWM_DIM	Sets PWM dimming for the corresponding channel.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

VBIAS_VOLT (0x27)

POR: Load from the OTP.

The VBIAS_VOLT command sets the pre-V_{BIAS} voltage. It can only be changed via the OTP.

<table>
<tr><th>Bits</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>D[15:8]</td><td>PRE-VBIAS</td><td>Sets the pre-V_{BIAS} voltage. When the register value increases by 1, V_{BIAS} increases by 0.05V, and V_{FBO} = 1.2V.
<table>
<tr><th>V_{BIAS} (V)</th><th>Bits[15:8] (Dec)</th><th>Bits[15:8] (Hex)</th></tr>
<tr><td>2.5</td><td>14</td><td>0E</td></tr>
<tr><td>2.55</td><td>15</td><td>0F</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>13.95</td><td>243</td><td>F3</td></tr>
<tr><td>14</td><td>244</td><td>F4</td></tr>
</table></td></tr>
<tr><td>D[7:0]</td><td>RRAL-VBIAS</td><td>The real value of the up-down counter.</td></tr>
</table>

DROP_ BAND (0x28)

POR: Load from the OTP.

The DROP_ BAND command controls V_{LEDx} for the AFC band, including the low band and the high band. It can only be changed via the OTP.

<table>
<tr><th>Bits</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[15:8]</td><td>RESERVED</td><td>0x21</td><td>Reserved.</td></tr>
<tr><td>D[7:5]</td><td>LOW_BAND</td><td>0b101</td><td>Sets the low-band value for AFC.
<table>
<tr><th>Bits[7:5]</th><th>Low-Band Value</th><th>Bits[7:5]</th><th>Low-Band Value</th></tr>
<tr><td>000</td><td>0.2V</td><td>100</td><td>0.4</td></tr>
<tr><td>001</td><td>0.25V</td><td>101</td><td>0.45</td></tr>
<tr><td>010</td><td>0.3V</td><td>110</td><td>0.5</td></tr>
<tr><td>011</td><td>0.35V</td><td>111</td><td>0.55</td></tr>
</table></td></tr>
<tr><td>D[4:2]</td><td>HIGH_BAND</td><td>0b110</td><td>Sets the high-band value for AFC.
<table>
<tr><th>Bits[4:2]</th><th>High-Band Value</th><th>Bits[4:2]</th><th>High-Band Value</th></tr>
<tr><td>000</td><td>0.25V</td><td>100</td><td>0.45</td></tr>
<tr><td>001</td><td>0.3V</td><td>101</td><td>0.5</td></tr>
<tr><td>010</td><td>0.35V</td><td>110</td><td>0.55</td></tr>
<tr><td>011</td><td>0.4</td><td>111</td><td>0.6</td></tr>
</table></td></tr>
<tr><td>D[1:0]</td><td>RESERVED</td><td>0b01</td><td>Reserved.</td></tr>
</table>

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

APPLICATION INFORMATION

Build-In Animation Selection

The MPQ7224 supports three kinds of built-in dimming patterns. The desired dimming and configuration settings are preconfigured by the factory and are stored in the OTP (see Table 2 on page 23). There is no synchronous delay between READYIN and READYOUT during immediate and breathing animation. READYOUT can be left floating, and READYIN can use the MCU to control the on sequence. Figure 9 shows the connections for sequential animation.

Adaptive Feedback Control (AFC) Network Connection

The FBI, FBO, and MODE pins are related to AFC. If AFC is not used, float the FBO pin, then connect FBI and MODE to GND (see Figure 9).

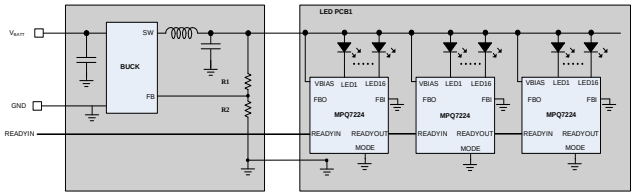


Figure 9: Application Circuit without AFC

V_{BIAS} can be set by the DC/DC converter's feedback voltage (V_{FB}). V_{BIAS} can be calculated with Equation (3):

$$V_{BIAS} = V_{FB}(1+\frac{R_1}{R_2}) \quad (3)$$

Consider the maximum V_{LEDx} and ensure that (V_{BIAS} - V_{LEDx}) exceeds the headroom of each V_{LEDx}.

When using AFC, connect the FBI pin of the last slave device or single chip to GND; otherwise, connect FBI to the FBO pin of the next MPQ7224 for the current sink headroom information (see Figure 10).

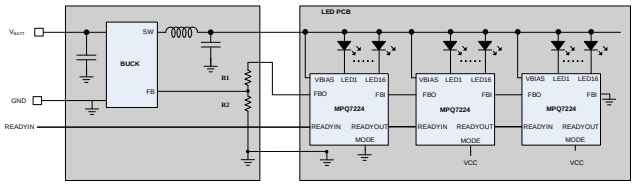


Figure 10: Application Circuit with AFC and Connected FBO

For example, slave 2's FBI pin should be connected to slave 3's FBO pin. For the master device, the FBO pin is the feedback output, and it should be connected to the DC/DC converter's feedback pin through a resistor divider network.

If the MPQ7224 and DC/DC converter are on the same board, or there is a connected FBO wire condition, the resistor network can be connected following Figure 11. Then the feedback resistors can be estimated with Equation (4):

$$V_{FBO} = V_{FB}(1+\frac{R_1}{R_2}) \quad (4)$$

Where V_{FB} is the DC/DC converter's reference voltage (e.g. for the MPQ4323C, it is 0.8V), and FBO is between 0.6V and 2.2V. If V_{FBO} = 1.2V and R2 = 80.6kΩ, then R1 is 40.2kΩ.

The pre-V_{BIAS} voltage is set via the OTP, internal modulator, and resistors R1 and R2 (see Figure 11).

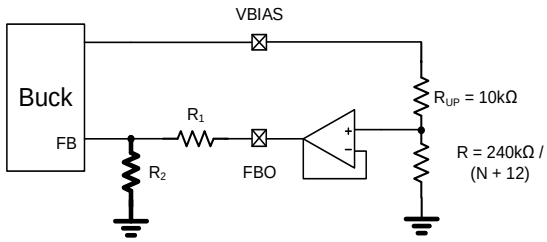


Figure 11: AFC Modulator Network

In Figure 11, N can be adjusted from 14 to 244 via OTP register 0x27. Note that the pre-V_{BIAS} voltage should match V_{LED}, or the device detects an LED open or short when the LED is on. So if V_{FBO} = 1.2V and N = 100 (0x6464), then the pre-V_{BIAS} voltage should be set to 6.8V.

N automatically adjusts when V_{LED} changes after the device starts operating. If V_{FB} = 0.8V, R2 = 80.6kΩ, and R1 = 40.2kΩ, V_{FBO} is about 1.2V, and V_{BIAS} can be set between 2.5V and 14V with an N change between 14 and 244. See the VBIAS_VOLT (0x27) section on page 29 for more details.

If the MPQ7224 and DC/DC converter are not on the same PCB, there must be an FBO line between the converter and the MPQ7224. If the FBO line is open, V_{BIAS} is regulated to the battery voltage (V_{BATT}), and an LED short is triggered.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

A resistor network can be used to prevent V_{BIAS} from regulating to V_{BATT} when the FBO line is open.

Figure 12 shows the AFC modulator network.

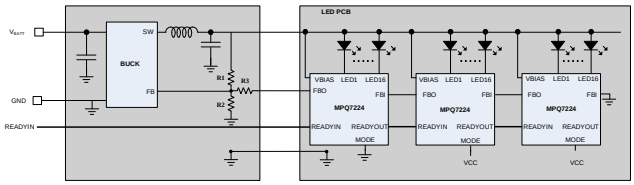


Figure 12: AFC Modulator Network

V_{BIAS} can be calculated with Equation (5):

$$VBIAS=\frac{V_{FB}\times(R1+R3)+\frac{V_{FB}}{R2}\times R1\times R3}{R_1\times\frac{\frac{240}{N+12}}{10+\frac{240}{N+12}}+R3} \quad (5)$$

When R3 is disconnected, V_{BIAS} while FBO line is open (V_{BIAS_O}) can be estimated with Equation (6):

$$V_{BIAS_O}=V_{FB}\times(1+\frac{R_1}{R_2}) \quad (6)$$

Figure 13 shows the AFC network with FBO open protection.

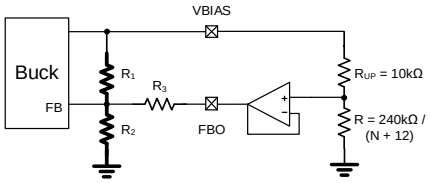


Figure 13: AFC Modulator Network with FBO Open Protection

For example, when the MPQ7224 has two LEDs in series (V_{LED} = 6.3V), set V_{BIAS_O} at 7.1V when FBO is open. If the DC/DC converter's V_{FB} is 0.8V (based on Equation (5)), choose R1 to be 100kΩ, so that R2 is 12.7kΩ. If N is set to 100 via the OTP, choose R3 to be 100kΩ. Then the pre-V_{BIAS} voltage is 6.71V based on Equation (4). When N changes from 14 to 244, V_{BIAS} changes from 5.9V to 7.6V, so consider the pre-V_{BIAS} value set via the OTP, as well as resistor selection when making this connection. The connection in Figure 13 minimizes the V_{BIAS} range.

Selecting the VBIAS Capacitor

The VBIAS pin is the bias supply. The MPQ7224 operates from an input voltage (V_{IN}) between 2.5V and 18V. A capacitor (C_{IN}) is required to decouple the VBIAS line's voltage noise. If using the MPQ4323 output as the V_{BIAS} for the MPQ7224, a decoupling capacitance is required for the MPQ7224's VBIAS: 2 x 22µF, 2 x 10µF, and 0.1µF. Place the 22µF capacitors close to the MPQ4323. Place the 10µF capacitors close the LEDs, and place the 0.1µF capacitor close to the MPQ7224's VBIAS pin.

Selecting the VCC Capacitor and Current Capability

The VCC is pin is the internal bias power supply. An internal LDO from VBIAS generates the 3.3V VCC. VCC supplies power to the internal control circuit and gate drivers. A ≥10µF capacitor and 1kΩ to 10kΩ resistor should be placed in parallel from VCC to ground. This resistor ensures that V_{CC} discharges to about 0V during the start-up cycle. VCC requires power from the external LDO if V_{BIAS} cannot sufficiently power VCC. The external LDO should be between 3.1V and 3.5V and with a 20mA current ability. When there are multiple devices in parallel, the external DC source current ability should be (n x 20mA), where *n* is the number of devices.

LED Current Setting

Set the LED currents of all channels with an external resistor at ISET pin (R_{ISET}), calculated with Equation (7):

$$I_{SET}(mA)=\frac{600}{R_{ISET}(k\Omega)} \quad (7)$$

If I_{LED} is below 200mA, certain ISET resistors are recommended (see Table 4).

Table 4: Resistor Selection when I_{LED} ≤ 200mA.

I_{LED} (mA)	R_{ISET} (kΩ)
200	3.01
100	6.04
50	12.1
25	24.3

MODE Pin Configuration

If AFC is disabled, connect the MODE pin to GND. If AFC is enabled and the part is the

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

master, connect MODE to GND; if it is a slave device, connect MODE to VCC.

ESD Protection Design

Electrostatic discharge (ESD) is the release of static electricity when two objects come into contact. If any pin of the MPQ7224 need connect to other board through connector with line, it may suffer the ESD problem; generally, the LEDx pin, READYIN, READYOUT and FBO pin has chance to connect with other board through line. For LEDx pins, it is recommended to place a ≤100nF in parallel with them to protect the ESD issue if the LED load and MPQ7224 is not on the same board. For the other pin, it recommended to place an ESD diode in parallel with a <10nF capacitor to protect those pin.

PCB Layout Guidelines for BCI/EMC

Consider the bulk current injection (BCI), as FBO has a maximum current capability of 5mA for anti-interference. To improve BCI and EMC results, refer to Figure 14 on page 33 and follow the guidelines below:

1. For the MPQ4323C, place the symmetric input capacitors as close to VIN and GND as possible.
2. For the MPQ4323C, ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
3. For the MPQ4323C, place the VCC capacitor as close to VCC and GND as possible.
4. For the MPQ4323C, route SW and BST away from sensitive analog areas, such as FB.
5. For the MPQ7224, place the feedback resistors close to the chip to ensure that the trace connected to FB is as short as possible.
6. For the MPQ7224, place the capacitors as close to the input as possible.
7. For the MPQ7224, add a small capacitor as close to the IC pins as possible to improve anti-interference abilities.
8. For the MPQ7224, a GND polygon is required to improve anti-interference abilities and heat dissipation.
9. For the MPQ7224, make the GND polygon large.

2-Layer Layout Guidelines

For a 2-layer PCB layout, follow the steps below:

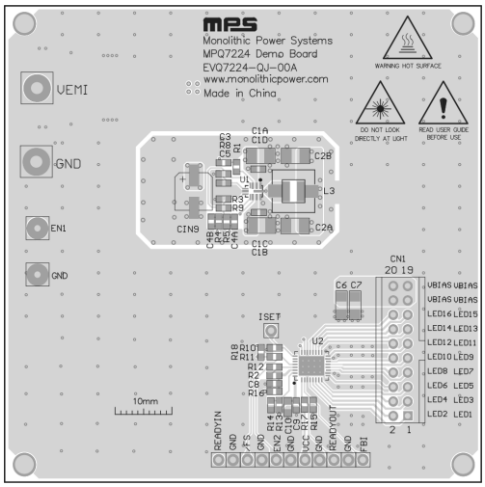
1. The top layer should include the power, signal, and GND.
2. Cover GND in all areas except for the signal and power path.
3. The bottom layer should only include the GND polygon to shield noise interference, unless there is not enough PCB space.

4-Layer Layout Guidelines

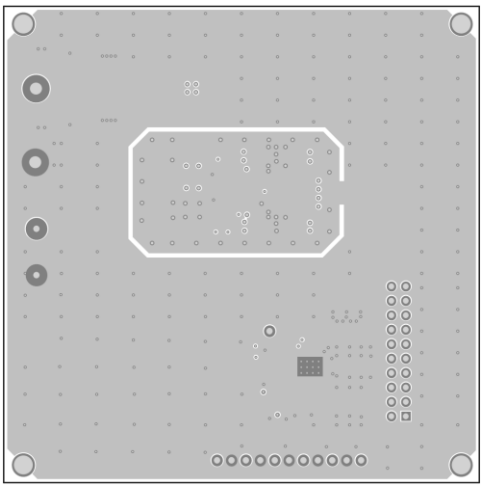
For a 4-layer PCB layout, follow the steps below:

1. The top layer should include the power, signal, and GND.
2. Cover GND in all areas on the top layer except for the signal and power path.
3. The second layer should only include GND to shield noise interference on the top layer.
4. The third layer should include the power, signal, and GND.
5. Cover GND in all areas on the third layer except for the signal path.
6. Cover GND in all areas on the bottom layer except for the signal and power path.

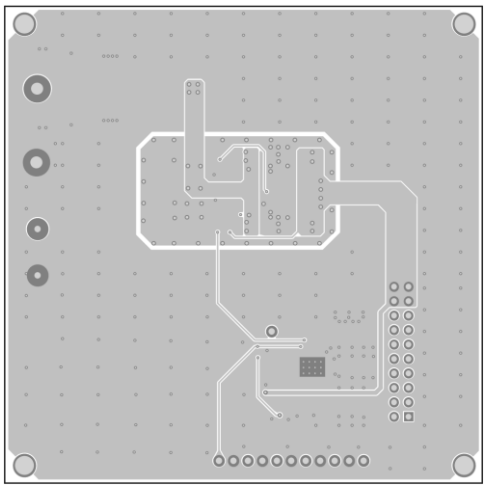
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.



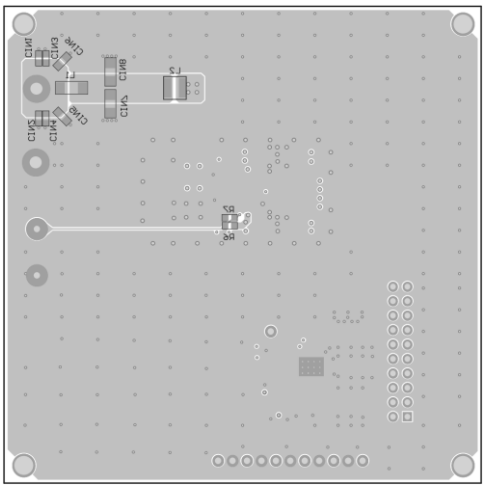
Top Layer



Mid-Layer 2



Mid-Layer 1



Bottom Layer

Figure 14: Recommended PCB Layout

Note:

10) The recommended PCB layout is based on the Figure 15 on page 34.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

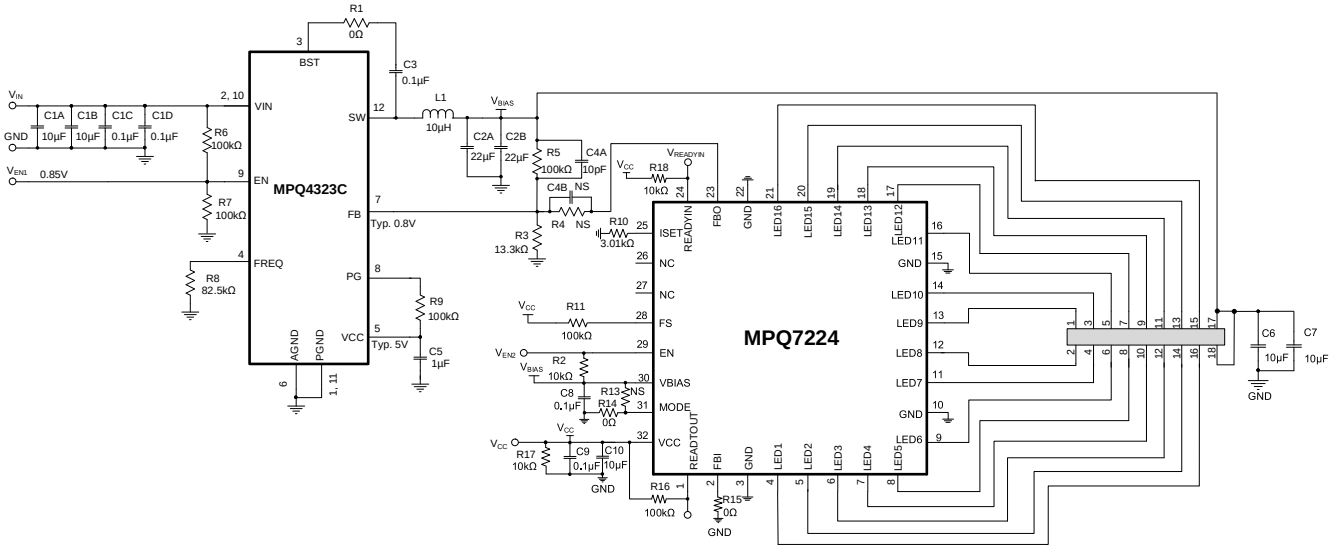


Figure 15: Typical Application Circuit without AFC (I_{LED} = 200mA/Channel, V_{LED} = 6.3V)

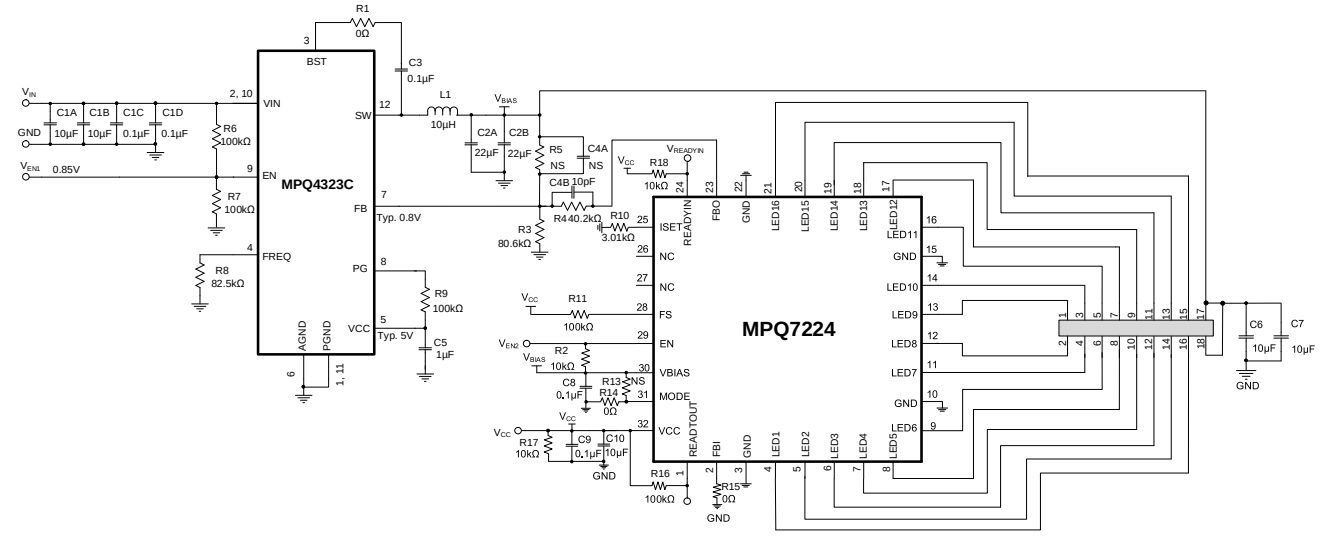


Figure 16: Typical Application Circuit with AFC (I_{LED} = 200mA/Channel, V_{LED} = 6.3V)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

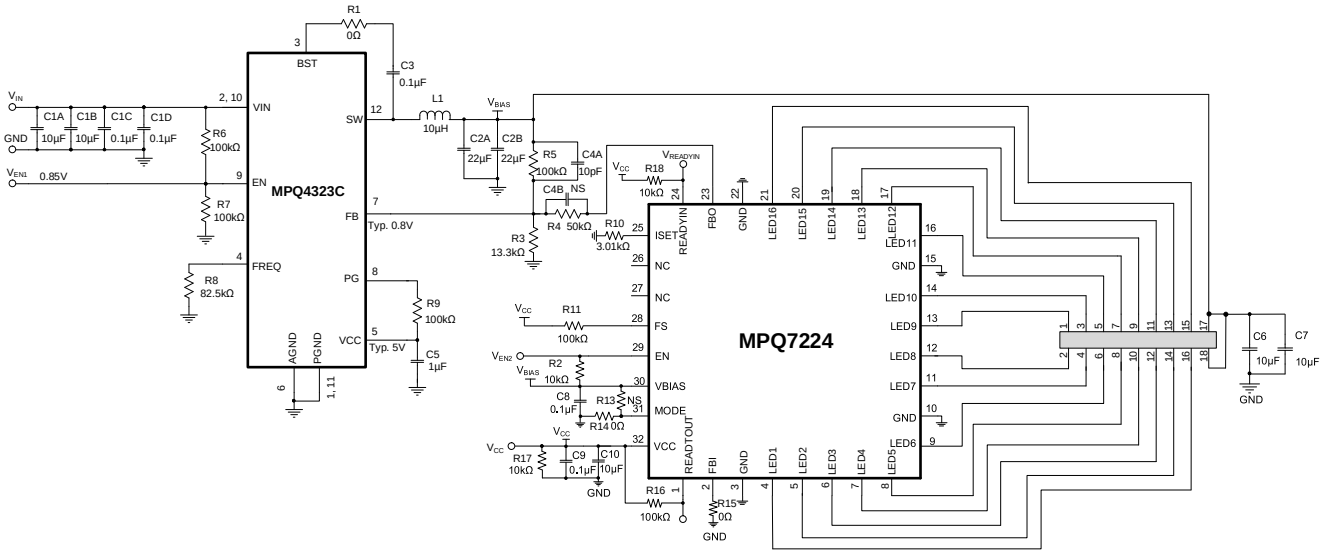
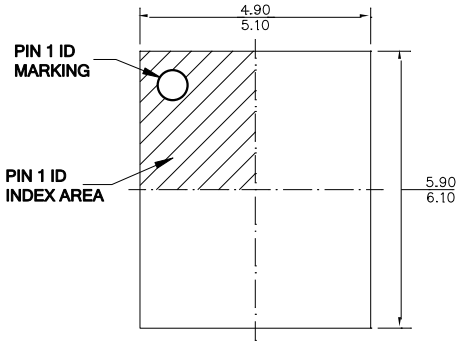


Figure 17: Typical Application Circuit with AFC and Separated Board (I_{LED} = 200mA/Channel)

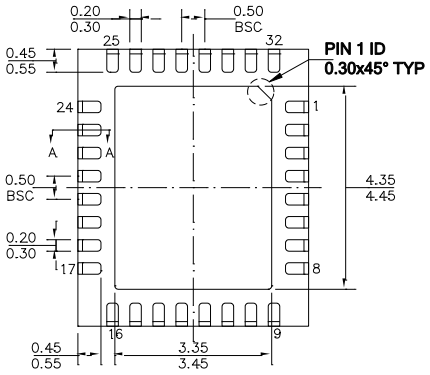
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE INFORMATION

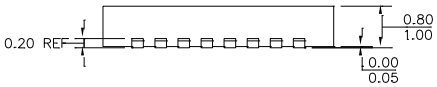
QFN-32 (5mmx6mm)
Wettable Flank



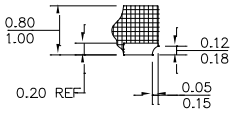
TOP VIEW



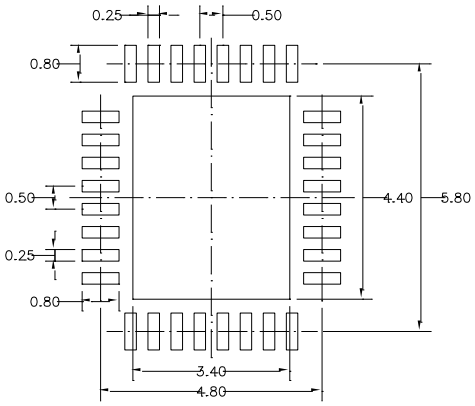
BOTTOM VIEW



SIDE VIEW



SECTION A-A



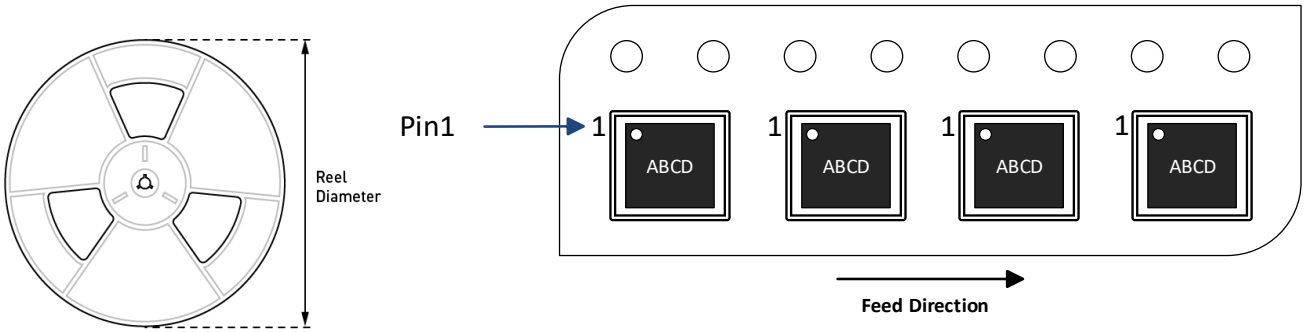
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ7224QGJE-xxxx-AEC1-Z	QFN-32 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/8/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.