MPQ70331FS

45V, 3A HV Buck, 2A LV Buck, 250mA LV Boost, ASIL-D PMIC, AEC-Q100 Qualified

DESCRIPTION

The MPQ70331FS is an ASIL-D compliant power management integrated circuit (PMIC) with advanced safety features for automotive applications. It consists of a high-voltage (HV) primary synchronous buck converter, a low-voltage (LV) secondary synchronous buck converter, and a synchronous boost converter with excellent transient response.

Voltage monitoring is implemented via a voltage supervisor to monitor the battery input voltage (V_{IN}), output rails, and two external channels, along with critical internal voltage signals, including the VCC voltage (V_{CC}) and bandgap reference. Clock monitoring, leakage monitoring, and thermal monitoring are also implemented.

Built-in self-testing (BIST) is included for critical analog and logic functions. A failsafe state machine manages fault handling and controls the safety outputs. An integrated, configurable watchdog can be configured in window and Q&A modes. The safety-related blocks have independent voltage regulators, bandgaps, and oscillators, which offer redundancy to achieve failsafe operation.

The serial peripheral interface (SPI) allows for flexibility through configurability. The one-time programmable (OTP) memory allows settings to be permanently stored. SPI transactions and the data in the registers and OTP are protected via cyclic redundancy check (CRC).

The MPQ70331FS is available in TQFN-34 (6mmx6mm) package, and it is AEC-Q100 qualified.

FEATURES

- Built for Tough Automotive Transients
  - Load Dump Up to 45V
  - Cold Crank Down to 4.5V
- Optimize Board Size and BOM
  - 3A High-Voltage (HV) Buck Regulator
  - 2A Low-Voltage (LV) Buck Regulator
  - 250mA LV Boost Regulator

FEATURES *(continued)*

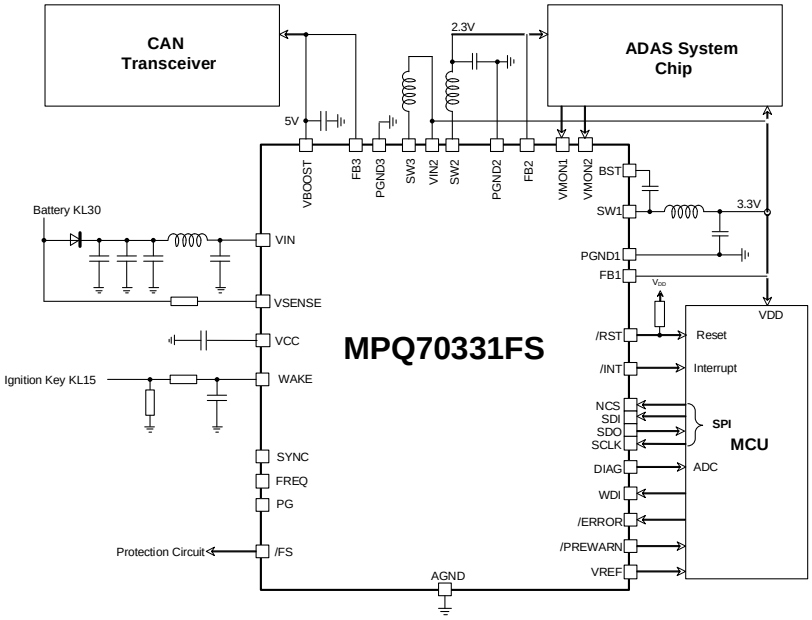
- Optimized for EMC/EMI
  - Configurable Fixed Switching Frequency (f_{SW}) from 0.38MHz to 2.5MHz
  - Frequency Spread Spectrum (FSS) for EMI Reduction
  - CISPR25 Class 5 Compliant
- Advanced Monitoring
  - Window or Q&A Watchdog
  - Battery Failure Pre-Warning
  - Microcontroller (MCU) Alive Detection
  - Clock Monitoring
  - Reset and Interrupt to the MCU
  - Error Input Signal Monitoring
  - Diagnostic Output Pin
  - Short-Circuit Protection (SCP) and Over-Current Protection (OCP)
  - Thermal Warning and Shutdown
- Functional Safety
  - Built-In Self-Testing (BIST)
  - Hardware Capable Up to ASIL-D
  - Documents Available for ISO26262 System Design to ASIL-D
  - Failure Modes Effects and Diagnostic Analysis (FMEDA)
  - Safety Manual
- Additional Features
  - Buffered Voltage Reference Output
  - SPI Interface with CRC
  - One-Time Programmable (OTP) Memory
  - Available in a TQFN-34 (6mmx6mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

MPSafe™ Developed for Functional Safety Applications: ISO26262 Compliant

APPLICATIONS

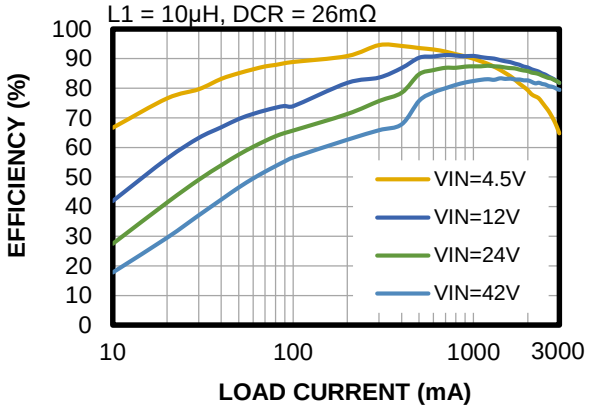
- Advanced Driver-Assistance Systems (ADAS)
- Ultra-Short Range to Long-Range Radar
- Safety Microcontroller (MCU) Power Supplies

TYPICAL APPLICATION



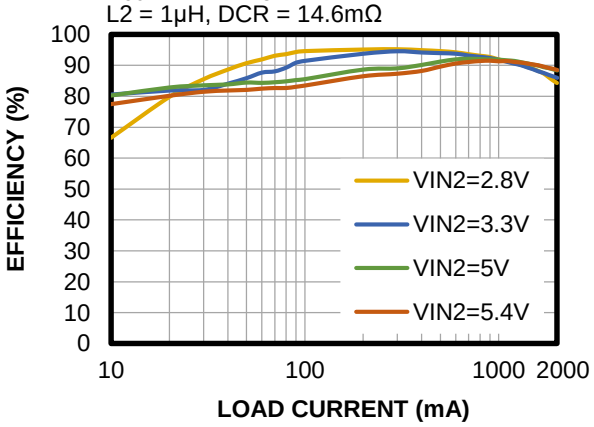
Efficiency vs. Load Current (HV Buck)

V_{OUT1} = 3.3V, f_{SW1} = 500kHz, AAM mode, other channels disabled,
L1 = 10µH, DCR = 26mΩ



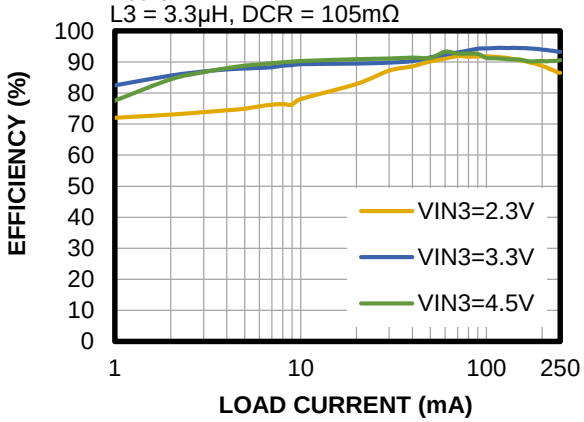
Efficiency vs. Load Current (LV Buck)

V_{OUT2} = 2.3V, f_{SW2} = 2MHz, AAM mode,
L2 = 1µH, DCR = 14.6mΩ



Efficiency vs. Load Current (Boost)

V_{OUT3} = 5V, f_{SW3} = 2MHz, AAM mode,
L3 = 3.3µH, DCR = 105mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ70331FSGQKTE-xxxxAEC***	TQFN-34 (6mmx6mm)	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MPQ70331FSGQKTE-xxxxAEC-Z).

** Moisture Sensitivity Level Rating

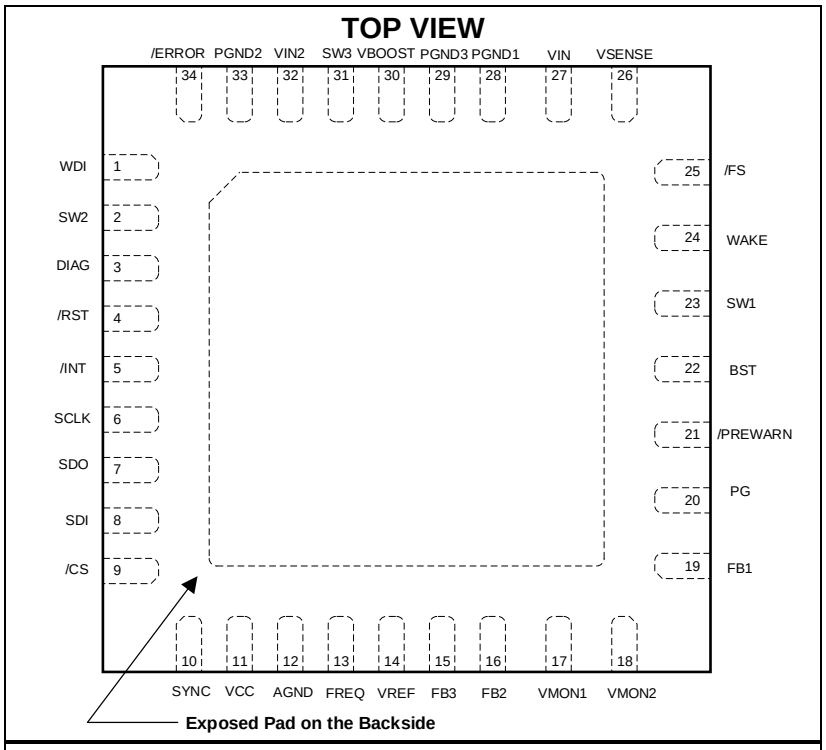
*** “xxxx” is the configuration code identifier for the register settings stored in the OTP register. The default code is “0000”. Contact MPS for details.

TOP MARKING

MPSYYWW
MP70331
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP70331: Part number
LLLLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



TQFN-34 (6mmx6mm)

PIN FUNCTIONS

Pin #	Name	Type	Description
1	WDI	I	**Window watchdog input.** While the watchdog is in window mode, a transition between the low and high logic levels within the watchdog timeout period on the WDI input is required to prevent the /RST pin from pulling low. Connect WDI to ground if it is not used.
2	SW2	PWR	**Switching node 2.** The SW2 pin is the switching node of the internal power MOSFETs for the low-voltage (LV) synchronous buck converter. Connect this pin to an external inductor using a wide PCB trace.
3	DIAG	O	**Diagnostics mux output pin.** The DIAG pin delivers analog and digital diagnostic signals, which are selectable via the SPI to a microcontroller (MCU). Float this pin if it is not used.
4	/RST	O	**Reset output.** The /RST pin has an open-drain structure. If the watchdog error counter overflows or a reset command is requested from the MCU, it is pulled low for one pulse. A resistor must be connected from this pin to a pull-up power source.
5	/INT	O	**Interrupt output pin.** If an interrupt condition occurs, the INT pin pulls low. Only writing 1 to the INTERRUPT register resets the interrupt circuit and pulls this pin high. It is required to connect a pull-up resistor from this pin to VCC. Connect this pin to ground if it is not used.
6	SCLK	I	**SPI bus serial clock.**
7	SDO	O	**SPI bus serial data out.** The SDO pin is an open-drain structure. It is required to connect a pull-up resistor from this pin to a power source.
8	SDI	I	**SPI bus serial data in.**
9	/CS	I	**SPI chip selection.** Active low.
10	SYNC	I/O	**Clock synchronization input/output pin.** If SYNC is set to SYNCIN, apply a clock signal to this pin to synchronize the internal switching frequency (f_{SW}) to the external clock signal. If this pin is set to SYNCOUT, the MPQ70331FS can output the internal clock with a 0° or 180° phase shift. Float this pin if it is not used and SYNCOUT is selected. Connect this pin to GND if it is not used and SYNCIN is selected.
11	VCC	PWR	**Internal bias supply.** The VCC pin is the internal 5V low-dropout (LDO) regulator 1 supplies power to the control circuit and gate drivers. Place a 4.7µF decoupling capacitor from VCC to ground, and close to VCC.
12	AGND	GND	**Analog ground.** AGND is the reference ground for the internal logic and signals circuit. AGND is not internally connected to power ground (PGND1, PGND2, or PGND3), so ensure that AGND is connected to power ground when designing the PCB layout.
13	FREQ	I	**Switching frequency.** Connect a resistor from the FREQ pin to the ground to set the output f_{SW}, or use the SPI to directly set f_{SW}. Float this pin if using the SPI to set f_{SW}.
14	VREF	O	**Buffered voltage reference output.** The VREF pin is the buffered output of internal bandgap reference 1. Float this pin if it is not used.
15	FB3	PWR	**Feedback input pin 3.** Connect the FB3 pin directly to the low-voltage (LV) boost converter's output. See the BOOST_PWR (0x28) section on page 83 to set V_{OUT3}.
16	FB2	PWR	**Feedback input pin 2.** Connect the FB2 pin directly to the LV buck converter's output. See the LV_BUCK_PWR (0x27) section on page 83 to set V_{OUT2}.
17	VMON1	I	**External voltage monitoring input 1 (VEXT1).** The VMON1 pin monitors over-voltage (OV) and under-voltage (UV) conditions for external voltages with a configurable threshold. No external resistor is required. ±5% monitoring accuracy is guaranteed. Float this pin if it is not used.
18	VMON2	I	**External voltage monitoring input 2 (VEXT2).** The VMON2 pin monitors OV and UV conditions for external voltages with a configurable threshold. No external resistor is required. ±5% monitoring accuracy is guaranteed. Float this pin if it is not used.

PIN FUNCTIONS *(continued)*

Pin #	Name	Type	Description
19	FB1	PWR	**Feedback input pin 1.** Connect the FB1 pin directly to the high-voltage (HV) buck converter's output. See the HV_BUCK_PWR (0x26) section on page 83 to set V_{OUT1}.
20	PG	O	**Power good indicator.** The output of the PG pin is the open drain of an N-channel MOSFET. If all of the output voltages are within the power good (PG) range of their nominal voltages, this pin goes high. Use a pull-up resistor to connect PG to a power source. Float this pin if it is not used.
21	/PREWARN	O	**Battery failure warning output.** This pin provides a battery under-voltage (UV) early warning when VSENSE drops below 8.5V. It is required to connect /PREWARN to VCC with a pull-up resistor. Connect this pin to ground if it is not used.
22	BST	PWR	**Bootstrap.** BST is the positive power supply of the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between BST and SW.
23	SW1	PWR	**Switch node 1.** The SW1 pin is the switching node of the internal MOSFETs for the HV synchronous buck converter. Connect SW1 to an external inductor using a wide PCB trace.
24	WAKE	I	**Wake-up input signal.** A wake-up signal received from the ignition (key), CAN transceiver, or the other sources at this pin all wake the device.
25	/FS	O	**Failsafe output.** Drive an electrical safe circuit independent from the MCU to deactivate the entire system and send the ECU into a known protected state. Once the watchdog error counter is cleared, the /FS pin pulls low due to a deep safe event, or /RST pulls low and recovers. It is required to connect with pin to VCC with a pull-up resistor. Float this pin if it is not used.
26	VSENSE	PWR	**Battery-sensing input.** This pin senses the battery voltage (V_{BATT}) and provides a battery failure early warning. Connect the VSENSE pin directly to the battery line. Connect this pin to VIN if it is not used.
27	VIN	PWR	**Input supply voltage.** VIN supplies power to all of the internal control circuitries and the MOSFETs. Place a decoupling capacitor to ground close to VIN to minimize switching spikes. An external reverse battery protection diode in series is required.
28	PGND1	GND	**Power ground 1.** PGND 1 is the HV synchronous buck converter's reference ground. It requires careful consideration during PCB layout. For the best results, connect PGND1, PGND2, and PGND3 with copper pours and vias.
29	PGND3	GND	**Power ground 3.** PGND3 is the synchronous boost converter's reference ground. It requires careful consideration during PCB layout. For the best results, connect PGND1, PGND2, and PGND3 with copper pours and vias.
30	VBOOST	PWR	**Synchronous boost output voltage.** The VBOOST pin is the synchronous boost converter's output pin.
31	SW3	PWR	**Switch node 3.** The SW3 pin is the switching node of the synchronous boost converter's internal power MOSFETs. Connect this pin to an external inductor using a wide PCB trace.
32	VIN2	PWR	**Input supply voltage of LV synchronous buck converter.** Connect the VIN2 pin directly to FB1. Bypass each input with a low-ESR capacitor connected to the adjacent ground pin.
33	PGND2	GND	**Power ground 2.** PGND2 is the LV synchronous buck converter's reference ground. It requires careful consideration during PCB layout. For the best results, connect PGND1, PGND2, and PGND3 with copper pours and vias.
34	/ERROR	I	**Error input.** This pin monitors error outputs from the MCU or peripheral circuit, which can bring the MPQ70331FS into a deep safe state. Connect this pin to ground if it is not used.
-	Exposed pad	-	**Exposed thermal power pad.** The exposed pad may be left open or connected to the device ground.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, WAKE, /FS.....-0.3V to +45V
VSENSE (2) .....-14V to +45V
VMON1, VMON2 .....-0.3V to +40V
FB3 .....-0.3V to +9V
VBOOST.....-0.3V to +6.5V
FB1 .....-0.3V to +6.5V
SW1 .....-0.3V to V_{IN} + 0.3V
SW2 .....-0.3V to V_{IN2} + 0.3V
SW3 .....-0.3V to + 6V
BST ..... -0.3V to V_{SW1} + 6V
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (3) (7)
TQFN-34 (6mmx6mm)..... 6.25W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (4)
Charged-device model (CDM)……..Class C2b (5)

Recommended Operating Conditions

Input voltage (V_{IN}) .....4.5V to 42V
HV buck output voltage (V_{OUT1}).....2.3V to 5.45V
LV buck output voltage (V_{OUT2}) .....0.6V to 3.75V
LV boost output voltage (V_{OUT3}) .....4.5V to 7.5V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

TQFN-34 (6mmx6mm)
JESD51-7…...……..…..30.....6.. °C/W (6)
EVQ70331FS-QK-00A.....…20...2.6.. °C/W (7)

Notes:

1) Absolute maximum ratings are rated under room temperatures, unless otherwise noted. Exceeding these ratings may damage the device.
2) The VSENSE pin is robust against ISO7637 pulses through a resistor. Contact an MPS FAE for more details.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per AEC-Q100-002.
5) Per AEC-Q100-011.
6) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application, the value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
7) Measured on an MPS standard EVB for the MPQ70331FS: 8.3cmx8.3cm, 2oz. copper, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage-Current Parameters						
Supply current (quiescent)	I_Q	No load, switching, AAM, normal state, disable WD/PIN FB check /ERROR pin monitor, /VMON monitor		500	650	µA
		No load, switching, AAM, normal state, enable WD/PIN FB check /ERROR pin monitor /VMON monitor		3.2	4.3	mA
		No load, switching, FCCM, normal state, disable WD/PIN FB check /ERROR pin monitor, /VMON monitor (8)		11.8		mA
		No load, switching, FCCM, normal state, enable WD/PIN FB check /ERROR pin monitor /VMON monitor (8)		14.5		mA
Supply current (shutdown)	I_{SD}	V_{WU} = 0V, T_J = 25°C		0.2	1	µA
		V_{WU} = 0V, T_J = -40°C to +150°C		0.2	4	µA
Input voltage (V_{IN}) power-on reset rising threshold	POR_{VTH-R}		3.7	3.9	4.1	V
V_{IN} power-on reset falling threshold	POR_{VTH-F}		3.25	3.45	3.65	V
V_{IN} power-on reset threshold hysteresis	POR_{HYS}			450		mV
Battery Under-Voltage (UV) Pre-Warning						
V_{SENSE} pre-warning threshold range	$SNSUV_{VTH}$	SPI selectable	6.5		10	V
		Default setting, falling		8.5		V
V_{SENSE} pre-warning hysteresis	$SNSUV_{HYS}$		100	350		mV
Blanking time of battery pre-warning	$t_{SNS-BLK}$	V_{SENSEW} < SNSUVVTH to /PREWARN pin assertion		100	150	µs
Leakage current at VSENSE Pin	$I_{SNS-LKG}$	V_{SENSE} = 40V			1	µA
Internal resistance between GND and VSENSE pin	$R_{SNS-GND}$	V_{SENSE} = 14V	0.55	0.8	1.05	MΩ
Thermal Shutdown and Over-Temperature Protection						
Thermal shutdown (9)	T_{SD}	T_J rising	160	175		°C
Thermal shutdown hysteresis (9)	T_{SD-HYS}			25		°C
Blanking time before thermal shutdown (9)	t_{SD-BLK}			45		µs
Over-temperature warning flag (9)	T_{OT}	T_J rising	140	155	170	°C
Over-temperature warning flag hysteresis (9)	T_{OT-HYS}			25		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Blanking time before over-temperature warning flag (9)	t_{OT-BLK}			45		µs
Power Good (PG)						
PG sink current capacity	$V_{PG-SINK}$	Sink 4mA			200	mV
PG delay time	$t_{PG-DELAY}$	Rising edge, V_{OUT1} OV		60		µs
		Falling edge, V_{OUT1} OV		60		µs
PG leakage current	I_{PG-LKG}			1	200	nA
PG lower trip threshold		As a percentage of V_{FB}	86	90	94	%
PG upper trip threshold		As a percentage of V_{FB}	106	110	114	%
PG trip threshold hysteresis		As a percentage of V_{FB}		2.5		%
Wake Up						
Wake-up input threshold	WU_{Vth}	Level sensitive input	2.3	2.5	2.7	V
Wake-up threshold hysteresis	V_{WU-HYS}		50	150	250	mV
Wake-up input current	I_{WU}	V_{WU} = 5V		0.9	2	µA
Wake-up deglitch filter time	$t_{WU-DEGLITCH}$			1.1	1.5	ms
Wake-up to power-up delay	$t_{WU-DELAY}$	Wake-up detected to all rails are PG, default setting		19	25	ms
Internal VCC						
VCC regulator 1	V_{CC1}	I_{CC} = 0mA	4.8	5	5.2	V
		I_{CC} = 10mA	4.8	5	5.2	V
VCC regulator 2	V_{CC2}	I_{CC} = 0mA	4.8	5	5.2	V
		I_{CC} = 10mA (8)	4.8	5	5.2	V
Voltage reference 1	V_{REF1}	T_J = 25°C	0.772	0.8	0.828	V
		T_J = -40°C to +150°C	0.768	0.8	0.832	V
Voltage reference 2	V_{REF2}	T_J = 25°C	0.772	0.8	0.828	V
		T_J = -40°C to +150°C	0.768	0.8	0.832	V
High-Voltage (HV) Synchronous Buck Converter						
Regulated output range	V_{OUT1}	V_{IN} - V_{OUT} > 0.5V	2.3		5.45	V
		Default setting	3.25	3.3	3.35	V
Low-side (LS) switch current limit to LS switch reverse current limit	$I_{LS-LIMIT1}$	Sinking, CCM	-3.7	-2.75	-1.8	A
Peak current limit	$I_{PEAK-LIMIT1}$	Default setting	3	4	5	A
Valley current limit	$I_{VALLEY-LIMIT1}$	Default setting	2.3	3	3.7	A
Zero-current detection (ZCD) threshold	I_{ZCD1}		-100	+250	+400	mA
FB input current	I_{FB1}	V_{FB1} = 4V		35	60	µA
High-side (HS) switch on resistance	$R_{DSON-H1}$	V_{BST} - V_{SW1} = 5V		240	450	mΩ
LS switch on resistance	$R_{DSON-L1}$	V_{BST} - V_{SW1} = 5V		100	180	mΩ
SW leakage current	$I_{SW-LKG1}$	V_{WU} = 0V, V_{SW1} = 0V			1.5	µA
		V_{SW1} = 60V			3	µA
Frequency ratio to HV buck			25		100	%
Sync voltage rising threshold	$V_{SYNC-RISING1}$			1.5	1.7	V
Sync voltage falling threshold	$V_{SYNC-FALLING1}$		0.8	1.3		V
Minimum on time (8)	$t_{ON-MIN1}$			90		ns
Minimum off time (8)	$t_{OFF-MIN1}$			110		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Maximum duty cycle	D_{MAX1}			99		%
BST-SW under-voltage lockout (UVLO)				2.5	3	V
BST-SW UVLO hysteresis			0.1	0.25		V
Soft-start time	t_{SS1}		0.5	0.9	1.3	ms
Phase shift to main CLK				0		degree
Low-Voltage (LV) Synchronous Buck Converter (V_{IN2} = 3.3V)						
LV buck supply voltage range	V_{IN2}		2.3		5.5	V
Switching frequency	f_{SW}	Default setting	1.7	2	2.3	MHz
Regulated output range	V_{OUT2}	V_{IN} - V_{OUT} > 0.5V	0.6		3.75	V
		Default setting	2.265	2.3	2.335	V
		V_{OUT2} > 2V	-1.5	0	+1.5	%
		V_{OUT2} < 2V, T_J = 25°C	-1.5	0	+1.5	%
		V_{OUT2} < 2V, T_J = -40°C to +150°C	-2	0	+2	%
LS switch reverse current limit	$I_{LS-LIMIT2}$	Sinking, CCM	-3.7	-2.75	-1.8	A
Peak current limit	$I_{PEAK-LIMIT2}$	Default setting	3	4	5	A
Valley current limit	$I_{VALLEY-LIMIT2}$	Default setting	2.3	3	3.7	A
ZCD threshold	I_{ZCD2}		-100	+250	+400	mA
FB input current	I_{FB2}	V_{FB2} = 3V		10	25	µA
HS switch on resistance (P-channel)	$R_{DSON-H2}$	V_{IN2} = 3.3V		130	200	mΩ
LS switch on resistance (N-channel)	$R_{DSON-L2}$	V_{IN2} = 3.3V		75	130	mΩ
SW leakage current	$I_{SW-LKG2}$	V_{WU} = 0V, V_{SW2} = 0V, V_{IN2} = 6V			15	µA
		V_{SW2} = 6V, V_{IN2} = 6V			20	
Frequency configurable range	f_{PROG2}		0.4		2.5	MHz
Sync frequency range	f_{SYNC2}		0.4		2.5	MHz
Minimum on time (8)	$t_{ON-MIN2}$			45		ns
Minimum off time (8)	$t_{OFF-MIN2}$			75		ns
Maximum duty cycle	D_{MAX2}			100		%
Soft-start time	t_{SS2}		0.6	1	1.4	ms
Phase shift to main CLK				0		degree
LV Synchronous Boost Converter (V_{IN3} = 3.3V)						
Boost supply voltage range	V_{IN3}		2.3		5.5	V
Regulated output range	V_{OUT3}	V_{IN} - V_{OUT} > 0.5V	4.4		7.75	V
		Default setting	4.9	5	5.1	V
Peak current limit	$I_{PEAK-LIMIT3}$	Default setting	0.9	1.2	1.5	A
Valley current limit	$I_{VALLEY-LIMIT3}$	Default setting	0.55	0.7	0.9	A
ZCD threshold	I_{ZCD3}	Default setting	-0.1	+0.1	+0.35	A
FB input current	I_{FB3}	V_{FB3} = 5V		50	65	µA
HS switch on resistance (P-channel)	$R_{DSON-H3}$			250	400	mΩ
LS switch on resistance (N-channel)	$R_{DSON-L3}$			220	400	mΩ
HS switch leakage current (P-channel)	I_{P-LKG3}	V_{SW} = 0V, V_{BOOST} = 6.5V			15	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
LS switch leakage current (N-channel)	I_{N-LKG3}	V_{SW} = 6.2V, V_{OUT} = 0V			5	µA
Minimum on time (8)	$t_{ON-MIN3}$			57		ns
Minimum off time (8)	$t_{OFF-MIN3}$			61		ns
Maximum duty cycle	D_{MAX3}			99		%
Soft-start time	t_{SS3}		0.6	1	1.4	ms
Phase shift to main CLK				180		degree
Voltage Supervisor						
HV buck output V_{OUT1} over-voltage (OV) threshold	$V_{OUT1-OV-VTH}$	SPI selectable	104		116	%
		Default setting and accuracy	102	104	106	%
HV buck output V_{OUT1} OV hysteresis	$V_{OUT1-OV-HYS}$	Inner hysteresis		1.2		%
HV buck output V_{OUT1} Undervoltage threshold	$V_{OUT1-UV-VTH}$	SPI selectable	84		96	%
		Default setting and accuracy	94.5	96	97.5	%
HV buck output V_{OUT1} Undervoltage hysteresis	$V_{OUT1-UV-HYS}$	Inner hysteresis		1.2		%
LV buck output V_{OUT2} OV threshold	$V_{OUT2-OV-VTH}$	SPI selectable	104		116	%
		Default setting and accuracy	102	104	106	%
LV buck output V_{OUT2} OV hysteresis	$V_{OUT2-OV-HYS}$	Inner hysteresis		1.2		%
LV buck output V_{OUT2} UV threshold	$V_{OUT2-UV-VTH}$	SPI selectable	84		96	%
		Default setting and accuracy	94.5	96	97.5	%
LV buck output V_{OUT2} UV hysteresis	$V_{OUT2-UV-HYS}$	Inner hysteresis		1.2		%
Boost output V_{OUT3} OV threshold	$V_{OUT3-OV-VTH}$	SPI selectable	104		116	%
		Default setting and accuracy	102	104	106	%
Boost output V_{OUT3} OV hysteresis	$V_{OUT3-OV-HYS}$	Inner hysteresis		1.2		%
Boost output V_{OUT3} UV threshold	$V_{OUT3-UV-VTH}$	SPI selectable	84		96	%
		Default setting and accuracy	94.5	96	97.5	%
Boost output V_{OUT3} UV hysteresis	$V_{OUT3-UV-HYS}$	Inner hysteresis		1.2		%
VMON1 pin input OV threshold	$V_{MON1-OV-VTH}$	SPI selectable	104		116	%
		Default setting and accuracy	102	104	106	%
VMON1 pin input OV hysteresis	$V_{MON1-OV-HYS}$	Inner hysteresis		1.2		%
VMON1 pin input UV threshold	$V_{MON1-UV-VTH}$	SPI selectable	84		96	%
		Default setting and accuracy	94	96	98	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VMON1 pin input UV hysteresis	$V_{MON1-UV-HYS}$	Inner hysteresis		1.2		%
VMON2 pin input OV threshold	$V_{MON1-OV-VTH}$	SPI selectable	104		116	%
		Default setting and accuracy	102	104	106	%
VMON2 pin input OV hysteresis	$V_{MON1-OV-HYS}$	Inner hysteresis		1.2		%
VMON2 pin input UV threshold	$V_{MON1-UV-VTH}$	SPI selectable	84		96	%
		Default setting and accuracy	94	96	98	%
VMON2 pin input UV hysteresis	$V_{MON1-UV-HYS}$	Inner hysteresis		1.2		%
Deglitch time	$t_{UVOV\_DEGLICH}$	V_{OUT1} OV		100		µs
Interrupt Output						
Interrupt low output level	V_{INT-OL}	I_{INT} = 2.5mA			200	mV
Interrupt input leakage current	$I_{INT-LKG}$				200	nA
Reset Output						
/RST low output level	V_{RST-OL}	I_{RST} = 2mA, active			200	mV
/RST input leakage current	$I_{RST-LKG}$				200	nA
/RST minimum holding time (10)	$t_{RST-HOLD}$			1		ms
Fail-Safe Output						
/FS pin low output level	V_{FS-OL}	I_{FS} = 2mA, active			300	mV
/FS pin input current leakage	I_{FS-LKG}	Inactive, pull up is 5V			200	nA
Watchdog						
Window watchdog WDI pin deglitch time for input pulse (10)	$t_{WD\_DEGLICH}$			30	50	µs
Internal System Clock						
System clock frequency	$f_{SYS-CLK}$	T_J = 25°C	7.2	8	8.8	MHz
		T_J = -40°C to +150°C	6.8	8	9.2	MHz
Other Digital Input/Output						
Digital input high level (11)	$V_{DIG\_IN\_H}$		2.0			V
Digital input low level (11)	$V_{DIG\_IN\_L}$				0.8	V
Digital input hysteresis (11)	$V_{DIG\_IN\_HYS}$		0.1			V
Output sink ability at DIAG pin in AMUX mode	I_{DIAG_AMUX}			566		µA
Digital output low level (12)	$V_{DIG\_OUT\_L}$	I_{OUT} = 2mA (into pin), /PREWARN, SDO, and DIAG in DMUX mode			200	mV

Notes:

8) Not tested in production. Guaranteed by design and characterization.
9) Tested in test mode under room temperature.
10) Guaranteed by scan chain testing.
11) Tested for the /ERROR, WDI, NCS, SDI, and SCLK pins.
12) Tested for the /PREWARN, SDO, and DIAG pins in DMUX mode.

SPI CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
SPI Interface Timing Requirements						
SCLK period (13)	t_{SPI}	Maximum SCLK frequency supported is 4MHz	225	250	275	ns
MISO low-to-high transition speed with 2V rising threshold and 0.8V falling threshold (13)	t_{MISO_L2H}	V_{DDIO} = 5V, R = 250Ω, C_{LOAD} = 50pF	10		34	ns
MISO high-to-low transition speed with 2V rising threshold and 0.8V falling threshold (13)	t_{MISO_H2L}	V_{DDIO} = 5V, R = 250Ω, C_{LOAD} = 50pF	4.6		20	ns
SCLK low time (13)	t_{SCKL}		95			ns
SCLK high time (13)	t_{SCKH}		95			ns
Propagation delay (13)	t_{PCLD}	SCLK falling edge to data at 10% MISO falling edge			34	ns
NCS falling edge to when MISO is active (13)	t_{FSIV}				112	ns
SDI set-up time (13)	t_{SIS}	Set-up time of MOSI before rising edge of SCLK	40			ns
SDI holding time (13)	t_{SIH}	Hold time for MOSI after rising edge of SCLK	40			ns
NCS rising edge to MISO high impedance (Hi-Z) (13)	t_{SOTRI}				112	ns
NCS deglitch time (13)	t_{NCS_MIN}		10		40	ns
Minimum time between two SPI commands (13)	$t_{MIN2SPI}$		1			µs
High-level input voltage (13)	V_{I_HIGH}	CS, SCLK, MOSI, V_{IO} = 3.3V, 5V	2			V
Low-level input voltage (13)	V_{I_LOW}	CS, SCLK, MOSI, V_{IO} = 3.3V, 5V			0.8	V
Input voltage hysteresis (13)	V_{I_HYS}	CS, SCLK, MOSI, V_{IO} =3.3V, 5V		0.1		mV
MISO output high voltage (13)	V_{O_HIGH}		2			V
MISO output low voltage (13)	V_{O_LOW}				0.8	V

Note:

13) Not tested in production. Guaranteed by design and characterization.

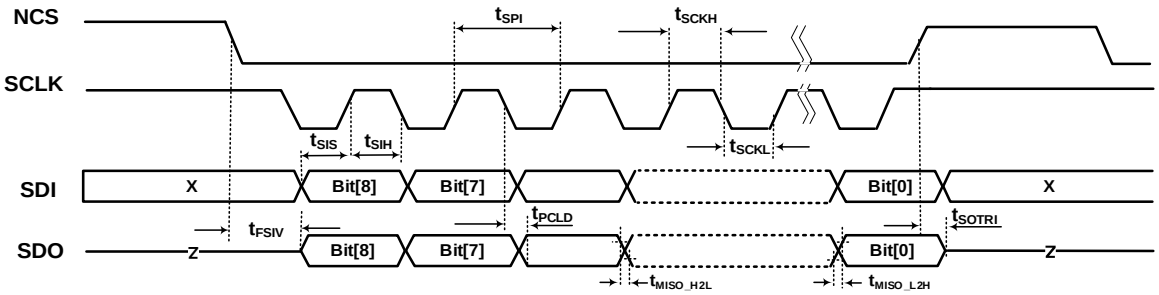


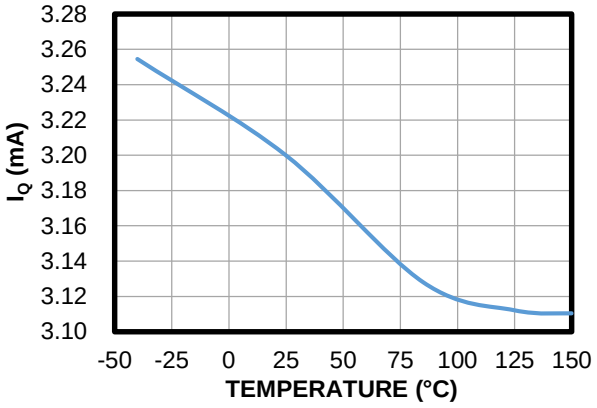
Figure 1: SPI Timing Diagram

TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_A = -40°C to +150°C, unless otherwise noted.

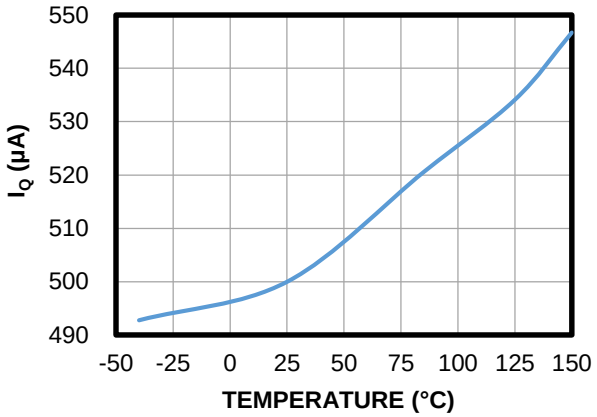
I_Q vs. Temperature

AAM, normal state

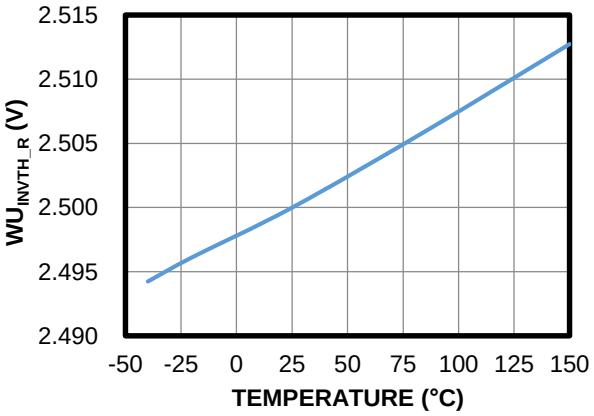


I_Q vs. Temperature

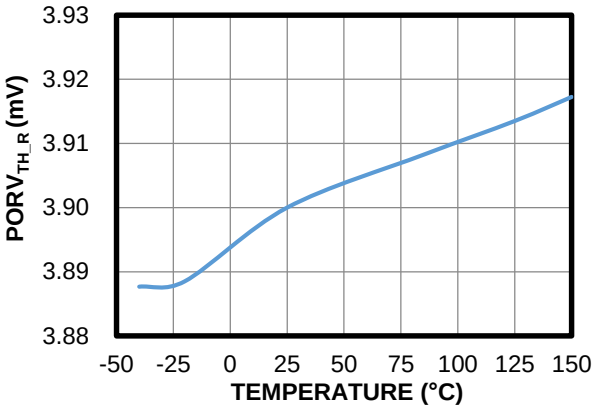
AAM, normal, disable part of digital



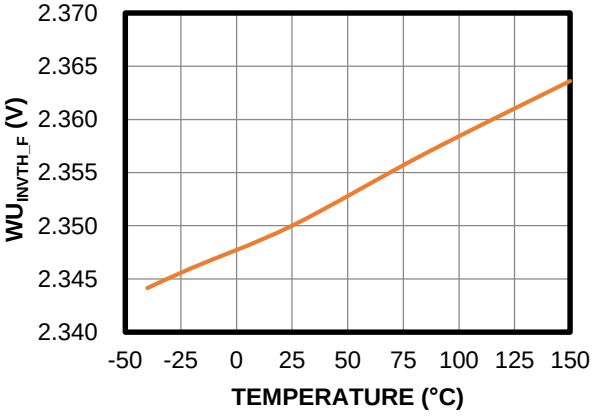
WU_{VTH_R} vs. Temperature



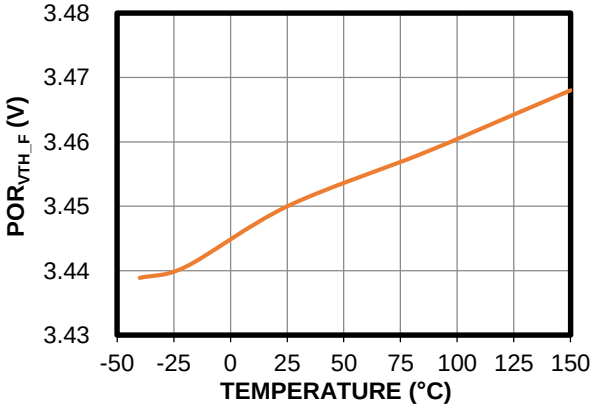
POR_{VTH_R} vs. Temperature



WU_{VTH_F} vs. Temperature



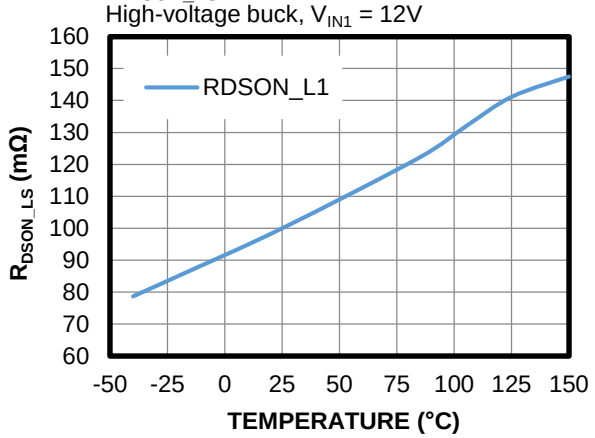
POR_{VTH_F} vs. Temperature



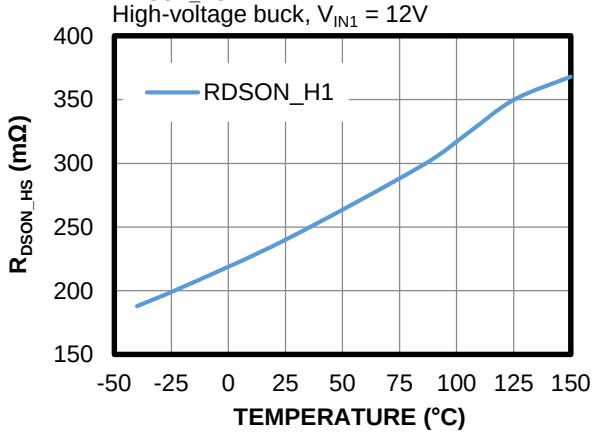
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = -40°C to +150°C, unless otherwise noted.

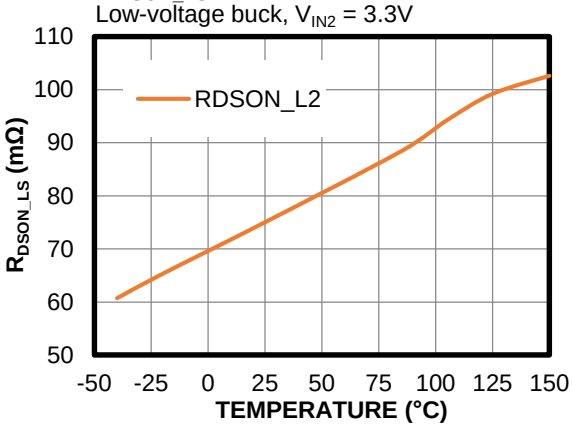
R_{DSON_LS} vs. Temperature
High-voltage buck, V_{IN1} = 12V



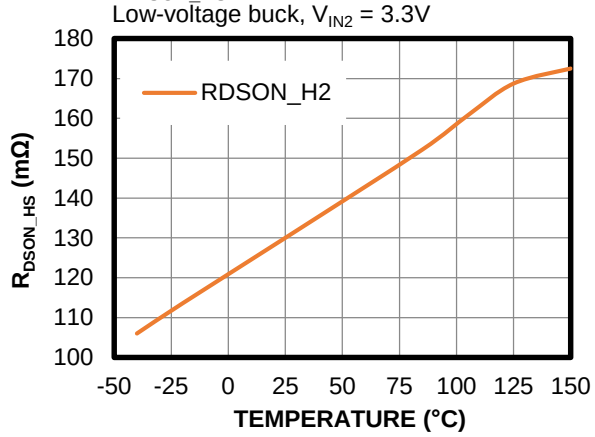
R_{DSON_HS} vs. Temperature
High-voltage buck, V_{IN1} = 12V



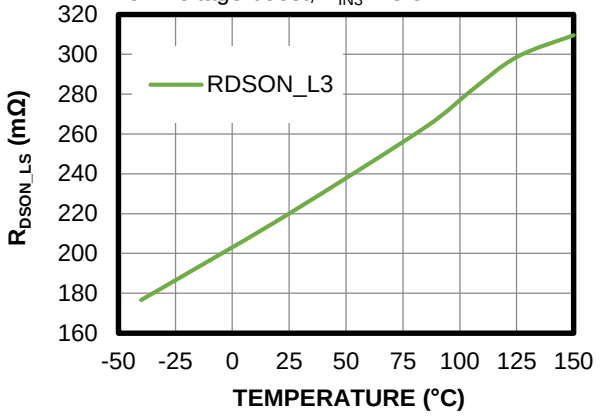
R_{DSON_LS} vs. Temperature
Low-voltage buck, V_{IN2} = 3.3V



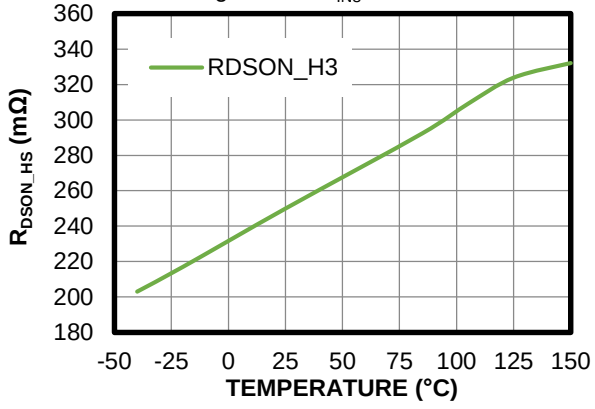
R_{DSON_HS} vs. Temperature
Low-voltage buck, V_{IN2} = 3.3V



R_{DSON_LS} vs. Temperature
Low-voltage boost, V_{IN3} = 3.3V



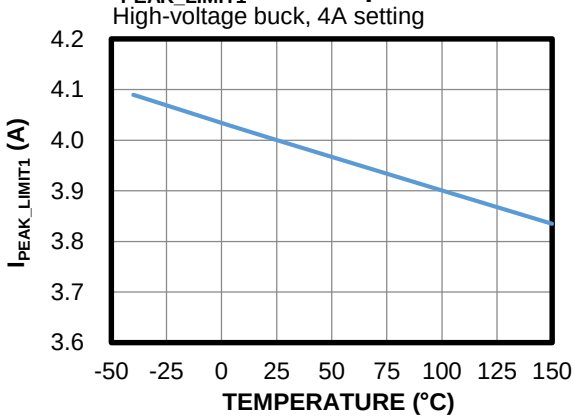
R_{DSON_HS} vs. Temperature
Low-voltage boost, V_{IN3} = 3.3V



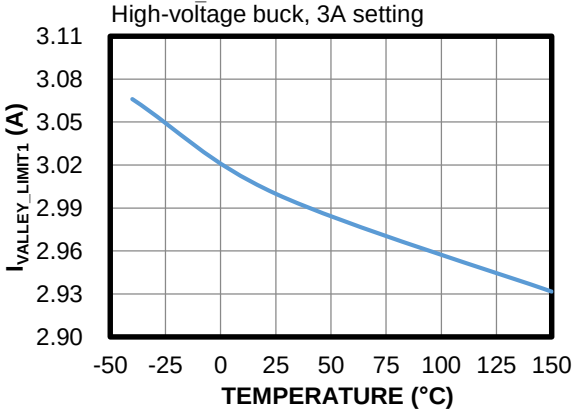
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = -40°C to +150°C, unless otherwise noted.

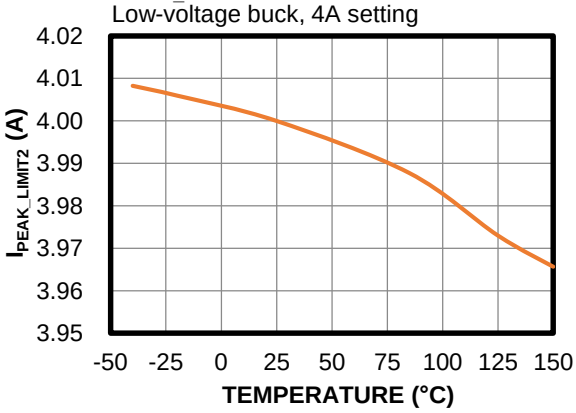
I_{PEAK_LIMIT1} vs. Temperature
High-voltage buck, 4A setting



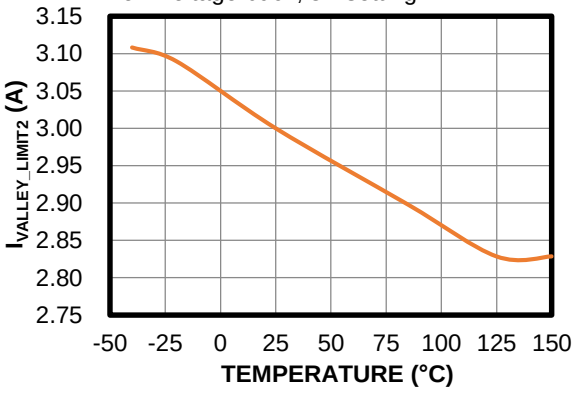
I_{VALLEY_LIMIT1} vs. Temperature
High-voltage buck, 3A setting



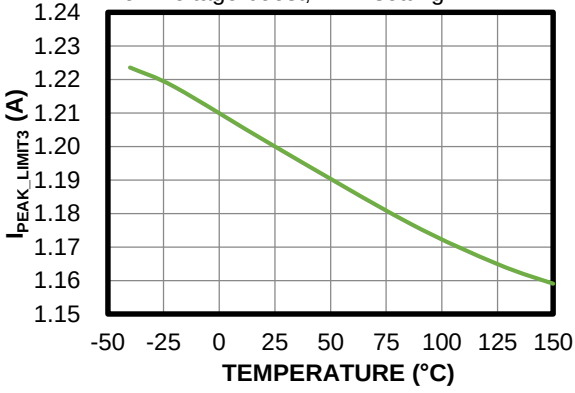
I_{PEAK_LIMIT2} vs. Temperature
Low-voltage buck, 4A setting



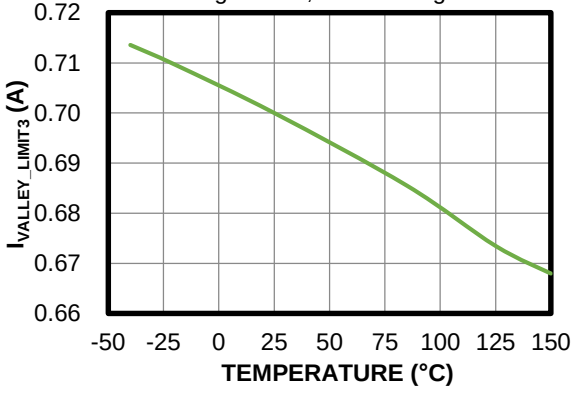
I_{VALLEY_LIMIT2} vs. Temperature
Low-voltage buck, 3A setting



I_{PEAK_LIMIT3} vs. Temperature
Low-voltage boost, 1.2A setting



I_{VALLEY_LIMIT3} vs. Temperature
Low-voltage boost, 0.7A setting

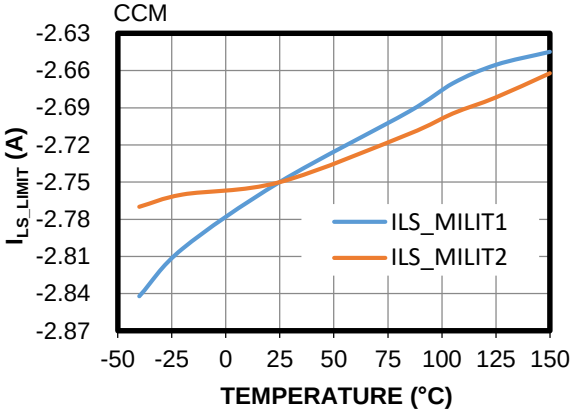


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = -40°C to +150°C, unless otherwise noted.

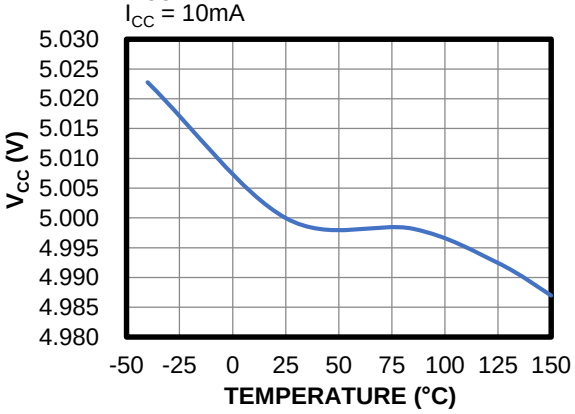
Reverse Current Limit vs. Temperature

CCM



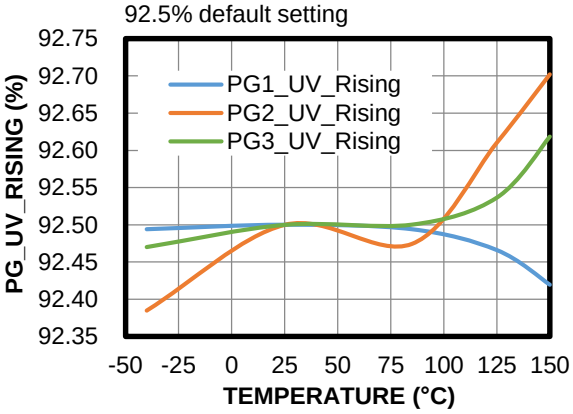
V_{CC} vs. Temperature

I_{CC} = 10mA



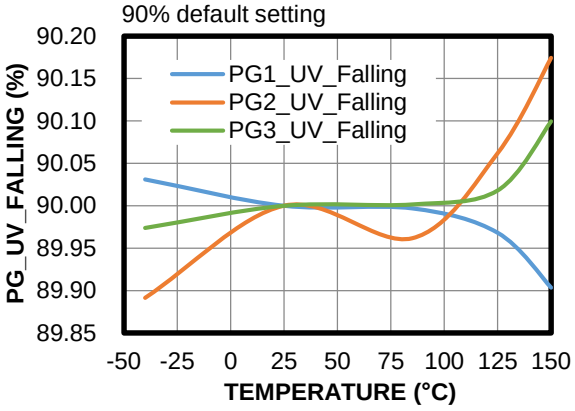
PG_UV_RISING vs. Temperature

92.5% default setting



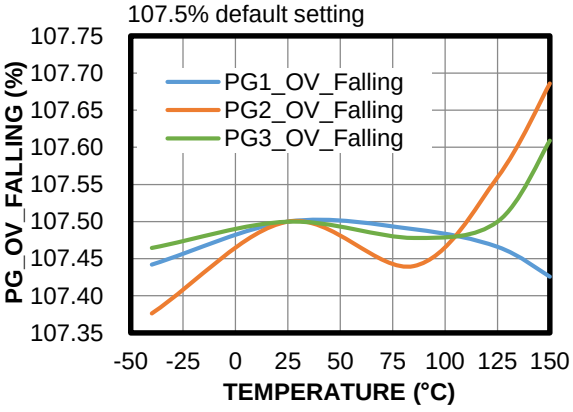
PG_UV_FALLING vs. Temperature

90% default setting



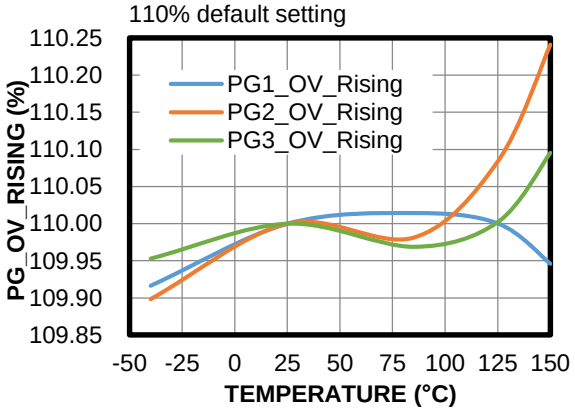
PG_OV_FALLING vs. Temperature

107.5% default setting



PG_OV_RISING vs. Temperature

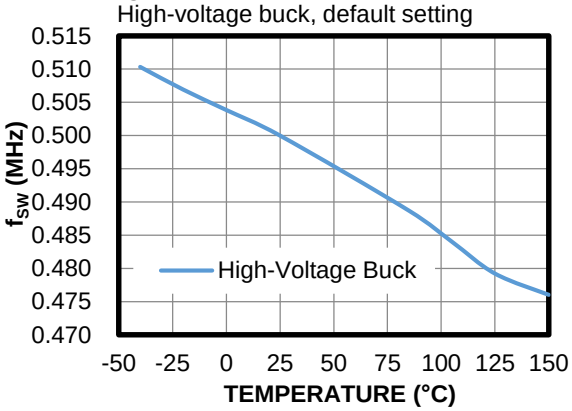
110% default setting



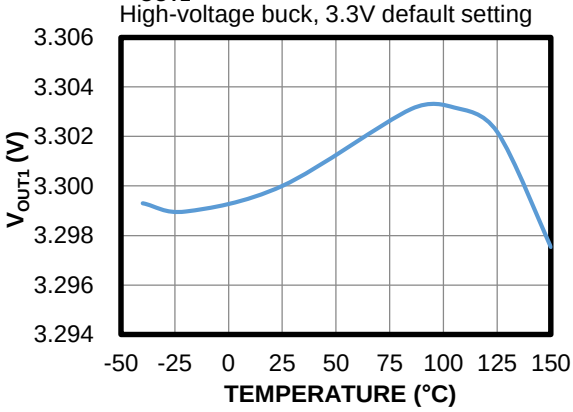
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = -40°C to +150°C, unless otherwise noted.

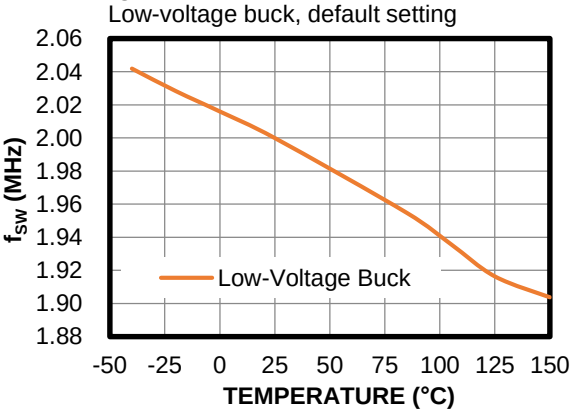
f_{SW} vs. Temperature
High-voltage buck, default setting



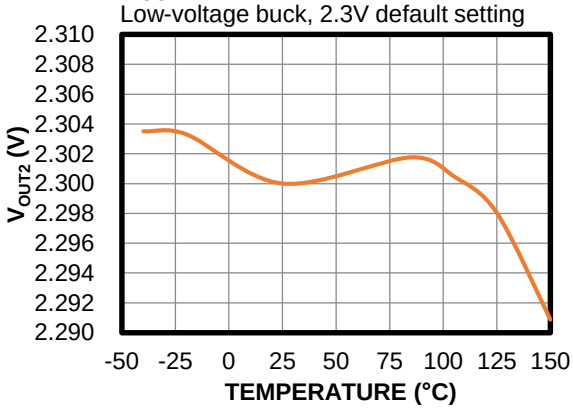
V_{OUT1} vs. Temperature
High-voltage buck, 3.3V default setting



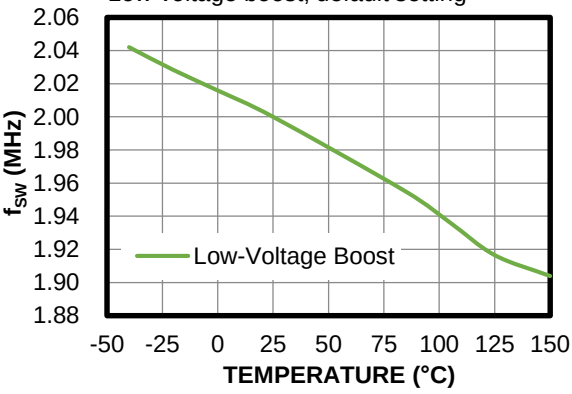
f_{SW} vs. Temperature
Low-voltage buck, default setting



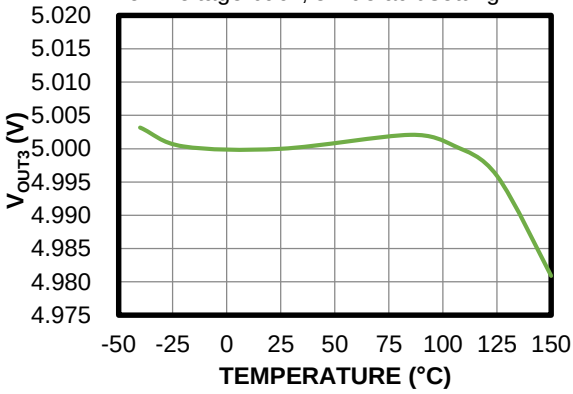
V_{OUT2} vs. Temperature
Low-voltage buck, 2.3V default setting



f_{SW} vs. Temperature
Low-voltage boost, default setting



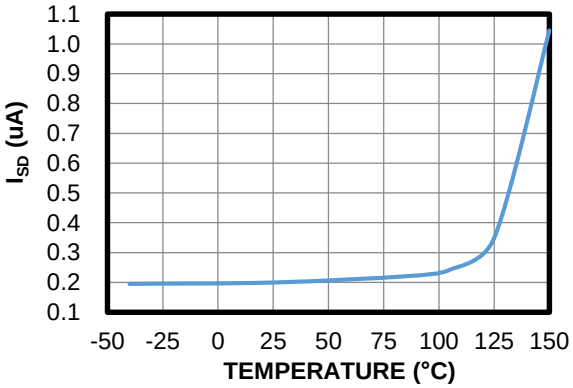
V_{OUT3} vs. Temperature
Low-voltage buck, 5V default setting



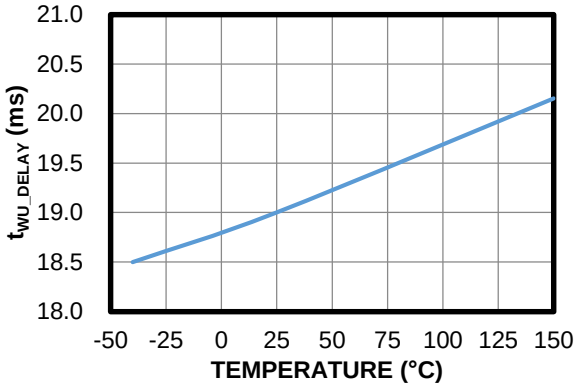
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = -40°C to +150°C, unless otherwise noted.

I_{SD} vs. Temperature



t_{WU_DELAY} vs. Temperature

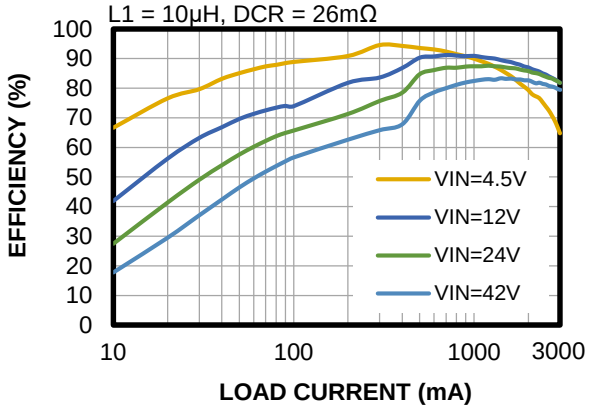


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

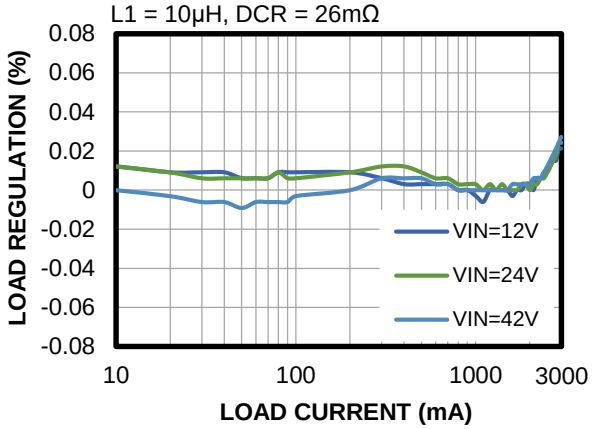
Efficiency vs. Load Current (HV Buck)

V_{OUT1} = 3.3V, f_{SW1} = 500kHz, AAM mode, other channels disabled, L1 = 10µH, DCR = 26mΩ



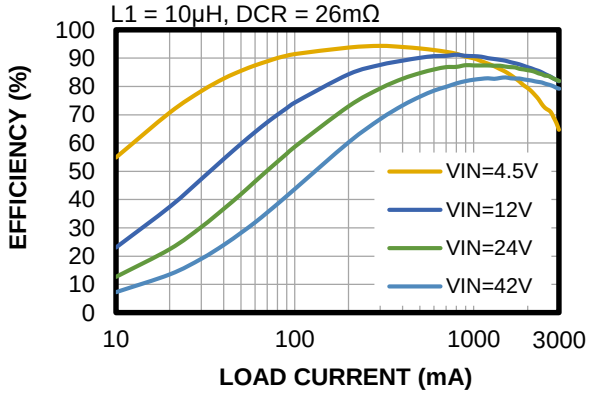
Load Regulation (HV Buck)

V_{OUT1} = 3.3V, f_{SW1} = 500kHz, AAM mode, other channels disabled, L1 = 10µH, DCR = 26mΩ



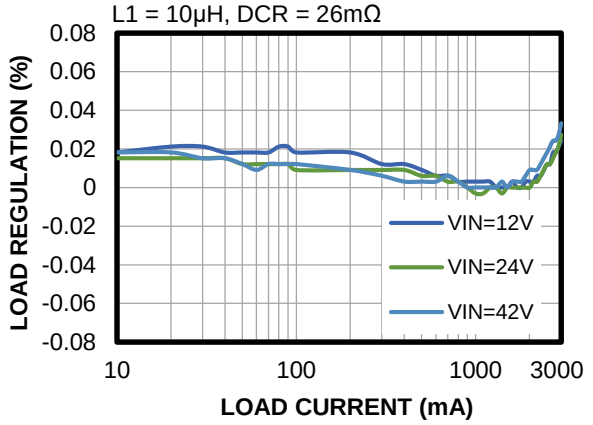
Efficiency vs. Load Current (HV Buck)

V_{OUT1} = 3.3V, f_{SW1} = 500kHz, FCCM, other channels disabled, L1 = 10µH, DCR = 26mΩ



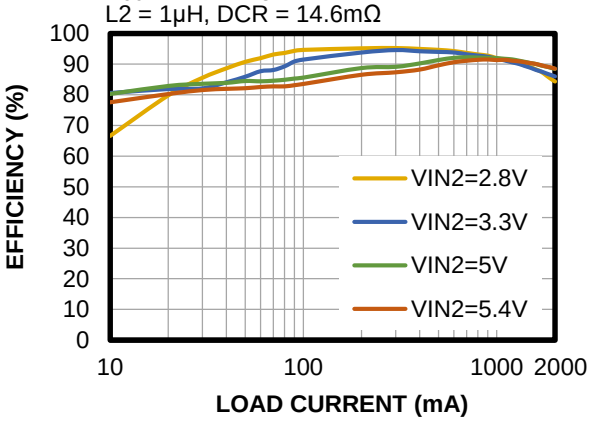
Load Regulation (HV Buck)

V_{OUT1} = 3.3V, f_{SW1} = 500kHz, FCCM, other channels disabled, L1 = 10µH, DCR = 26mΩ



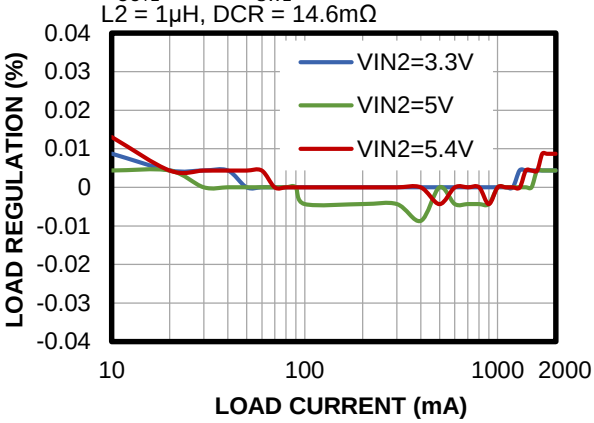
Efficiency vs. Load Current (LV Buck)

V_{OUT2} = 2.3V, f_{SW2} = 2MHz, AAM mode, L2 = 1µH, DCR = 14.6mΩ



Load Regulation (LV Buck)

V_{OUT2} = 2.3V, f_{SW2} = 2MHz, AAM mode, L2 = 1µH, DCR = 14.6mΩ

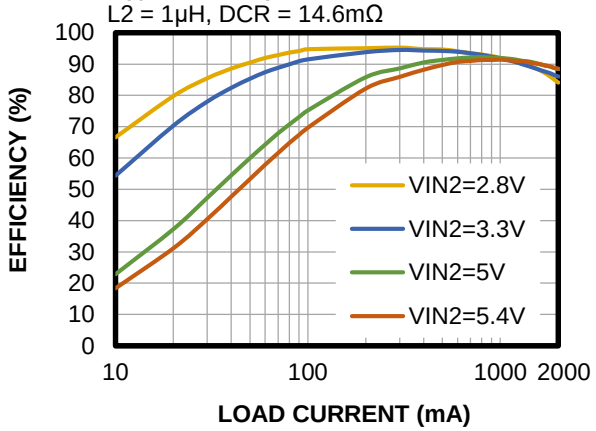


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

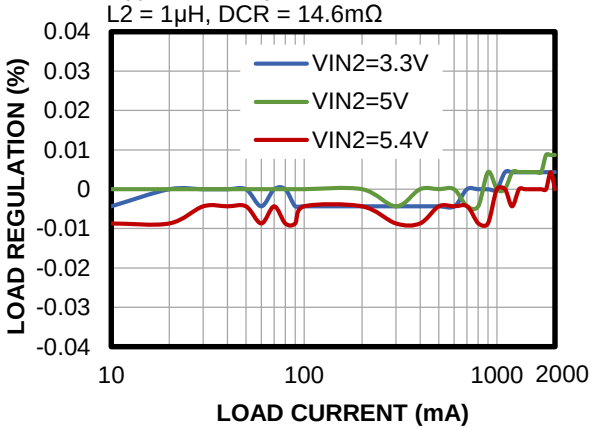
Efficiency vs. Load Current (LV Buck)

V_{OUT2} = 2.3V, f_{SW2} = 2MHz, FCCM, L2 = 1µH, DCR = 14.6mΩ



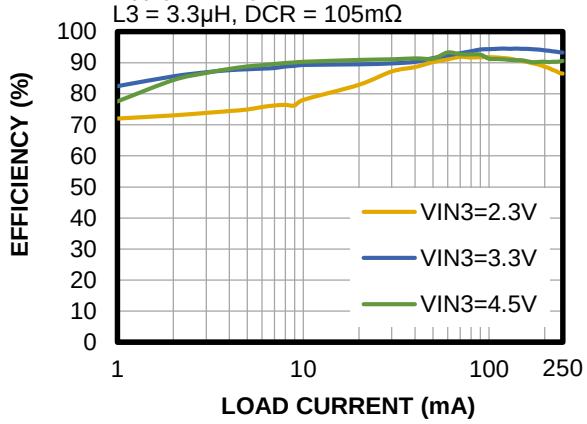
Load Regulation (LV Buck)

V_{OUT2} = 2.3V, f_{SW2} = 2MHz, FCCM, L2 = 1µH, DCR = 14.6mΩ



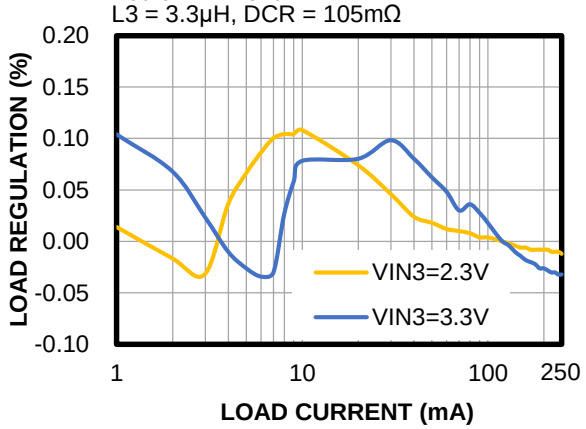
Efficiency vs. Load Current (Boost)

V_{OUT3} = 5V, f_{SW3} = 2MHz, AAM mode, L3 = 3.3µH, DCR = 105mΩ



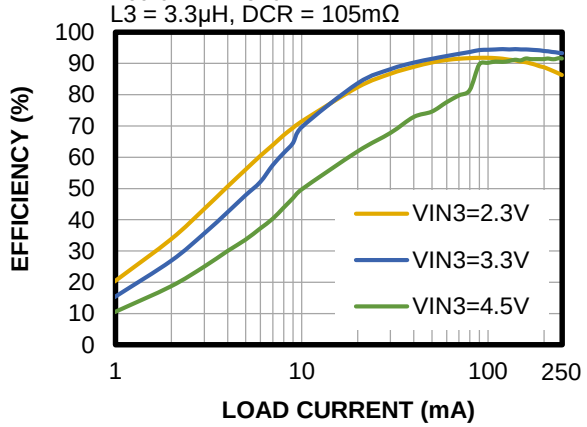
Load Regulation (Boost)

V_{OUT3} = 5V, f_{SW3} = 2MHz, AAM mode, L3 = 3.3µH, DCR = 105mΩ



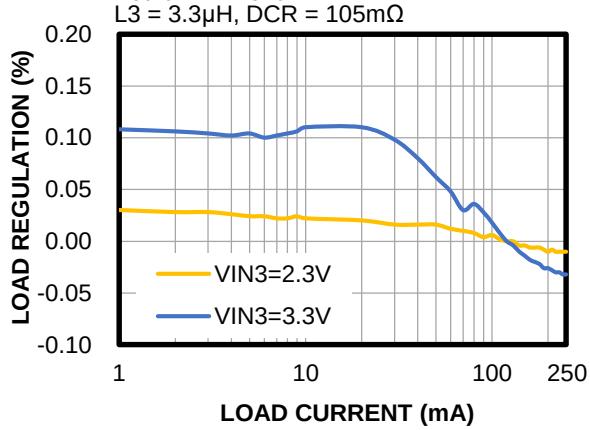
Efficiency vs. Load Current (Boost)

V_{OUT3} = 5V, f_{SW3} = 2MHz, FCCM, L3 = 3.3µH, DCR = 105mΩ



Load Regulation (Boost)

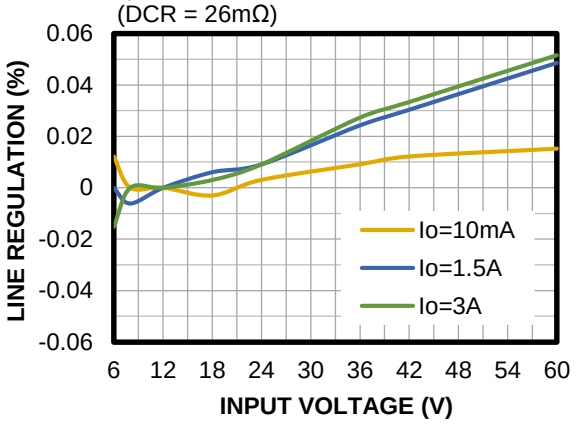
V_{OUT3} = 5V, f_{SW3} = 2MHz, FCCM, L3 = 3.3µH, DCR = 105mΩ



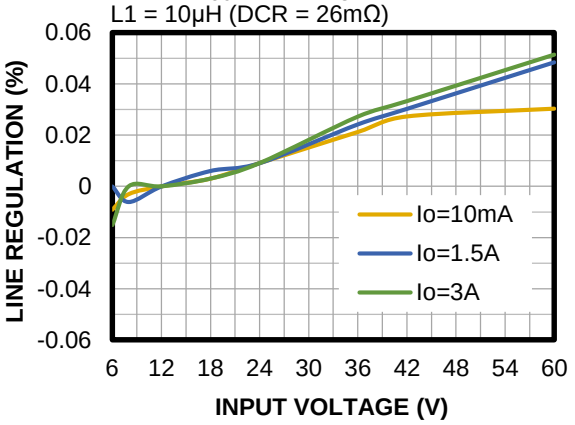
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

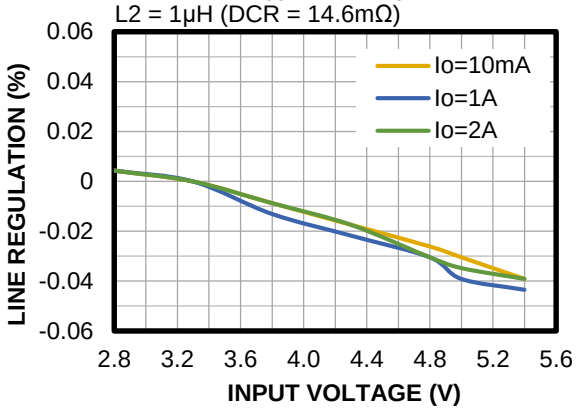
Line Regulation (HV Buck)
AAM mode, V_{OUT} = 3.3V,
f_{SW1} = 500kHz, L1 = 10µH
(DCR = 26mΩ)



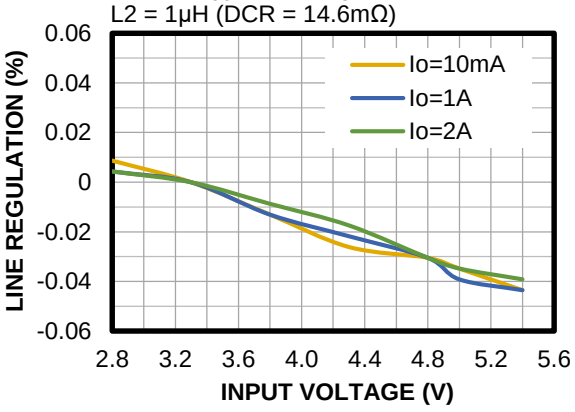
Line Regulation (HV Buck)
FCCM, V_{OUT} = 3.3V, f_{SW1} = 500kHz,
L1 = 10µH (DCR = 26mΩ)



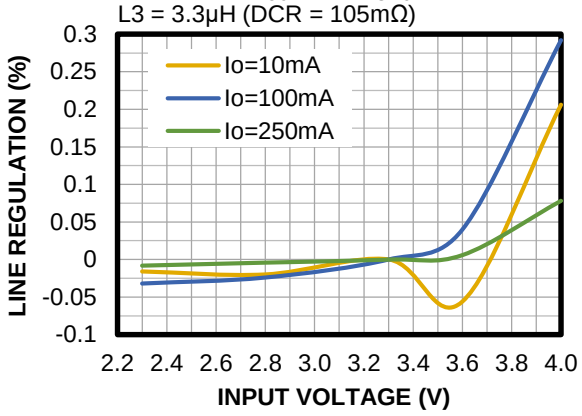
Line Regulation (LV Buck)
AAM mode, V_{OUT} = 2.3V, f_{SW2} = 2MHz,
L2 = 1µH (DCR = 14.6mΩ)



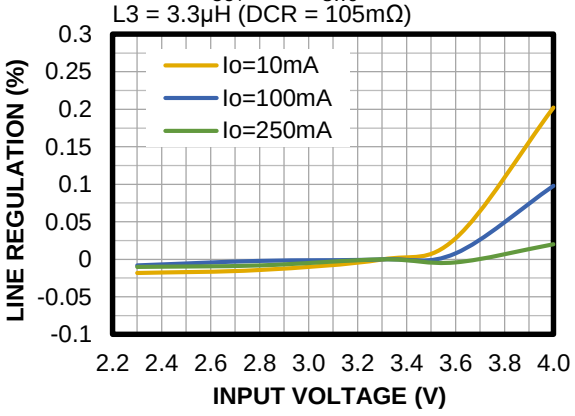
Line Regulation (LV Buck)
FCCM, V_{OUT} = 2.3V, f_{SW2} = 2MHz,
L2 = 1µH (DCR = 14.6mΩ)



Line Regulation (Boost)
AAM mode, V_{OUT} = 5V, f_{SW3} = 2MHz,
L3 = 3.3µH (DCR = 105mΩ)



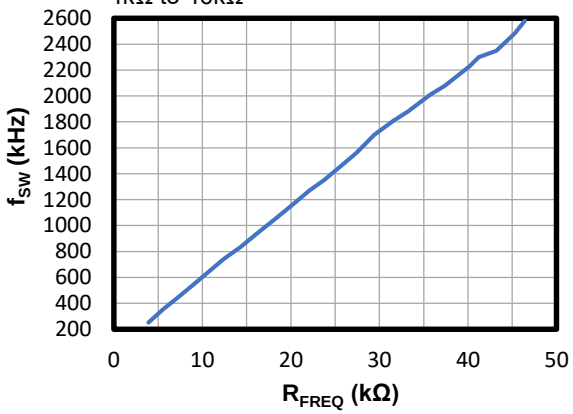
Line Regulation (Boost)
FCCM, V_{OUT} = 5V, f_{SW3} = 2MHz,
L3 = 3.3µH (DCR = 105mΩ)



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

f_{SW} vs. R_{FREQ}
4kΩ to 46kΩ

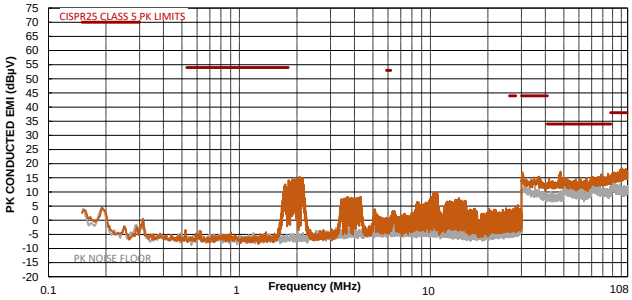


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, I_{OUT1} = 0.4A, I_{OUT2} = 1.5A, I_{OUT3} = 250mA, L1 = 2.2µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = f_{SW2} = f_{SW3} = 2MHz, T_A = 25°C, FSS cycle = 78µs, range = 25.55%, unless otherwise noted. (14)

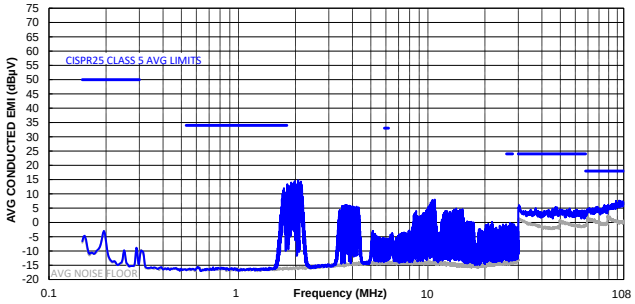
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



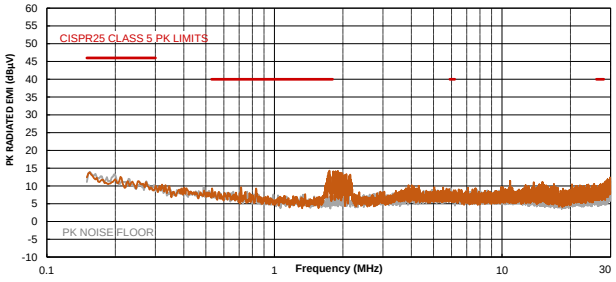
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



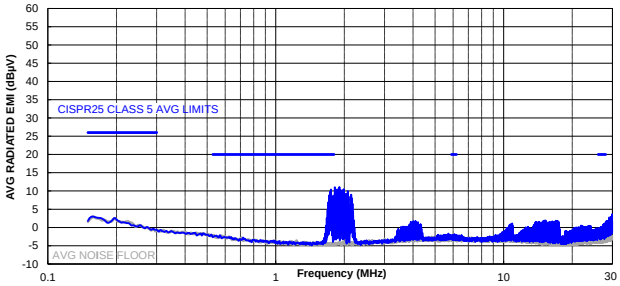
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



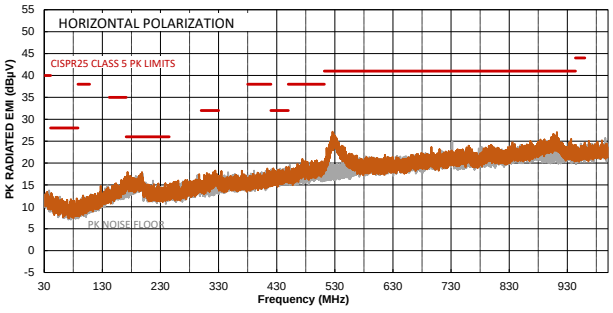
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



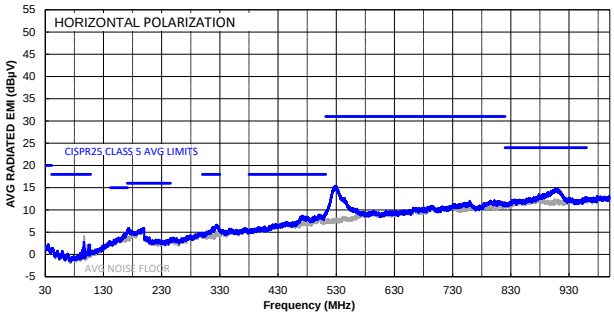
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz

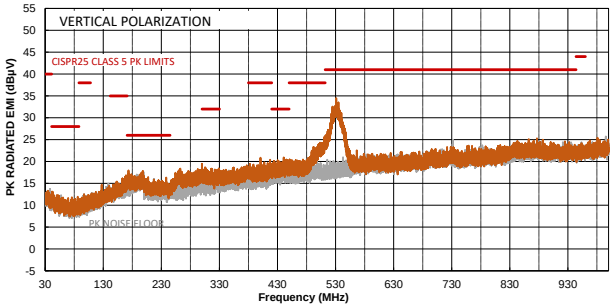


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, I_{OUT1} = 0.4A, I_{OUT2} = 1.5A, I_{OUT3} = 250mA, L1 = 2.2µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = f_{SW2} = f_{SW3} = 2MHz, T_A = 25°C, FSS cycle = 78µs, range = 25.55%, unless otherwise noted. (14)

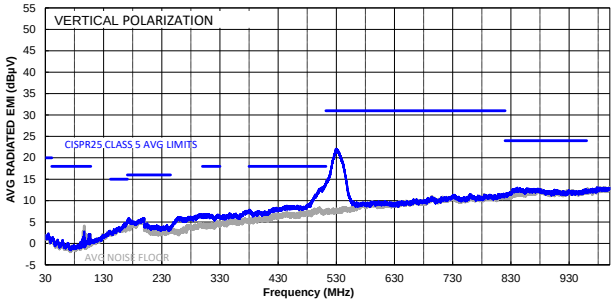
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Note:

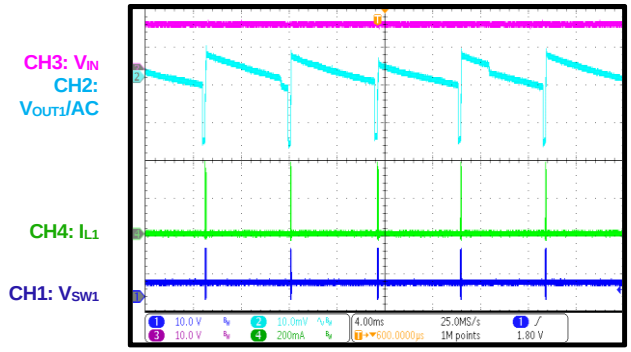
14) The EMC test results are based on the typical application circuit with EMI filters (see Figure 24).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

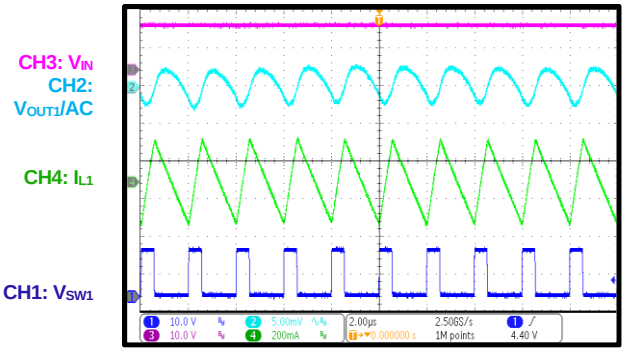
Steady State (HV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A, FCCM



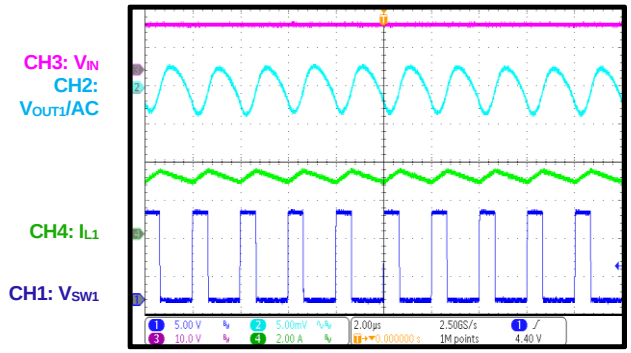
Steady State (HV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A, FCCM



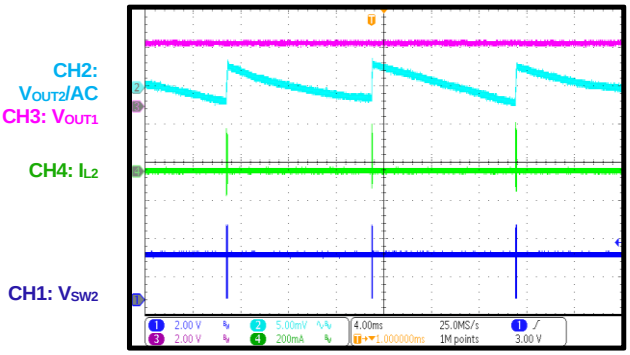
Steady State (HV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



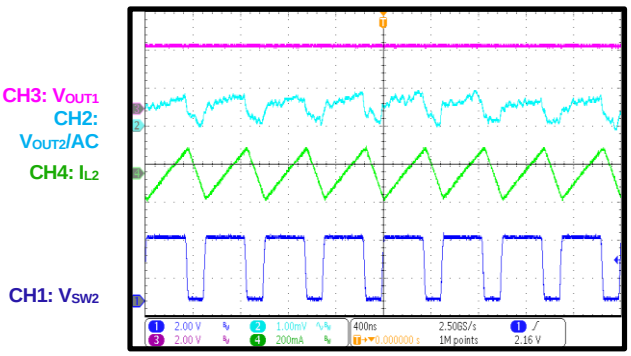
Steady State (LV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A, AAM mode



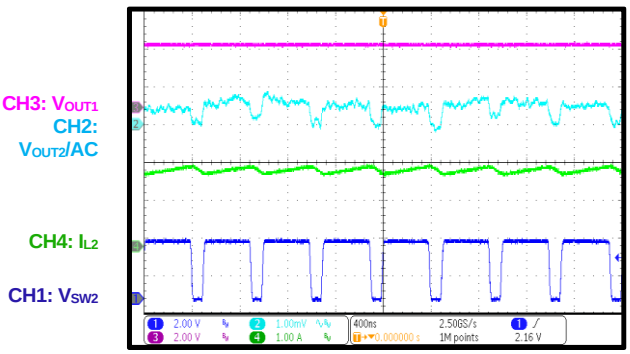
Steady State (LV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A, FCCM



Steady State (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA

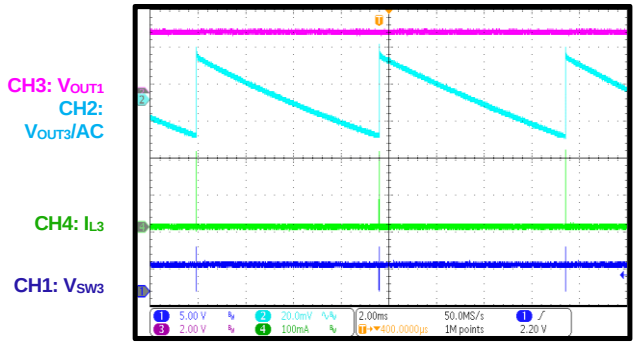


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

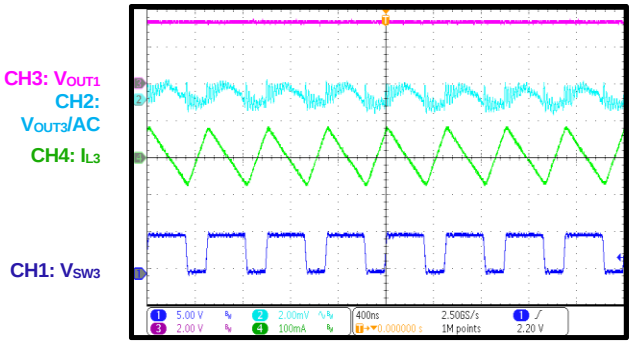
Steady State (Boost)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A, AAM mode



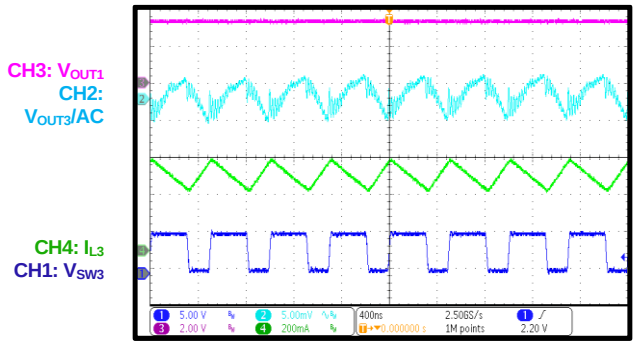
Steady State (Boost)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A, FCCM



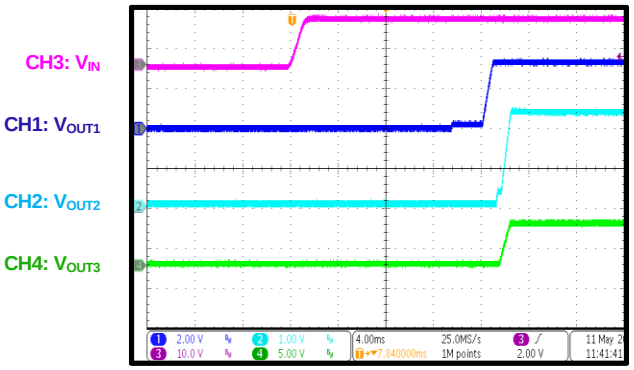
Steady State (Boost)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



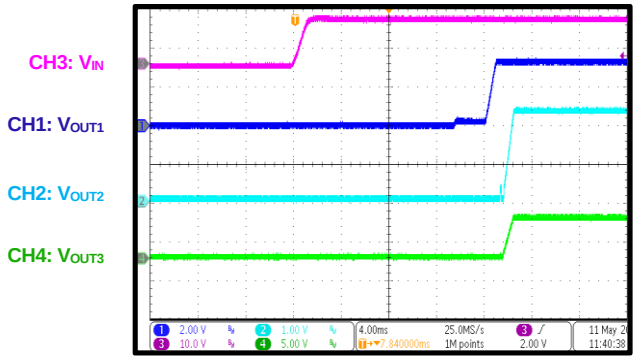
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



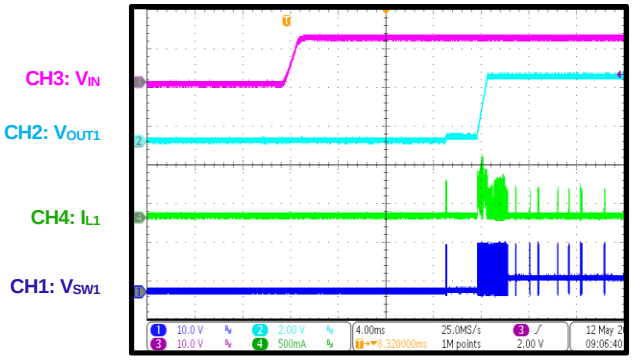
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



Start-Up through VIN (HV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A

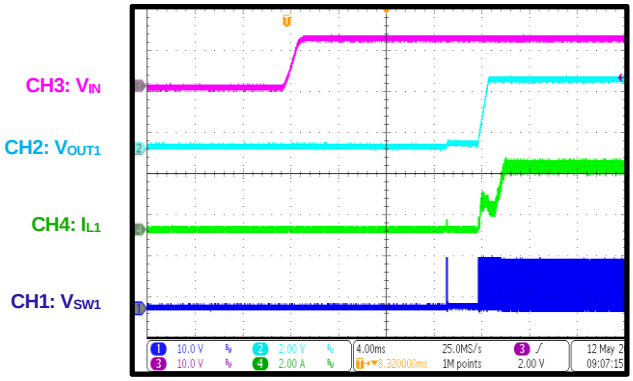


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

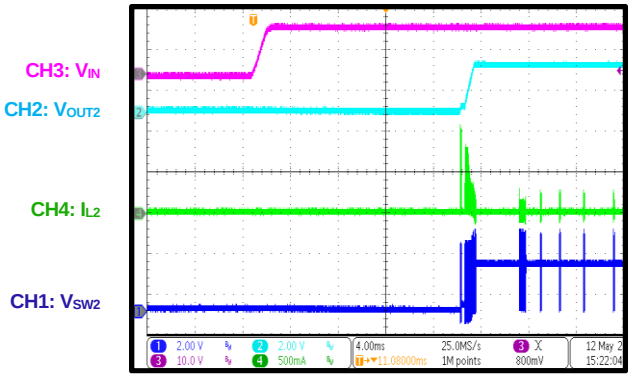
Start-Up through VIN (HV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



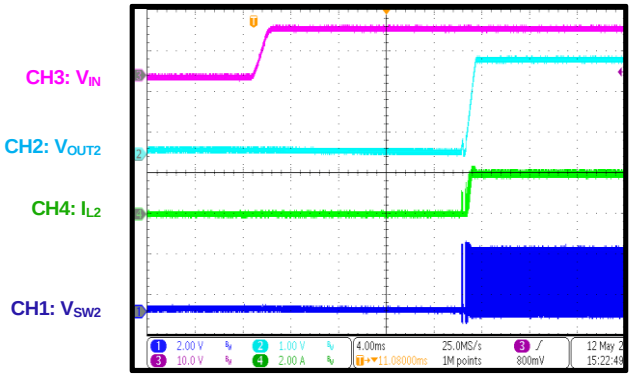
Start-Up through VIN (LV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



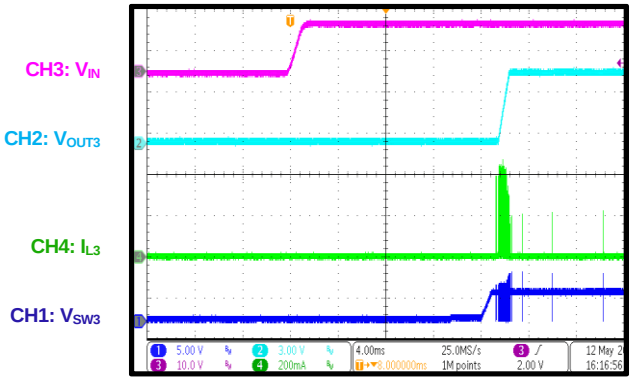
Start-Up through VIN (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



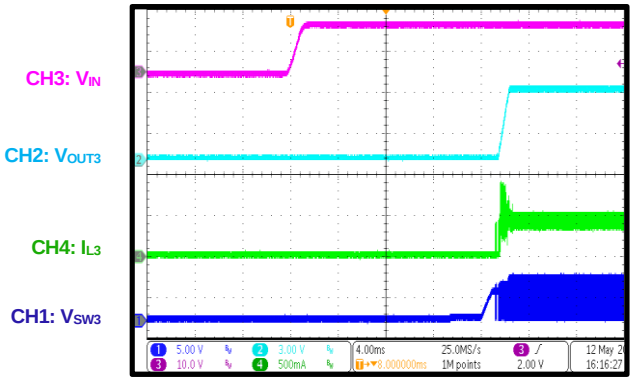
Start-Up through VIN (Boost)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



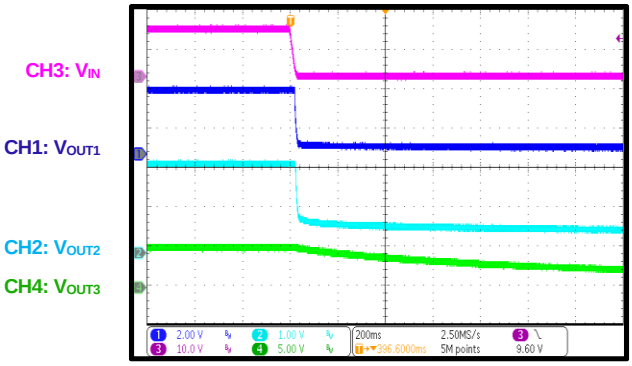
Start-Up through VIN (Boost)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



Shutdown through VIN (Shutdown Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A

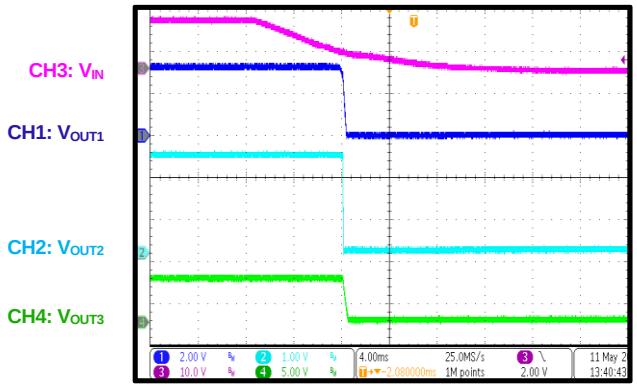


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

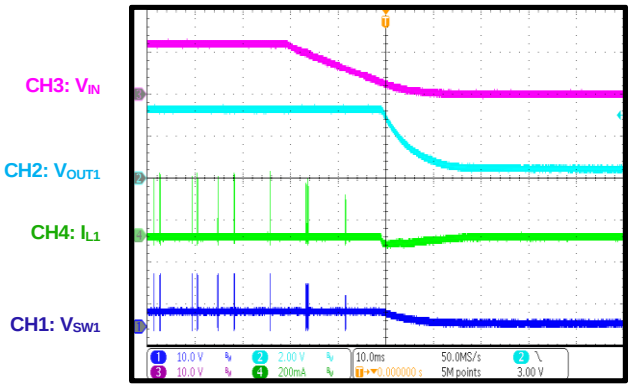
Shutdown through VIN (Shutdown Sequence)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



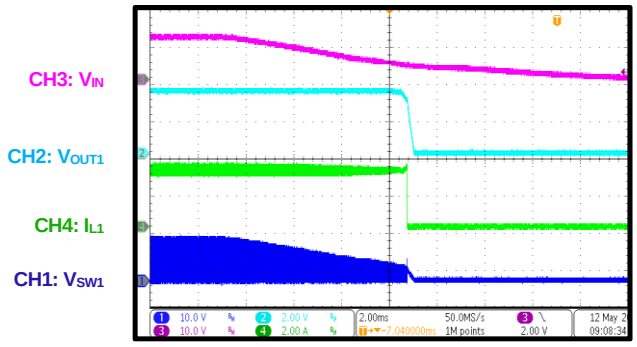
Shutdown through VIN (HV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



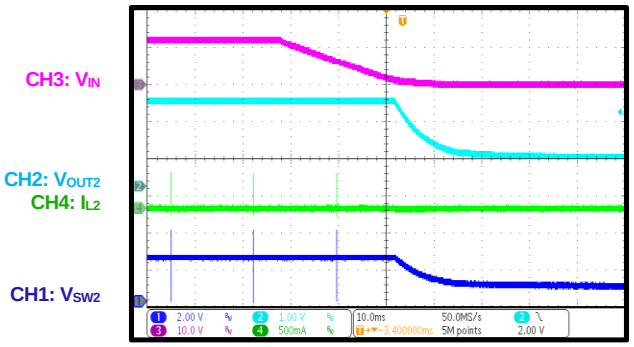
Shutdown through VIN (HV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



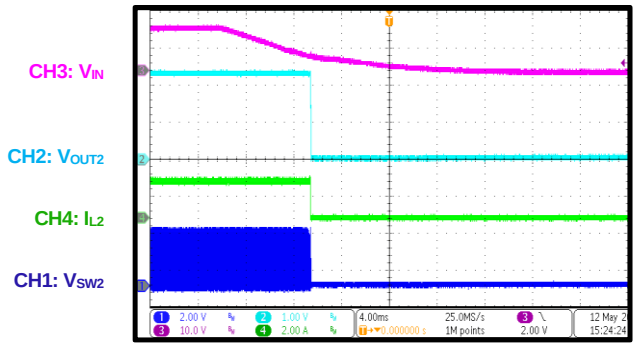
Shutdown through VIN (LV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



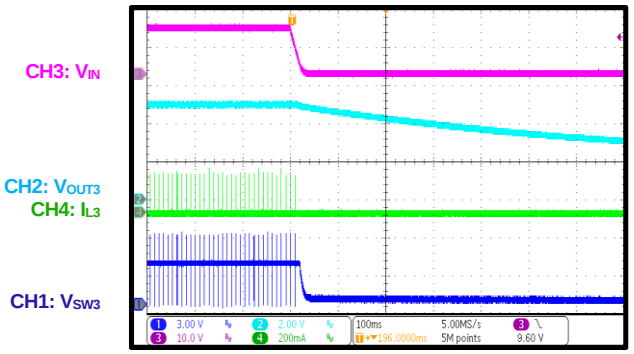
Shutdown through VIN (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



Shutdown through VIN (Boost)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A

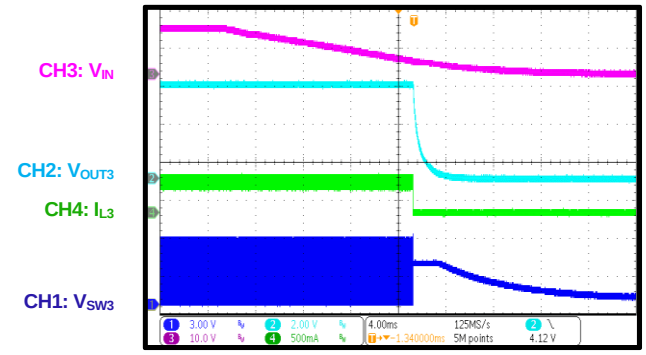


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

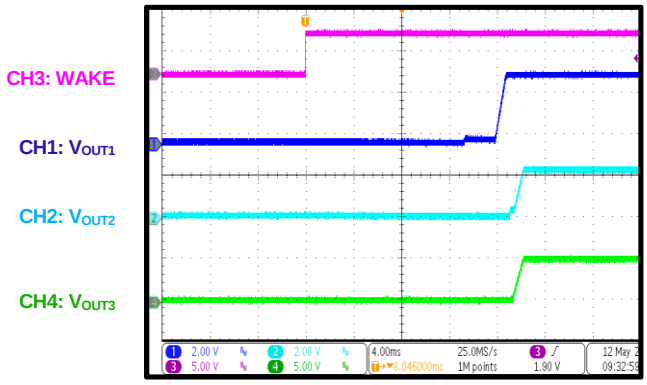
Shutdown through VIN (Boost)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



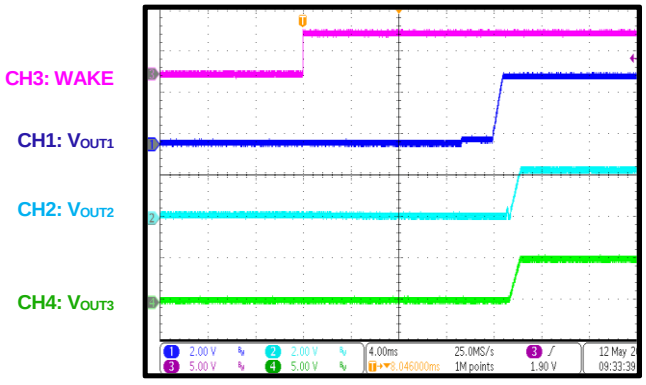
Start-Up through WAKE (Start-Up Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



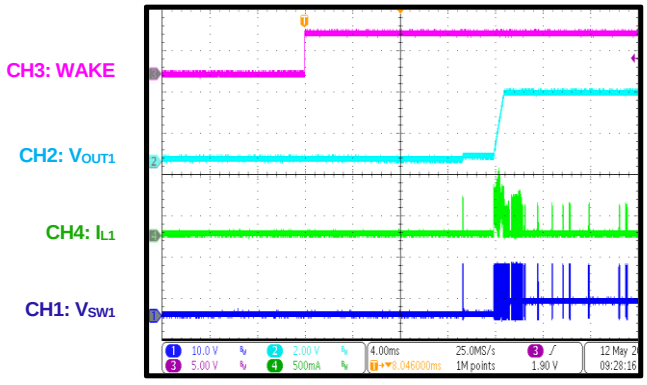
Start-Up through WAKE (Start-Up Sequence)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



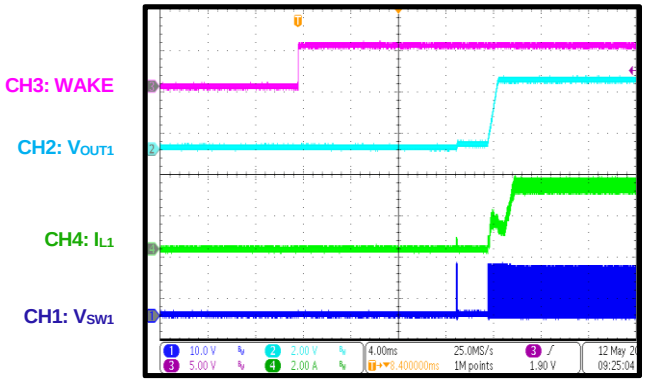
Start-Up through WAKE (HV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



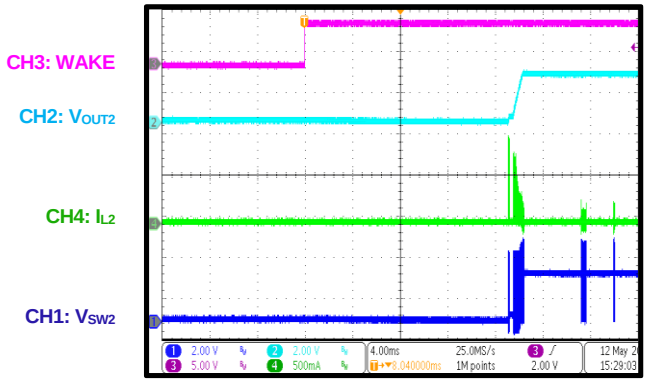
Start-Up through WAKE (HV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



Start-Up through WAKE (LV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A

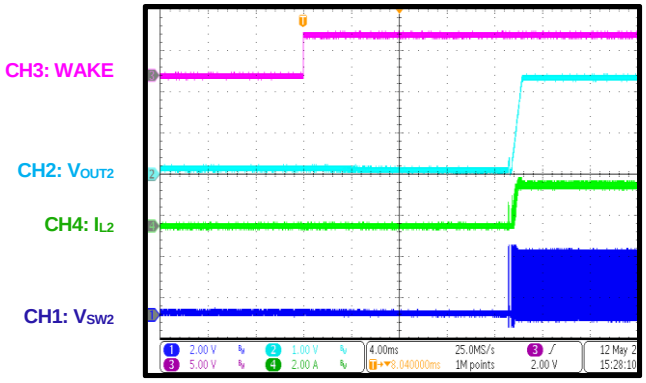


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

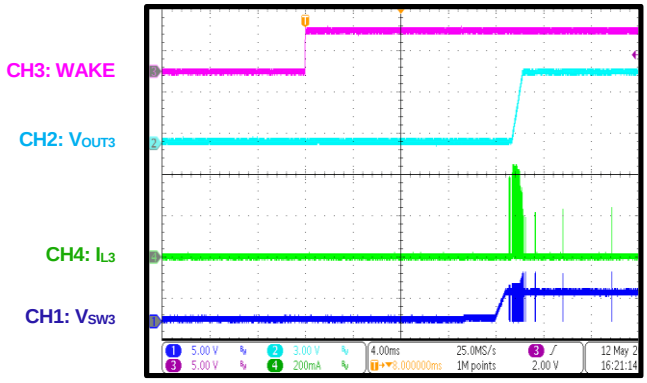
Start-Up through WAKE (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



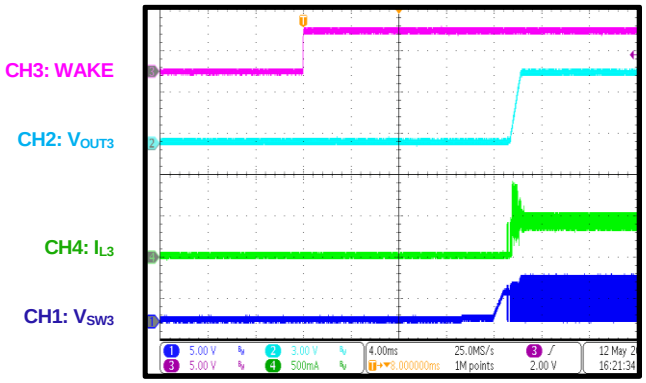
Start-Up through WAKE (Boost)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



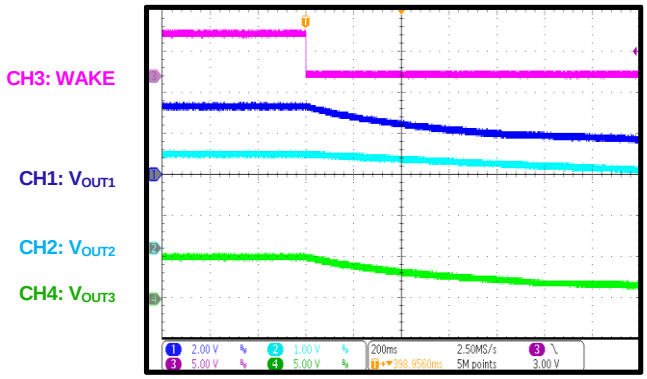
Start-Up through WAKE (Boost)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



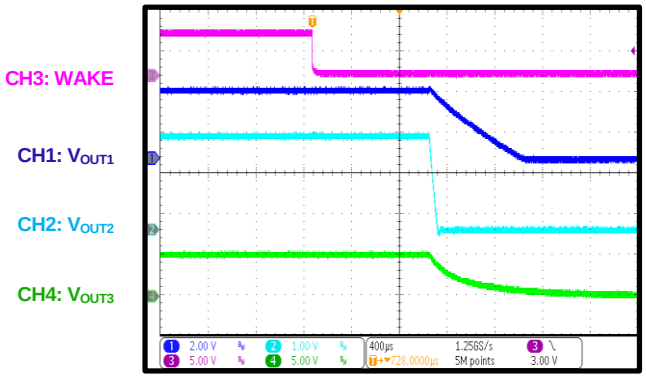
Shutdown through WAKE (Shutdown Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



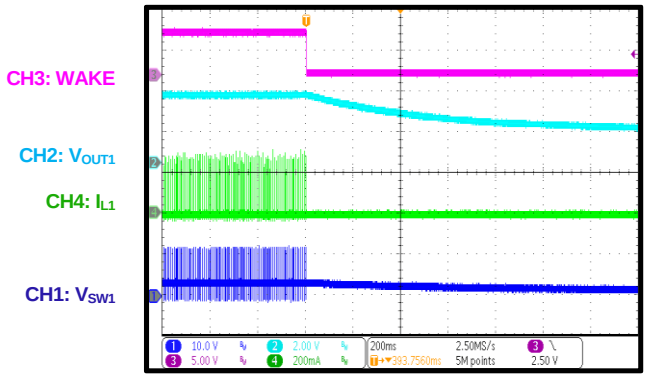
Shutdown through WAKE (Shutdown Sequence)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



Shutdown through WAKE (HV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A

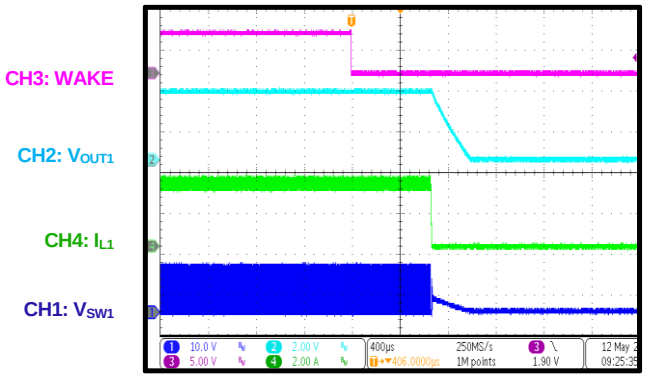


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

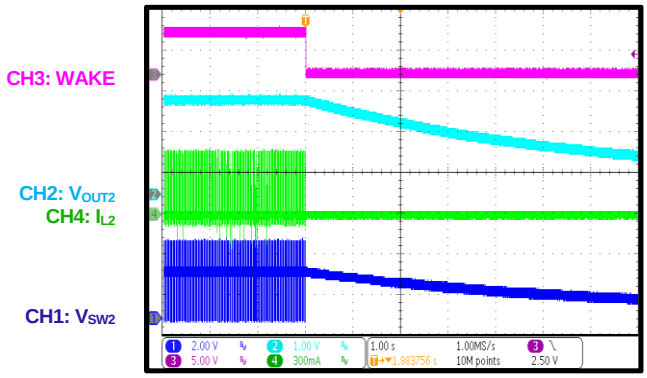
Shutdown through WAKE (HV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



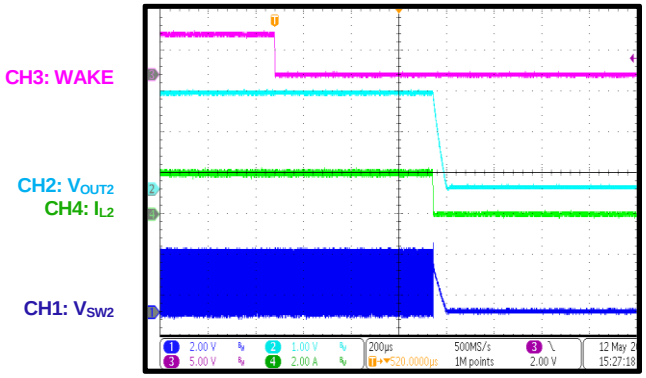
Shutdown through WAKE (LV Buck)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A



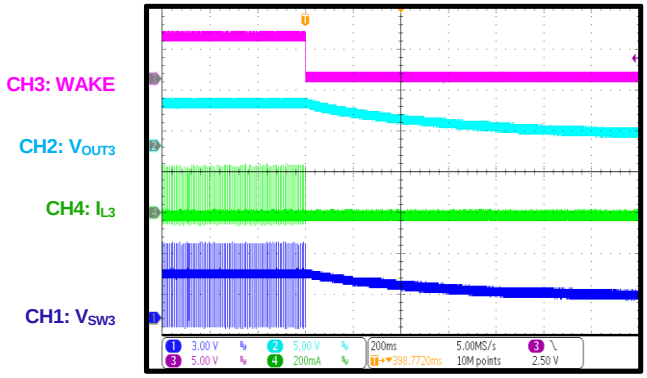
Shutdown through WAKE (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



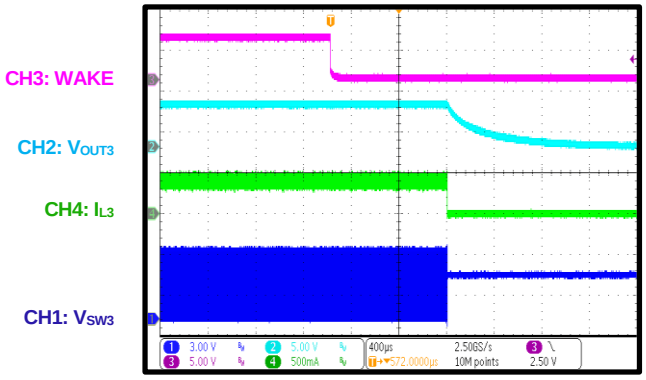
Shutdown through WAKE (Boost)

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A

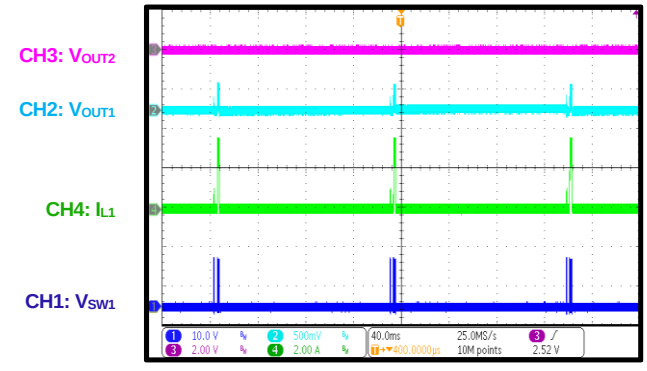


Start-Up through WAKE (Boost)

I_{OUT1} = 400mA, I_{OUT2} = 1.5A, I_{OUT3} = 250mA



SCP Steady State (HV Buck)

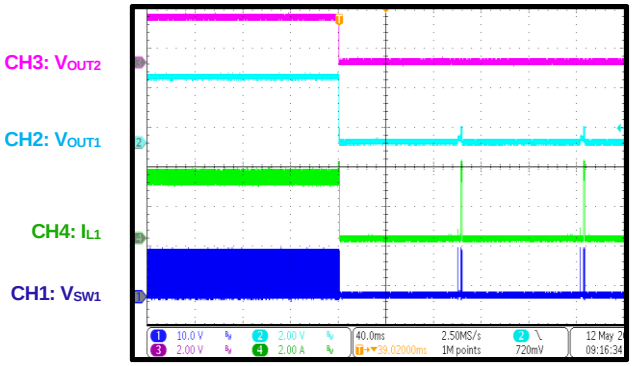


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

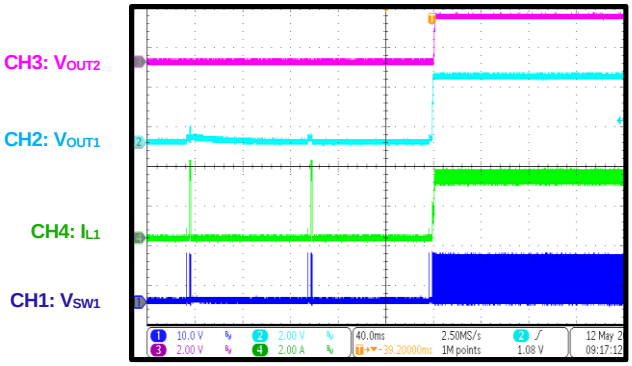
SCP Entry (HV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA

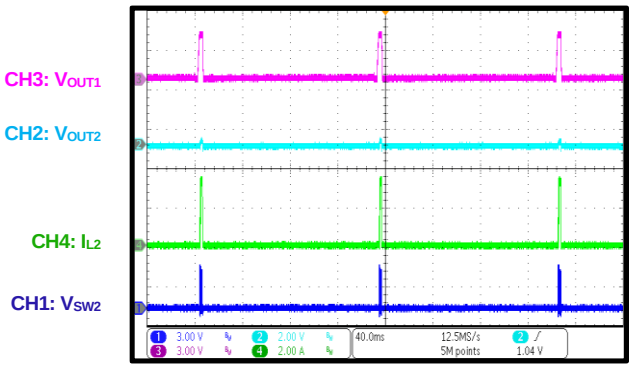


SCP Recovery (HV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA

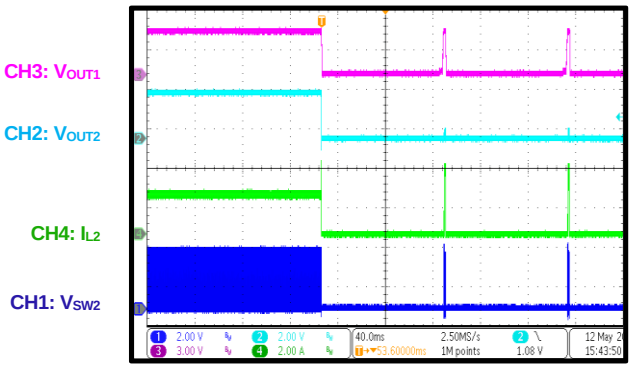


SCP Steady State (LV Buck)



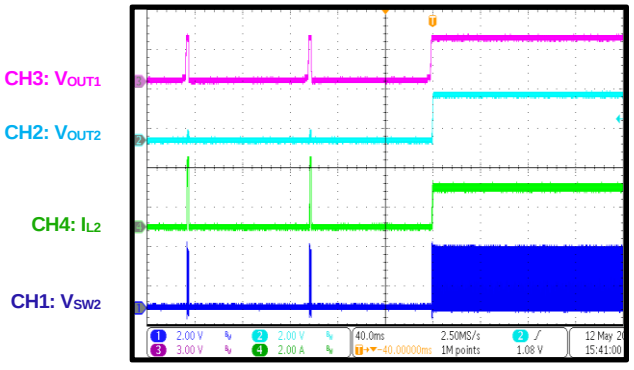
SCP Entry (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA

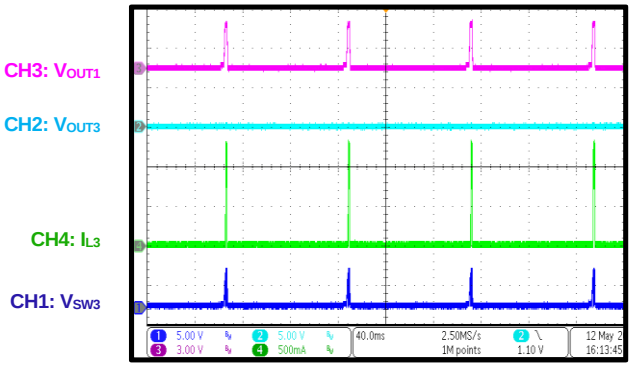


SCP Recovery (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



SCP Steady State (Boost)

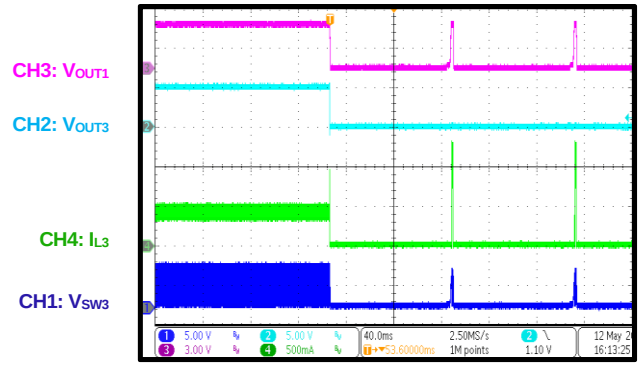


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

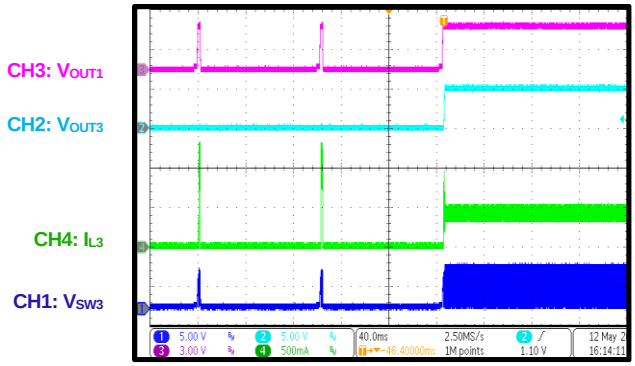
SCP Entry (Boost)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



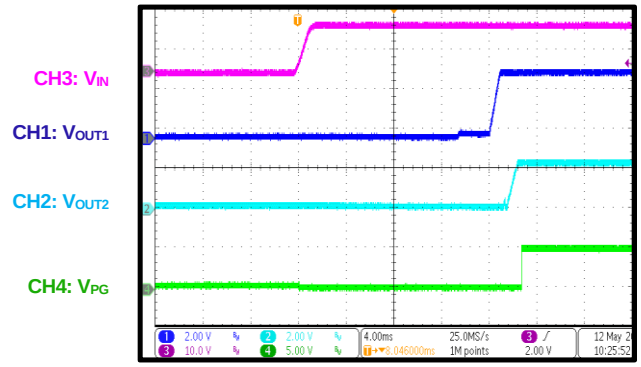
SCP Recovery (Boost)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



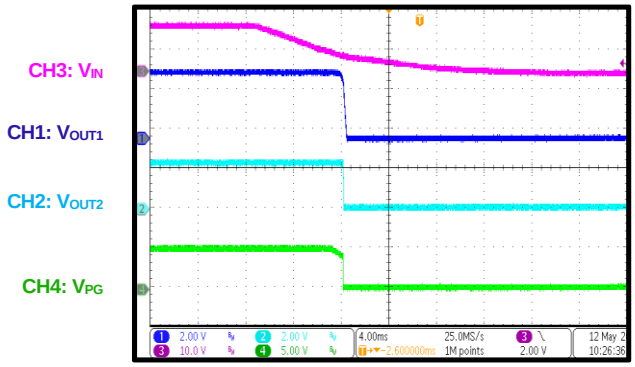
PG in Start-Up through VIN

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



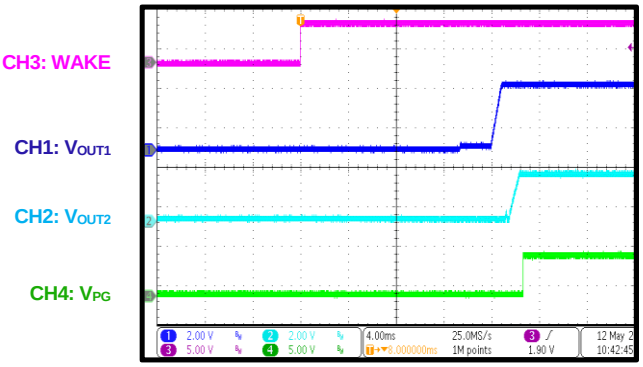
PG in Shutdown through VIN

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



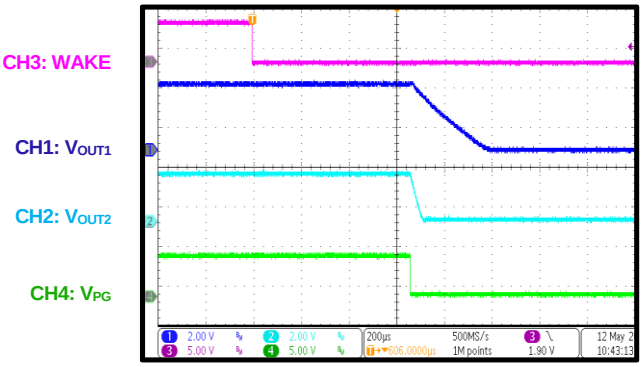
PG in Start-Up through WAKE

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



PG in Shutdown through WAKE

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA

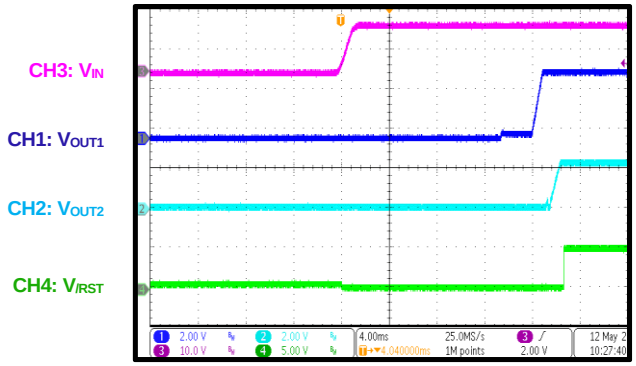


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

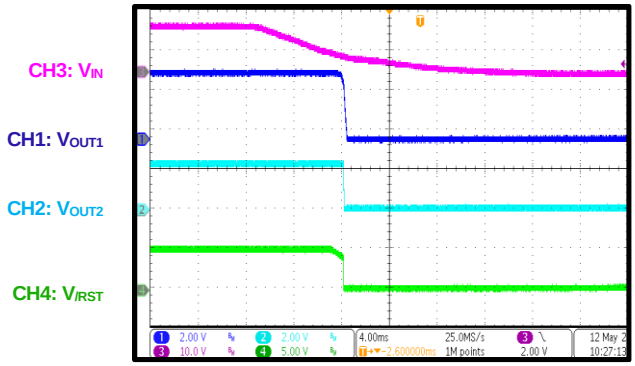
/RST in Start-Up through VIN

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



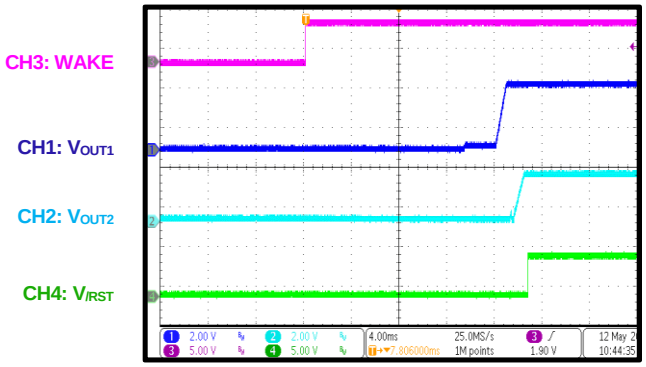
/RST in Shutdown through VIN

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



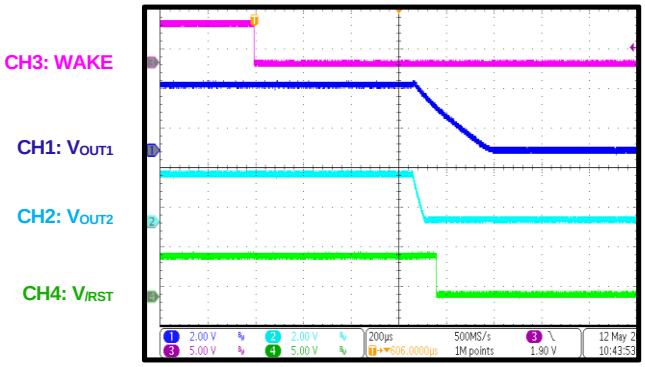
/RST in Start-Up through WAKE

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



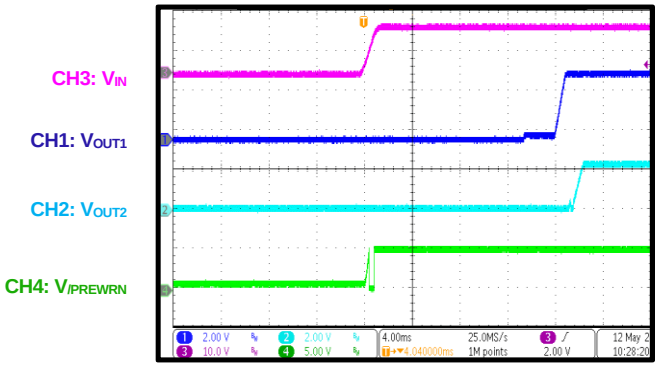
/RST in Shutdown through WAKE

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



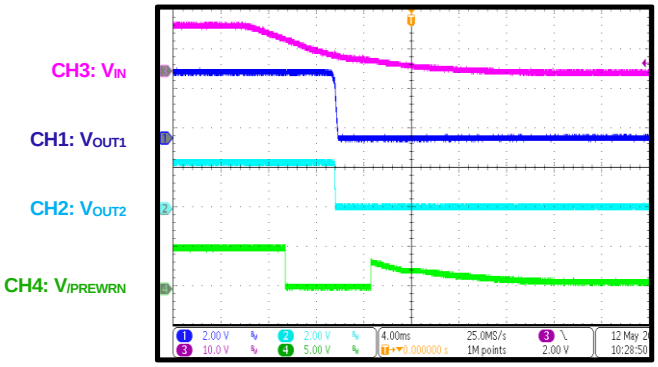
/PREWRN in Start-Up through VIN

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



/PREWRN in Shutdown through VIN

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA

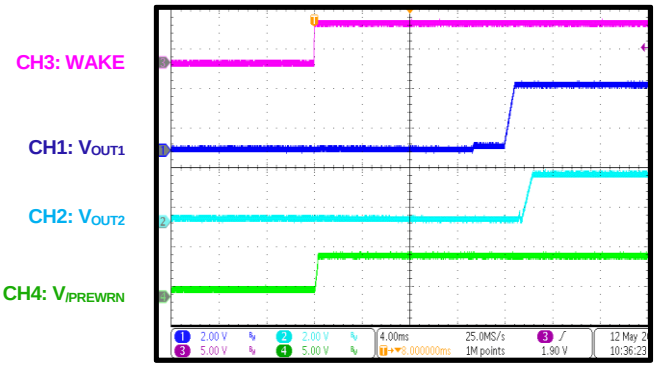


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

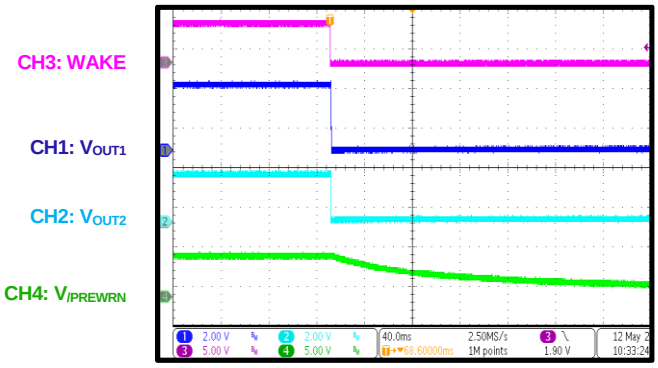
/PREWRN in Start-Up through WAKE

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



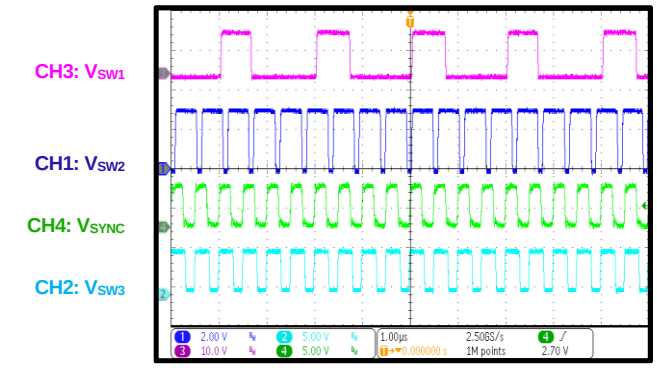
/PREWRN in Shutdown through WAKE

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA



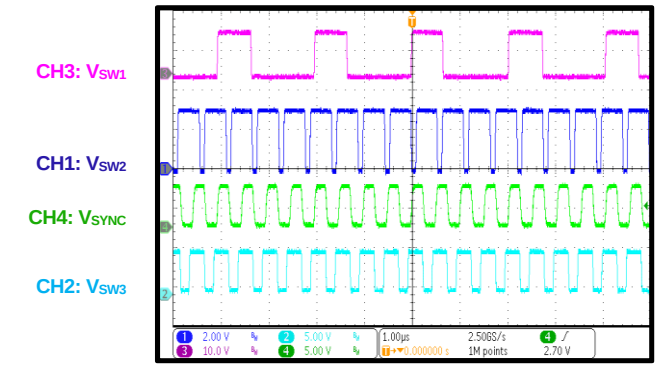
SYNCIN Operation

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA, SYNC frequency = 2MHz, HV buck: LV buck = 1:4



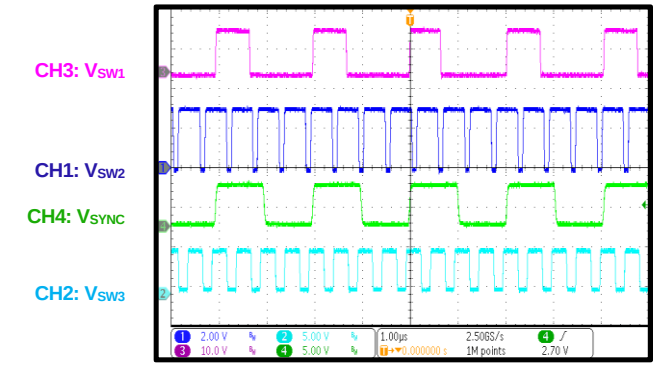
SYNCOUT Operation

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA, SYNCOUT LV buck frequency



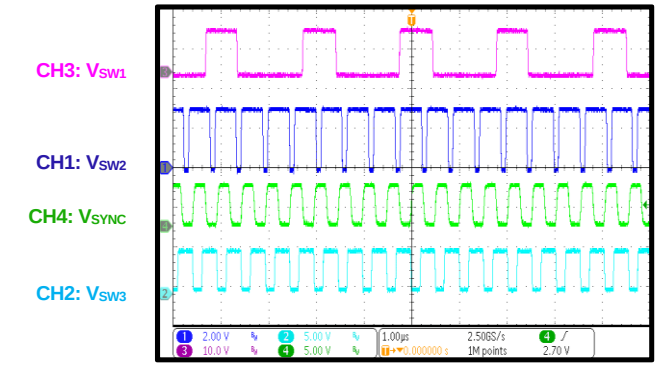
SYNCOUT Operation

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA, SYNCOUT HV buck frequency



SYNCOUT Operation

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 250mA, SYNCOUT LV boost frequency

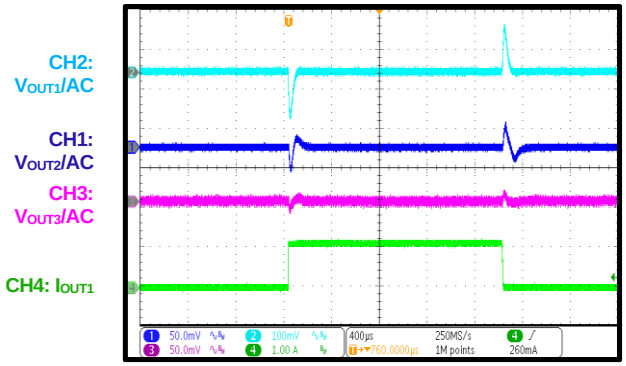


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

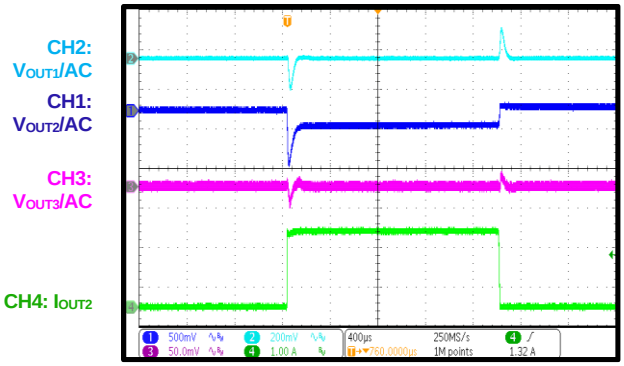
Load Transient (HV Buck)

I_{OUT1} = 0A to 3A, I_{OUT2} = I_{OUT3} = 0A



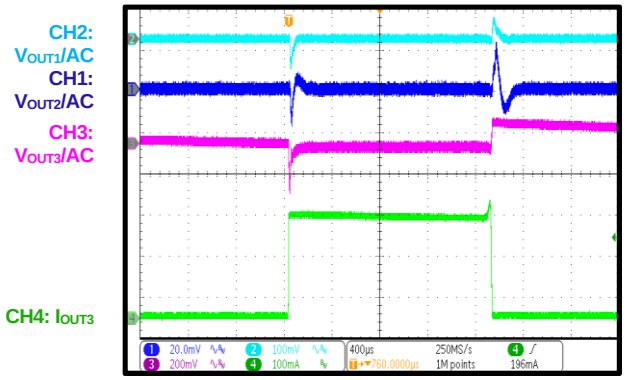
Load Transient (LV Buck)

I_{OUT1} = 1A, I_{OUT2} = 0A to 2A, I_{OUT3} = 250mA



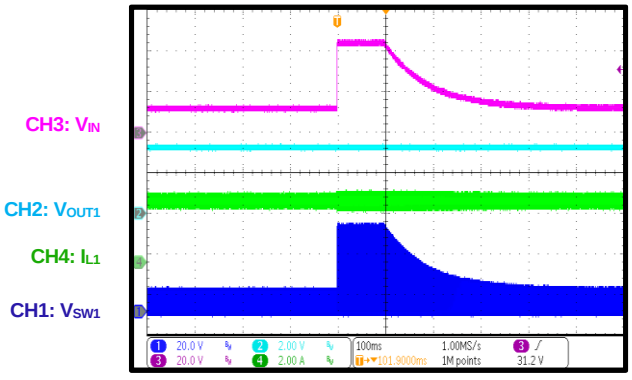
Load Transient (Boost)

I_{OUT1} = 1A, I_{OUT2} = 2A, I_{OUT3} = 0A to 250mA



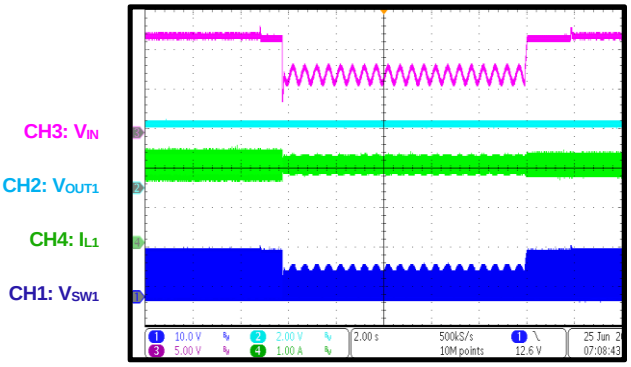
Load Dump

V_{IN} = 12V to 45V, I_{OUT1} = 2A, I_{OUT2} = I_{OUT3} = 0A



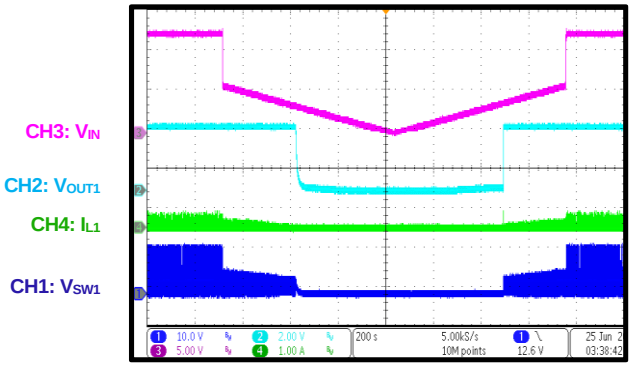
Cold Crank

V_{IN} = 12V to 4.5V to 6.5V, I_{OUT1} = 2A,
I_{OUT2} = I_{OUT3} = 0A



V_{IN} Ramping Down and Up

I_{OUT1} = I_{OUT2} = I_{OUT3} = 0A, AAM mode

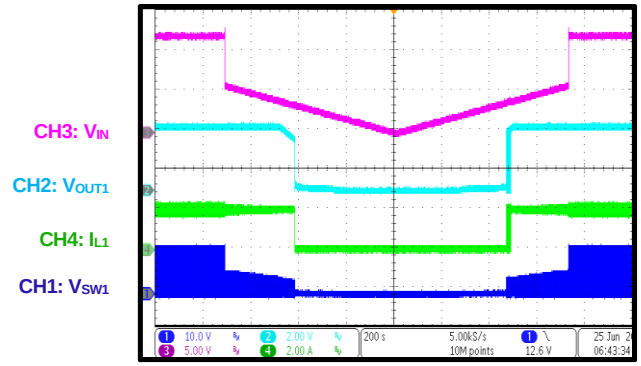


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, L1 = 10µH, L2 = 1µH, L3 = 3.3µH, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

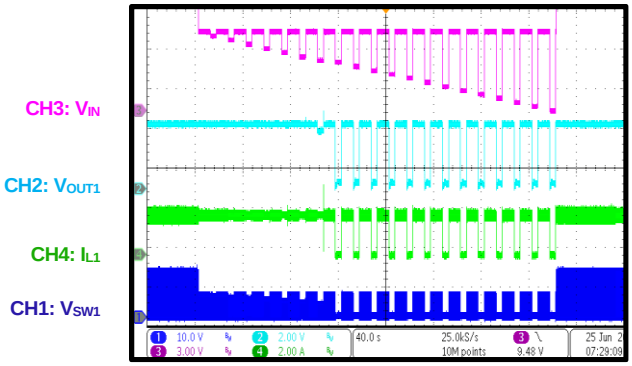
V_{IN} Ramping Down and Up

I_{OUT1} = 2A, I_{OUT2} = I_{OUT3} = 0A



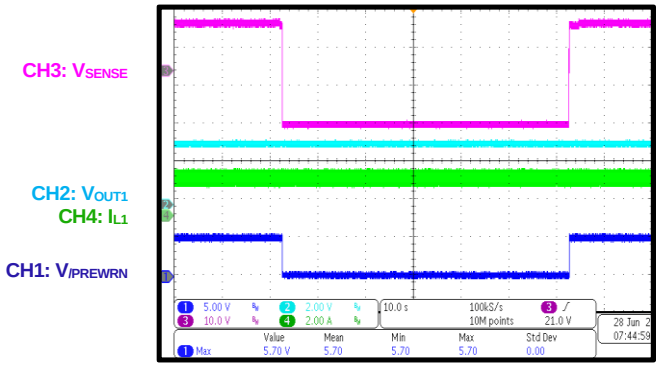
Reset Behavior

I_{OUT1} = 2A, I_{OUT2} = I_{OUT3} = 0A



Reversed Voltage

I_{OUT1} = 2A, I_{OUT2} = I_{OUT3} = 0A



FUNCTIONAL BLOCK DIAGRAM

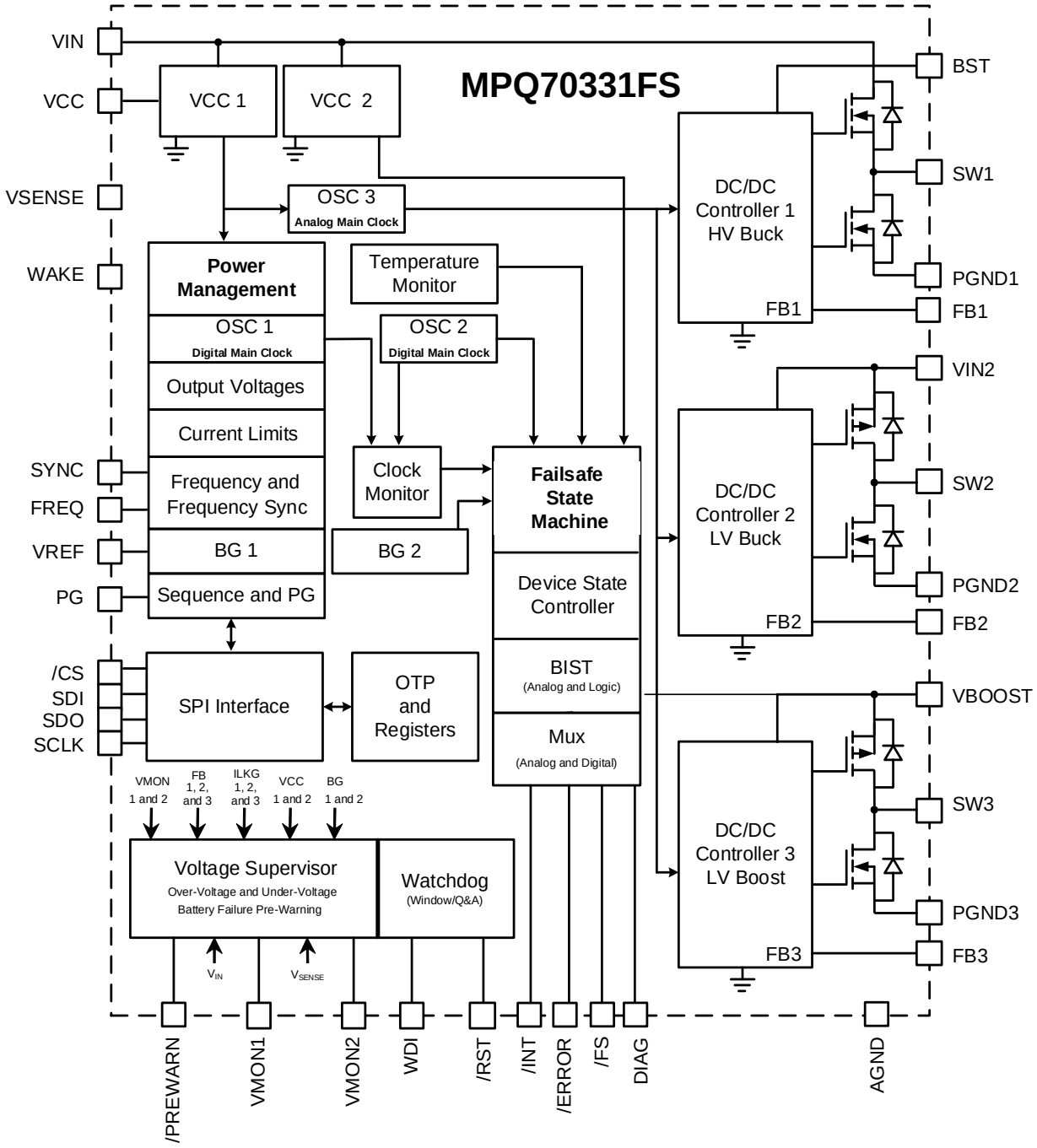


Figure 2: Functional Block Diagram

OPERATION

FUNCTIONAL BLOCK DESCRIPTION

High-Voltage (HV) Buck Converter

The high-voltage (HV) voltage regulator is a step-down, synchronous buck converter with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It operates in peak current control mode. The regulated output voltage (V_{OUT1}) has a nominal voltage of 3.3V and can be configured between 2.3V and 5.45V (50mV steps) without external resistors. The voltage accuracy is ±1.5% across the full temperature and battery supply range. It achieves up to 3A of continuous output current (I_{OUT}).

Low-Voltage (LV) Buck Converter

The low-voltage (LV) regulator is a step-down, synchronous buck converter with a 2.3V to 5.5V input voltage (V_{IN}) range, which should be supplied by the HV buck converter. An HS-FET and LS-FET are integrated into the device. The LV buck converter also operates in peak current control mode to regulate the output voltage (V_{OUT2}). The nominal V_{OUT2} is 2.3V, and it can be configured between 0.6V and 3.75V (50mV steps) without external resistors. The voltage accuracy is ±1.5%. Its maximum I_{OUT} is 2A.

Low-Voltage Boost Converter

The low-voltage, step-up, synchronous boost converter with an integrated HS-FET and LS-FET can be used to power a CAN transceiver or other safety-critical sensors. Its V_{IN} range is also 2.3V to 5.5V, which is supplied by the HV buck converter. Its output voltage (V_{OUT3}) can be configured between 4.5V and 7.5V (50mV steps) without external resistors. The voltage accuracy is ±2% across the full temperature and battery supply range. Its maximum I_{OUT} is 250mA.

The stability of the overall converters is achieved via an internal configurable compensation network. The high-voltage buck (HVBK), low-voltage buck (LVBK), and low-voltage boost (LVBT) output voltages are monitored by the voltage monitoring function. If an over-voltage (OV) or under-voltage (UV) condition is detected, the regulator switches off. The default OV and UV thresholds are ±4% of the preset output voltage with a 1% internal hysteresis. The threshold and hysteresis values can be configured via the SPI interface. Any failure is reported by the dedicated register, and generates an interrupt signal and forces the application into a failsafe state (all regulators are off by default) depending on the supervisory circuit configuration.

Light-Load Operation

To improve converter efficiency and avoid any unwanted V_{OUTx} increases, all three regulators can operate in advanced asynchronous modulation (AAM) mode during light-load conditions. If the load is light enough and the internal COMP voltage (V_{COMP}) drops below the set value, the internal clock resets. Once the inductor current (I_L) approaches 0A, switching turns off. When the load increases and V_{COMP} exceeds the set value, the device operates in discontinuous conduction mode (DCM) or forced continuous conduction mode (FCCM), both of which have a constant switching frequency (f_{SW}). The AAM mode threshold and mode selection can be configured via the SPI interface.

When the regulator operates in FCCM, the device works with a fixed frequency from no-load to full-load conditions. The advantages of FCCM are its controllable frequency and lower output ripple under light loads.

Frequency Setting

All three regulators share the same internal oscillator. f_{SW} can be set up to 2.5MHz, with a fixed frequency ratio between the HV and LV buck converters. The frequency ratio between the HV and LV buck converters can be set via the SPI interface. The ratio options are 1:1, 1:2, and 1:4. The LV boost converter's f_{SW} always follows the LV buck converter's f_{SW}.

Since the HV and LV buck converters have no phase shift to the internal main clock, a 180° phase shift is applied between the boost converter and internal main clock to improve EMC/EMI performance.

In addition to being configurable via the SPI interface, f_{SW} can also be set by an external resistor connected to the FREQ pin. It is recommended to use a 1% accuracy resistor to obtain the main frequency.

Ensure that the minimum on time is not triggered for each channel to avoid output OV conditions, especially in high-frequency applications.

SYNCIN and SYNCOUT

External input/output synchronization is available. The SYNC pin can be configured via the SPI interface. When the SYNC pin is set to SYNCIN, the internal LVBK's internal switching frequency can be synchronized by an external clock via this pin. The HVBK and LVBT switching frequency also refers to this frequency, with a ratio set via register FREQ_CTRL_1, bits[7:6]. For more details, see the Frequency Setting section on page 39. When the SYNC pin is set to SYNCOUT, the MPQ70331FS can output one of the three regulators' f_{SW}.

Oscillator (OSC)

Two 8MHz internal oscillators (OSC 1 and OSC 2) are dedicated to the digital blocks. They are identical but independent. The regulators' switching frequencies are determined by the independent analog oscillator.

VCC Regulator

A 5V internal VCC regulator (VCC1) powers most of the internal circuitries. This regulator takes V_{IN} and operates across the full V_{IN} range. When V_{IN} exceeds 5V, the regulator's output is in full regulation. Lower V_{IN} values result in lower output voltages. Once V_{IN} exceeds its under-voltage lockout (UVLO) threshold, the regulator is enabled. A second VCC regulator (VCC2) is used for powering safety-related blocks. VCC2 is identical but independent from VCC1.

Bandgap Reference

The main bandgap reference (bandgap reference 1) is used for non-safety power stages. There is a buffered voltage reference pin (VREF) for this internal bandgap reference to cross-check the analog-to-digital (A/D) internal reference in the microcontroller (MCU). A second bandgap reference (bandgap reference 2) is used for UV/OV monitoring and the other safety-related blocks to ensure that any drifts in bandgap reference 1 are detected. Bandgap reference 2 is independent of bandgap reference 1.

Configurable Watchdog

The MPQ70331FS implements a configurable watchdog with a window and question and answer (Q&A) operating modes. The watchdog monitors the external MCU's proper functioning. The MCU indicates normal operation by periodically sending signals to the watchdog.

In window mode, the watchdog must receive a trigger within a defined time window to generate a "good event" if window mode is selected. If the MCU fails to send a trigger or a trigger is not sent within the timing window, a "bad event" is generated. The external MCU sends the watchdog trigger by asserting the WDI input pin for an open-close window scheme configuration.

In Q&A mode, the watchdog provides a question to the MCU. The MCU performs a fixed series of arithmetic operations on the question to calculate the required answer. The MCU writes these answer bytes through the SPI, 1 byte at a time, to the dedicated register. The MPQ70331FS verifies that the MCU returned the answer bytes within the specified timing window and that the answer bytes are correct. When the MCU sends the correct answer bytes calculated for the current question within the correct watchdog window and in the correct order, a "good event" is generated. If any of these conditions are not met, a "bad event" is generated.

The watchdog configuration is controlled by the WD_CFG bit in the SAFETY_FUNC_CFG_1 register. The default configuration is a windowed scheme with an external MCU trigger driven through the WDI pin. A certain number of "bad events" causes the watchdog to reset the external MCU by asserting the /RST pin low. In addition to internal voltage-monitoring functions, this is one of the MCU's reset sources.

Voltage Supervisor

A voltage supervisor monitors the battery supply voltage, all regulator rails, and internally generated voltages. The corresponding register status flag bits indicate whether a UV or OV condition has occurred. UV and OV comparators perform the monitoring. The bandgap 2 reference voltage for the voltage supervisor module is independent of the system reference voltage (bandgap 1) used by the regulators.

A glitch-filtering function ensures reliable monitoring without a false setting of the status flag bits. A separate VCC2 voltage (V_{CC2}) supplies the complete voltage supervisor block.

Analog built-in self-testing (ABIST) covers voltage supervisor comparator diagnostics, which are executed during device start-up or activated by an external MCU SPI request.

Emulation of each monitored voltage rail for a UV or OV condition on the corresponding comparator inputs forces the corresponding comparator to toggle multiple times.

Battery Under-Voltage Pre-Warning Indicator

The /PREWRN pin integrates an open-drain structure internally. Connect /PREWRN to a voltage source through an external pull-up resistor to act as a battery UV indicator. Connect the VSENSE pin directly to the battery line. If the VSENSE voltage (V_{SENSE}) falls below the VSNS_UV_THR threshold, set by register UV_CTRL_3, bits[3:1], then /PREWRN is pulled down to indicate a battery UV warning.

Over-Current Protection (OCP)

For the two bucks and one boost converter, the MPQ70331FS provides a peak/valley current limit scheme designed to limit the peak/valley inductor current and ensure that the switching currents remain within the device capabilities during overload conditions or during an output short circuit.

The chip monitors the increased I_L through the relevant operating main MOSFET. If the peak I_L exceeds the peak current limit threshold, the main MOSFET turns off immediately, and the other MOSFET turns on to conduct and decrease I_L. The operating main MOSFET does not turn on again until I_L returns to below the valley current limit threshold.

Below conditions will trigger the device from MAIN DIAGNOSTIC or Normal state into START-UP state: High-voltage Buck OC and current across valley current limit for more than 16 times; Boost OC and current across valley current limit for more than16 times; The output voltage of Boost is lower than the PG3_LOW_THR.

Clock Monitoring

Clock monitoring detects possible failures of the two 8MHz clocks, including a stack-at fault, the clock being stuck high or stuck low, or the clock running too fast or too slowly. It remains active during normal operation. This monitor has its own ABIST structure.

Frequency Spread Spectrum (FSS)

To further optimize EMI performance, the MPQ70331FS features frequency spread spectrum (FSS) (see Figure 3).

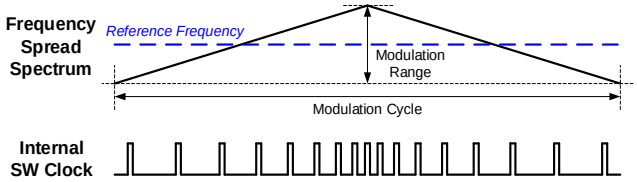


Figure 3: Frequency Spread Spectrum

The reference frequency FSS modulation range is set via the SPI interface. Once FSS is enabled, the triangular frequency modulation mode is used to vary f_{SW} between the same ratio above and below the reference. f_{SW} varies from the lowest to the highest, then drops back to the lowest across a single modulation cycle. See the FREQ_CTRL_3 (0x2B) section on page 84 for detailed modulation cycle and range information.

Temperature Monitoring

The MPQ70331FS features over-temperature protection (OTP) provided by an internal temperature monitor. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature (T_J) exceeds the threshold (default 175°C), the entire chip shuts down. This is non-latch protection, and there is a default 25°C hysteresis. Once T_J drops to about 150°C, the device initiates a soft start and resumes normal operation.

Power Good (PG) Indicator

The PG pin is connected to the open drain of an internal MOSFET. PG should be connected to a voltage source via an external pull-up resistor to act as the power good indicator. The PG pin is pulled down to ground during soft start, or if V_{OUTx} is not within the allowable window. If V_{OUTx} is in regulation, then the PG MOSFET turns off and the PG pin is pulled high to indicate a good output status. There is a delay time of about 60µs if the PG status flip-flops.

Failsafe State Machine

To fulfill safety-critical applications, the MPQ70331FS integrates a dedicated failsafe state machine. All of the safety-relevant signals feed the failsafe state machine, which manages error handling and controls the failsafe outputs.

The failsafe state machine is electrically independent of the rest of the circuitry to avoid common cause failures.

SPI Interface

The MPQ70331FS is controlled via a 16-bit SPI interface. The configuration and the diagnosis results are handled via the SPI registers. For the MPQ70331FS's SPI register mapping information, see the Serial Peripheral Interface section on page 61.

BUILT-IN SELF-TESTING (BIST)

The MPQ70331FS provides built-in self-testing (BIST) for critical analog and logic functions.

Analog Built-In Self-Testing (ABIST)

The goal of ABIST is to verify that the diagnostic circuits (e.g. the voltage supervisor) are operating correctly and increase the detection of latent faults.

ABIST typically involves exercising diagnostic circuits into and out of fault scenarios by injecting currents or voltages into the diagnostic circuit. This process ensures that the diagnostic circuit (e.g. UV and OV monitoring, current limit protection, and thermal protection circuits) can switch to both fault and non-fault states. In other words, it is an analog circuit controlled by a digital circuit that verifies the correct functionality of analog safety mechanisms.

While ABIST is performing:

1. The /RST pin cannot assert. Resets caused by the assertion of /RST due to any trigger event that is part of the logic affected by ABIST control are blocked.
2. The state machine cannot transition. The state machine does not change its state or react based on detected emulated faults.
3. The output rails cannot change. All voltages remain enabled regardless of any out-of-range detection caused by ABIST itself.

ABIST tests the following items:

- The UV and OV comparators in the voltage supervisor
- Oscillators and clock monitor
- Stuck-at fault test output pins

Logic Built-In Self-Testing (LBIST)

The goal of logic built-in self-testing (LBIST) is to check the bit error of the OTP register and combinatorial/sequential logic blocks.

LBIST tests the following items:

- Memory cyclic redundancy check (CRC) (registers)
- One-time programmable (OTP) memory content check, including trim bits (CRC protection)
- On-demand diagnosis initiated by the external MCU (ON_DEMAND_DIAG = 1)
- SPI interface and communication testing
- Diagnostic output mux interconnection check
- Other customized tests

Scan Logic Built-In Self-Testing (Scan LBIST)

The MPQ70331FS's full digital core is checked by a scan LBIST. Scan LBIST test vectors are applied to the digital core to verify the correct functionality. If scan LBIST fails, the MPQ70331FS remains in DEEP SAFE and the /INT pin pulls low.

STATE MACHINE DESCRIPTION

The state machine describes the different states of operation. The device has 11 states: POWER OFF, SCAN LBIST, RESTORE OTP, DEEP SAFE, PRE-DIAGNOSTIC, START-UP, MAIN DIAGNOSTIC, NORMAL, RESET, STORE USER, and RESTORE USER.

The different states are shown in register DEV_STAT, bits[7:4]. The bits indicating the current state are updated when entering a new state. Each state is described below and represented in the state diagram (see Figure 4). Table 1 also lists the device functions for each state.

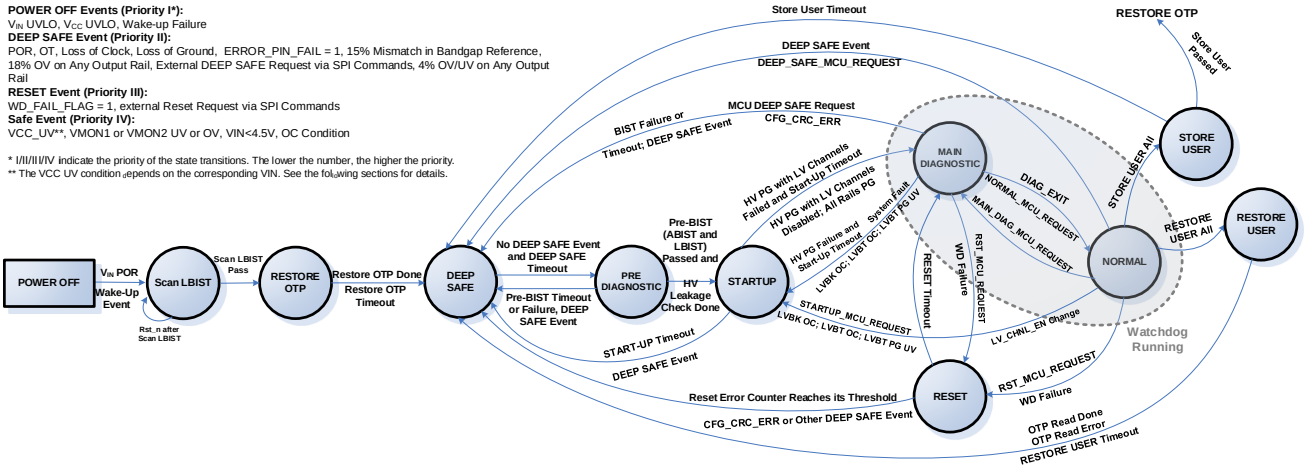


Figure 4: Operating State Diagram

Table 1: MPQ70331FS Device Function Table

Functions	MPQ70331FS States										
	POWER OFF	Scan LBIST	RESTORE OTP	DEEP SAFE	PRE-DIAGNOSTIC	START-UP	MAIN DIAGNOSTIC	NORMAL	RESET	STORE USER	RESTORE USER
Wake-Up Circuitry	Off	On	On	On	On	On	On	On	On	On	On
Internal VCC1 Regulator	Off	On	On	On	On	On	On	On	On	On	On
Internal VCC2 Regulator	Off	On	On	On	On	On	On	On	On	On	On
Voltage Supervisor	Off	Off	Off	On	On	On	On	On	On	On	On
HV Sync Buck	Off	Off	Off	Off	Off	On	On	On	On	Off	Off
LV Sync Buck	Off	Off	Off	Off	Off	On	On	On	On	Off	Off
Sync Boost	Off	Off	Off	Off	Off	On	On	On	On	Off	Off
SPI	Off	Off	Off	On	On	On	On	On	On	Off	Off
Watchdog	Off	Off	Off	Off	Off	Off	On	On	On	Off	Off
Diagnostics Output Mux	Off	Off	Off	Off	Off	Off	On	On	On	Off	Off
MCU Reset Pin (/RST)	Tri-state	Low	Low	Low	Low	Low	High	High	Low	Low	Low
Failsafe Output (/FS)	Tri-state	Low	Low	Low	Low	Low	According to WD and some faults	According to WD and some faults	Low	Low	Low

Power Off State (POWER OFF)

The MPQ70331FS remains in POWER OFF as long the power-on-reset (POR) is not released. Table 2 shows the POWER OFF state settings.

Table 2: POWER OFF State Settings

Functions	Value	Description
Wake-Up Circuitry	Off	The wake-up circuitry is off
VCC1	Off	The internal VCC1 regulator is off
VCC2	Off	The internal VCC2 regulator is off
Voltage Supervisor	Off	The voltage supervisor is off
HV Buck	Off	The HV sync buck is off
LV Buck	Off	The LV sync buck is off
LV Boost	Off	The sync boost is off
SPI	Off	The SPI is off
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Tri-state	The reset is in a high-impedance (Hi-Z) state
/FS	Tri-state	The failsafe is in a Hi-Z state

Scan LBIST State (SCAN LBIST)

When V_{IN} exceeds its rising UVLO threshold, POR is released and a valid wake-up event forces the MPQ70331FS into the SCAN LBIST state. A scan LBIST is performed, and then the device transitions to the RESTORE OTP state. Table 3 shows the SCAN LBIST state settings.

Restore OTP State (RESTORE OTP)

The MPQ70331FS restores the register configuration from embedded OTP content data. Once restoration is complete, the MPQ70331FS automatically enters the DEEP SAFE state. Table 4 shows the RESTORE OTP state settings.

Deep Safe State (DEEP SAFE)

DEEP SAFE is the MPQ70331FS's default state after OTP restoration completes, which reduces the overall current drawn from the battery to the minimum needed to react to state transitions. All output rails are disabled in DEEP SAFE. /FS drives low to disable the peripheral circuits, and /RST to the external MCU is also driven low.

Table 3: SCAN LBIST State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	Off	The voltage supervisor is off
HV Buck	Off	The HV sync buck is off
LV Buck	Off	The LV sync buck is off
LV Boost	Off	The sync boost is off
SPI	Off	The SPI is off
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

Table 4: RESTORE OTP State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	Off	The voltage supervisor is off
HV Buck	Off	The HV sync buck is off
LV Buck	Off	The LV sync buck is off
LV Boost	Off	The sync boost is off
SPI	Off	The SPI is off
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

There are multiple reasons that the device may enter DEEP SAFE. Every state has unique trigger events that result in a transition to DEEP SAFE. These trigger events are listed in the state diagram (see Figure 4 on page 43). These triggers are also demonstrated in the following sections. In addition, the device automatically enters DEEP SAFE regardless of the current state if any of the following events occur:

- POR
- Over-temperature (OT) condition
- Main clock (CLK1 or CLK2) fails
- PGND open
- Request from the /ERROR pin
- OV or UV condition at any output rail (default 104% OV, 96% UV)
- Destructive OV condition on any output rail (default 18% OV)
- 15% mismatch in bandgap references
- Request from the dedicated SPI commands that set register SAFETY_CHECK_CTRL_2, bit[3]

Table 5 shows the DEEP SAFE state settings.

Table 5: DEEP SAFE State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	Off	The HV sync buck is off
LV Buck	Off	The LV sync buck is off
LV Boost	Off	The sync boost is off
SPI	On	The SPI is on
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

DEEP SAFE brings the system to a known safe status after a critical failure occurs by turning off all the output rails. The /FS pin automatically asserts low to deactivate the peripheral circuits. The device remains in DEEP SAFE for a set wait time (100ms by default) to avoid any fast toggling behavior. This wait time can be configured by register SAFETY_ERR_CFG_2, bits[7:5]. All wake sources are masked during this time. Once the wait time expires, the MPQ70331FS automatically transitions to the PRE-DIAGNOSTIC state. Note that during power up, the time in the deep safe state is 1ms.

For debugging purposes, there is a small delay before the MPQ70331FS transitions to DEEP SAFE and shuts down the MCU. The MCU can read and store the fault code(s) from the INTERRUPT register before shutdown.

The voltage supervisor is activated when the MPQ70331FS enters DEEP SAFE.

Pre-Diagnostic State (PRE-DIAGNOSTIC)

In the pre-diagnostic state (PRE-DIAGNOSTIC), power-on diagnosis is performed before the output rails ramp up.

The pre-diagnosis includes the following items, as well as ABIST and LBIST:

- OTP content check, including trimming bits (CRC protection)
- Memory CRC (registers)
- Checking the leakage current of every internal power MOSFET
- Functionality check of the interrupt pin (/INT), MCU reset pin (/RST), and failsafe output pin (/FS) to prevent them from being stuck in a particular state due to a pin fault

Table 6 shows the PRE-DIAGNOSTIC state settings.

Table 6: PRE-DIAGNOSTIC State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	Off	The HV sync buck is off
LV Buck	Off	The LV sync buck is off
LV Boost	Off	The sync boost is off
SPI	On	The SPI is on
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

If the MPQ70331FS fails to finish a pre-diagnosis within a set time, the device enters DEEP SAFE.

The pre-diagnostic timeout is configured via SAFETY_ERR_CFG_1, bits[7:6].

Start-Up State (START-UP)

Once the pre-diagnostic state is passed and the voltage supervisor is fully active, the device enters the start-up state (START-UP). In START-UP, all other power supplies are enabled and start to ramp up.

If any deep safe trigger events occur or the device fails to reach PG within the configured time window, the MPQ70331FS enters DEEP SAFE. The START-UP timeout is configured via SAFETY_ERR_CFG_1, bits[1:0]. Ensure all that channels finish starting up before the START-UP timeout is triggered.

Table 7 shows the START-UP state settings.

Table 7: START-UP State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	On	The HV sync buck is on
LV Buck	On	The LV sync buck is on
LV Boost	On	The sync boost is on
SPI	On	The SPI is on
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

Main Diagnostic State (MAIN DIAGNOSTIC)

The MPQ70331FS enters the main diagnostic state (MAIN DIAGNOSTIC) once every output regulator voltage is power good. The /RST pin is then released, allowing the MCU and other devices in the system to begin their start-up sequence. The watchdog starts to run, and can only be reconfigured in the main diagnostic state.

Upon entering MAIN DIAGNOSTIC, the watchdog error counter bits in register WDT_STATUS_2, bits[2:0] are reinitialized. The diagnostic output mux and SPI engine are fully activated, and the /FS pin is released.

Table 8 shows the MAIN DIAGNOSTIC state settings.

Table 8: MAIN DIAGNOSTIC State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	On	The HV sync buck is on
LV Buck	On	The LV sync buck is on
LV Boost	On	The sync boost is on
SPI	On	The SPI is on
Watchdog	On	The watchdog is on
DIAG	On	The diagnostic output mux is on
/RST	High	The reset output is high
/FS	According to WD and some faults	The watchdog reset counter and some faults determine the failsafe output

MAIN DIAGNOSTIC performs BIST and any other on-demand diagnoses initiated by the external MCU. BIST consists of ABIST for analog functions and LBIST for logic functions.

If BIST fails to finish within a set time window, the device enters DEEP SAFE. The MCU should be set via SAFETY_CHECK_CTRL_2, bit[1] before the main diagnostic timeout is triggered. Only then can the MPQ70331FS enter a NORMAL state.

The main diagnostic timeout can be configured via SAFETY_ERR_CFG_1, bits[5:4]. The /ERROR pin monitoring functions can be configured and can operate during this state. Any emulated MCU error on the /ERROR pin does not trigger the device to enter DEEP SAFE. The /FS pin status is determined by the WD reset status and some faults, such as an /ERROR pin error, CFG_CRC_ERR, a reset error reaching its threshold or /RST going low for 8s, or a VMONx (VEXTx) OV or UV condition.

The following three registers are cleared every time the part enters MAIN DIAGNOSTIC:

- SAFETY_CHECK_CTRL_2 (0x0F)
- DIAG_CFG_CTRL (0x19)
- DIAG_MUX_SEL (0x1A)

Normal State (NORMAL)

The normal state (NORMAL) is the MPQ70331FS's standard operating state. The part enters this state if both the self-diagnostics and on-demand diagnostic complete before the main diagnostic timeout expires and register SAFETY_CHECK_CTRL_2, bit[1] is set by the MCU. Dedicated SPI commands can force the device back to MAIN DIAGNOSTIC. Table 9 shows the NORMAL state settings.

Table 9: NORMAL State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	On	The HV sync buck is on
LV Buck	On	The LV sync buck is on
LV Boost	On	The sync boost is on
SPI	On	The SPI is on
Watchdog	On	The watchdog is on
DIAG	On	The diagnostic output mux is on
/RST	High	The reset output is high
/FS	According to WD and some faults	The watchdog reset counter and some faults determine the failsafe output

During this state, all output regulators are up and running. Watchdog and /ERROR pin monitoring functions operate as they were configured, but they cannot be reconfigured because the registers related to the watchdog can only configured in MAIN DIAGNOSTIC. The diagnostic mux output can only be configured via the SPI interface in NORMAL.

Reset State (RESET)

The reset state (RESET) resets the external MCU. In RESET, the /RST pin asserts low for at least the reset holding time (default 1ms), which is configured via SAFETY_ERR_CFG_1, bits[3:2].

If consecutive watchdog refresh failures occur, the watchdog error count increases. When the watchdog error count exceeds the watchdog error counter threshold, or any other active reset conditions occur, the device enters RESET. The device can only transition to RESET from MAIN DIAGNOSTIC or NORMAL if one of the following MCU reset events occurs:

- Watchdog reset: WD_RST_EN = 1 and WD_FAIL_FLAG = 1
- The external MCU requests a reset via the dedicated SPI commands set via SAFETY_CHECK_CTRL_2, bit[4]

Table 10 shows the RESET state settings.

Table 10: RESET State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	On	The HV sync buck is on
LV Buck	On	The LV sync buck is on
LV Boost	On	The sync boost is on
SPI	On	The SPI is on
Watchdog	On	The watchdog is on
DIAG	On	The diagnostic output mux is on
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

Once the reset hold time has expired, the MPQ70331FS automatically enters MAIN DIAGNOSTIC from RESET. The /RST pin is released at the transition between the two states. The reset error counter increases by 1 each time a reset is generated. The reset error counter is reduced by 1 after 6 consecutive successful watchdog refreshes.

Meanwhile, the failsafe state machine monitors the /RST pin and counts the number of resets using register SAFETY_ERR_STAT, bits[3:0]. If the reset error counter reaches its final value (stored in register SAFETY_ERR_CFG_2, bits[4:1]), or the /RST pin remains asserted low for more than 8s, the device enters DEEP SAFE.

The state transitions from NORMAL or MAIN DIAGNOSTIC after a RESET event occurs. In all transitions to RESET, the output regulator remains on.

/FS asserts low to disable the peripheral circuit and recovers once the watchdog error counter is cleared.

Store User State (STORE USER)

The store user state (STORE USER) writes the present data from the registers to the internal OTP. To initiate this process, the MCU sends a STORE_USER command to the MPQ70331FS. Then the MPQ70331FS transitions to the RESTORE OTP state and restarts. Only writing to the STORE_USER_ALL register from the NORMAL state can make the device enter STORE USER.

Table 11 shows the STORE USER state settings.

Table 11: STORE USER State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	Off	The HV sync buck is off
LV Buck	Off	The LV sync buck is off
LV Boost	Off	The sync boost is off
SPI	Off	The SPI is off
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

Restore User State (RESTORE USER)

The restore user state (RESTORE USER) copies the entire contents of the OTP memory to the matching locations in the registers. The values in the registers are overwritten by the values retrieved from the OTP. Any items in the OTP that do not have matching locations in the operating memory are ignored. To initiate this process, the MCU sends a RESTORE_USER command to the MPQ70331FS. Then the MPQ70331FS transitions to DEEP SAFE and restarts. Only writing to the RESTORE_USER_ALL register from NORMAL can make the device enter RESTORE USER. Table 12 shows the RESTORE USER state settings.

Table 12: RESTORE USER State Settings

Functions	Value	Description
Wake-Up Circuitry	On	The wake-up circuitry is on
VCC1	On	The internal VCC1 regulator is on
VCC2	On	The internal VCC2 regulator is on
Voltage Supervisor	On	The voltage supervisor is on
HV Buck	Off	The HV sync buck is off
LV Buck	Off	The LV sync buck is off
LV Boost	Off	The sync boost is off
SPI	Off	The SPI is off
Watchdog	Off	The watchdog is off
DIAG	Off	The diagnostic output mux is off
/RST	Low	The reset output is low
/FS	Low	The failsafe output is low

Fault Reaction

Faults and errors are classified in four different categories according to their severity and the device's response:

- Move to POWER OFF Events (Priority I): The most critical errors with a high risk of damaging the MPQ70331FS, MCU, and/or system (e.g. a V_{CC} hard UV condition or V_{IN} falling below POR_{VTH-F} when decreasing).
- Move to DEEP SAFE Events (Priority II): Critical errors with a high risk of damaging the MCU and/or system.
- Reset MCU Events (Priority III): Medium severity faults bring the device back to the reset state and generate a reset for the MCU.

- Safe Events (Priority IV): Minor faults without state transitions. Interruption and errors bits in the relevant register(s) assert.

These error classes can overrule one another according to their severity. For example, movement to POWER OFF takes precedence over the movement to DEEP SAFE, which takes precedence over a reset event.

WATCHDOG OPERATION

The watchdog (WD) monitors the software execution of the external MCU and sends a reset signal if the MCU stops serving the watchdog due to a lock-up in the software.

The MCU reset signal is asserted in RESET. In MAIN DIAGNOSTIC and NORMAL, the watchdog is actively running. The respective watchdog configurations can only be selected and programmed in MAIN DIAGNOSTIC. The configuration remains unchanged in any of the other states.

There MPQ70331FS offers two different watchdog configurations: window watchdog and question and answer (Q&A) watchdog. The configuration can be selected via SAFETY_FUNC_CFG_1, bit[5].

Window Watchdog Operation

Window watchdog is the MPQ70331FS's default configuration (SAFETY_FUNC_CFG_1, bit[5] = 0).

Figure 5 shows the window watchdog flowchart.

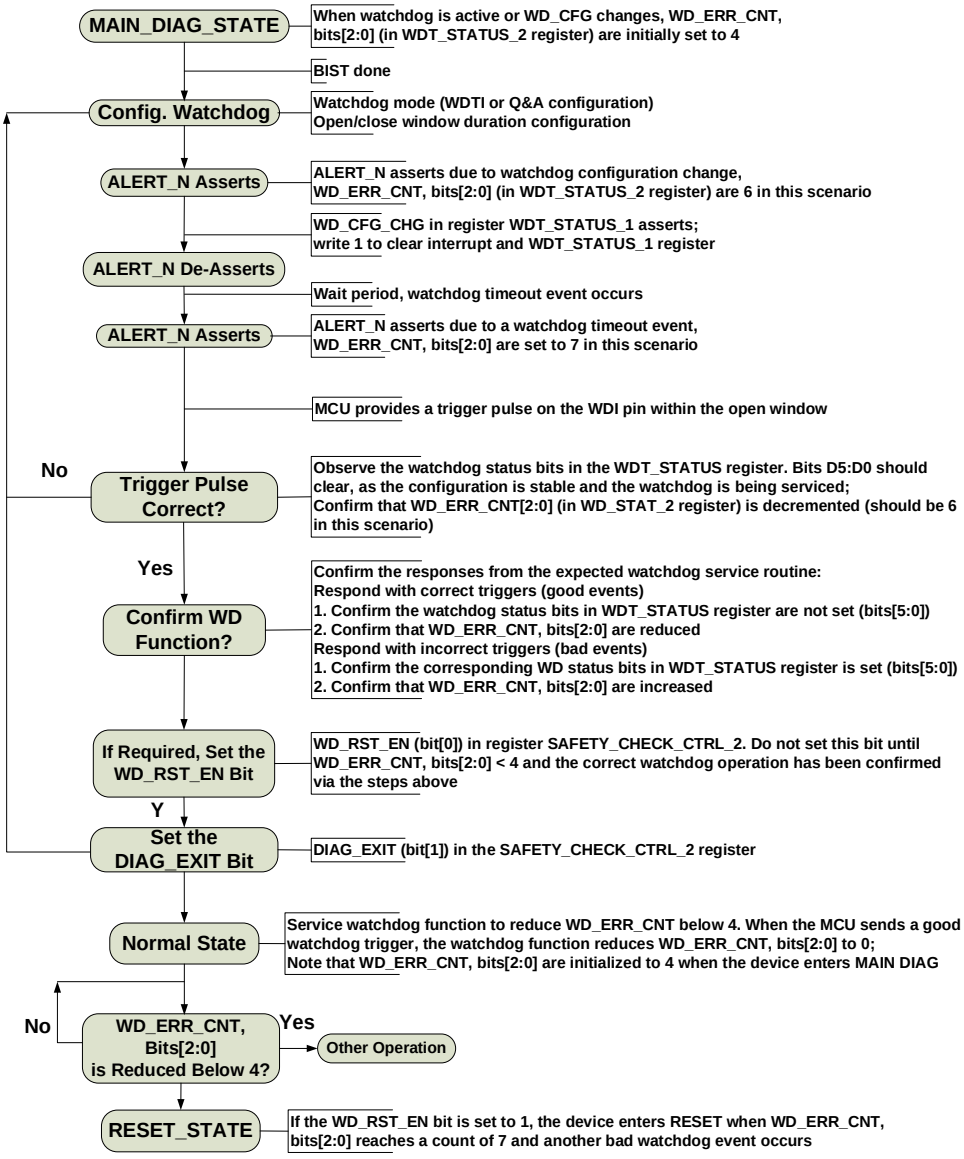


Figure 5: Window Watchdog Flowchart

The watchdog refresh is defined following the timing diagram (see Figure 6 and Figure 7).

- The MCU that is being monitored must send a periodic pulse signal to the watchdog input pin (WDI) within the “open window,” which is called a good WD refresh. Then the watchdog error counter decreases by 1.
- If a pulse is sent during the “closed window,” which is called a bad WD refreshment, then the watchdog error counter increases by 1, signaling that a potential MCU fault has occurred.

If a pulse is not sent, which is called a WD timeout, then WDT_STATUS_1, bit[1] is set and the watchdog error counter increases by 1.

A good WD refreshment, bad WD refreshment, or WD timeout all immediately trigger the start of a new window watchdog sequence by a new “closed window” followed by an “open window.”

Moreover, the watchdog uses a deglitch filter with a filter time ($t_{WD\_DEGLITCH}$) and an internal system clock to create the internally generated watchdog pulse. The WDI pin trigger’s rising edge must occur at least $t_{WD\_DEGLITCH}$ before the end of the “open window” to generate a good WD refresh.

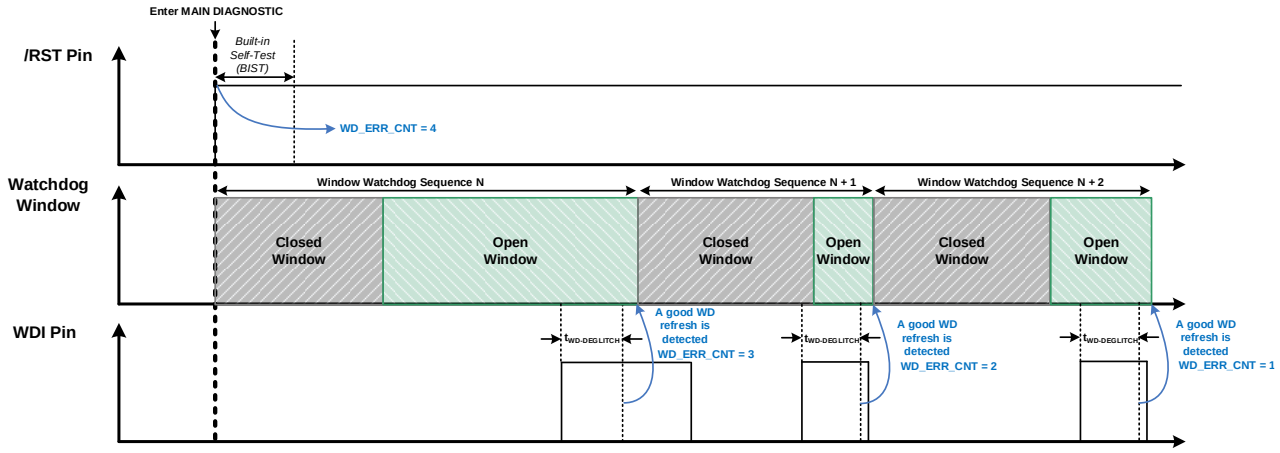


Figure 6: Window Watchdog Timing Diagram – Good WD Refresh

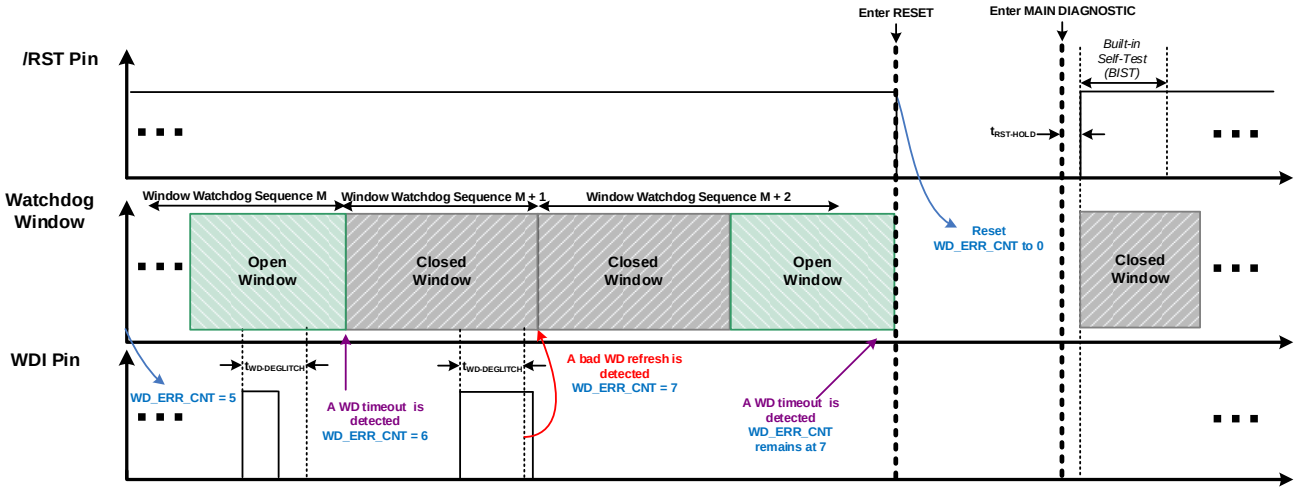


Figure 7: Window Watchdog Timing Diagram – Bad WD Refresh and WD Timeout

Question and Answer (Q&A) Watchdog Operation

Question and answer (Q&A) watchdog is another operation mode to monitor the MCU. Setting SAFETY_FUNC_CFG_1, bit[5] to 1 while the device is in MAIN DIAGNOSTIC configures the watchdog for Q&A mode.

In Q&A watchdog, the device provides a question (token) for the MCU in the WDT_TOKEN_VALUE register. The MCU performs a fixed series of arithmetic operations on the question to calculate the required 32-bit answer. This answer is split into 4 answer bytes. The MCU writes these answer bytes via the SPI, 1 byte at a time, to the WDT_ANSWER register. The MPQ70331FS verifies that the MCU returns the answer bytes within the specified time windows and that the answer bytes are correct. A new question is only generated if a good WD refresh occurred in the previous Q&A watchdog sequence, causing the internal token counter to increase and generate a new question.

If the MCU sends the correct answer bytes calculated for the current question within the correct Q&A watchdog window and in the correct order, it is considered a good WD refresh. Then the watchdog error counter, WD_ERR_CNT, reduces by 1 and the internal token counter increases by 1, causing a new question to be generated. Register WDT_STATUS_1, bit[2] and bit[0] reset to 0.

If the MCU sends any of the following, it is considered a bad WD refresh:

- The correct answer bytes, but not in the correct Q&A watchdog window
- The incorrectly calculated answer bytes
- The correct answer bytes in the wrong order

Then the watchdog error counter WD_ERR_CNT increases by 1, signaling that a potential MCU fault has occurred. The internal token counter does not change; thus the question does not change. Register WDT_STATUS_1, bit[2] sets to 1 and bit[0] of the same register is determined by whether all 4 answer bytes are returned during the “closed window.”

If a bad watchdog refresh occurs, the latest time for WD_ERR_CNT to report is the open window timeout. For example, if WD_TOKEN_ERR is triggered, then WD_ERR_CNT does not increase by 1 until the open window times out. For the following conditions, WD_ERR_CNT increases by 1 immediately:

1. WD_SEQ_ERR reports.
2. The open window times out without sending Answer-0.
3. The configuration changes online during the closed or open window.
4. Answer-3, -2, -1, and -0 are all sent during the closed window, and WD_TOKEN_EARLY reports.

If the MCU stops sending answer bytes (a WD timeout occurs), the WD_TIME_OUT bit is be set and the watchdog error counter increases by 1.

A good WD refresh, bad WD refresh, or WD timeout all immediately result in starting a new Q&A watchdog sequence.

The Q&A watchdog is performed step by step, as described below.

Step 1: A 5-bit seed in register WDT_TOKEN_FDBCK, bits[4:0] (either stored in the MPQ70331FS or the MCU) is applied to a linear feedback shift register (LFSR) in the MPQ70331FS to generate a 5-bit word question (token).

Step 2: The MCU reads register WDT_TOKEN_VALUE, bits[4:0]; register WDT_STATUS_2, bits[7:6]; and WDT_TOKEN_FDBCK, bits[7:5] at the beginning of each Q&A watchdog sequence.

Step 3: The MCU performs a predefined calculation to calculate the corresponding 8-bit answer.

Step 4: Answer-3, Answer-2, Answer-1, and Answer-0 are sent one by one by the MCU via the SPI to the MPQ70331FS during the correct Q&A watchdog window.

Step 5: The watchdog receives the answer byte when the MCU writes to WDT_ANSWER, bits[7:0].

Step 6: The answer sent by the MCU is verified by the MPQ70331FS. For each question, the

watchdog requires 4 correct answer bytes from the MCU in the correct timing and order.

Answer-3, Answer-2, and Answer-1 may be sent during the “closed window” or “open window” in the correct order, but Answer-0 must be sent during the “open window” to be detected as a good WD refresh.

Step 7: A good WD refresh and a new question for the MCU result in a new Q&A watchdog sequence. In the event of a bad WD refresh or WD timeout, a new question is not generated.

Figure 8 shows the watchdog Q&A answer generation. Figure 9 on page 53 shows the Q&A watchdog flowchart. Figure 10 on page 54 shows the Q&A watchdog timer refresh.

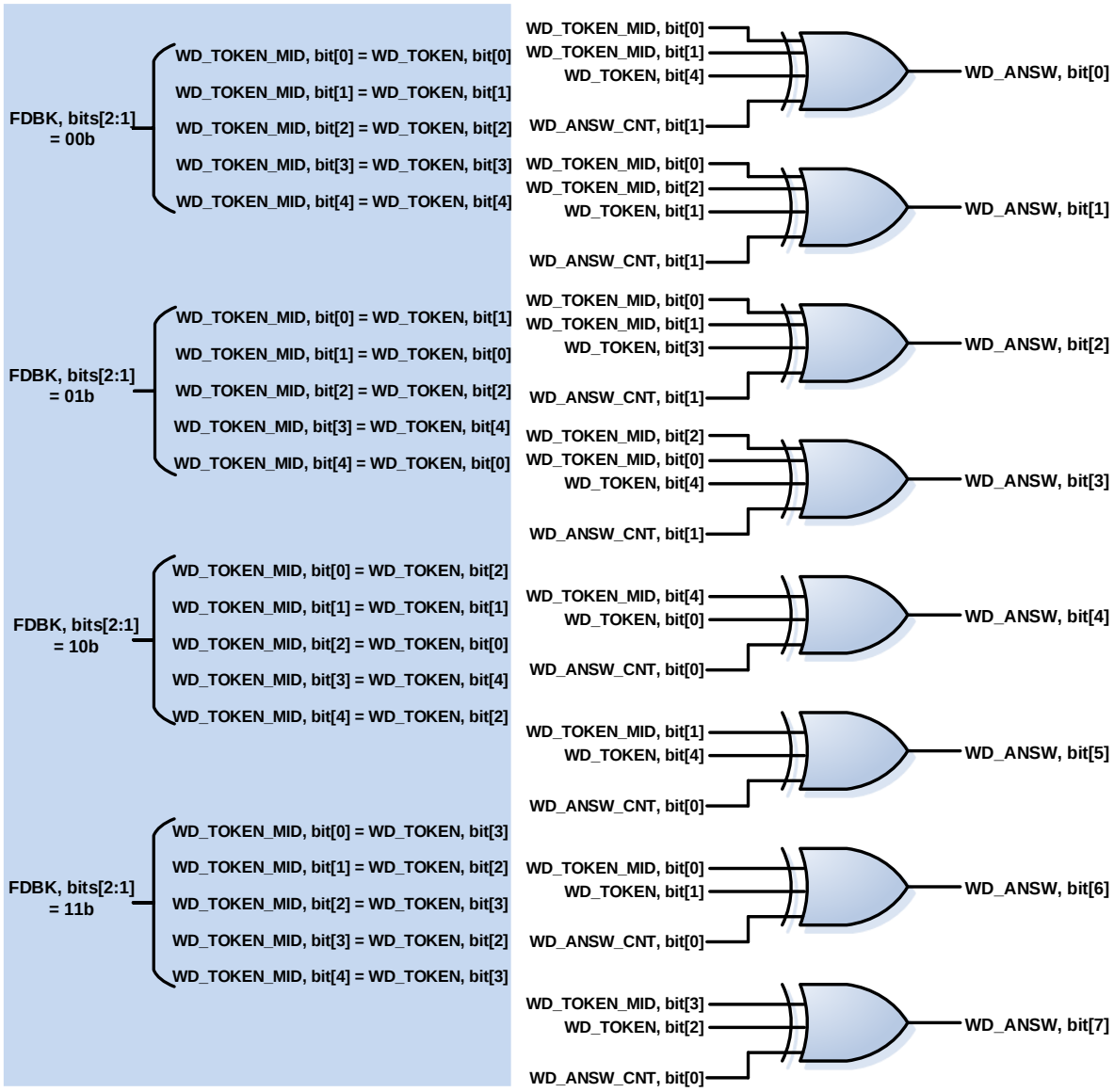


Figure 8: Question and Answer Watchdog Answer Generation

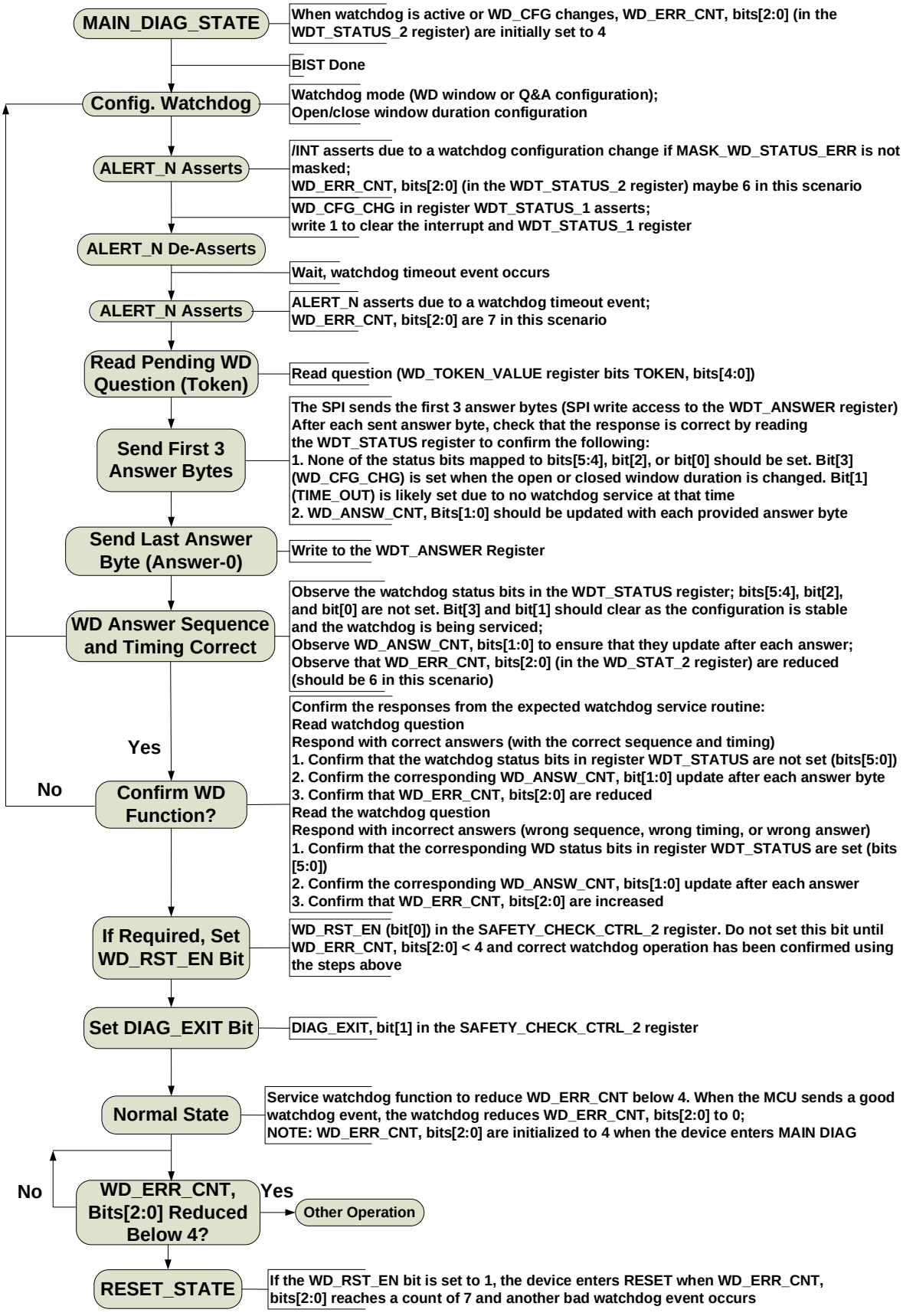


Figure 9: Question and Answer Watchdog Flowchart

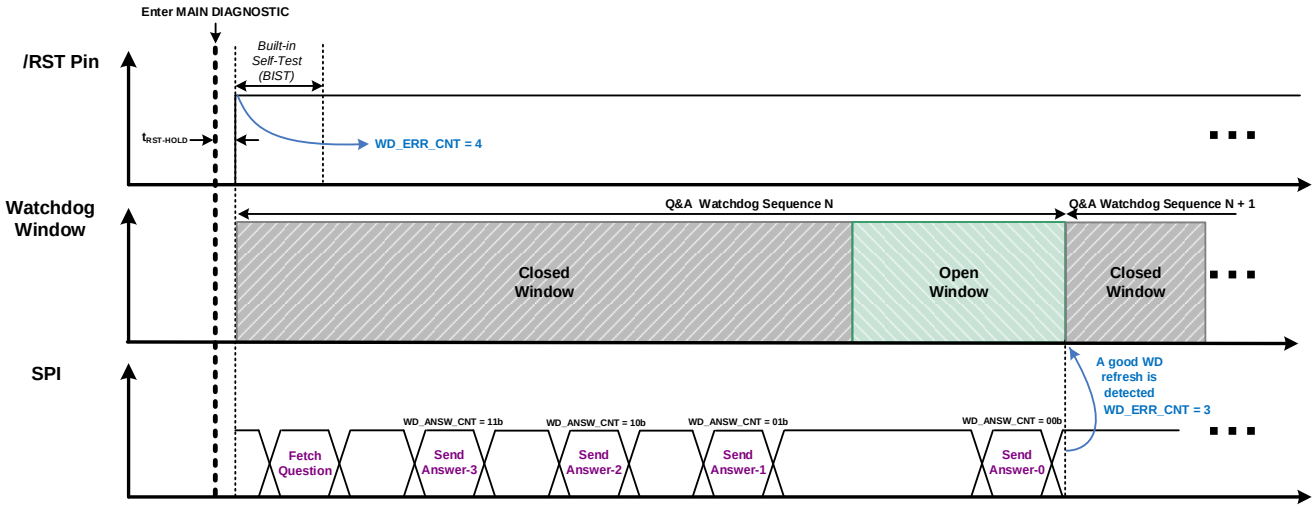


Figure 10: Q&A Watchdog WD Refresh Timing Diagram

Watchdog Error Counter and Watchdog Failure Flag

The MPQ70331FS includes a watchdog error counter (WD_ERR_CNT in the SAFETY_STAT_2 register) that increases or is reduced after every watchdog refresh.

The watchdog error counter ranges from 0 to 7, and is initialized to 0 after POR. A good WD refresh reduces WD_ERR_CNT by 1, down to a minimum of 0. A bad WD refreshment and WD timeout increase the WD_ERR_CNT by 1, up to a maximum of 7. A WD timeout also sets register WDT_STATUS_1, bit[1]. Once the watchdog error counter reaches a count of 7, any new bad WD refresh or WD timeout leads to a watchdog failure, but the watchdog error counter remains at 7 if the IC does not enter RESET.

When the watchdog error counter is below 7, only WD_CNT_STAT and WD_ERR_CNT reflect the situation. When the watchdog error counter reaches 7, the watchdog failure flag in register SAFETY_ERR_STAT, bit[4] is set to 1, which forces the device into the RESET state and resets the MCU by asserting the /RST pin low. In RESET, the watchdog error counter resets to 0 and is automatically initialized to 4 once the MPQ70331FS returns to MAIN DIAGNOSTIC.

For debugging purposes, the MCU reset assertion can be blocked by setting SAFETY_CHECK_CTRL_2, bit[0]. In this case, though the watchdog fail flag is still set, there is no transition to RESET. However, the watchdog error counter operates independently of the WD_RST_EN bit's state.

The MCU must manually reset the watchdog error counter to 0 via the SPI interface.

Watchdog Sequence

One window watchdog sequence in the MPQ70331FS is comprised of a "closed window" followed by an "open window." The window and Q&A watchdog configurations share the same watchdog sequence settings.

The watchdog window sequence is derived from the values in register WDT_CLOSED_WIN_CFG, bits[6:0] and WDT_OPEN_WIN_CFG, bits[4:0]. The MCU can set the "closed window" period (t_{WIN_CLOSED}) and "open window" period (t_{WIN_OPEN}) by writing the above registers, respectively. Write access to these registers is also only available in MAIN DIAGNOSTIC.

The watchdog uses the MPQ70331FS's internal system clock as a time reference for creating the 0.55ms watchdog time step. Calculate t_{WIN_CLOSED} and t_{WIN_OPEN} using Equation (1) and Equation (2), respectively:

$$t_{WIN\_CLOSED} = (RT\ [6:0] + 1) \times 0.55ms \quad (1)$$

$$t_{WIN\_OPEN} = (RW\ [4:0] + 1) \times 0.55ms \quad (2)$$

Due to the internal oscillator's ±15% tolerance, the MCU should allow a reasonable time margin during programming.

Watchdog Synchronization

When the MPQ70331FS enters MAIN DIAGNOSTIC, the external MCU should be powered properly and have started its initialization. Once the MPQ70331FS enters MAIN DIAGNOSTIC, the watchdog starts to run with the default settings (see Figure 11). The watchdog can be reconfigured by the external MCU before exiting MAIN DIAGNOSTIC.

To synchronize the MCU timer with the watchdog timer, the MCU can write to the WDT_OPEN_WIN_CFG register or WDT_CLOSED_WIN_CFG register to start a new watchdog sequence. After the MCU writes to these two registers, then WDT_STATUS_1, bit[3] is set to 1; the watchdog error counter increases by 1; and the device immediately starts a new watchdog sequence. This is true even when the WDT_OPEN_WIN_CFG and WDT_CLOSED_WIN_CFG registers are locked or the MPQ70331FS is in NORMAL. Therefore, write access only takes effect in the new watchdog sequence.

When the MCU timer is synchronized with the watchdog timer, a good WD refresh from the MCU immediately starts a new watchdog sequence. In this way, the MCU remains synchronized with the watchdog sequence.

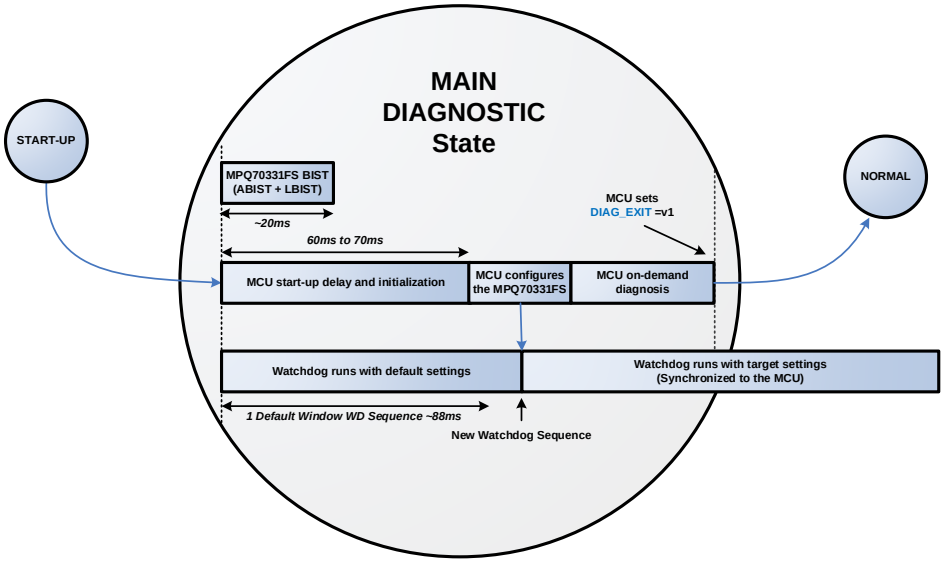


Figure 11: Watchdog Synchronization

FAILSAFE

The /FS pin is only activated in MAIN DIAGNOSTIC, NORMAL, and RESET, and indicates reset MCU events and deep safe events for peripheral protection circuits. /FS is always low when the device is in any other state. Any DEEP SAFE event pulls down the /FS pin.

If a watchdog failure event occurs, the reset error counter increases by 1, the MPQ70331FS enters RESET, and /FS asserts. After the MPQ70331FS returns to MAIN DIAGNOSTIC or NORMAL, the /FS pin is not released until the reset error counter is cleared (see Figure 12). /FS follows the watchdog fail event if WD_RST_EN is enabled, RST_MCU_REQUEST is enabled, or ON_DEMAND_DIAG is enabled.

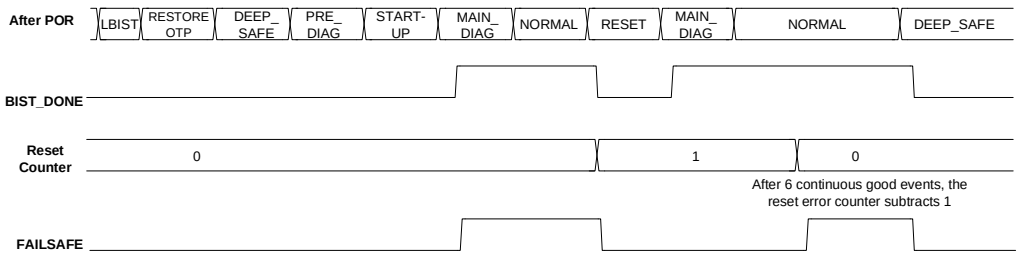


Figure 12: FAILSAFE Behavior According to the WD Status

WAKE-UP

The MPQ70331FS's wake-up circuitry automatically turns on when POR is released, while the device transitions to SCAN LBIST.

The WAKE pin is level-sensitive and has a deglitch filter time to suppress undesired state changes resulting from transients or glitches. It functions as an enable pin. A signal with a voltage that exceeds the wake-up threshold (WU_{VTH}) applied to the WAKE pin for a time longer than the wake-up deglitch time ($t_{WU-DEGLITCH}$) represents a valid wake-up event. A valid wake-up event transitions the device from POWER OFF to SCAN LBIST. $t_{WU-DEGLITCH}$ is also applied for the falling edge.

If the WAKE pin is connected to lines with transients, the application should provide proper filters and protection to ensure that the pin remains within the specified voltage range. A higher voltage compliance level in the application can be achieved by applying an external series resistor between the WAKE pin and the external wake-up signal.

If the application does not require a wake-up from ignition but the device should wake up any time that power is supplied, then the WAKE pin can be connected to VIN via a 100kΩ resistor. Once the battery supply is turned on, the WAKE pin also goes high and allows the device to wake up.

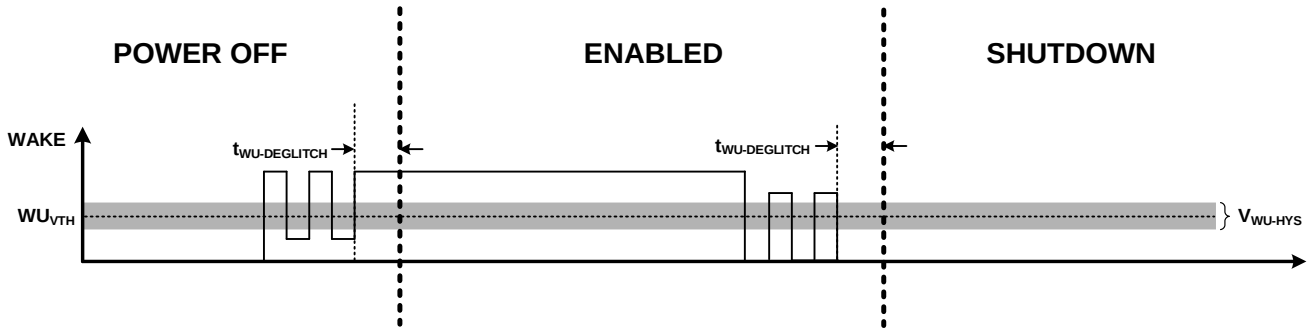


Figure 13: Wake-Up Signal

INTERRUPT

The /INT output pin pulls down when an interrupt condition occurs. Only writing FFh to the interrupt status register (INTERRUPT) can reset the interrupt circuit and pull /INT high. /INT is reset in read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. To initialize the interrupt circuit, the MCU must write FFh to the INTERRUPT register once the PG pin goes high. After a reset, each I/O change is detected and transmitted as an interrupt.

The values in the interrupt status register are sampled on the SCL's rising edge during the read address ACK. If an interrupt occurs before this event, it is reflected in this register during the next read cycle. If an interrupt occurs very close to this event, it may be reflected in both the current and the next read cycle. At no point is a valid interrupt ever missed.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O pin from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents in the input default state register The /INT output has an open-drain structure and requires a pull-up resistor connected to VCCP or VCCI, depending on the application. /INT should be connected to the voltage source of the device that requires the interrupt information.

For debugging purposes, the MCU can read the bit value from INTERRUPT to identify the corresponding fault register. Any of the faults listed in the SAFETY_STAT_x registers set the corresponding bit to 1. The value always indicates the latest source.

Table 13 on page 57 lists all interrupt sources

.

Table 13: MPQ70331FS Interrupt Table

Interrupt Bit	Mask Option	Interrupt Source (Status Bit Name)	Source Register	Description
D[0]	MASK_VIN_OVUV	VIN_OV	SAFETY_STAT_1	V_{IN} OV.
	MASK_VIN_OVUV	VIN_UV	SAFETY_STAT_1	V_{IN} UV.
	MASK_VEXT1_UVOV	VEXT1_OV	SAFETY_STAT_1	External monitored signal 1 (VMON1) OV detection.
	MASK_VEXT1_UVOV	VEXT1_UV	SAFETY_STAT_1	External monitored signal 1 (VMON1) UV detection.
	MASK_VEXT2_UVOV	VEXT2_OV	SAFETY_STAT_1	External monitored signal 2 (VMON2) OV detection.
	MASK_VEXT2_UVOV	VEXT2_UV	SAFETY_STAT_1	External monitored signal 2 (VMON2) UV detection.
	MASK_VCC2_UV	VCC2_UV	SAFETY_STAT_1	Internal VCC2 UV detection.
	MASK_VCC1_UV	VCC1_UV	SAFETY_STAT_1	Internal VCC1 UV detection.
D[1]	MASK_VSNS_UV	VSNS_UV	SAFETY_STAT_2	Battery failure indicator, V_{SENSE} below 8.5V detection.
	No	HV_BUCK_ILKG_ERR	SAFETY_STAT_2	HV buck internal MOSFET over-current (OC) leakage detection.
	No	LV_BUCK_ILKG_ERR	SAFETY_STAT_2	LV buck internal MOSFET OC leakage detection.
	No	BOOST_ILKG_ERR	SAFETY_STAT_2	LV boost internal MOSFET OC leakage detection.
	MASK_HV_BUCK_OC	HV_BUCK_ILIM	SAFETY_STAT_2	HV buck output OC detection.
	MASK_LV_BUCK_OC	LV_BUCK_ILIM	SAFETY_STAT_2	LV buck output OC detection.
	MASK_BOOST_OC	BOOST_ILIM	SAFETY_STAT_2	LV boost output OC detection.
	No	BG_ERR	SAFETY_STAT_2	>15% voltage difference between bandgap (BG) references detection, BG1 error.
D[2]	MASK_HV_BUCK_UVOV	HV_BUCK_OV	SAFETY_STAT_3	HV buck OV detection.
	MASK_HV_BUCK_UVOV	HV_BUCK_UV	SAFETY_STAT_3	HV buck UV detection (the UV threshold is defined in the UV_CTRL_x registers).
	MASK_LV_BUCK_UVOV	LV_BUCK_OV	SAFETY_STAT_3	LV buck OV detection.
	MASK_LV_BUCK_UVOV	LV_BUCK_UV	SAFETY_STAT_3	LV buck UV detection.
	MASK_BOOST_UVOV	BOOST_OV	SAFETY_STAT_3	LV boost OV detection.
	MASK_BOOST_UVOV	BOOST_UV	SAFETY_STAT_3	LV boost UV detection.
	MASK_LVBK_BT_PO_UV	LV_BUCK_PO_UV	SAFETY_STAT_3	LV buck V_{IN} UV detection.
	MASK_LVBK_BT_PO_UV	BOOST_PO_UV	SAFETY_STAT_3	LV boost V_{IN} UV detection.
D[3]	No	HV_BUCK_18%OV	SAFETY_STAT_4	HV buck 18% OV detection.
	No	LV_BUCK_18%OV	SAFETY_STAT_4	LV buck 18% OV detection.
	No	BOOST_18%OV	SAFETY_STAT_4	LV boost 18% OV detection.
	No	OT	SAFETY_STAT_4	Over-temperature (OT) detected.
	MASK_OT_WARN	OT_WARN	SAFETY_STAT_4	OT warning.
	MASK_ALL_PG_OK	HV_BUCK_PG_OK	SAFETY_STAT_4	HV buck PG is not okay.
	MASK_ALL_PG_OK	LV_BUCK_PG_OK	SAFETY_STAT_4	LV buck PG is not okay.
	MASK_ALL_PG_OK	BOOST_PG_OK	SAFETY_STAT_4	LV boost PG is not okay.
D[4]	No	PRE_DIAG_TOUT	SAFETY_STAT_5	Failed to finish pre-diagnosis within the set time window.
	No	MIAN_DIAG_TOUT	SAFETY_STAT_5	Failed to finish main diagnosis within the set time window.
	MASK_RST_TOUT	RST_TOUT	SAFETY_STAT_5	Failed to finish the MCU reset within the set time window.
	No	STARTUP_TOUT	SAFETY_STAT_5	Failed to finish start-up within the set time window.
	MASK_DEEP_SAFE_TOUT	DEEP_SAFE_TOUT	SAFETY_STAT_5	Failed to finish deep safe within the set time window.
	No	RST_8S	SAFETY_STAT_5	Reset MCU remains low for longer than 8s.
	No	SCAN_LBIST_DONE	SAFETY_STAT_5	Report at the posedge when scan chain based LBIST is complete.

Table 13: MPQ70331FS Interrupt Table *(continued)*

Interrupt Bit	Mask Option	Interrupt Source (Status Bit Name)	Source Register	Description
D[5]	MASK_FS_ASSERT	FS_ASSERT	SAFETY_STAT_6	Failsafe change leads to an interrupt, and report the real-time state. This bit reports once the fault is triggered, and can be cleared after W1C once the fault has been removed.
	MASK_RST_ASSERT	RST_ASSERT	SAFETY_STAT_6	Resetting the MCU triggers an interrupt, and RST reports its real-time state. This bit reports once the fault is triggered, and can be cleared after W1C once the fault has been removed.
	No	PIN_FB_MISMATCH	SAFETY_STAT_6	Mismatch between /PREWRN, PG, /RST, /FS, /INT pin feedback and /PREWRN, PG, /RST, /FS, /INT logic output command detection.
	No	SCAN_LBIST_ERR	SAFETY_STAT_6	SCAN logic BIST fail detection.
	MASK_WD_ERR_CNT_FULL	WD_ERR_CNT_FULL	SAFETY_STAT_6	Watchdog fail counter has reached max value.
	MASK_RST_CNT_FULL	RST_ERR_CNT_FULL	SAFETY_STAT_6	Reset counter has reached max value.
	MASK_BG_WARN	BG_WARN	SAFETY_STAT_6	BG warning.
D[6]	No	LOGND	SAFETY_STAT_7	Loss of ground.
	MASK_BIST_DONE	BIST_DONE	SAFETY_STAT_7	Reports at the posedge once BIST is complete.
	No	LOCLK1	SAFETY_STAT_7	Loss of clock 1 error has been detected.
	No	LOCLK2	SAFETY_STAT_7	Loss of clock 2 error has been detected.
	MASK_BIST_ERR	LBIST_ERR	SAFETY_STAT_7	Error detected when running the MEM/OTP/MUX/COMPUTER logic self-test.
	MASK_BIST_ERR	ABIST_ERR	SAFETY_STAT_7	Error detected when running analog self-test.
	MASK_BIST_RUN	LBIST_RUN	SAFETY_STAT_7	MEM/OTP/MUX/COMPUTER logic self-test run sign.
	MASK_BIST_RUN	ABIST_RUN	SAFETY_STAT_7	Analog self-test run sign.
D[7]	No	SPI_ERR_DETECTED	SAFETY_STAT_8	Invalid SPI access (incorrect write or read, write to protected registers outside MAIN DIAGNOSTIC state, wrong address).
	No	MEMORY_CRC_FAIL	SAFETY_STAT_8	Register content CRC, including trimming bits, failure detection.
	No	OTP_CRC_FAIL	SAFETY_STAT_8	OTP content CRC, including trimming bits, failure detection.
	No	PIN_ERR_DETECT	SAFETY_STAT_8	A valid error signal on the /ERROR pin is detected.
	MASK_WD_STATUS_ERR	WD_STATUS_ERR	SAFETY_STAT_8	Watchdog status error.
	No	DEEP_SAFE_MCU_REQ	SAFETY_STAT_8	MCU request to enter DEEP SAFE.
	No	REG_WRITE/RESTORE_MISMATCH	SAFETY_STAT_8	Register WRITE/RESTORE mismatch is detected.

ERROR INPUT

The /ERROR pin is a safety input to monitor the error outputs from either the MCU or peripheral circuit. A signal from a valid detected error sets register SAFETY_ERR_STAT, bit[5] to 1, which transitions the part to DEEP SAFE. The /ERROR pin check occurs in MAIN DIAGNOSTIC and NORMAL.

/ERROR is active by default; it is deactivated by setting SAFETY_FUNC_CFG_1, bit[3] to 1. The /ERROR pin has two detection modes: low-pulse mode and pulse-width modulation (PWM) mode. The mode can be selected via SAFETY_FUNC_CFG_1, bit[6]. These modes are described in more detail in the following sections. Any signal shorter than 7.5µs ($t_{ERR-DEGLITCH}$) is not counted.

Low-Pulse Mode Detection

Low-pulse mode (ERR_PIN_MODE = 0) can detect a low-pulse signal (with a configurable low-pulse duration threshold) as a valid error input signal.

It is the MPQ70331FS's default mode after POR. If the /ERROR pin remains low for the low-pulse duration (set by the SAFETY_ERR_PIN_L register), this is considered a valid error signal. The configurable time range is between 15µs and 3.84ms, with 15µs steps. The low-pulse duration can be calculated with Equation (3):

Low-Pulse Duration = ERR_PIN_L[7:0] x 15µs (3)

The ERR_PIN_L command must be set to the target value based on the maximum required time for the MCU to detect an error or fault and potentially recover from or correct the error or fault. Figure 14 shows the low-pulse mode error-detection case scenarios.

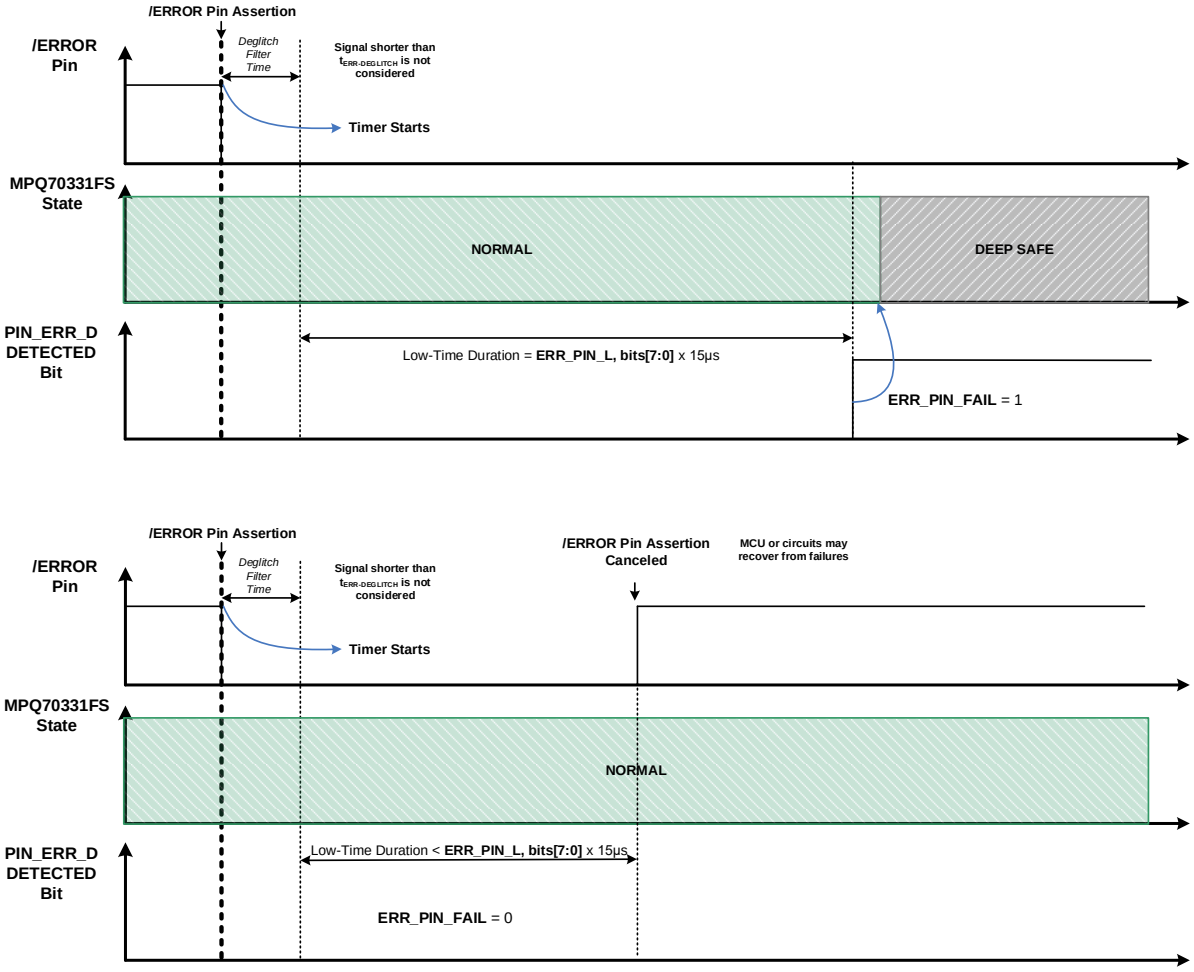


Figure 14: /ERROR Reaction in Low-Pulse Mode

Pulse-Width Modulation (PWM) Mode Detection

PWM mode (ERR_PIN_MODE = 1) detects a PWM sequence with a configurable frequency and duty cycle as a valid error input signal. The expected PWM low-pulse duration is also set via the SAFETY_ERR_PIN_L register, and the high-pulse duration is set via the SAFETY_ERR_PIN_H register. The configurable time range for the expected high- and low-pulse duration is 15µs to 3.825ms, with 15µs resolution steps. The PWM low-time and high-time thresholds can be calculated with Equation (4) and Equation (5), respectively:

Low-Time Threshold = ERR_PIN_L[7:0] x 15µs (4)

High-Time Threshold = ERR_PIN_H[7:0] x 15µs (5)

In PWM mode, the MPQ70331FS detects a valid error signal on the /ERROR pin if either of the following conditions occur:

- The /ERROR pin low-pulse duration is longer than the PWM low-time threshold

- The /ERROR pin high-pulse duration is longer than the PWM high-time threshold

Figure 15 shows the PWM mode error-detection case scenarios.

In low-pulse mode, PIN_ERR_DETECTED is set to 1 when the /ERROR pin signal remains low for longer than the specified low-pulse duration (ERR_PIN_L[7:0] x 15µs). In PWM mode, PIN_ERR_DETECTED is set to 1 if either the /ERROR pin signal remains low for longer than the specified low-time threshold (ERR_PIN_L[7:0] x 15µs) or remains high for longer than the specified high-time threshold (ERR_PIN_H[7:0] x 15µs).

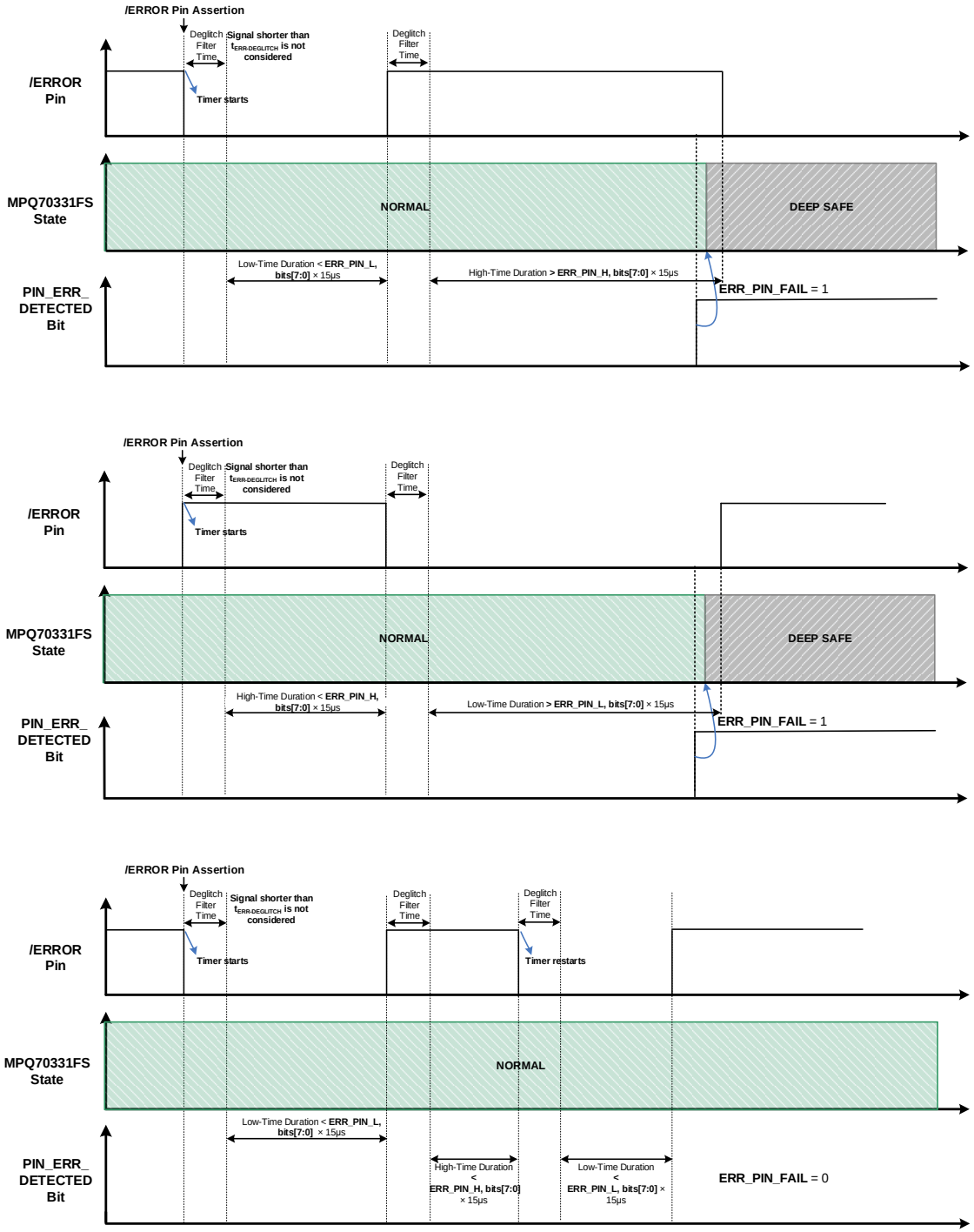


Figure 15: /ERROR Reaction in PWM Mode

DATA PROTECTION

Register Protection

The MPQ70331FS offers two mechanisms to protect the safety-related registers:

- Write protection: Protected register(s) can only be written via the SPI when the device is in MAIN DIAGNOSTIC.
- CRC protection: A CRC polynomial is used to verify the SPI register contents and ensure that they are correctly programmed to the key configuration registers.

If the calculated CRC value for the key register content does not match the expected CRC value stored in the SAFETY_CFG_CRC_1 register, then register SAFETY_STAT_8, bit[5] is set to 1, and the MPQ70331FS transitions to DEEP SAFE.

Table 14 shows which key registers are protected. They can only be written in MAIN DIAGNOSTIC; they cannot be written in NORMAL.

Table 14: MPQ70331FS Protected Registers

Register Short Name	R/W	Address
SAFETY_ERR_CFG_1	R/W	0x0B
SAFETY_ERR_CFG_2	R/W	0x0C
SAFETY_FUNC_CFG_1	R/W	0x10
SAFETY_FUNC_CFG_2	R/W	0x11
SAFETY_ERR_PIN_H	R/W	0x13
SAFETY_ERR_PIN_L	R/W	0x14
INT_MASK_CFG1	R/W	0x1C
INT_MASK_CFG2	R/W	0x1D
INT_MASK_CFG3	R/W	0x1E
WDT_TOKEN_FDBCK	R/W	0x1F
WDT_CLOSED_WIN_CFG	R/W	0x20
WDT_OPEN_WIN_CFG	R/W	0x21

One-Time Programmable (OTP) Memory Protection

The data content and trimming bits in the OTP memory are protected by a cyclic redundancy check (CRC). If the calculated CRC value for the OTP content does not match the expected CRC value stored in the SAFETY_CFG_CRC_2 register, then SAFETY_STAT_8, bit[4] is set to 1, and the MPQ70331FS transitions to DEEP SAFE.

Serial Peripheral Interface (SPI) Communication Protection

SPI communication data is protected by parity bit and CRC (polynomial = $x^8 + x^2 + x + 1$).

Every data stream is monitored, and faults are reported to the SPI error status bits (SAFETY_STAT_8, bits[7:6]). The error statuses include invalid access, command error(s), format error(s), and data output mismatch (e.g. parity bit or CRC error). SPI_ERR_DETECTED is cleared to 00 after SPI read access.

If an MCU reset asserts during an SPI frame transfer (leading to a truncated SPI frame), these SPI error status bits are not cleared. Instead, they maintain the status according to the previous, truncated SPI frame until SPI read access.

Register Write Check

Every time a register is written via the OTP or SPI, a dedicated circuit is implemented to read the register value. If the readback value does not match the expected write data from the OTP/SPI, then SAFETY_STAT_8, bit[0] is set.

DIAGNOSTIC MUX OUTPUT

The DIAG pin is a diagnostic output pin allowing the MCU to observe internal analog and digital signals, selectable through the multiplexer (mux).

Analog and digital critical signals are not directly connected to the MCU; rather they are switched by the mux to the external DIAG pin. Setting the MUX_CHANNEL_GROUP and MUX_CHANNEL bits (DIAG_MUX_SEL, bits[7:4] and bits[3:0], respectively) configures the mux. The digital signals are buffered to have sufficient drive capabilities. The mux facilitates the external pin interconnection tests by feeding back the input pin state, the internal module self-test status, or the safety comparator outputs.

After receiving a DIAG pin selection SPI write command, the DIAG pin outputs immediately. It takes 100µs for the DIAG pin to begin outputting steadily.

The DIAG pin signal type (analog, digital, or interconnection) can be configured with register DIAG_CFG_CTRL, bits[1:0]. The mux is enabled by default, and can be disabled with register DIAG_CFG_CTRL, bit[7]. When it is disabled, the DIAG pin is in a high-ohmic state.

Analog Mux Mode

Table 15 lists the selectable analog internal signals on the DIAG pin. DIAG_CFG_CTRL, bits[1:0] must be set to 10 for analog mux mode.

Digital Mux Mode

Table 16 lists the selectable digital internal signals on the DIAG pin. DIAG_CFG_CTRL, bits[1:0] must be set to 01 for digital mux mode.

Table 15: Selectable Analog Internal Signals

DIAG_MUX_SEL	Group #	Signal Name	Description
0x01	0	VCC_1	Internal VCC1 voltage divider (divided by 4)
0x02	0	VCC_2	Internal VCC2 voltage divider (divided by 4)
0x03	0	BG_1	Internal bandgap reference 1 (1.21V)
0x04	0	BG_2	Internal bandgap reference 2 (1.21V)
0x05	0	VIN	V_{IN} voltage divider (divided by 50)
0x06	0	VSNS	Sensed battery voltage divider (divided by 50)
0x00, 0x07~0x0F	0	RESERVED	Reserved for production testing

Table 16: Selectable Digital Internal Signals

DIAG_MUX_SEL	Group #	Signal Name	Description
0x10	1	HV_BUCK_UV_COMP	HV buck UV comparator
0x11	1	LV_BUCK_UV_COMP	LV buck UV comparator
0x12	1	LV_BOOST_UV_COMP	LV boost UV comparator
0x13	1	HV_BUCK_OV_COMP	HV buck OV comparator
0x14	1	LV_BUCK_OV_COMP	LV buck OV comparator
0x15	1	LV_BOOST_OV_COMP	LV boost OV comparator
0x16	1	VEXT1_UV_COMP	External voltage 1 (VMON1) UV comparator
0x17	1	VEXT2_UV_COMP	External voltage 2 (VMON2) UV comparator
0x18	1	VEXT1_OV_COMP	External voltage 1 (VMON1) OV comparator
0x19	1	VEXT2_OV_COMP	External voltage 2 (VMON2) OV comparator
0x1A	1	VCC1_UV_COMP	Internal VCC1 UV comparator
0x1B	1	VCC2_UV_COMP	Internal VCC2 UV comparator
0x1C, 0x1D	1	RESERVED	Reserved for production testing
0x1E	1	LV_BUCK_VINUV_COMP	LV buck input UV comparator
0x1F	1	LV_BOOST_VINUV_COMP	LV boost input UV comparator
0x20	2	BG_ERR_COMP	BG error comparator
0x21	2	BG_WRN_COMP	BG warning comparator
0x22	2	VSNS_UV_COMP	Sensed battery voltage UV comparator
0x23	2	VIN_UV_COMP	V_{IN} UV comparator
0x24	2	VIN_OV_COMP	V_{IN} OV comparator
0x25	2	HV_BUCK_OC	HV buck regulator output OC
0x26	2	LV_BUCK_OC	LV buck regulator output OC
0x27	2	LV_BOOST_OC	LV boost regulator output OC
0x28	2	OT	OT shutdown
0x29	2	HV_BUCK_DOV	HV buck 18% OV comparator
0x2A	2	LV_BUCK_DOV	LV buck 18% OV comparator
0x2B	2	LV_BOOST_DOV	LV boost 18% OV comparator
0x2C	2	LCLK_COMP1	Loss of clock 1 comparator
0x2D	2	LCLK_COMP2	Loss of clock 2 comparator
0x2E	2	LGND_COMP	Loss of ground comparator
0x2F	2	OT_WRN	OT warning
0x30	3	CLK_MAIN	Main system clock
0x2E	2	LGND_COMP	Loss of ground comparator

Table 16: Selectable Digital Internal Signals *(continued)*

DIAG_MUX_SEL	Group #	Signal Name	Description
0x2F	2	OT_WRN	OT warning
0x30	3	CLK_MAIN	Main system clock
0x31	3	15US_REF	15µs time reference
0x32	3	SPI_NCS	SPI chip selection input pin
0x33	3	SPI_SDI	SPI slave data input pin
0x34	3	SPI_CLK	SPI clock input pin
0x35	3	SPI_SDO	SPI output pin
0x36	3	WDI_READBACK	WDI pin readback
0x37	3	/RST_READBACK	/RST pin readback
0x38	3	/FS_READBACK	/FS pin readback
0x39	3	/INT_READBACK	/INT pin readback
0x3A	3	/ERROR_READBACK	/ERROR pin readback
0x3B	3	WD_WIN_SIGN	Watchdog window sign (1: closed 0: open)
0x3C	3	/PREWRN_READBACK	/PREWRN pin readback
0x3D	3	PG_READBACK	PG pin readback
0x3E	3	RESERVED	Reserved, logic 0
0x3F	3	RESERVED	Reserved, logic 0

Slave Mode

The DIAG pin's state is controlled by register DIAG_CFG_CTRL, bit[5]. To use slave mode, the MUX_CFG bits in the DIAG_CFG_CTRL register must be set to 10, then 00.

Interconnection Mode

DIAG_CFG_CTRL, bits[4:2] can be set to make the MPQ703331FS perform a diagnostic interconnection check at the digital input pins (/ERROR, WDI, NCS, SDI, and SCLK). To use interconnection mode, the MUX_CFG bits in the DIAG_CFG_CTRL register must be set to 10, then set to 11.

Table 17 shows the observed digital inputs on the DIAG pin.

Table 17: Observed Digital Inputs on the DIAG Pin

	Observed Digital Inputs
000	No active interconnection test
001	/ERROR input state observed on the diagnostic mux output
010	NCS input state observed on the diagnostic mux output
011	SDI input state observed on the diagnostic mux output
100	SCLK input observed on the diagnostic mux output
101	WDI input observed on the diagnostic mux output
110	Invalid
111	Invalid

SAFETY DESCRIPTION (15)

Independent Voltage Supervisor

There are two external voltage monitoring channels (VMON1 and VMON2). These channels are independent from the output rails, and have a separate reference voltage, OV/UV threshold register, and comparators.

SPI Communication CRC

The MPQ70331FS implements CRC to detect whether there are fewer than 3 bits of communication error in the SPI.

Digital Clock Monitoring

The MPQ70331FS implements two digital clocks: CLK1 and CLK2. CLK1 or CLK2 can be configured to be the main digital clock. CLK3 is an individual clock and is used to monitor CLK1 and CLK2. If the default main clock configuration is CLK1 and CLK1 fails, then CLK2 becomes the main clock automatically, and the device enters DEEP SAFE then shuts off the output rails. The MPQ70331FS remains in DEEP SAFE if CLK1 does not recover. If CLK1 recovers later, CLK1 becomes the main clock again and the part restarts then resumes normal operation. The same principles apply for CLK2.

If the failed clock is not the configured main clock, the device simply reports the failure.

OTP CRC Monitoring

The MPQ70331FS implements CRC to detect whether there are fewer than 3 bits of failure in the OTP content.

Register CRC

The MPQ70331FS implements CRC to detect whether there are <3 bits of failure in the register.

Register Write Check

A separate circuit is implemented to read back the register value after the register is written.

V_{IN}/V_{CCx} Under-Voltage Lockout (UVLO)

If V_{CC1}, V_{CC2}, or V_{IN} fall below their respective UVLO threshold, the device shuts off so that no unintended functionalities occur.

Over-Voltage (OV) Monitoring

The MPQ70331FS monitors the voltage output on SW1, SW2, and SW3 against the OV thresholds, as defined by registers OV_CTRL_1, OV_CTRL_2, and OV_CTRL_3.

Under-Voltage (UV) Monitoring

The MPQ70331FS monitors the voltage output on SW1, SW2, and SW3 against the UV thresholds, as defined by registers UV_CTRL_1, UV_CTRL_2, and UV_CTRL_3.

Device Protection

DEEP SAFE (device shutdown) is trigged if any of the following failures occur:

- OC fault
- OT fault
- Deep OV (118% of the high-voltage buck (HVBK), low-voltage buck (LVBK), or low-voltage boost (LVBT) output voltages)

Reference Voltage Monitoring

The MPQ70331FS compares the primary reference voltage (V_{REF1}) with the secondary reference voltage (V_{REF2}). V_{REF1} and V_{REF2} come from different bandgaps.

Analog Built-In Self-Testing (ABIST)

ABIST is performed during start-up. The IC performs ABIST in PRE-DIAGNOSTIC before entering START-UP and upon entering MAIN DIAGNOSTIC from NORMAL or RESET. The device does not perform ABIST when transitioning from the START-UP state to MAIN DIAGNOSTIC. The defined test values are used to check the functionality of the comparators for all safety mechanisms.

Scan Logic Built-In Self-Testing (Scan LBIST)

The MPQ70331FS tests all digital logic while the device is powered on. Only two scan LBIST tests are allowed per power cycle. As a result, if a second failure occurs, the device remains in DEEP SAFE until power is cycled.

Safety Path Open-Circuit Detection

The MPQ70331FS implements open-circuit detection at the /INT, /FS, /PREWRN, /RST, and PG pins.

Note:

15) A detailed safety manual with descriptions of the safety architecture, assumptions, and implemented safety mechanisms is available. Contact MPS for details.

SERIAL PERIPHERAL INTERFACE

SPI Overview

The primary communication between the MPQ70331FS and the external MCU is through an SPI bus, which provides full-duplex communications in a master-slave configuration.

The external MCU is always an SPI master; it sends the command requests on the SDI pin and receives device responses on the SDO pin. The MPQ70331FS is an SPI slave device; it receives command requests and sends responses (e.g. status, measured values) to the external MCU over the SDO line.

The SPI is a 4-pin interface. The pins are listed below:

- /CS: SPI chip selection (active-low)
- SCLK: SPI serial clock
- SDI: Master-out / SPI slave-in (MOSI)
- SDO: Master-in / SPI slave-out (MISO, tri-state output)

The MPQ70331FS uses SPI mode 3. The SPI features a 16-bit frame size and speed up to 4Mbps. Commands and data are shifted by the most significant bits (MSB) first, and least significant bits (LSB) last. The SDI line is sampled on the rising edge of SCLK. The SDO line shifts out on the falling edge of SCLK.

SPI communication starts with the /CS falling edge and ends with the /CS rising edge. Figure 17 on page 66 shows the SPI timing chart. The /CS high level keeps the SPI's slave interface in the reset state, and the SDO output is tri-state.

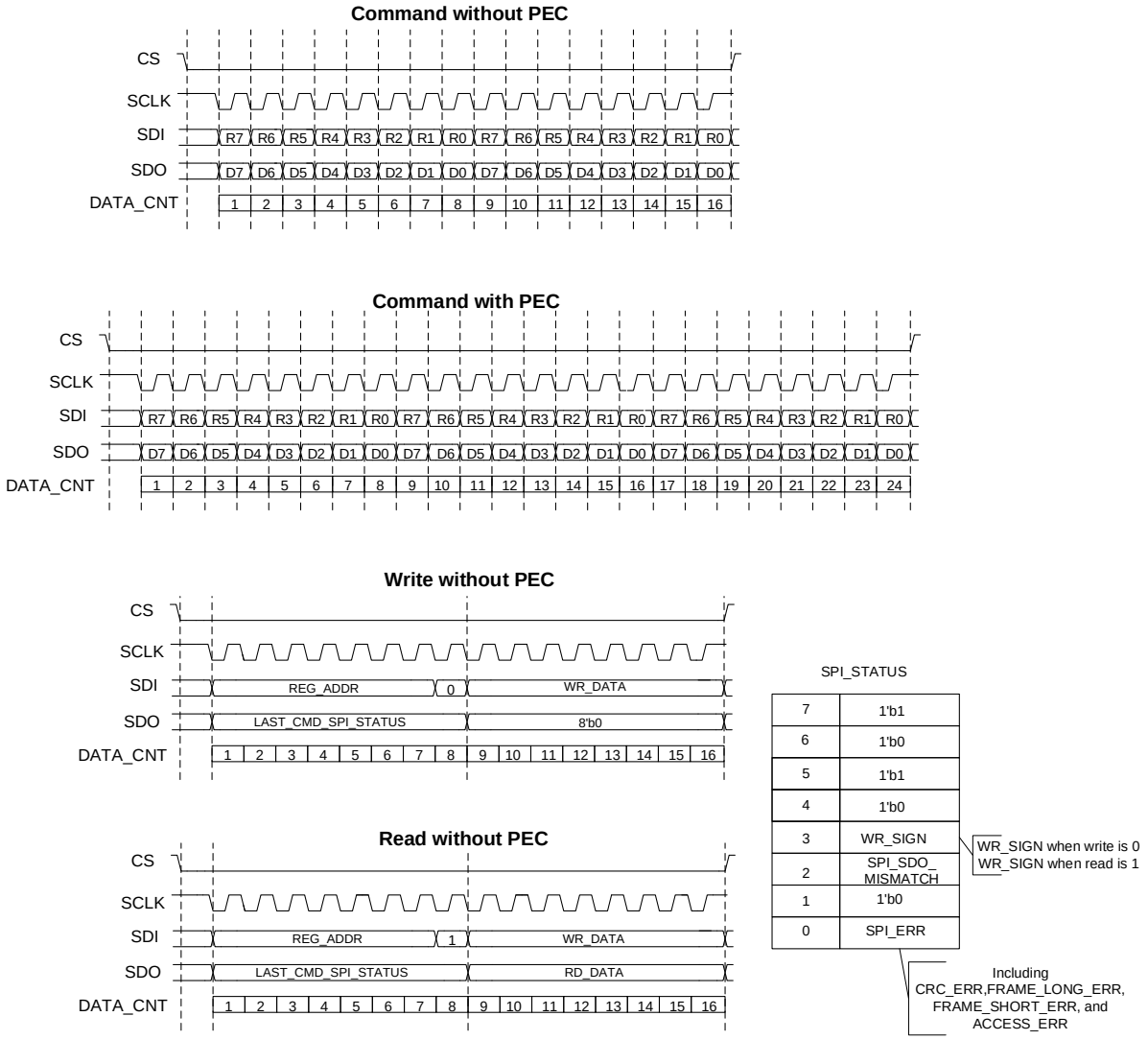


Figure 17: SPI Timing Chart

REGISTER BITMAPPING

Table 18: SPI Bitmapping

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default Value (16)	OTP (18)
Device Status												
0x00	DEV_REV	R/W	MAJOR_REV				MINOR_REV				00h	Yes
0x01	DEV_ID	R/W	ID				SILICON_INFO				00h	Yes
0x02	DEV_STAT	R	CURRENT_STATE				WU_LVL	OTP_IND	RESERVED	RESERVED	00h	No
Safety and Diagnostics												
0x03	SAFETY_STAT_1	R	VIN_OV	VIN_UV	VEXT1_OV	VEXT1_UV	VEXT2_OV	VEXT2_UV	VCC2_UV	VCC1_UV	00h	No
0x04	SAFETY_STAT_2	R	VSNS_UV	HV_BUCK_ILKG_ERR	LV_BUCK_ILKG_ERR	BOOST_ILKG_ERR	HV_BUCK_ILIM	LV_BUCK_ILIM	BOOST_ILIM	BG_ER	00h	No
0x05	SAFETY_STAT_3	R	HV_BUCK_OV	HV_BUCK_UV	LV_BUCK_OV	LV_BUCK_UV	BOOST_OV	BOOST_UV	LV_BUCK_PO_UV	BOOST_PO_UV	00h	No
0x06	SAFETY_STAT_4	R	HV_BUCK_18%OV	LV_BUCK_18%OV	BOOST_18%OV	OT	OT_WARN	HV_BUCK_PG_OK	LV_BUCK_PG_OK	BOOST_PG_OK	00h	No
0x07	SAFETY_STAT_5	R	PRE_DIAG_TOUT	MAIN_DIAG_TOUT	RST_TOUT	START-UP_TOUT	DEEP_SAFE_TOUT	RST_8S	SCAN_LBIST_DONE	RESERVED	00h	No
0x08	SAFETY_STAT_6	R	FS_ASSERT	RST_ASSERT	PIN_FB_MISMATCH	SCAN_LBIST_ERR	FSM_ERR	WD_ERR_CNT_FULL	RST_ERR_CNT_FULL	BG_WARN	00h	No
0x09	SAFETY_STAT_7	R	LOGND	BIST_DONE	LOCLK1	LOCLK2	LBIST_ERR	ABIST_ERR	LBIST_RUN	ABIST_RUN	00h	No
0x0A	SAFETY_STAT_8	R	SPI_ERR_DETECTED		CFG_CRC_ERR	OTP_CRC_ERR	PIN_ERR_DETECTED	WD_STATUS_ERR	DEEP_SAFE_MCU_REQ	REG_WRITE/RESTORE_MISMATCH	00h	No
0x0B	SAFETY_ERR_CFG_1 (17)	R/W	PRE_DIAG_TIMEOUT		MAIN_DIAG_TIMEOUT		RST_TIMEOUT		START-UP_TIMEOUT		00h	Yes
0x0C	SAFETY_ERR_CFG_2 (17)	R/W	DEEP_SAFE_TIMEOUT			RST_ERR_THR				CFG_REG_WR_LOCK	06h	Yes
0x0D	SAFETY_BIST_CTRL (17)	R/W	BIST_DEGLITCH		BIST_DIS	RESERVED	RESERVED	OC_BIST_EN	LBIST_EN	ABIST_EN	07h	Yes
0x0E	SAFETY_CHECK_CTRL_1	R/W	ERR_PIN_DEEP_SAFE_EN	FS_EN	SEL_VREF	RESERVED	WD_DIS	CFG_CRC_ERR_DEEP_SAFE_EN	RESERVED	RESERVED	40h	Yes
0x0F	SAFETY_CHECK_CTRL_2	R/W	RESERVED	START-UP_MCU_REQUEST	MAIN_DIAG_MCU_REQUEST	RST_MCU_REQUEST	DEEP_SAFE_MCU_REQUEST	NORMAL_MCU_REQUEST	DIAG_EXIT	WD_RST_EN	00h	No
0x10	SAFETY_FUNC_CFG_1 (17)	R/W	NO_RST_TO_DEEP_SAFE	ERR_PIN_MODE	WD_CFG	ON_DEMAND_DIAG	DIS_ERR_PIN_MON	DIS_FB_MISMATCH_MON	VCC_UV_THR		04h	Yes
0x11	SAFETY_FUNC_CFG_2 (17)	R/W	EN_EXIT_MAIN_DAIG	EN_EXIT_NORMAL	EN_OVUV_TEST_DEEP_SAFE	EN_EXIT_RESET	EN_EXIT_DEEP_SAFE	EN_EXIT_PRE_DIAG	EN_EXIT_START-UP	RESERVED	DEh	Yes
0x12	SAFETY_ERR_STAT	R	RESERVED	RESERVED	ERR_PIN_FAIL	WD_FAIL_FLAG	RST_ERR_CNT				00h	No
0x13	SAFETY_ERR_PIN_H (17)	R/W	ERR_PIN_H								A8h	Yes
0x14	SAFETY_ERR_PIN_L (17)	R/W	ERR_PIN_L								3Dh	Yes
0x15	SAFETY_CFG_CRC_1	R	CFG_CRC_1								00h	No
0x16	SAFETY_CFG_CRC_2	R	CFG_CRC_2								00h	No
0x19	DIAG_CFG_CTRL	R/W	MUX_EN	SPI_SDO_CTRL	MUX_OUTPUT_CTRL	INT_CON_TEST_CFG			MUX_CFG		00h	No
0x1A	DIAG_MUX_SEL	R/W	MUX_CHANNEL_GROUP				MUX_CHANNEL				00h	No
0x1B	INTERRUPT	W1C	INTERRUPT_CODE								00h	No
0x1C	INT_MASK_CFG_1 (17)	R/W	MASK_HV_BUCK_OVUV	MASK_LV_BUCK_OVUV	MASK_BOOST_OVUV	MASK_LVBK_BT_PO_UV	MASK_BG_WARN	MASK_HV_BUCK_OC	MASK_LV_BUCK_OC	MASK_BOOST_OC	00h	Yes
0x1D	INT_MASK_CFG_2 (17)	R/W	MASK_OT_WARN	MASK_BIST_RUN	MASK_VSNS_UV	MASK_VIN_OVUV	MASK_ALL_PG_OK	MASK_BIST_ERR	MASK_VCC_UV	MASK_VEXT_OVUV	00h	Yes
0x1E	INT_MASK_CFG_3 (17)	R/W	MASK_DEEP_SAFE_TOUT	MASK_RST_TOUT	MASK_BIST_DONE	MASK_FS_ASSERT	MASK_RST_ASSERT	MASK_RST_ERR_CNT_FULL	MASK_WD_ERR_CNT_FULL	MASK_WD_STATUS_ERR	00h	Yes

Table 18: SPI Bitmapping *(continued)*

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default Value (16)	OTP
Watchdog Timer												
0x1F	WDT_TOKEN_FDBCK (17)	R/W	FDBK			SEED					00h	Yes
0x20	WDT_CLOSED_WIN_CFG (17)	R/W	RESERVED	RT							3Fh	Yes
0x21	WDT_OPEN_WIN_CFG (17)	R/W	RESERVED	RESERVED	RESERVED	RW					18h	Yes
0x22	WDT_TOKEN_VALUE	R	WD_CNT_STAT		RESERVED	WD_TOKEN					00h	N
0x23	WDT_STATUS_1	W1C	RESERVED		WD_TOKEN_ERR	WD_WRONG_CFG	WD_CFG_CHG	WD_SEQ_ERR	WD_TIMEOUT	WD_TOKEN_EARLY	00h	N
0x24	WDT_STATUS_2	R	WD_ANSW_CNT		RESERVED	RESERVED	RESERVED	WD_ERR_CNT			00h	N
0x25	WDT_ANSWER	R/W	WD_ANSW								00h	N
Power Management												
0x26	HV_BUCK_PWR	R/W	SEQ1		HV_BUCK_FB_REF						14h	Yes
0x27	LV_BUCK_PWR	R/W	SEQ2		LV_BUCK_FB_REF						22h	Yes
0x28	BOOST_PWR	R/W	SEQ3		BOOST_FB_REF						0Ch	Yes
0x29	FREQ_CTRL_1	R/W	FREQ_RATIO_HVLVBUCK		LV_BUCK_FREQ						E2h	Yes
0x2A	FREQ_CTRL_2	R/W	FREQ_SET	SYNC_OUT_CHNL		PHASE_SHIFT1	PHASE_SHIFT 2	PHASE_SHIFT 3	SYNC_OUT_EN	SYNC_INOUT_SEL	46h	Yes
0x2B	FREQ_CTRL_3	R/W	FREQ_DITHER_EN	FREQ_DITHER_CYCLE				FREQ_DITHER_RANGE			37h	Yes
0x2C	PG_CTRL_1	R/W	MASK_PG	RESERVED	PG_SEL		PG1_LOW_HYS	PG1_LOW_THR	PG1_UPPER_HYS	PG1_UPPER_THR	0Ah	Yes
0x2D	PG_CTRL_2	R/W	PG2_LOW_HYS	PG2_LOW_THR	PG2_UPPER_HYS	PG2_UPPER_THR	PG3_LOW_HYS	PG3_LOW_THR	PG3_UPPER_HYS	PG3_UPPER_THR	AAh	Yes
0x2E	AAM_CCM_1	R/W	AAM_THR_1							AAM/CCM_1	50h	Yes
0x2F	AAM_CCM_2	R/W	AAM_THR_2					RESERVED	AAM/CCM_2	NON_SYNC_MD	50h	Yes
0x30	AAM_CCM_3	R/W	AAM_THR_3							AAM/CCM_3	00h	Yes
0x31	SOFT_START_TIME	R/W	SOFT_START_TIME_1		SOFT_START_TIME_2		SOFT_START_TIME_3		INIT_PKCLM_BT		55h	Yes
0x32	OV_CTRL_1	R/W	HV_BUCK_OV_THR			HV_BUCK_OV_HYS	LV_BUCK_OV_THR			LV_BUCK_OV_HYS	22h	Yes
0x33	OV_CTRL_2	R/W	VEXT1_OV_THR			VEXT1_OV_HYS	BOOST_OV_THR			BOOST_OV_HYS	22h	Yes
0x34	OV_CTRL_3	R/W	VEXT2_OV_THR			VEXT2_OV_HYS	VIN_OVP_THR		VEXT1_OVUV_EN	VEXT2_OVUV_EN	20h	Yes
0x35	UV_CTRL_1	R/W	HV_BUCK_UV_THR			HV_BUCK_UV_HYS	LV_BUCK_UV_THR			LV_BUCK_UV_HYS	22h	Yes
0x36	UV_CTRL_2	R/W	VEXT1_UV_THR			VEXT1_UV_HYS	BOOST_UV_THR			BOOST_UV_HYS	22h	Yes
0x37	UV_CTRL_3	R/W	VEXT2_UV_THR			VEXT2_UV_HYS	VSNS_UV_THR			RESERVED	28h	Yes
0x38	CURRENT_LIM_1	R/W	PEAK_ILIM1_THR				VALLEY_ILIM1_THR				00h	Yes
0x39	CURRENT_LIM_2	R/W	PEAK_ILIM2_THR				VALLEY_ILIM2_THR				00h	Yes
0x3A	CURRENT_LIM_3	R/W	PEAK_ILIM3_THR				VALLEY_ILIM3_THR				00h	Yes
0x3B	VEXT_1	R/W	VEXT_1_SET								16h	Yes
0x3C	VEXT_2	R/W	VEXT_2_SET								24h	Yes
0x3E	DIG_CTRL (17)	R/W	RESERVED		CRC_CHK_SEL	RST_BF_ST	SPI_PEC_EN	LV_CHNL_EN		MAIN_CLK_SEL_CFG	26h	Yes
0x3F	TOFF_DELAY	R/W	RESERVED		HVBK_TOFF_DELAY		LVBK_TOFF_DELAY		BOOST_TOFF_DELAY		00h	Yes

Table 18: SPI Bitmapping *(continued)*

Add.	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default Value (16)	OTP
0x40	MEM_OTP_CHK_EN	R/W	RESERVED						OTP_CRC_CHK	CRC_CHK_EN	00h	No
0x44	STORE_USER_ALL	Send	RESERVED							STORE_USER_ALL	-	No
0x45	RESTORE_USER_ALL	Send	RESERVED							RESTORE_USER_ALL	-	No
0x6F	PIN_FB_STATUS	W1C	RESERVED			PREWRN_FB_MISMATCH	PG_FB_MISMATCH	FS_FB_MISMATCH	RST_FB_MISMATCH	INT_FB_MISMATCH	00h	No
0x7E	FREQ_REFRESH (17)	R/W	RESERVED							FREQ_REFRESH	00h	No
0x7F	PWD_WR_LOCK	R/W	RESERVED							SW_LOCK	00h	No

Notes:

16) This is applicable to the initial factory “0000” code default. If available, the default values can be redefined via the OTP.
17) This register is protected by SW_LOCK; disable PWD_WR_LOCK to enable write access.
18) In addition to the above registers, the MPQ79331FS also provides some trimming options to enable or mask some actions, such as VMON1/2 OV/UV triggering the device to enter DEEP SAFE, HVBK/LVBK/LVBT OV/UV triggering the device to enter DEEP SAFE, V_{IN} < 4.5V triggering the device to enter DEEP SAFE, and MAIN DIAGNOSTIC timeout. Contact an MPS FAE for more details regarding these configuration options.

REGISTER DESCRIPTION

DEVICE STATUS REGISTERS

DEV_REV (0x00)

The DEV_REV command returns the device information.

Bits	Access	Name	Description
D[7:4]	R/W	MAJOR_REV	Returns the device's major revision code.
D[3:0]	R/W	MINOR_REV	Returns the device's minor revision code.

DEV_ID (0x01)

The DEV_ID command returns the revision information.

Bits	Access	Name	Description
D[7:4]	R/W	ID	Returns the device's identification number.
D[3:0]	R/W	SILICON_INFO	Returns the device's silicon information.

DEV_STAT (0x02)

The DEV_STAT command returns the device's state.

Bits	Access	Name	Description
D[7:4]	R	CURRENT_STATE	0000: Scan LBIST state 0001: RESTORE OTP state 0010: DEEP SAFE state 0011: PRE-DIAGNOSTIC state 0100: START-UP state 0101: MAIN DIAGNOSTIC state 0110: NORMAL state 0111: RESET state 1000: STORE USER state 1001: RESTORE USER state Other values are not valid.
D[3]	R	WU_LVL	0: The WAKE pin's current level is low 1: The WAKE pin's current level is high
D[2]	R	OTP_IND	0: OTP programming is not complete 1: OTP programming is complete
D[1:0]	R	RESERVED	Reserved.

SAFETY AND DIAGNOSTIC REGISTERS

SAFETY_STAT_1 (0x03)

The SAFETY_STAT_1 command returns the over-voltage/under-voltage (OV/UV) statuses of the monitored voltage and BG error flags. The flags can only be cleared once the fault has been removed and a write-one-to-clear (W1C) has been sent to register 0x1B.

Bits	Access	Name	Description
D[7]	R	VIN_OV	0: No OV condition has occurred at the VIN pin 1: An OV condition has occurred at the VIN pin
D[6]	R	VIN_UV	0: No UV condition has occurred at the VIN pin 1: A UV condition has occurred at the VIN pin
D[5]	R	VEXT1_OV	0: No OV condition has occurred at the VMON1 pin 1: An OV condition has occurred at the VMON1 pin

D[4]	R	VEXT1_UV	0: No UV condition has occurred at the VMON1 pin 1: A UV condition has occurred at the VMON1 pin
D[3]	R	VEXT2_OV	0: No OV condition has occurred at the VMON2 pin 1: An OV condition has occurred at the VMON2 pin
D[2]	R	VEXT2_UV	0: No UV condition has occurred at the VMON2 pin 1: A UV condition has occurred at the VMON2 pin
D[1]	R	VCC2_UV	0: No UV condition has occurred on VCC2 1: A UV condition has occurred on VCC2
D[0]	R	VCC1_UV	0: No UV condition has occurred on VCC1 1: A UV condition has occurred on VCC1

SAFETY_STAT_2 (0x04)

The SAFETY_STAT_2 command returns the battery pre-warning and current error flag statuses.

Bits	Access	Name	Description
D[7]	R	VSNS_UV	0: No UV condition has occurred at the VSNS pin 1: An UV condition has occurred at the VSNS pin
D[6]	R	HV_BUCK_ILKG_ERR	0: The HV buck leakage current is within the normal range 1: The HV buck leakage current is beyond the normal range
D[5]	R	LV_BUCK_ILKG_ERR	0: The LV buck leakage current is within the normal range 1: The LV buck leakage current is beyond the normal range
D[4]	R	BOOST_ILKG_ERR	0: The boost leakage current is within the normal range 1: The boost leakage current is beyond the normal range
D[3]	R	HV_BUCK_ILIM	0: No current limit violation has occurred on the HV buck 1: A current limit violation has occurred on the HV buck
D[2]	R	LV_BUCK_ILIM	0: No current limit violation has occurred on the LV buck 1: A current limit violation has occurred on the LV buck
D[1]	R	BOOST_ILIM	0: No current limit violation has occurred on the boost 1: A current limit violation has occurred on the boost
D[0]	R	BG_ERR	0: The bandgap reference is within the regulated range 1: The bandgap reference is out of the regulated range This bit reports if the voltage difference between bandgap (BG) references exceeds 15%. If so, the device enters DEEP SAFE; a BG fault can pull the /INT pin low.

SAFETY_STAT_3 (0x05)

The SAFETY_STAT_3 command returns the UV/OV statuses for the output rails and VCC.

Bits	Access	Name	Description
D[7]	R	HV_BUCK_OV	0: No OV condition has occurred at the HV buck output 1: An OV condition has occurred at the HV buck output
D[6]	R	HV_BUCK_UV	0: No UV condition has occurred at the HV buck output 1: A UV condition has occurred at the HV buck output
D[5]	R	LV_BUCK_OV	0: No OV condition has occurred at the LV buck output 1: An OV condition has occurred at the LV buck output
D[4]	R	LV_BUCK_UV	0: No UV condition has occurred at the LV buck output 1: A UV condition has occurred at the LV buck output
D[3]	R	BOOST_OV	0: No OV condition has occurred at the boost output 1: An OV condition has occurred at the boost output

D[2]	R	BOOST_UV	0: No UV condition has occurred at the boost output 1: A UV condition has occurred at the boost output
D[1]	R	LV_BUCK_PO_UV	0: No UV condition has occurred at the LV buck power stage 1: A UV condition has occurred at the LV buck power stage
D[0]	R	BOOST_PO_UV	0: No UV condition has occurred at the boost power stage 1: A UV condition has occurred at the boost power stage

SAFETY_STAT_4 (0x06)

The SAFETY_STAT_4 command returns the OV and OT flag statuses.

Bits	Access	Name	Description
D[7]	R	HV_BUCK_18%OV	0: No 18% OV condition has occurred at the HV buck output 1: An 18% OV has occurred at the HV buck output
D[6]	R	LV_BUCK_18%OV	0: No 18% OV condition has occurred at the LV buck output 1: An 18% OV has occurred at the LV buck output
D[5]	R	BOOST_18%OV	0: No 18% OV condition has occurred at the boost output 1: An 18% OV has occurred at the boost output
D[4]	R	OT	0: No OT error flag 1: There is an OT error flag
D[3]	R	OT_WARN	0: No OT warning flag 1: There is an OT warning flag
D[2]	R	HV_BUCK_PG_OK	0: The HV buck's power good (PG) is okay 1: The HV buck's PG is not okay
D[1]	R	LV_BUCK_PG_OK	0: The LV buck's power good (PG) is okay 1: The LV buck's PG is not okay
D[0]	R	BOOST_PG_OK	0: The boost converter's PG is okay 1: The boost converter's PG is not okay

SAFETY_STAT_5 (0x07)

The SAFETY_STAT_5 command returns the overtime flags.

Bits	Access	Name	Description
D[7]	R	PRE_DIAG_TOUT	0: No PRE-DIAGNOSTIC state overtime sign has occurred 1: A PRE-DIAGNOSTIC state overtime sign has occurred
D[6]	R	MAIN_DIAG_TOUT	0: No MAIN DIAGNOSTIC state overtime sign has occurred 1: A MAIN DIAGNOSTIC state overtime sign has occurred
D[5]	R	RST_TOUT	0: No RESET state overtime sign has occurred 1: A RESET state overtime sign has occurred
D[4]	R	STARTUP_TOUT	0: No START-UP state overtime sign has occurred 1: A START-UP state overtime sign has occurred
D[3]	R	DEEP_SAFE_TOUT	0: No DEEP SAFE state overtime sign has occurred 1: A DEEP SAFE state overtime sign has occurred
D[2]	R	RST_8S	0: The /RST pin has asserted low for less than 8s 1: The /RST pin has asserted low for more than 8s
D[1]	R	SCAN_LBIST_DONE	0: The LBIST scan is not complete 1: The LBIST scan has completed This bit cannot be cleared once the LBIST scan has completed.
D[0]	R	RESERVED	Reserved. Always reads as 0.

SAFETY_STAT_6 (0x08)

The SAFETY_STAT_6 command returns the /FS and /RST statuses, as well as the WD error counter.

Bits	Access	Name	Description
D[7]	R	FS_ASSERT	0: The /FS pin asserts low (active) 1: The /FS pin is high (inactive)
D[6]	R	RST_ASSERT	0: /RST pin asserts low (active) 1: The /RST pin is high (inactive)
D[5]	R	PIN_FB_MISMATCH	0: No mismatch has been detected between the /PREWRN, PG, /RST, /FS, or /INT pin feedback, as well as the /PREWRN, PG, /RST, /FS, or /INT logic output commands 1: A mismatch between the /PREWRN, PG, /RST, /FS, or /INT pin feedback and /PREWRN, PG, /R 0.08 ST, /FS, or /INT logic output commands has been detected, such as a short to GND or VDD or open circuit This function can be disabled or enabled via SAFETY_FUNC_CFG_1, bit[2]. Register PIN_FB_STATUS provides mismatch details. Either of the following conditions will also trigger this fault report: • If the MPQ70331's PG pin is connected to another IC's output pin in the system (such as another PG pin) and the external output pin outputs a high or low voltage which is different from the MPQ70331FS's PG pin, this bit reports a fault because the feedback on PG is not the same as its logic output command. The same applies for the /PREWRN, /RST, /FS, and /INT pins. • If the PG pin was not used in a system and was not pulled up, this bit may report a fault. The same applies for the /PREWRN, /RST, /FS, and /INT pins.
D[4]	R	SCAN_LBIST_ERR	0: Scan LBIST ran and was completed without failure 1: Scan LBIST has failed
D[3]	R	RESERVED	Reserved. Always reads as 0.
D[2]	R	WD_ERR_CNT_FULL	0: The watchdog error counter has not reached 7 (7 + 1 times the watchdog error counter makes this register full) 1: The watchdog error counter has reached 7 (7 + 1 times the watchdog error counter makes this register full) When the watchdog error counter reaches the count of 7, this bit reports. It cannot be cleared automatically, even if the watchdog is okay; write 1 to 0x1B, bit[5] to clear the fault.
D[1]	R	RST_ERR_CNT_FULL	0: The RST counter has not reached the RST_ERR_THR count 1: The RST counter has reached the RST_ERR_THR count
D[0]	R	BG_WARN	0: The bandgap reference is within the regulated range 1: The bandgap reference is out of the regulated range This bit reports if the voltage difference between bandgap (BG) references exceeds 5%. The MPQ70331FS does not enter DEEP SAFE. The BG fault can pull the /INT pin low if this function is not masked in register INT_MASK_CFG1, bit[3].

SAFETY_STAT_7 (0x09)

The SAFETY_STAT_7 command returns the BIST statuses and error flags.

Bits	Access	Name	Description
D[7]	R	LOGND	0: No loss of ground has been detected 1: A loss of ground error has been detected
D[6]	R	BIST_DONE	0: MAIN DIAGNOSTIC state BIST is not complete 1: MAIN DIAGNOSTIC state BIST has completed

D[5]	R	LOCLK1	0: No loss of clock 1 has been detected 1: A loss of clock 1 error has been detected
D[4]	R	LOCLK2	0: No loss of clock 2 has been detected 1: A loss of clock 2 error has been detected
D[3]	R	LBIST_ERR	0: LBIST ran and completed without failure 1: LBIST has failed
D[2]	R	ABIST_ERR	0: ABIST ran and completed without failure 1: ABIST has failed
D[1]	R	LBIST_RUN	0: LBIST has not run since the last write-1-to-clear (W1C) 1: LBIST has run at least once after the last W1C to 0x1B, or LBIST is running Write 1 to 0x1B, bit[6] to clear this bit after LBIST is complete.
D[0]	R	ABIST_RUN	0: ABIST has not run since the last W1C 1: ABIST has run at least once after the last W1C to 0x1B, or ABIST is running Write 1 to 0x1B, bit[6] to clear this bit after ABIST is complete.

SAFETY_STAT_8 (0x0A)

The SAFETY_STAT_8 command returns the detected errors.

Bits	Access	Name	Description
D[7:6]	R	SPI_ERR_DETECTED	Indicates the SPI error status. These bits are cleared to 00 after SPI read access. If a reset to the MCU is asserted during an SPI frame transfer (causing a truncated SPI frame), then these SPI error status bits are not cleared. In this scenario, these bits maintain their status according to the truncated previous SPI frame until SPI read access. 00: No error has been detected 01: SPI SDO mismatch. If the SDO pin's expected output is not the same as the result on the SDO pin, this bit reports 10: Reserved 11: CRC error and SPI frame long/short/access error
D[5]	R	CFG_CRC_ERR	Indicates the CRC error flag status for the safety configuration registers (memory CRC). 1: The calculated CRC value for safety configuration registers does not match the expected CRC value stored in the SAFETY_CFG_CRC_1 register 0: No CRC mismatch is present
D[4]	R	OTP_CRC_ERR	Indicates the CRC error flag status for OTP (including trim bits and user page bits). 1: The calculated CRC value for OTP content does not match the expected CRC value stored in the SAFETY_CFG_CRC_2 register. If this bit is set to 1 and the device is in MAIN DIAGNOSTIC, the device transitions to DEEP SAFE 0: No CRC mismatch is present
D[3]	R	PIN_ERR_DETECTED	Indicates the /ERROR pin signal fault status. 0: A valid external /ERROR signal has been detected on the /ERROR pin 1: An invalid external /ERROR signal has been detected on the /ERROR pin The trigger condition for PIN_ERR_DETECTED is the same as ERR_PIN_FAIL. If an error occurs, the /INT pin pulls low. After an error occurs, PIN_ERR_DETECTED can be W1C by writing to the 0x1B register. The /INT pin pulls high once the error is cleared. If /ERROR status monitoring is disabled (DIS_ERR_PIN_MON = 1), then PIN_ERR_DETECTED does not report. If /ERROR status monitoring is disabled after PIN_ERR_DETECTED has reported, the fault is not cleared automatically; after W1C, the value in PIN_ERR_DETECTED is cleared to 0.

D[2]	R	WD_STATUS_ERR	0: No watchdog status error has been detected 1: A watchdog status error has been detected This includes the WDT_STAT_1 and WDT_STAT_2 register errors. It records the detailed WD information.
D[1]	R	DEEP_SAFE_MCU_ REQ	0: The MCU has not requested that the state machine transition to DEEP SAFE 1: The MCU has requested that the state machine transition to DEEP SAFE
D[0]	R	REG_WRITE/ RESTORE_ MISMATCH	0: No register WRITE/RESTORE mismatch has been detected 1: A register WRITE/RESTORE mismatch has been detected

SAFETY_ERR_CFG_1 (0x0B)

The SAFETY_ERR_CFG_1 command sets some timeout configurations.

Bits	Access	Name	Description
D[7:6]	R/W	PRE_DIAG_TIMEOUT	Sets the PRE-DIAGNOSTIC state timeout. In PRE-DIAGNOSTIC, if the pre-diagnostic is not finished within the given time window, the device transitions to DEEP SAFE. A 22ms time reference has 15% accuracy coming from the 8MHz internal oscillator. 00: 22ms 01: 44ms 10: 66ms 11: 88ms
D[5:4]	R/W	MAIN_DIAG_ TIMEOUT	Sets the MAIN DIAGNOSTIC state timeout. In MAIN DIAGNOSTIC, if the main diagnostic is not finished within the given time window, the device transitions to DEEP SAFE. A 22ms time reference has 15% accuracy coming from the 8MHz internal oscillator. 00: 350ms 01: 400ms 10: 450ms 11: 500ms
D[3:2]	R/W	RST_TIMEOUT	Sets the /RST pin hold time. The /RST output pin generates a low pulse in RESET; the pulse duration is set through this register. 00: 1ms 01: 5ms 10: 9ms 11: 15ms
D[1:0]	R/W	START-UP_TIMEOUT	Sets the START-UP state timeout. In START-UP, if all output rails are not PG within the given time window, the device transitions to DEEP SAFE. A 6ms time reference has 15% accuracy from the 8MHz internal oscillator. 00: 6ms 01: 8ms 10: 10ms 11: 15ms

SAFETY_ERR_CFG_2 (0x0C)

The SAFETY_ERR_CFG_2 command sets some timeout configurations.

Bits	Access	Name	Description
D[7:5]	R/W	DEEP_SAFE_ TIMEOUT	Sets the DEEP SAFE state timeout. DEEP SAFE is maintained for at least the DEEP_SAFE_TIME_OUT waiting time (default 100ms), in case a failure event occurs. All wake sources are masked during this time, but any wake-up events are stored. Stored wake-up events and wake-up events after this minimum wait time lead to PRE-DIAGNOSTIC or START-UP. Note that the deep safe time is as below, except for start-up. During start-up， the time in the deep safe state is 1ms. 000: 100ms 001: 150ms 010: 200ms 011: 250ms
D[4:1]	R/W	RST_ERR_THR	Resets the error counter threshold. When RST_ERR_CNT reaches this configured threshold, the device transitions to DEEP SAFE. This register can only be updated in MAIN DIAGNOSTIC.
D[0]	R/W	CFG_REG_WR_ LOCK	0: Configuration registers access is unlocked 1: Configuration registers access is locked. Only 0x0C and 0x7F can be written; other registers are all locked and cannot be written

SAFETY_BIST_CTRL (0x0D)

The SAFETY_BIST_CTRL command configures BIST control.

Bits	Access	Name	Description
D[7:6]	R/W	BIST_DEGLITCH	Controls the deglitch filter duration for every safety-monitored voltage. 00: 100μs 01: 80μs 10: 60μs 11: 40μs
D[5]	R/W	BIST_DIS	0: BIST is enabled 1: BIST is disabled When BIST_DIS is disabled, ABIST and LBIST are disabled (scan BIST is not included in this register).
D[4:3]	R/W	RESERVED	Reserved. Always reads as 0.
D[2]	R/W	OC_BIST_EN	1: OC BIST is enabled in MAIN DIAGNOSTIC 0: OC BIST is disabled in MAIN DIAGNOSTIC
D[1]	R/W	LBIST_EN	0: LBIST is disabled 1: LBIST is enabled
D[0]	R/W	ABIST_EN	0: ABIST is disabled 1: ABIST is enabled

SAFETY_CHECK_CTRL_1 (0x0E)

The SAFETY_CHECK_CTRL_1 command configures safety check control.

Bits	Access	Name	Description
D[7]	R/W	ERR_PIN_DEEP_ SAFE_EN	1: The /ERROR pin has failed to enable DEEP SAFE 0: The /ERROR pin has failed to disable DEEP SAFE
D[6]	R/W	FS_EN	0: The /FS pin’s output is disabled (always high) 1: The /FS pin’s output is enabled

D[5]	R/W	SEL_VREF	0: The VREF pin's reference is from VCC1 domain 1: The VREF pin's reference is from VCC2 domain
D[4]	R/W	RESERVED	Reserved. Always reads as 0.
D[3]	R/W	WD_DIS	0: Enable watchdog function 1: Disable watchdog function
D[2]	R/W	CFG_CRC_ERR_ DEEP_SAFE_EN	0: A CFG CRC error in MAIN DIAGNOSTIC, NORMAL, or RESET does not trigger the device to enter DEEP SAFE 1: A CFG CRC error in MAIN DIAGNOSTIC, NORMAL, or RESET triggers the device to enter DEEP SAFE
D[1:0]	R/W	RESERVED	Reserved. Always reads as 0.

SAFETY_CHECK_CTRL_2 (0x0F)

The SAFETY_CHECK_CTRL_2 command configures state control.

Bits	Access	Name	Description
D[7]	R/W	RESERVED	Reserved. Always reads as 0.
D[6]	R/W	STARTUP_MCU_ REQUEST	0: No start-up command has been received from the MCU 1: A start-up command has been received from the MCU
D[5]	R/W	MAIN_DIAG_MCU_ REQUEST	0: No MCU MAIN DIAGNOSTIC command has been received 1: An MCU MAIN DIAGNOSTIC command has been received
D[4]	R/W	RST_MCU_REQUEST	0: No RESET command has been received from the MCU 1: A RESET command has been received from the MCU
D[3]	R/W	DEEP_SAFE_MCU_ REQUEST	0: No MCU DEEP SAFE command has been received 1: An MCU DEEP SAFE command has been received
D[2]	R/W	NORMAL_MCU_ REQUEST	0: No go to NORMAL state command has been received from the MCU 1: A go to NORMAL state command has been received from the MCU
D[1]	R/W	DIAG_EXIT	0: No exit from MAIN DIAGNOSTIC to NORMAL command has been received 1: An exit from MAIN DIAGNOSTIC to NORMAL command has been received
D[0]	R/W	WD_RST_EN	0: A watchdog failure does not reset the MCU 1: A watchdog failure resets the MCU

SAFETY_FUNC_CFG_1 (0x10)

The SAFETY_FUNC_CFG_1 command sets some safety function configurations.

Bits	Access	Name	Description
D[7]	R/W	NO_RST_TO_DEEP_ SAFE	0: The device transitions from RESET to DEEP SAFE if the reset error counter reaches its threshold or /RST is low for 8s 1: The device does not transition from RESET to DEEP SAFE if the reset error counter reaches its threshold or /RST is low for 8s
D[6]	R/W	ERR_PIN_MODE	0: Low-pulse mode 1: PWM mode
D[5]	R/W	WD_CFG	0: Window watchdog 1: Question and answer watchdog
D[4]	R/W	ON_DEMAND_DIAG	0: No MCU on-demand diagnosis request has been received 1: An MCU on-demand diagnosis request has been received
D[3]	R/W	DIS_ERR_PIN_MON	0: /ERROR status monitoring is enabled 1: /ERROR status monitoring is disabled
D[2]	R/W	DIS_FB_MISMATCH_ MON	0: /PREWRN, PG, /FS, /RST, and /INT status monitoring is enabled 1: /PREWRN, PG, /FS, /RST, and /INT status monitoring is disabled

D[1:0]	R/W	VCC_UV_THR	Sets the V_{CCx} under-voltage (UV) threshold. 00: 3V (for both VCC1 and VCC2) 01: 3.5V (for both VCC1 and VCC2) 10: 4V (for both VCC1 and VCC2) 11: 4.5V (for both VCC1 and VCC2)

SAFETY_FUNC_CFG_2 (0x11)

The SAFETY_FUNC_CFG_2 command indicates sets some safety function configurations.

Bits	Access	Name	Description
D[7]	R/W	EN_EXIT_MAIN_DIAG	0: Exiting MAIN DIAGNOSTIC is disabled 1: Exiting MAIN DIAGNOSTIC is enabled
D[6]	R/W	EN_EXIT_NORMAL	0: Exiting NORMAL is disabled 1: Exiting NORMAL is enabled
D[5]	R/W	EN_OVUV_TEST_ DEEP_SAFE	0: If a VEXTx (VMONx) over-voltage (OV) or under-voltage (UV) event occurs, the device does not enter DEEP SAFE 1: If a VEXTx (VMONx) OV or UV event occurs, the device enters DEEP SAFE
D[4]	R/W	EN_EXIT_RESET	0: Exiting RESET is disabled 1: Exiting RESET is enabled
D[3]	R/W	EN_EXIT_DEEP_ SAFE	0: Exiting DEEP SAFE is disabled 1: Exiting DEEP SAFE is enabled
D[2]	R/W	EN_EXIT_PRE_DIAG	0: Exiting PRE-DIAGNOSTIC is disabled 1: Exiting PRE-DIAGNOSTIC is enabled
D[1]	R/W	EN_EXIT_STARTUP	0: Exiting START-UP is disabled 1: Exiting START-UP is enabled
D[0]	R/W	RESERVED	Reserved. Always reads as 0.

SAFETY_ERR_STAT (0x12)

The SAFETY_ERR_STAT command indicates the safety error status.

Bits	Access	Name	Description
D[7:6]	R	RESERVED	Reserved. Always reads as 0.
D[5]	R	ERR_PIN_FAIL	0: A valid external /ERROR signal has been detected on /ERROR 1: An invalid external /ERROR signal has been detected on /ERROR Once /ERROR pin monitoring is disabled via SAFETY_FUNC_CFG_1 bit[3], or a good high and a good low pulse received, this bit recovers to 0 automatically.
D[4]	R	WD_FAIL_FLAG	0: No watchdog failure has been detected 1: A watchdog failure has been detected When the watchdog error count exceeds 7, WD_FAIL_FLAG = 1, and the device enters RESET if WD_RST_EN is enabled. The WD_FAIL_FLAG returns to 0 automatically once a good WD signal occurs. WD_FAIL_FLAG returns to 0 each time the device enters MAIN DIAGNOSTIC.
D[3:0]	R	RST_ERR_CNT	Reset error counter. The default value is 0; this value is initialized upon entering DEEP SAFE. This counter increases every time the device sends a reset signal to the MCU by asserting the /RST pin low (in RESET) and is reduced every time six consecutive good watchdog refreshes are received, or power is cycled on the device. This is selectable via register SAFETY_ERR_CFG_2, bits[4:1].

SAFETY_ERR_PIN_H (0x13)

The SAFETY_ERR_PIN_H command sets the /ERROR pin's high-phase configuration.

Bits	Access	Name	Description
D[7:0]	R/W	ERR_PIN_H	Sets the /ERROR pin high-phase duration in PWM mode. This controls the expected high-phase duration with a 15μs resolution, calculated with the following equation: High-Time Duration = ERR_PIN_H, bits[7:0] x 15μs The 15μs time reference has 15% accuracy from the 8MHz internal oscillator.

SAFETY_ERR_PIN_L (0x14)

The SAFETY_ERR_PIN_L command sets the /ERROR pin's low-phase configuration.

Bits	Access	Name	Description
D[7:0]	R/W	ERR_PIN_L	Sets the /ERROR pin low-phase duration in both default low-pulse mode and PWM mode. This controls the expected low-phase duration with a 15μs resolution, calculated using the following equation: Low-Time Duration = ERR_PIN_L, bits[7:0] x 15μs The 15μs time reference has 15% accuracy from the 8MHz internal oscillator.

SAFETY_CFG_CRC_1 (0x15)

The SAFETY_CFG_CRC_1 command returns the CRC value for some safety configuration registers.

Bits	Access	Name	Description
D[7:0]	R	CFG_CRC_1	Returns the stored CRC value for the safety configuration registers.

SAFETY_CFG_CRC_2 (0x16)

The SAFETY_CFG_CRC_2 command returns the CRC value for some safety configuration registers.

Bits	Access	Name	Description
D[7:0]	R	CFG_CRC_2	Returns the stored CRC value for the OTP registers.

DIAG_CFG_CTRL (0x19)

The DIAG_CFG_CTRL command sets the diagnostic configuration control.

Bits	Access	Name	Description
D[7]	R/W	MUX_EN	0: Mux output is disabled (tri-state) 1: Mux output is enabled
D[6]	R/W	SPI_SDO_CTRL	0: The SDO pin should be low when MUX_CFG = 01 1: The SDO pin should be high when MUX_CFG = 01
D[5]	R/W	MUX_OUTPUT_CTRL	0: The mux output should be 0 when MUX_CFG = 00 1: The mux output should be 1 when MUX_CFG = 00
D[4:2]	R/W	INT_CON_TEST_CFG	000: No active interconnection test 001: The /ERROR input state is observed on the diagnostic mux output 010: The NCS input state is observed on the diagnostic mux output 011: The SDI input state is observed on the diagnostic mux output 100: The SCLK input is observed on the diagnostic mux output 101: The WDI input is observed on the diagnostic mux output 110: Invalid command 111: Invalid command

D[1:0]	R/W	MUX_CFG	00: The mux output is controlled by bit[5] of this command 01: Digital mux mode 10: Analog mux mode 11: Device interconnection mode

DIAG_MUX_SEL (0x1A)

The DIAG_MUX_SEL command sets the diagnostic configuration control.

Bits	Access	Name	Description
D[7:4]	R/W	MUX_CHANNEL_ GROUP	Selects the diagnostic mux channel group. The mux channel table is dependent on the MUX_CFG bit in the DIAG_CFG_CTRL register.
D[3:0]	R/W	MUX_CHANNEL	Selects the diagnostic mux channel. The mux channel table is dependent on the MUX_CFG bit in the DIAG_CFG_CTRL register.

INTERRUPT (0x1B)

The INTERRUPT command indicates the interruption code.

Bits	Access	Name	Description
D[7:0]	RW1C	INTERRUPT_CODE	Indicates the interrupt source code for register SAFETY_STAT_1 to SAFETY_STAT_8 (register 0x03, 0x04…0x0A). It is recommended to write 1 to clear to this register once the MPQ70331FS starts up. For more details, see Table 13 on Page 57. RW1C means this bit can be read and can be write 1 to clear.

INT_MASK_CFG1 (0x1C)

The INT_MASK_CFG1 command configures the device's under-voltage (UV), over-voltage (OV), and leakage masks for interrupts on the /INT pin.

Bits	Access	Name	Description
D[7]	R/W	MASK_HV_BUCK_ OVUV	0: A UV/OV interrupt signal sent by the HV buck is valid 1: A UV/OV interrupt signal sent by the HV buck is masked
D[6]	R/W	MASK_LV_BUCK_ OVUV	0: A UV/OV interrupt signal sent by the LV buck is valid 1: A UV/OV interrupt signal sent by the LV buck is masked
D[5]	R/W	MASK_BOOST_OVUV	0: A UV/OV interrupt signal sent by the boost is valid 1: A UV/OV interrupt signal sent by the boost is masked
D[4]	R/W	MASK_LVBK_BT_ PO_UV	0: A UV interrupt signal sent by the LV buck or LV boost power stage is valid 1: A UV interrupt signal sent by the LV buck or LV boost power stage is masked
D[3]	R/W	MASK_BG_WARN	0: The bandgap reference out of range flag is valid 1: The bandgap reference out of range flag is masked
D[2]	R/W	MASK_HV_BUCK_OC	0: An over-current (OC) interrupt signal sent by the HV buck is valid 1: An OC interrupt signal sent by the HV buck is masked
D[1]	R/W	MASK_LV_BUCK_OC	0: An OC interrupt signal sent by the LV buck is valid 1: An OC interrupt signal sent by the LV buck is masked
D[0]	R/W	MASK_BOOST_OC	0: An OC interrupt signal sent by the boost is valid 1: An OC interrupt signal sent by the boost is masked

INT_MASK_CFG2 (0x1D)

The INT_MASK_CFG2 command configures the over-temperature (OT), BIST, VCC, and battery masks for interrupts on the /INT pin.

Bits	Access	Name	Description
D[7]	R/W	MASK_OT_WARN	0: An OT error flag interrupt signal is valid 1: An OT error flag interrupt signal is masked

D[6]	R/W	MASK_BIST_RUN	0: Memory, OTP, mux, and computer logic self-test and analog self-test run signs are valid 1: Memory, OTP, mux, and computer logic self-test and analog self-test run signs are masked
D[5]	R/W	MASK_VSNS_UV	0: A UV error flag interrupt signal sent by VSNS is valid 1: A UV error flag interrupt signal sent by VSNS is masked
D[4]	R/W	MASK_VIN_OVUV	0: An OV/UV error flag interrupt signal sent by VIN is valid 1: An OV/UV error flag interrupt signal sent by VIN is masked
D[3]	R/W	MASK_ALL_PG_OK	0: Three-output PG flag interrupt signal is valid 1: Three-output PG flag interrupt signal is masked If one channel is disabled (e.g. LVBT), set MASK_ALL_PG_OK to 0; otherwise, any disabled channel always pulls /INT low.
D[2]	R/W	MASK_BIST_ERR	0: The ABIST and LBIST failure flag interrupt signal is valid 1: The ABIST and LBIST failure flag interrupt signal is masked
D[1]	R/W	MASK_VCC2_UV	0: A UV interrupt signal sent by VCC1/VCC2 is valid 1: A UV interrupt signal sent by VCC1/VCC2 is masked
D[0]	R/W	MASK_VEXT_OVUV	0: An OV/UV error flag interrupt signal sent by VEXTx (VMONx) is valid 1: An OV/UV error flag interrupt signal sent by VEXTx (VMONx) is masked

INT_MASK_CFG3 (0x1E)

The INT_MASK_CFG3 command sets the overtime, reset, and watchdog masks for interrupts on the /INT pins.

Bits	Access	Name	Description
D[7]	R/W	MASK_DEEP_SAFE_TOUT	0: The DEEP SAFE timeout interrupt signal is valid 1: The DEEP SAFE timeout interrupt signal is masked
D[6]	R/W	MASK_RST_TOUT	0: The RESET timeout interrupt signal is valid 1: RESET timeout interrupt signal is masked
D[5]	R/W	MASK_BIST_DONE	0: The BIST done interrupt signal is valid 1: The BIST done interrupt signal is masked
D[4]	R/W	MASK_FS_ASSERT	0: The /FS pin assertion interrupt signal is valid 1: The /FS pin assertion interrupt signal is masked
D[3]	R/W	MASK_RST_ASSERT	0: The /RST pin assertion interrupt signal is valid 1: The /RST pin assertion interrupt signal is masked
D[2]	R/W	MASK_RST_ERR_CNT_FULL	0: The RST_ERR_CNT full interrupt signal is valid 1: The RST_ERR_CNT full interrupt signal is masked
D[1]	R/W	MASK_WD_ERR_CNT_FULL	0: The watchdog error counter full interrupt signal is valid 1: The watchdog error counter full interrupt signal is masked
D[0]	R/W	MASK_WD_STATUS_ERR	0: The watchdog status error interrupt signal is valid 1: The watchdog status error interrupt signal is masked

WATCHDOG TIMER REGISTERS

WDT_TOKEN_FDBCK (0x1F)

The WDT_TOKEN_FDBCK command configures the watchdog token and feedback.

Bits	Access	Name	Description
D[7:5]	R/W	FDBK	These bits control the sequence of the generated questions and respective answers. There is a set of 16 generated questions; the repetition or sequence order can be adjusted by FDBK, bits[2:0]. FDBK, bits[2:1] can be used to calculate the answer.

D[4:0]	R/W	SEED	Sets the watchdog token seed value used to generate a set of new questions. The token seed value can be updated by the MCU only after watchdog initialization in MAIN DIAGNOSTIC after RESET. This only applies for Q&A mode.

WDT_CLOSED_WIN_CFG (0x20)

The WDT_CLOSED_WIN_CFG command configures the watchdog closed window.

Bits	Access	Name	Description
D[7]	R/W	RESERVED	Reserved. Always reads as 0.
D[6:0]	R/W	RT	Sets the watchdog closed window duration. See the Watchdog Operation section on page 49 for equations and more details.

WDT_OPEN_WIN_CFG (0x21)

The WDT_OPEN_WIN_CFG command configures the watchdog open window.

Bits	Access	Name	Description
D[7:5]	R/W	RESERVED	Reserved. Always reads as 0.
D[4:0]	R/W	RW	Sets the watchdog open window duration. See the Watchdog Operation section on page 49 for equations and more details.

WDT_TOKEN_VALUE (0x22)

The WDT_TOKEN_VALUE command indicates the watchdog question.

Bits	Access	Name	Description
D[7:6]	R	WD_CNT_STAT	Returns the current WD_ERR_CNT value. 00: 7 times 01: 4 times 10: 3 times 11: 1 time
D[5]	R	RESERVED	Reserved. Always reads as 0.
D[4:0]	R	WD_TOKEN	Returns the watchdog question that the MCU must read.

WDT_STATUS_1 (0x23)

The WDT_STATUS_1 command indicates the watchdog status.

Bits	Access	Name	Description
D[7:6]	R	RESERVED	Reserved. Always reads as 0.
D[5]	R	WD_TOKEN_ERR	0: Answer byte is correct 1: Answer byte is incorrect This bit is read-only, and cannot be written 1 to clear. This bit is cleared automatically by a good watchdog answer.
D[4]	RW1C	WD_WRONG_CFG	This bit is set to 1 when either WDT_OPEN_WIN_CFG or WDT_CLOSED_WIN_CFG is set to 0x00.
D[3]	RW1C	WD_CFG_CHG	This bit is set to 1 when switching between the trigger and Q&A mode, or when the settings for WDT_WIN1_CFG or WDT_WIN2_CFG is changed.
D[2]	RW1C	WD_SEQ_ERR	0: No error 1: Incorrect timing or wrong answer
D[1]	RW1C	WD_TIME_OUT	0: No watchdog timeout event has occurred 1: A watchdog timeout event has occurred
D[0]	RW1C	WD_TOKEN_EARLY	0: No error 1: All 4 answer bytes were returned during the closed window

WDT_STATUS_2 (0x24)

The WDT_STATUS_2 command indicates the watchdog status.

Bits	Access	Name	Description
D[7:6]	R	WD_ANSW_CNT	00: Watchdog answer 0 must be written 01: Watchdog answer 1 must be written 10: Watchdog answer 2 must be written 11: Watchdog answer 3 must be written
D[5:3]	R	RESERVED	Reserved. Always reads as 0.
D[2:0]	R	WD_ERR_CNT	Watchdog error counter.

WDT_ANSWER (0x25)

The WDT_ANSWER command configures the watchdog answer.

Bits	Access	Name	Description
D[7:0]	R/W	WD_ANSW	Configures the Q&A watchdog answer. See the Watchdog Operation section on page 49 for more details.

POWER MANAGEMENT REGISTERS

HV_BUCK_PWR (0x26)

The HV_BUCK_PWR command configures the HV buck's power settings.

Bits	Access	Name	Description
D[7:6]	R/W	SEQ1	00: No delay; the HV buck ramps up immediately upon entering START-UP 01: 35ms delay 10: 65ms delay 11: 100ms delay
D[5:0]	R/W	HV_BUCK_FB_REF	Sets the HV buck's output voltage. 2.3V to 5.45V, with 50mV steps.

LV_BUCK_PWR (0x27)

The LV_BUCK_PWR command configures the LV buck's power settings.

Bits	Access	Name	Description
D[7:6]	R/W	SEQ2	00: No delay; the LV buck ramps up immediately once the HV buck is power good 01: 35ms delay 10: 65ms delay 11: 100ms delay
D[5:0]	R/W	LV_BUCK_FB_REF	Sets the LV buck's output voltage. 0.6V to 3.75V with 50mV steps.

BOOST_PWR (0x28)

The BOOST_PWR command configures the LV boost converter's power settings.

Bits	Access	Name	Description
D[7:6]	R/W	SEQ3	00: No delay; the LV boost ramps up immediately once the HV buck is power good 01: 35ms delay 10: 65ms delay 11: 100ms delay
D[5:0]	R/W	BOOST_FB_REF	Sets the LV boost's output voltage. 4.4V to 7.55V with 50mV steps.

FREQ_CTRL_1 (0x29)

The FREQ_CTRL_1 command configures frequency control 1. Configure FREQ_REFRESH or restart the outputs to achieve f_{SW} control.

Bits	Access	Name	Description
D[7:6]	R/W	FREQ_RATIO_ HVLVBUCK	00: $f_{LV\_BUCK} = f_{HV\_BUCK}$ 01: $f_{LV\_BUCK} = 2 \times f_{HV\_BUCK}$ 11: $f_{LV\_BUCK} = 4 \times f_{HV\_BUCK}$ 10: Not supported
D[5:0]	R/W	LV_BUCK_FREQ	Sets the LV buck f_{SW}. 0.4MHz to 2.5MHz with 50kHz steps. After the register is changed, only a positive edge on FREQ_REFRESH can change f_{SW}. f_{LV_BUCK} = 50kHz x LV_BUCK_FREQ, bits[5:0] + 0.3MHz

FREQ_CTRL_2 (0x2A)

The FREQ_CTRL_2 command configures frequency control 2.

Bits	Access	Name	Description
D[7]	R/W	FREQ_SET	0: The frequency is set by REG FREQ_CTRL_1 1: The frequency is set by the FREQ pin
D[6:5]	R/W	SYNC_OUT_CHNL	11: SYNCOUT LV boost frequency 10: SYNCOUT LV buck frequency 01: SYNCOUT HV buck frequency 00: SYNCOUT main clock
D[4]	R/W	PHASE_SHIFT1	0: 0° between the HV buck and the main clock 1: 180° between the HV buck and the main clock
D[3]	R/W	PHASE_SHIFT2	0: 0° between the LV buck and the main clock 1: 180° between the LV buck and the main clock
D[2]	R/W	PHASE_SHIFT3	0: 0° between the LV boost and the main clock 1: 180° between the LV boost and the main clock
D[1]	R/W	SYNC_OUT_EN	0: The SYNCOUT function is disabled, the SYNC pin outputs V_{CC}. The SYNC pin can be floated 1: The SYNCOUT function is enabled
D[0]	R/W	SYNC_INOUT_SEL	0: SYNCOUT (see D[1]) 1: SYNCIN If SYNCIN is selected and there is no signal at the SYNC pin, connect the SYNC pin to GND; in this setting, the device switches with the internal default frequency.

FREQ_CTRL_3 (0x2B)

The FREQ_CTRL_3 command configures frequency control 3.

Bits	Access	Name	Description
D[7]	R/W	FREQ_DITHER_EN	0: Frequency dithering is disabled 1: Frequency dithering is enabled
D[6:3]	R/W	FREQ_DITHER_ CYCLE	The modulation cycle time (t_{MOD}) can be calculated with the following equation: t_{MOD} = FREQ_DITHER_CYCLE, bits[3:0] x 13µs
D[2:0]	R/W	FREQ_DITHER_ RANGE	The peak-to-peak modulation frequency range (FP2P) can be calculated with the following equation: FP2P = FREQ_DITHER_ RANGE, bits[2:0] x 3.85%

PG_CTRL_1 (0x2C)

The PG_CTRL_1 command configures PG control 1.

Bits	Access	Name	Description
D[7]	R/W	MASK_PG	0: The PG function is active 1: The PG function is masked
D[6]	R/W	RESERVED	Reserved. Always reads as 0.
D[5:4]	R/W	PG_SEL	00: The PG pin indicates that all 3 rails are PG 01: The PG pin indicates that V_{OUT1} is PG 10: The PG pin indicates that V_{OUT2} is PG 11: The PG pin indicates that V_{OUT3} is PG If one of the converter is disabled (e.g. LVBT), do not set PG_SEL to 00; otherwise PG will always assert because there is no output on VOUT3.
D[3]	R/W	PG1_LOW_HYS	0: 5% x VOUT1_SET 1: 2.5% x VOUT1_SET
D[2]	R/W	PG1_LOW_THR	0: 90% x VOUT1_SET 1: 85% x VOUT1_SET
D[1]	R/W	PG1_UPPER_HYS	0: 5% x VOUT1_SET 1: 2.5% x VOUT1_SET
D[0]	R/W	PG1_UPPER_THR	0: 110% x VOUT1_SET 1: 115% x VOUT1_SET

PG_CTRL_2 (0x2D)

The PG_CTRL_2 command configures PG control 2.

Bits	Access	Name	Description
D[7]	R/W	PG2_LOW_HYS	0: 5% of VOUT2_SET 1: 2.5% of VOUT2_SET
D[6]	R/W	PG2_LOW_THR	0: 90% of VOUT2_SET 1: 85% of VOUT2_SET
D[5]	R/W	PG2_UPPER_HYS	0: 5% of VOUT2_SET 1: 2.5% of VOUT2_SET
D[4]	R/W	PG2_UPPER_THR	0: 110% of VOUT2_SET 1: 115% of VOUT2_SET
D[3]	R/W	PG3_LOW_HYS	0: 5% of VOUT3_SET 1: 2.5% of VOUT3_SET
D[2]	R/W	PG3_LOW_THR	0: 90% of VOUT3_SET 1: 85% of VOUT3_SET
D[1]	R/W	PG3_UPPER_HYS	0: 5% of VOUT3_SET 1: 2.5% of VOUT3_SET
D[0]	R/W	PG3_UPPER_THR	0: 110% of VOUT3_SET 1: 115% of VOUT3_SET

AAM_CCM_1 (0x2E)

The AAM_CCM_1 command configures AAM mode and CCM for the HV buck.

Bits	Access	Name	Description
D[7:1]	R/W	AAM_THR_1	Sets the HV buck's AAM mode threshold. 0mA to 1055mA.
D[0]	R/W	AAM/CCM_1	0: HV buck operates in AAM mode 1: HV buck operates in CCM

AAM_CCM_2 (0x2F)

The AAM_CCM_2 command configures AAM mode and CCM for the LV buck.

Bits	Access	Name	Description
D[7:3]	R/W	AAM_THR_2	Sets the LV buck's AAM mode threshold. 0mA to 1055mA.
D[2]	R/W	RESERVED	Reserved. Always reads as 0.
D[1]	R/W	AAM/CCM_2	0: LV buck operates in AAM mode 1: LV buck operates in CCM
D[0]	R/W	NON_SYNC_MD	0: The boost operates in synchronous mode 1: The boost operates in asynchronous mode

AAM_CCM_3 (0x30)

The AAM_CCM_3 command configures AAM mode and CCM for the LV boost.

Bits	Access	Name	Description
D[7:1]	R/W	AAM_THR_3	Sets the LV boost's AAM mode threshold. 0mA to 1055mA.
D[0]	R/W	AAM/CCM_3	0: LV boost operates in AAM mode 1: LV boost operates in CCM

SOFT_START_TIME (0x31)

The SOFT_START_TIME command configures soft-start control.

Bits	Access	Name	Description
D[7:6]	R/W	SOFT_START_TIME_1	Sets the soft-start time for the HV buck. 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms
D[5:4]	R/W	SOFT_START_TIME_2	Sets the soft-start time for the LV buck. 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms
D[3:2]	R/W	SOFT_START_TIME_3	Sets the soft-start time for the LV boost. 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms
D[1:0]	R/W	RESERVED	Reserved. Always reads as 01.

OV_CTRL_1 (0x32)

The OV_CTRL_1 command configures the over-voltage (OV) threshold and hysteresis for the HV buck and LV buck.

Bits	Access	Name	Description
D[7:5]	R/W	HV_BUCK_OV_THR	The OV threshold can be calculated with the following equation: (1 + (HV_BUCK_OV_THR, bits[2:0] + 1) x 2%) x VOUT1_SET It is not recommended to use a 2% threshold.
D[4]	R/W	HV_BUCK_OV_HYS	1: 4% of VOUT1_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% of VOUT1_SET

D[3:1]	R/W	LV_BUCK_OV_THR	The OV threshold can be calculated with the following equation: (1 + (LV_BUCK_OV_THR, bits[2:0] + 1) x 2%) x VOUT2_SET It is not recommended to use a 2% threshold.
D[0]	R/W	LV_BUCK_OV_HYS	1: 4% x VOUT2_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VOUT2_SET

OV_CTRL_2 (0x33)

The OV_CTRL_2 command configures the OV threshold and hysteresis for VEXT1 and the LV boost.

Bits	Access	Name	Description
D[7:5]	R/W	VEXT1_OV_THR	The OV threshold can be calculated with the following equation: (1 + (VEXT1_OV_THR, bits[2:0] + 1) x 2%) x VEXT1_SET It is not recommended to use a 2% threshold.
D[4]	R/W	VEXT1_OV_HYS	1: 4% x VEXT1_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VEXT1_SET
D[3:1]	R/W	BOOST_OV_THR	The OV threshold can be calculated with the following equation: (1 + (BOOST_OV_THR, bits[2:0] + 1) x 2%) x VOUT3_SET It is not recommended to use a 2% threshold.
D[0]	R/W	BOOST_OV_HYS	1: 4% x VOUT3_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VOUT3_SET

OV_CTRL_3 (0x34)

The OV_CTRL_3 command configures the OV threshold and hysteresis for VEXT2, the OVP threshold for VIN, and enables OV/UV detection for VEXTx.

Bits	Access	Name	Description
D[7:5]	R/W	VEXT2_OV_THR	The OV threshold can be calculated with the following equation: (1 + (VEXT2_OV_THR, bits[2:0] + 1) x 2%) x VEXT1_SET It is not recommended to use a 2% threshold.
D[4]	R/W	VEXT2_OV_HYS	1: 4% x VEXT1_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VEXT1_SET
D[3:2]	R/W	VIN_OVP_THR	The OVP threshold can be calculated with the following equation: (1 + (VIN_OVP_THR, bits[1:0] + 1) x 10%) x 14V
D[1]	R/W	VEXT1_OVUV_EN	0: VEXT1 (VMON1) OV/UV detection is disabled 1: VEXT1 (VMON1) OV/UV detection is enabled VEXT1_OVUV_EN should be disabled in DEEP SAFE and enabled after the monitored voltage PG. It is recommended to configure this bit to be disabled first, then enabled after the monitored voltage PG in MAIN DIAGNOSTIC or NORMAL.
D[0]	R/W	VEXT2_OVUV_EN	0: VEXT2 (VMON2) OV/UV detection is disabled 1: VEXT2 (VMON2) OV/UV detection is enabled VEXT2_OVUV_EN should be disabled in DEEP SAFE and enabled after the monitored voltage PG. It is recommended to configure this bit to be disabled first, then enabled after the monitored voltage PG in MAIN DIAGNOSTIC or NORMAL.

UV_CTRL_1 (0x35)

The UV_CTRL_1 command configures the under-voltage (UV) control 1 threshold and hysteresis for the HV buck and LV buck..

Bits	Access	Name	Description
D[7:5]	R/W	HV_BUCK_UV_THR	The UV threshold can be calculated with the following equation: (1 - (HV_BUCK_UV_THR, bits[2:0] + 1) x 2%) x VOUT1_SET It is not recommended to use a 2% threshold.
D[4]	R/W	HV_BUCK_UV_HYS	1: 4% x VOUT1_SET (if the threshold is set to 4%, the hysteresis is 1%) 0: 1% x VOUT1_SET
D[3:1]	R/W	LV_BUCK_UV_THR	The UV threshold can be calculated with the following equation: (1 - (LV_BUCK_UV_THR, bits[2:0] + 1) x 2%) x VOUT2_SET It is not recommended to use a 2% threshold.
D[0]	R/W	LV_BUCK_UV_HYS	1: 4% x VOUT2_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VOUT2_SET

UV_CTRL_2 (0x36)

The UV_CTRL_2 command configures the UV threshold and hysteresis for VEXT1 and the LV boost.

Bits	Access	Name	Description
D[7:5]	R/W	VEXT1_UV_THR	The UV threshold can be calculated with the following equation: (1 - (VEXT1_UV_THR, bits[2:0] + 1) x 2%) x VEXT1_SET It is not recommended to use a 2% threshold.
D[4]	R/W	VEXT1_UV_HYS	1: 4% x VEXT1_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VEXT1_SET
D[3:1]	R/W	BOOST_UV_THR	The UV threshold can be calculated with the following equation: (1 - (BOOST_UV_THR, bits[2:0] + 1) x 2%) x VOUT3_SET It is not recommended to use a 2% threshold.
D[0]	R/W	BOOST_UV_HYS	1: 4% x VOUT3_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VOUT3_SET

UV_CTRL_3 (0x37)

The UV_CTRL_3 command configures the under-voltage (UV) threshold and hysteresis for VEXT2 and the VSENSE pin.

Bits	Access	Name	Description
D[7:5]	R/W	VEXT2_UV_THR	The UV threshold can be calculated with the following equation: (1 - (VEXT2_UV_THR, bits[2:0] + 1) x 2%) x VEXT2_SET It is not recommended to use a 2% threshold.
D[4]	R/W	VEXT2_UV_HYS	1: 4% x VEXT2_SET (if the threshold is set to 4%, the hysteresis is forced to 1%) 0: 1% x VEXT2_SET
D[3:1]	R/W	VSNS_UV_THR	Sets the VSENSE pin UV threshold. 6.5V to 10V with 0.5V steps (default 8.5V).

D[0]	R/W	RESERVED	Reserved. Always reads as 0.

CURRENT_LIM_1 (0x38)

The CURRENT_LIM_1 command configures current limit setting 1.

Bits	Access	Name	Description
D[7:4]	R/W	PEAK_ILIM1_THR	0000: 4A 0001: 3.5A 0010: 3A 1110: 5A 1111: 4.5A Others: Reserved
D[3:0]	R/W	VALLEY_ILIM1_THR	0000: 3A 0001: 2.5A 0010: 4A 0011: 3.5A 0110: 2A Others: Reserved

CURRENT_LIM_2 (0x39)

The CURRENT_LIM_2 command configures current limit setting 2.

Bits	Access	Name	Description
D[7:4]	R/W	PEAK_ILIM2_THR	0000: 4A 0001: 3.5A 0010: 3A 1110: 5A 1111: 4.5A Others: Reserved
D[3:0]	R/W	VALLEY_ILIM2_THR	0000: 3A 0001: 2.5A 0010: 4A 0011: 3.5A 0110: 2A Others: Reserved

CURRENT_LIM_3 (0x3A)

The CURRENT_LIM_3 command configures current limit setting 3.

Bits	Access	Name	Description
D[7:4]	R/W	PEAK_ILIM3_THR	0000: 1.2A 0010: 1.4A 0011: 1.3A 0100: 1.6A 0101: 1.5A 0110: 1.8A 0111: 1.7A Others: Reserved
D[3:0]	R/W	VALLEY_ILIM3_THR	0000: 0.7A 0001: 0.775A 0010: 0.85A 0011: 0.925A 0100: 1A 0101: 1.075A 0110: 1.15A 0111: 1.225A Others: Reserved

VEXT_1 (0x3B)

The VEXT_1 command configures external monitored voltage setting 1.

Bits	Access	Name	Description
D[7:0]	R/W	VEXT_1_SET	0.6V to 12.75V with 50mV steps (default 1.1V). Clamped to 0.6V when set below 0.6V. The value can be calculated with the following equation: $V_{EXT\_1\_SET}$ = VEXT_1_SET, bits[7:0] x 0.05

VEXT_2 (0x3C)

The VEXT_2 command configures external monitored voltage setting 2.

Bits	Access	Name	Description
D[7:0]	R/W	VEXT_2_SET	0.6V to 12.75V with 50mV steps (default 1.8V). Clamped to 0.6V when set below 0.6V. The value can be calculated with the following equation: $V_{EXT\_2\_SET}$ = VEXT_2_SET, bits[7:0] x 0.05

DIG_CTRL (0x3E)

The DIG_CTRL command configures the channel control.

Bits	Access	Name	Description
D[7:6]	R/W	RESERVED	Reserved. Always reads as 00.
D[5]	R/W	CRC_CHK_SEL	0: One-time CFG CRC check at the positive edge of CRC_CHK_EN; one-time OTP CRC check at the positive edge of OTP_CHK_EN 1: Continuous CFG CRC check when CRC_CHK_EN = 1; continuous OTP CRC check when OTP_CHK_EN = 1
D[4]	R/W	RST_BF_ST	0: The /RST pin value is 0 1: The /RST pin value is 1 In NORMAL and MAIN DIAGNOSTIC, /RST is always high. In SCAN LBIST and RESET, /RST is always low. In other states, the /RST default voltage depends on this bit.
D[3]	R/W	SPI_PEC_EN	0: SPI communication packet error checking (PEC) disabled 1: SPI communication packet error checking (PEC) enabled
D[2:1]	R/W	LV_CHNL_EN	00: Both LV buck and LV boost are disabled 01: LV boost is disabled, LV buck is enabled 10: LV boost is enabled, LV buck is disabled 11: Both LV buck and LV boost are enabled
D[0]	R/W	MAIN_CLK_SEL_CFG	0: The main clock is CLK2 1: The main clock is CLK1

TOFF_DELAY (0x3F)

The TOFF_DELAY command configures the turn-off delays for the HV buck, LV buck, and LV boost.

Bits	Access	Name	Description
D[7:6]	R/W	RESERVED	Reserved. Always reads as 00.
D[5:4]	R/W	HVBK_TOFF_DELAY	00: 100µs 01: 200µs 10: 400µs 11: 800µs
D[3:0]	R/W	LVBK_TOFF_DELAY	00: 100µs 01: 200µs 10: 400µs 11: 800µs

D[1:0]	R/W	BOOST_TOFF_ DELAY	00: 100µs 01: 200µs 10: 400µs 11: 800µs

MEM_OTP_CHK_EN (0x40)

The MEM_OTP_CHK_EN command configures cyclic redundancy check (CRC) control.

Bits	Access	Name	Description
D[7:2]	R/W	RESERVED	Reserved. Always reads as 000000.
D[1]	R/W	OTP_CHK_EN	0: OTP_CRC_CHK is disabled 1: OTP_CRC_CHK is enabled
D[0]	R/W	CRC_CHK_EN	0: MEM_CRC_CHK is disabled 1: MEM_CRC_CHK is enabled

STORE_USER_ALL (0x44)

The STORE_USER_ALL command indicates the OTP write status.

Bits	Access	Name	Description
D[7:1]	W	RESERVED	Reserved. Always reads as 0.
D[0]	W	STORE_USER_ALL	Any valid write action to this bit stores data to the device OTP.

RESTORE_USER_ALL (0x45)

The RESTORE_USER_ALL command indicates the OTP restore status.

Bits	Access	Name	Description
D[7:1]	W	RESERVED	Reserved. Always reads as 0.
D[0]	W	RESTORE_USER_ ALL	Any valid write action to this bit restores data from the OTP.

PIN_FB_STATUS (0x6F)

The STORE_USER_ALL command indicates the FB pin status. This function can be disabled and enabled via SAFETY_FUNC_CFG_1, bit[2]. For more details, see the SAFETY_STAT_6 (0x08) section on page 75.

Bits	Access	Name	Description
D[7:5]	RW1C	RESERVED	Reserved. Always reads as 0.
D[4]	RW1C	PREWRN_FB_ MISMATCH	0: No mismatch has been detected between the /PREWRN pin feedback and /PREWRN logic output command 1: A mismatch has been detected between the /PREWRN pin feedback and /PREWRN logic output command
D[3]	RW1C	PG_FB_MISMATCH	0: No mismatch has been detected between the PG pin feedback and PG logic output command 1: A mismatch has been detected between the PG pin feedback and PG logic output command
D[2]	RW1C	FS_FB_MISMATCH	0: No mismatch has been detected between the /FS pin feedback and /FS logic output command 1: A mismatch has been detected between the /FS pin feedback and /FS logic output command
D[1]	RW1C	RST_FB_MISMATCH	0: No mismatch has been detected between the /RST pin feedback and /RST logic output command 1: A mismatch has been detected between the /RST pin feedback and /RST logic output command

D[0]	RW1C	INT_FB_MISMATCH	0: No mismatch has been detected between the /INT pin feedback and /INT logic output command 1: A mismatch has been detected between the /INT pin feedback and /INT logic output command

FREQ_REFRESH (0x7E)

The FREQ_REFRESH command configures the frequency refresh.

Bits	Access	Name	Description
D[7:1]	R/W	RESERVED	Reserved. Always reads as 0000000.
D[0]	R/W	FREQ_REFRESH	The positive edge of FREQ_REFRESH refreshes the internal analog f_{SW}. After setting the frequency-related registers, set FREQ_REFRESH from 0 to 1, or f_{SW} will not change.

PWD_WR_LOCK (0x7F)

The PWD_WR_LOCK command configures write protection for some registers.

Bits	Access	Name	Description
D[7:1]	R/W	RESERVED	Reserved. Always reads as 0000000.
D[0]	R/W	SW_LOCK	Write 8'h55 to 0x7F to disable write register protection. In this setting, this bit reads back 0. Write 8'hAA to 0x7F to enable write register protection. In this setting, this bit reads back 1. For details regarding the registers that this write protection applies to, see note 17 on page 69.

APPLICATION INFORMATION

Start-Up Behavior

Figure 16 shows the MPQ70331FS's start-up behavior. The device may not be able to respond to MCU SPI communication during BIST, so if the MCU boots faster than BIST, SPI communication should not be used until BIST is complete. If the ABIST or LBIST fails, or both fail, then the device transitions to DEEP SAFE.

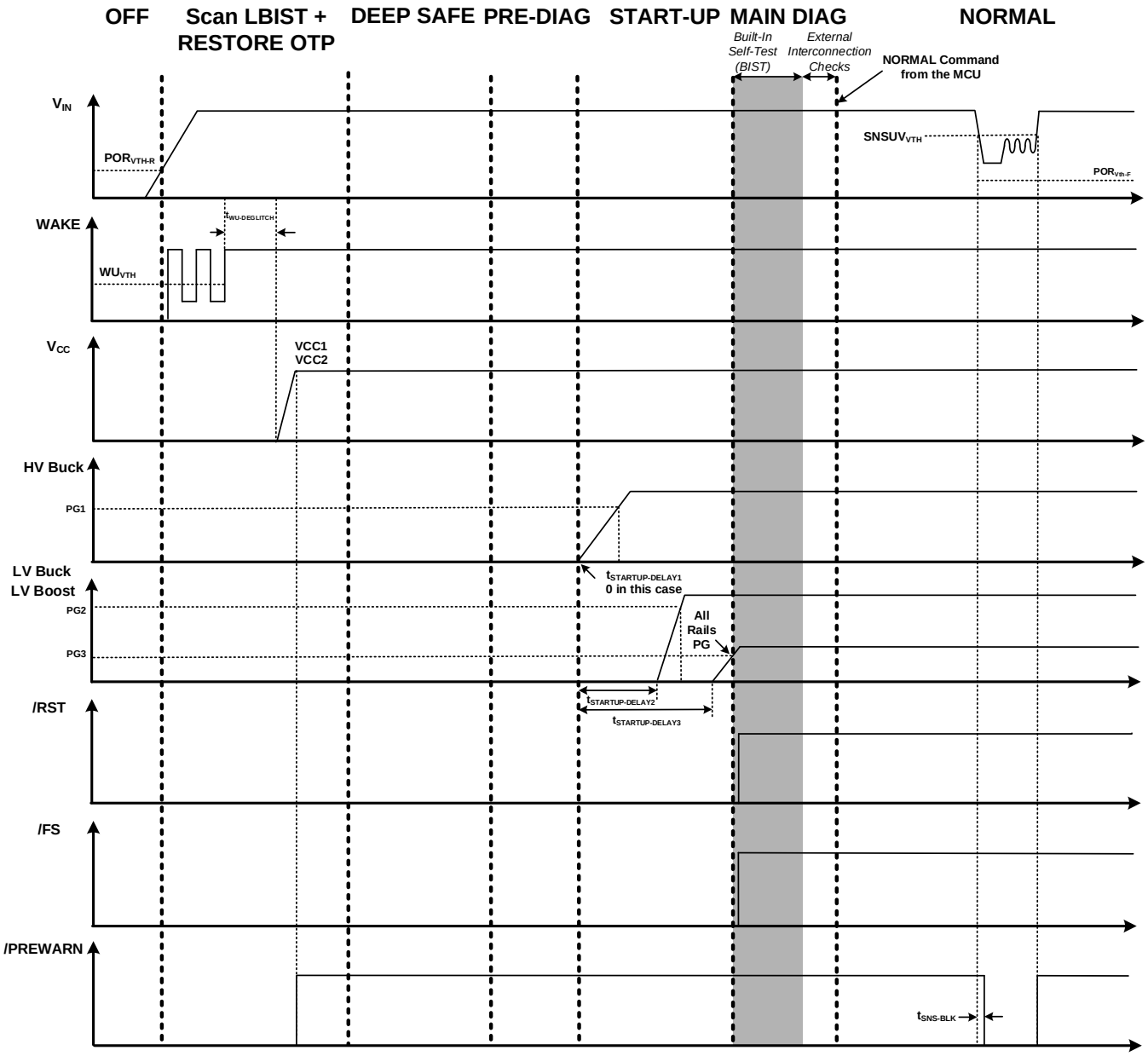


Figure 16: Start-Up Behavior

Figure 18 shows the MPQ70331FS's typical application circuit.

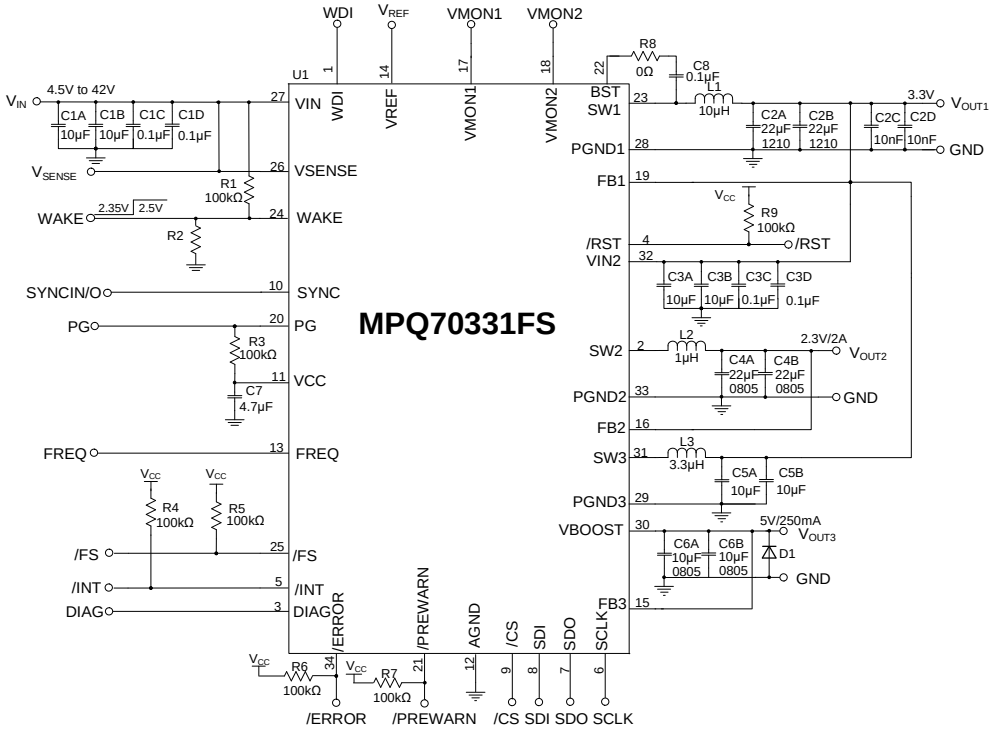


Figure 18: Typical Application Circuit (V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz)

Table 19: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1	WDI	-	Window Watchdog Input (WDI, Pin 1)
2	SW2	L2, C4A, C4B	Selecting the Output Capacitor (SW1, Pin 23; SW2, Pin 2; VBOOST, Pin 30) Selecting the Inductor (SW1, Pin 23; SW2, Pin 2; SW3, Pin 31)
23	SW1	L1, C2A, C2B, C2C, C2D	Selecting the Output Capacitor (SW1, Pin 23; SW2, Pin 2; VBOOST, Pin 30) Selecting the Inductor (SW1, Pin 23; SW2, Pin 2; SW3, Pin 31)
30	VBOOST	C6A, C6B	Selecting the Output Capacitor (SW1, Pin 23; SW2, Pin 2; VBOOST, Pin 30)
31	SW3	L3, C5A, C5B	Selecting the Input Capacitor (VIN, Pin 27; VIN2, Pin 32; SW3, Pin 31) Selecting the Inductor (SW1, Pin 23; SW2, Pin 2; SW3, Pin 31)
3	DIAG	-	Diagnostic Mux Output (DIAG, Pin 3)
4	/RST	R9	Reset Indicator (/RST, Pin 4)
5	/INT	R4	Interruption Indicator (/INT, Pin 5)
6	SCLK	-	SPI Interface (SCLK, Pin 6; SDO, Pin 7; SDI, Pin 8; /CS, Pin 9)
7	SDO	-	SPI Interface (SCLK, Pin 6; SDO, Pin 7; SDI, Pin 8; /CS, Pin 9)
8	SDI	-	SPI Interface (SCLK, Pin 6; SDO, Pin 7; SDI, Pin 8; /CS, Pin 9)
9	/CS	-	SPI Interface (SCLK, Pin 6; SDO, Pin 7; SDI, Pin 8; /CS, Pin 9)
10	SYNC	-	SYNCIN and SYNCOUT (SYNC, Pin 10)
11	VCC	C7	Selecting the VCC Capacitor (VCC, Pin 11)
12	AGND	-	GND Connection (AGND, Pin 12; PGND1, Pin 28; PGND3, Pin 29; PGND2, Pin 33)

Table 19: Design Guide Index *(continued)*

Pin #	Pin Name	Component	Design Guide Index
28	PGND1	-	GND Connection (AGND, Pins 12; PGND1, Pin 28; PGND3, Pin 29; PGND2, Pin 33)
29	PGND3	-	GND Connection (AGND, Pins 12; PGND1, Pin 28; PGND3, Pin 29; PGND2, Pin 33)
33	PGND2	-	GND Connection (AGND, Pins 12; PGND1, Pin 28; PGND3, Pin 29; PGND2, Pin 33)
13	FREQ	-	Setting the Switching Frequency (FREQ, Pin 13)
14	VREF	-	Voltage Reference (VREF, Pin 14)
15	FB3	-	Setting the Output Voltage (FB3, Pin 15; FB2, Pin 16; FB1, Pin 19) Selecting FB3 Negative Spike Protection Diode (FB3, Pin 15)
16	FB2	-	Setting the Output Voltage (FB3, Pin 15; FB2, Pin 16; FB1, Pin 19)
19	FB1	-	Setting the Output Voltage (FB3, Pin 15; FB2, Pin1 6; FB1, Pin 19)
17	VMON1	-	Voltage Monitor (VMON1, Pin 17; VMON2, Pin 18)
18	VMON2	-	Voltage Monitor (VMON1, Pin 17; VMON2, Pin 18)
20	PG	R3	Power Good (PG) Indicator (PG, Pin 20)
21	/PREWARN	R7	V_{IN} Pre-Warning Indicator (/PREWRN, Pin 21)
24	WAKE	R1, R2	Setting V_{IN} Under-Voltage Lockout (UVLO) (WAKE, Pin 24)
25	/FS	R5	Failsafe Indicator (/FS, Pin 25)
26	VSENSE	-	Battery Voltage Sense Input (VSENSE, Pin 26)
27	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitor (VIN, Pin 27; VIN2, Pin 32; SW3, Pin 31)
32	VIN2	C3A, C3B, C3C, C3D	Selecting the Input Capacitor (VIN, Pin 27; VIN2, Pin 32; SW3, Pin 31)
22	BST	C8, R8	Selecting the Bootstrap Capacitor (BST, Pin 22)
34	/ERROR	R6	External Error Input (/ERROR, Pin 34)

Window Watchdog Input (WDI, Pin 1)

The WDI pin receives signals from MCU. No external components are required.

Selecting the Output Capacitor (SW1, Pin 23; SW2, Pin 2; VBOOST, Pin 30)

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}.

For simplification, the buck converters' output voltage ripple ($\Delta V_{OUT-BUCK}$) can be estimated with Equation (6):

$$\Delta V_{OUT-BUCK} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For simplification, the boost converter's output voltage ripple ($\Delta V_{OUT-BOOST}$) can be estimated with Equation (7):

$$\Delta V_{OUT-BOOST} = I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{f_{SW} \times C_{OUT}} \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, the buck converters' output voltage ripple ($\Delta V_{OUT-BUCK}$) can be estimated with Equation (8):

$$\Delta V_{OUT-BUCK} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

For simplification, the boost converter's output voltage ripple ($\Delta V_{OUT-BOOST}$) can be estimated with Equation (9):

$$\Delta V_{OUT-BOOST} = I_{LOAD} \times (\frac{1-\frac{V_{IN}}{V_{OUT}}}{f_{SW} \times C_{OUT}} + \frac{V_{OUT}}{V_{IN}} \times R_{ESR}) \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ70331FS can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor (SW1, Pin 23; SW2, Pin 2; SW3, Pin 31)

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance (L) is to allow the inductor ripple current to be approximately 30% of the maximum load current. For the buck converters, the inductance (L_{BUCK}) can be calculated with Equation (10):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1-\frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For the boost converter, the inductance (L_{BOOST}) can be calculated with Equation (11):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (11)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The MPQ70331FS's internal peak current limit should be considered when selecting the power inductor. Select an inductor with a minimum saturation current (I_{SAT}) greater than the peak current limit so that the inductor is never saturated.

When I_{LOAD_HVBUCK} > 2A, the SCP valley current limit > 3A, or the peak current limit > 4A, it is recommended to place a Schottky diode with a forward voltage ≤ 0.5V at a 3A current between SW1 and GND (e.g. a B350A diode).

Diagnostic Mux Output (DIAG, Pin 3)

The diagnostic mux can output selectable signals. No external components are required.

Reset Indicator (/RST, Pin 4)

The /RST pin has an internal open-drain structure. Connect this pin to a power source with a pull-up resistor (e.g. 100kΩ).

Interruption Indicator (/INT, Pin 5)

The /INT pin has an internal open-drain structure. Connect this pin to a power source with a pull-up resistor (e.g. 100kΩ).

SPI Interface (SCLK, Pin6; SDO, Pin 7; SDI, Pin 8; /CS, Pin 9)

The MPQ70331FS works as a slave-only device, and supports up to 4Mbps of bidirectional data transfer, adding flexibility to the power supply solution. The SDO line is externally pulled to an I/O voltage with a resistor (e.g. 1kΩ).

SYNCIN and SYNCOUT (SYNC, Pin 10)

The SYNC pin has an internal push-pull structure when operating in SYNCIN mode, and receives external clock pulses when operating in SYNCOUT mode. No external components are required.

Selecting the VCC Capacitor (VCC, Pin 11)

During normal operation, an internal low-dropout (LDO) regulator outputs a nominal 5V VCC supply from VIN. This supply is for both control blocks and MOSFET gate drivers. Apply a 1µF to 10µF low-ESR ceramic capacitor as a bypass capacitor, and placed from VCC to AGND.

This regulator takes VIN as the input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, VCC is in full regulation. When V_{IN} is below 5V, the VCC output degrades.

GND Connection (AGND, Pins 12; PGND1, Pin 28; PGND3, Pin 29; PGND2, Pin 33)

See the PCB Layout Guidelines on page 100 for more details.

Setting the Switching Frequency (FREQ, Pin 13)

When f_{SW} is set by the FREQ pin (FREQ_SET = 1), the LV buck's frequency can be configured by an external resistor (R_{FREQ}) placed from the FREQ pin to ground.

Table 20 lists the relationship between R_{FREQ} and f_{SW2}.

Table 20: f_{SW2} vs. R_{FREQ}

R_{FREQ} (kΩ)	f_{SW2} (kHz)
4.7	300
7.15	440
9.09	550
14.3	835
18.2	1050
25.5	1450
29.4	1700
35.7	2010
40.2	2230
41.2	2300
43.2	2350
45.3	2485

When f_{SW} is set by the register (FREQ_SET = 0), the FREQ pin must be floated.

The HV buck's frequency ratio is determined by register FREQ_CTRL_1, bits[7:6]. The LV boost's f_{SW} always follows the LV buck.

Voltage Reference (VREF, Pin 14)

The VREF pin delivers an internal bandgap voltage for external monitoring with a buffered output. It does not require any external components.

Setting the Output Voltage (FB3, Pin 15; FB2, Pin 16; FB1, Pin 19)

The OTP registers HV_BUCK_PWR, LV_BUCK_PWR, and BOOST_PWR set V_{OUT1}, V_{OUT2}, and V_{OUT3}, respectively. Write to HV_BUCK_PWR, bits[5:0] to set V_{OUT1}. Write to LV_BUCK_PWR, bits[5:0] to set V_{OUT2}. Write to BOOST_PWR, bits[5:0] to set V_{OUT3}. See the Register Map section on page 85 for more information.

V_{OUT1}, V_{OUT2}, and V_{OUT3} can be calculated with Equation (12), Equation (13), and Equation (14), respectively:

$$V_{OUT1}(mV) = HV\_BUCK\_FB\_REF \times 50 + 2300 \quad (12)$$

$$V_{OUT2}(mV) = LV\_BUCK\_FB\_REF \times 50 + 600 \quad (13)$$

$$V_{OUT3}(mV) = BOOST\_FB\_REF \times 50 + 4400 \quad (14)$$

Connect the FB pins directly to the output voltages; resistor dividers are not required.

Selecting FB3 Negative Spike Protection Diode (FB3, Pin 15)

In applications when there is possibility that FB3 has abnormally high negative spike (such as during a VBOOST short circuit) and high V_{IN}, false actions or damage may occur.

To protect FB3 from too high of a negative spike at high input voltages, a low forward voltage Schottky diode (D1) must be placed from FB3 to GND to clamp the negative spike (see Figure 19).

A Schottky diode with forward voltage ≤ 0.5V at 2A current is recommended (e.g. B220A).

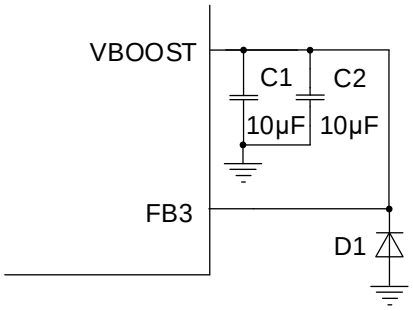


Figure 19: FB3 Negative Spike Protection Circuit

Voltage Monitor (VMON1, Pin 17; VMON2, Pin 18)

The VMON1 and VMON2 pins monitor external signals. No external components are required.

Power Good (PG) Indicator (PG, Pin 20)

The PG pin has an internal open-drain structure and requires an external pull-up resistor (e.g. 100kΩ).

V_{IN} Pre-Warning Indicator (/PREWRN, Pin 21)

The /PREWRN pin has an internal open-drain structure and requires an external pull-up resistor (e.g. 100kΩ).

Setting V_{IN} Under-Voltage Lockout (UVLO) (WAKE, Pin 24)

WAKE is a digital control pin that turns the regulator on and off.

WAKE can be enabled via an external logic high/low (H/L) signal. Drive WAKE above its upper system threshold (2.5V) to enable the converter and initiate soft start.

If WAKE is pulled below the lower system threshold (2.35V), the converter stops switching. There is no internal pull-up or pull-down resistor at EN, so do not leave it floating to avoid an uncertain state. An external pull-up or pull-down resistor may be required if the control signal cannot indicate a clear high or low logic.

The MPQ70331FS has an internal, fixed UVLO threshold. The rising threshold is 3.9V, while the falling threshold is about 3.45V. For applications that require a higher UVLO point, an external resistor divider placed between VIN and WAKE can be used to achieve a higher equivalent UVLO threshold (see Figure 20).

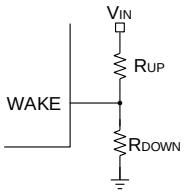


Figure 20: Adjustable UVLO Using WAKE Divide

The rising and falling UVLO thresholds can be calculated with Equation (15) and Equation (16), respectively:

$$INUV_{RISING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN\_RISING} \quad (15)$$

$$INUV_{FALLING} = \left(1 + \frac{R_{UP}}{R_{DOWN}}\right) \times V_{EN\_FALLING} \quad (16)$$

Where V_{EN_RISING} is 2.5V, and $V_{EN\_FALLING}$ is 2.35V.

Failsafe Indicator (/FS, Pin 25)

The /FS pin has an internal open-drain structure, and requires an external pull-up resistor (e.g. 100kΩ). A maximum 10mA current is allowed on the /FS pin.

Battery Voltage Sense Input (VSENSE, Pin 26)

The VSENSE pin monitors battery voltage. It does not require any external components.

Selecting the Input Capacitor (VIN, Pin 27; VIN2, Pin 32; SW3, Pin 31)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating.

For the buck converters, the RMS current in the input capacitor ($I_{CIN-BUCK}$) can be estimated with Equation (17):

$$I_{CIN-BUCK} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (17)$$

For the boost converter, the RMS current in the input capacitor ($I_{CIN-BOOST}$) can be estimated with Equation (18):

$$I_{CIN-BOOST} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(\frac{1}{1-D} - \frac{V_{OUT}}{V_{IN}}\right)}$$

(18)

Where D is the boost LS-FET duty cycle.

The worst-case condition for $I_{CIN-BUCK}$ can be calculated with Equation (19):

$$I_{CIN-BUCK} = \frac{I_{LOAD}}{2} \quad (19)$$

The worst-case condition for $I_{CIN-BOOST}$ can be calculated with Equation (20):

$$I_{CIN-BOOST} = \frac{I_{LOAD}}{2 \times \sqrt{1-D}} \quad (20)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF), placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

For the buck converters, the input voltage ripple ($\Delta V_{IN-BUCK}$) caused by the capacitance can be estimated with Equation (21):

$$\Delta V_{IN-BUCK} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (21)$$

For the buck converters, the input voltage ripple ($\Delta V_{IN-BOOST}$) caused by the capacitance can be estimated with Equation (22):

$$\Delta V_{IN-BOOST} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \times (1-D)\right)$$

(22)

Selecting the Bootstrap Capacitor (BST, Pin 22)

The recommended bootstrap (BST) capacitance (C_{BST}) is between 0.1μF and 1μF. Place a resistor capacitor (R_{BST}) in series with C_{BST} to reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce voltage stress at high input voltages. A higher resistance is better for SW spike reduction, but compromises efficiency. For a reasonable tradeoff between EMI and efficiency, a ≤ 20Ω R_{BST} is recommended.

External Error Input (/ERROR, Pin 34)

The /ERROR pin monitors the external fault signals from the MCU. An external pull-up resistor (e.g. 100kΩ) is required. If the related function and register are disabled, this pin can be floated.

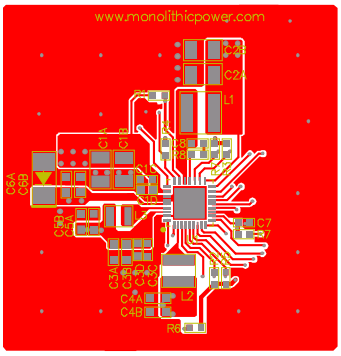
PCB Layout Guidelines [19]

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 21 and follow the guidelines below:

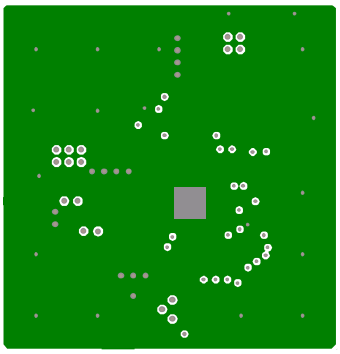
1. Place the symmetric input/output capacitors as close as possible to the VIN and GND pins.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths (e.g. PGND and VIN) have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input/output bypass capacitor, as close as possible to the VIN and PGND pins to minimize high-frequency noise.
6. Keep the connection between the input/output capacitor and the VIN/VOUT pins as short and wide as possible.
7. Place the VCC capacitor as close to the VCC and AGND pins as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Reduce the SW node routing size to improve EMI.
10. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
11. Use multiple vias to connect the power planes to the internal layers.

Note:

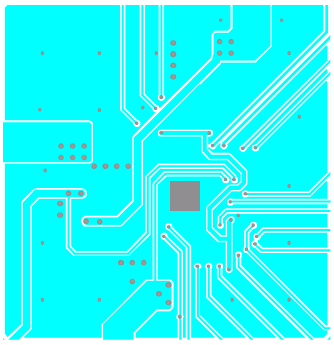
19) The recommended PCB layout is based on Figure 22 on page 101.



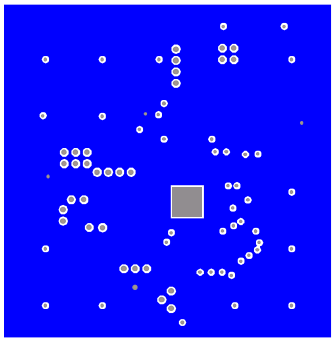
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 21: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

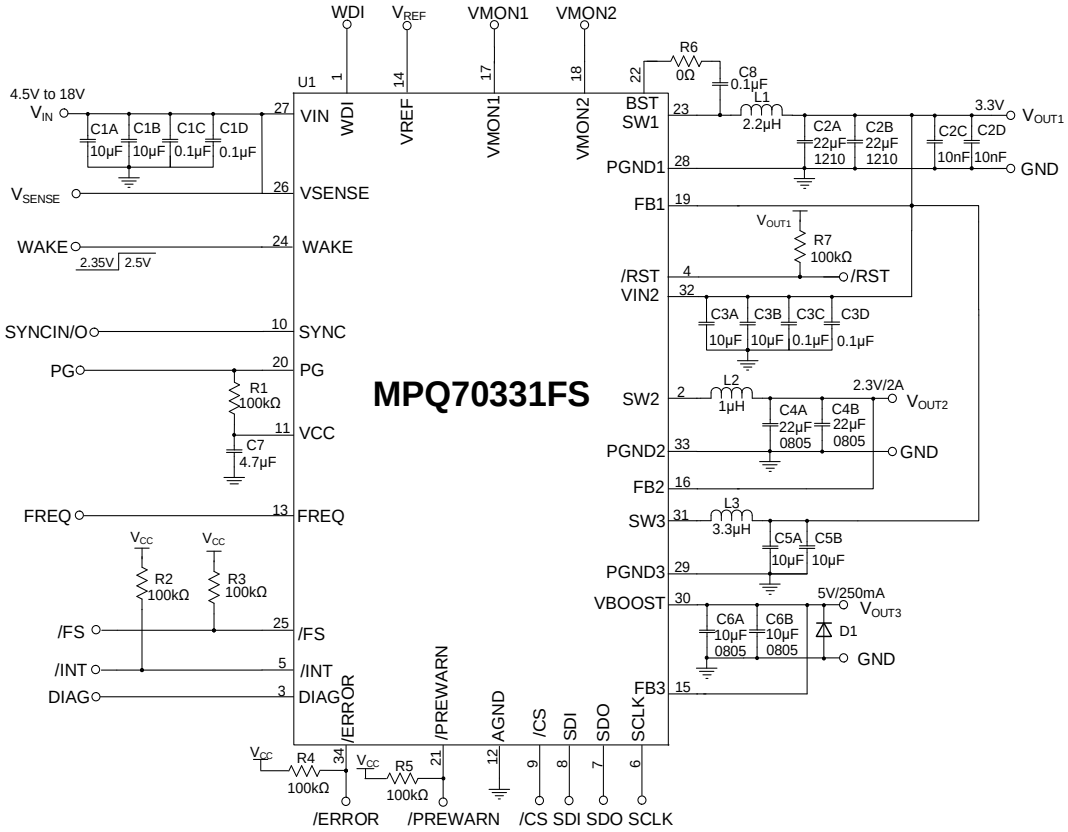


Figure 22: Typical Application Circuit (V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, f_{SW1} = f_{SW2} = f_{SW3} = 2MHz)

TYPICAL APPLICATION CIRCUITS *(continued)*

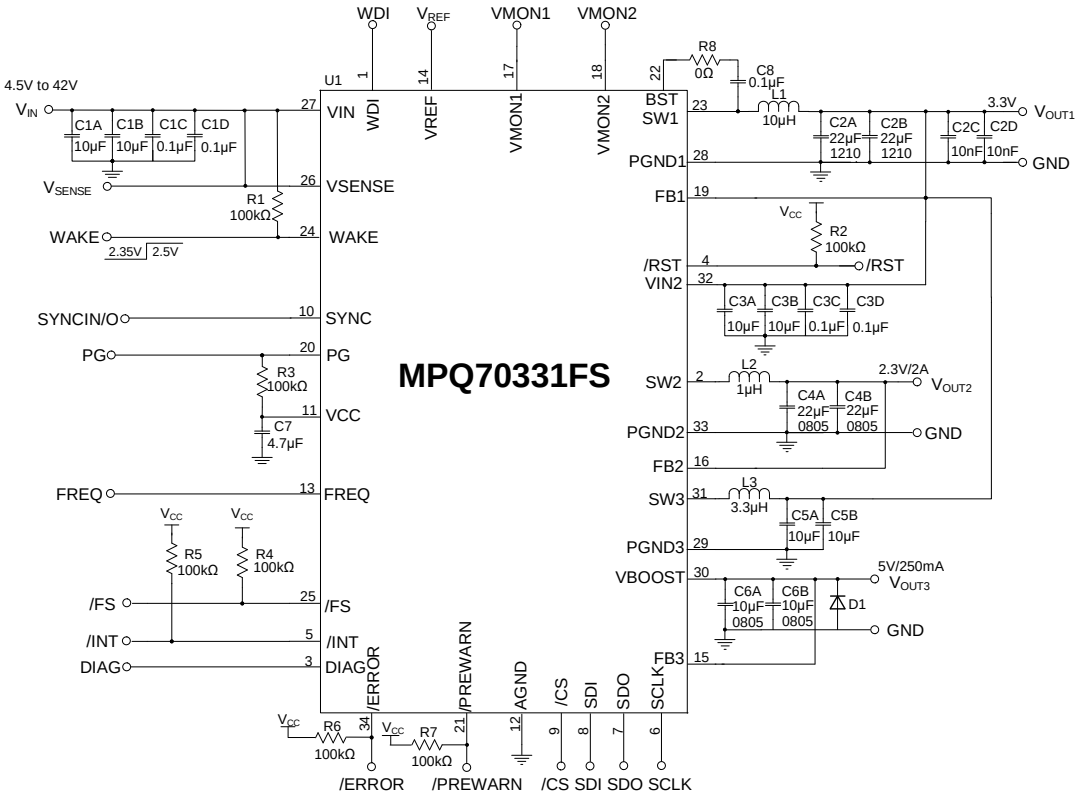


Figure 23: Typical Application Circuit (V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, f_{SW1} = 500kHz, f_{SW2} = f_{SW3} = 2MHz) (20)

Note:

20) D1 is recommended for applications where V_{IN} > 42V.

TYPICAL APPLICATION CIRCUITS *(continued)*

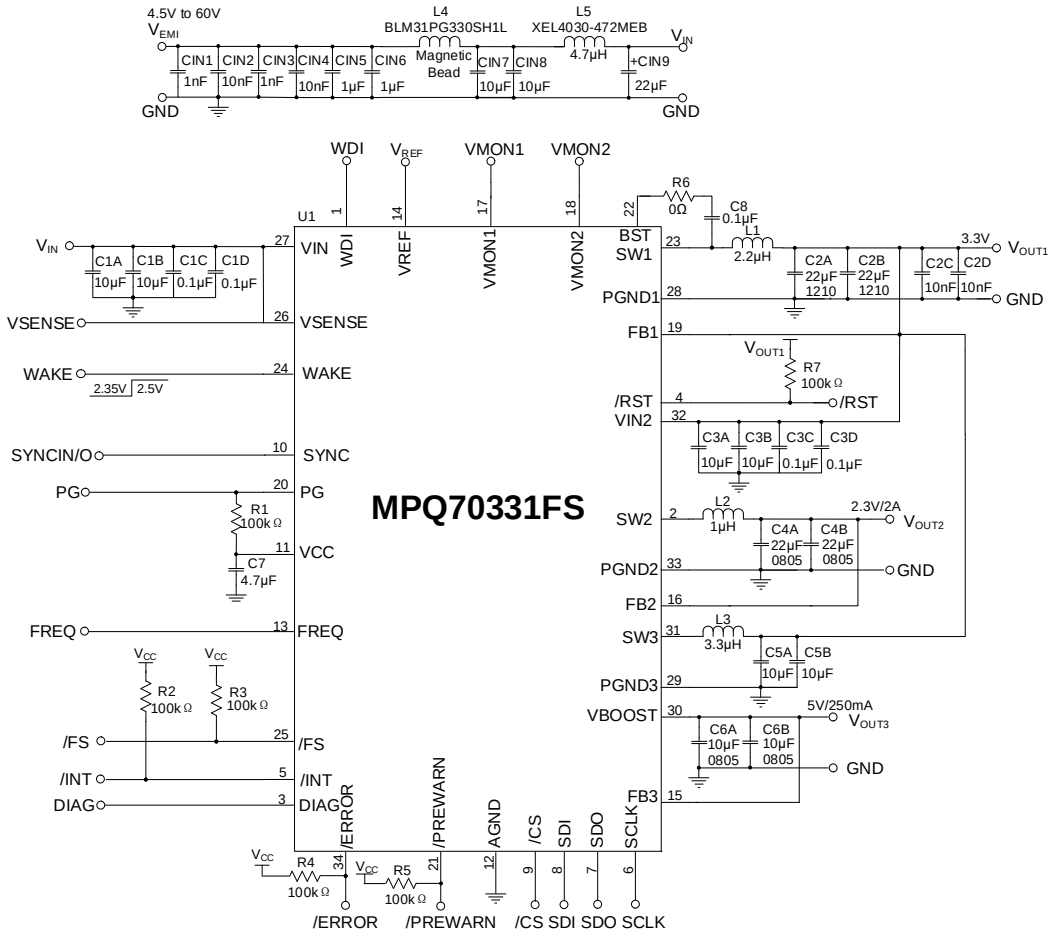
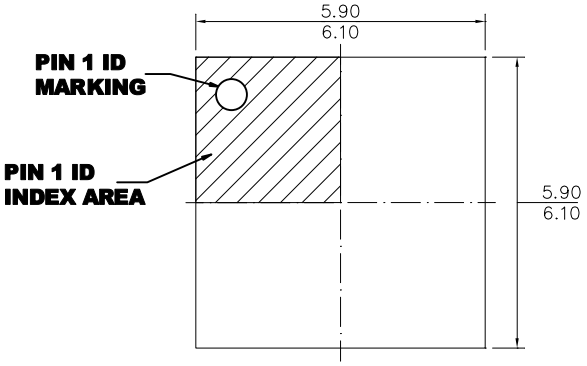


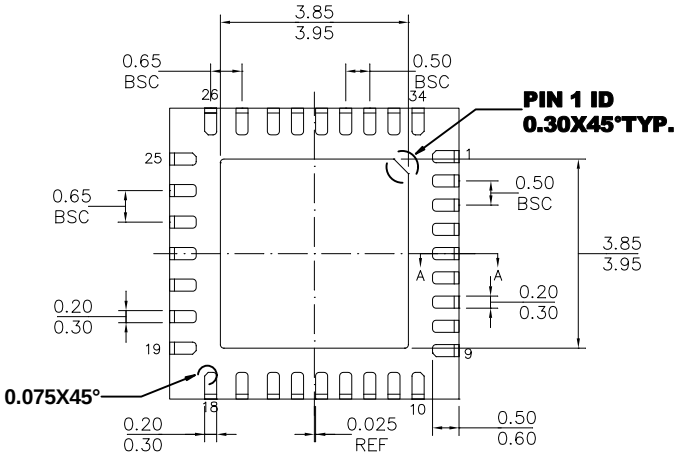
Figure 24: Typical Application Circuit (V_{OUT1} = 3.3V, V_{OUT2} = 2.3V, V_{OUT3} = 5V, f_{SW1} = f_{SW2} = f_{SW3} = 2MHz with EMI Filters)

PACKAGE INFORMATION

TQFN-34 (6mmx6mm)
Wettable Flank

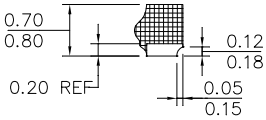


TOP VIEW

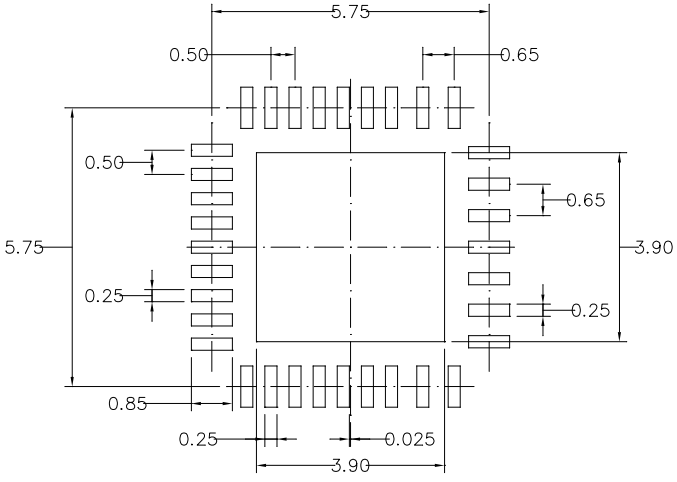


BOTTOM VIEW

SIDE VIEW



SECTION A-A

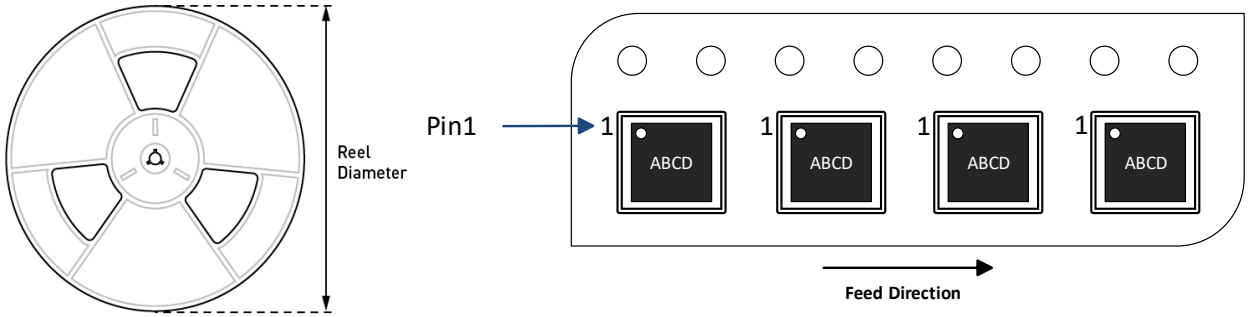


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (21)	Quantity/ Reel (21)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ70331FSGQKTE -xxxxAEC-Z	TQFN-34 (6mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

21) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. (The order code for 500-piece partial reel is “-P”; tape & reel dimensions are the same as for full reel.)

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/22/2023	Initial Release	-