MPQ6641

Two-Channel Automotive Pre-Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6641 is a gate driver IC designed for automotive DC motor driver applications. It is capable of driving four N-channel power MOSFETs to drive DC motors or other loads.

The MPQ6641 integrates a low-dropout (LDO) regulator to generate gate drive voltages for the low-side MOSFETs (LS-FETs). The high-side (HS) gate drive is generated by the bootstrap (BST) capacitors (C_{BST}) and an internal charge pump, which achieves 100% duty cycle operation. The device also provides a charge pump that generates a voltage to drive an external N-channel MOSFET for reverse battery protection.

An internal amplifier measures the voltage drop across the LS-FETs or external shunt resistors. Internal safety features include configurable over-current protection (OCP), adjustable dead-time (DT) control, under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6641 is available in a QFN-32 (5mmx5mm) package with an exposed thermal pad, and is AEC-Q100 qualified.

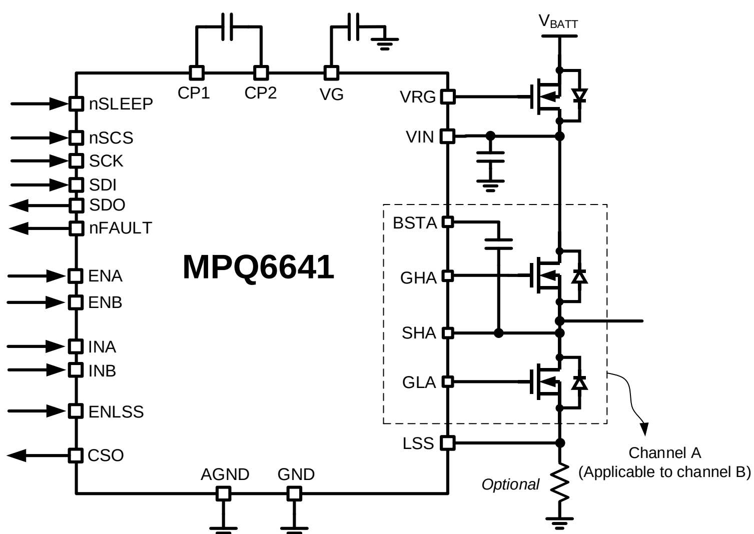
FEATURES

- Integrated Low-Dropout (LDO) Regulator for Gate Drive
- Charge Pump for External N-Channel MOSFET Reverse Battery Protection
- Current-Sense Amplifier to Measure the Drop across the Low-Side MOSFETs (LS-FETs) or External Shunt Resistor
- Low-Power Sleep Mode
- Configurable Short-Circuit Protection (SCP)
- Adjustable Slew Rate Control
- Adjustable Dead-Time (DT) Control
- Over-Temperature (OT) Shutdown
- Under-Voltage (UV) Warning and Shutdown
- Open and Short Load Detection
- Serial Peripheral Interface (SPI)
- Fault Indication Output
- Available in a QFN-32 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Actuators
- Brushed DC Motor Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6641GUE-AEC1	QFN-32 (5mmx5mm)	*See Below*	2

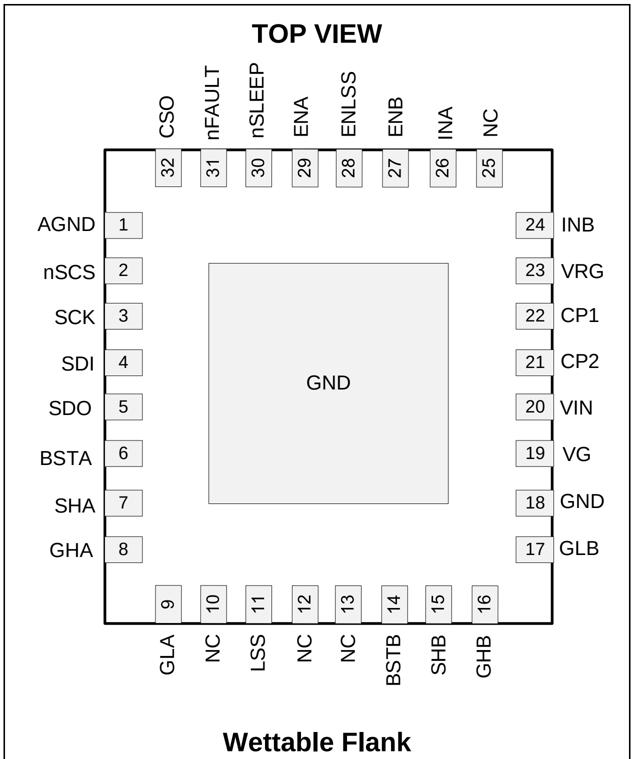
* For Tape & Reel, add suffix -Z (e.g. MPQ6641GUE-AEC1-Z).

TOP MARKING

MPSYYWW
MP6641
LLLLLLL
E

MPS: MPS Prefix
YY: Year code
WW: Week code
MP6641: Product code of MPQ6641GUE-AEC1
LLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-32 (5mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
18	GND	**Power ground.**
1	AGND	**Analog ground.**
20	VIN	**Input supply voltage.** Bypass the VIN pin using a minimum 1µF ceramic capacitor (X7R) connected to ground. Additional bulk capacitance may be required.
22	CP1	**Reverse battery gate drive charge pump capacitor.** Connect a 220nF ceramic capacitor (X7R) between the CP1 and CP2 pins.
21	CP2	
19	VG	**Gate drive low-dropout (LDO) output voltage.** Connect a 10µF, 10V ceramic capacitor (X7R) between the VG pin to ground.
23	VRG	**Reverse battery MOSFET gate drive output.**
6	BSTA	**Bootstrap (BST) capacitor for channel A.** Connect a ceramic capacitor between the BSTA and SHA pins.
7	SHA	**Channel A output.** The SHA pin is the drain of the low-side MOSFET (LS-FET) and the source of the high-side MOSFET (HS-FET) for channel A.
8	GHA	**High-side (HS) gate drive output for channel A.**
9	GLA	**Low-side (LS) gate drive output for channel A**
10	NC	**No connection.**
11	LSS	**Optional LS sense resistor.**
12	NC	**No connection.**
13	NC	**No connection.**
14	BSTB	**BST capacitor for channel B.** Connect a ceramic capacitor between the BSTB and SHB pins.
15	SHB	**Channel B output.** The SHB pin is the drain of LS-FET and the source of the HS-FET for channel B.
16	GHB	**HS gate drive output for channel B.**
17	GLB	**LS gate drive output for channel B.**
29	ENA	**Enable input for channel A.** The ENA pin is pulled down internally.
28	ENLSS	**LSS sense enable.** The ENLSS pin is pulled down internally.
27	ENB	**Enable input for channel B.** The ENB pin is pulled down internally.
26	INA	**Channel A input.** The INA pin is pulled down internally.
25	NC	**No connection.**
24	INB	**Channel B input.** The INB pin is pulled down internally.
32	CSO	**Current-sense output.**
31	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. nFAULT is pulled logic low if a fault occurs.
5	SDO	**Serial data output.** The SDO pin has a high impedance when nSCS is set to 1.
4	SDI	**Serial data input.** The SDI pin is pulled down internally.
3	SCK	**Serial clock input.** Data is captured on the SCK pin's rising edge. Pull down SCK internally.
2	nSCS	**Serial chip selection.** Drive the nSCS pin active low to enable serial data transfers. nSCS is pulled down internally.
30	nSLEEP	**Sleep mode input.** Drive the nSLEEP pin logic low to enter low-power sleep mode. nSLEEP is pulled down internally.

ABSOLUTE MAXIMUM RATINGS [1]

Input voltage (V_{IN}) ....-0.3V to +45V
VRG ....-40V to +59V
VG………………………………….....-0.3V to +14V
CP1…………………………………-0.3V to +14V
CP1 (transient <2µs)……….............-1V to +15V
CP2…………………..……….V_{IN} - 1V to V_{IN} + 14V
GHA, GHB, BSTA, BSTB………………………..
………….........SHA/SHB to SHA/SHB + 14V
GHA, GHB (transient <2µs)……….-8V to +59V
GLA, GLB……………..................-0.3V to +14V
GLA, GLB to AGND (transient <2µs)…………....
……..……..…………………………..-5V to +15V
SHA, SHB ....-0.3V to +45V
SHA, SHB (transient <2µs) ....-8V to +45V
LSS……………………………………..-1V to +1V
LSS (transient <2µs).........................-5V to +5V
All other pins to GND ....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) [2]
QFN-32 (5mmx5mm)……………………….3.4W
Storage temperature .... -55°C to +150°C
Junction temperature (T_J) ....165°C
Lead temperature (solder) ....260°C

ESD Ratings

Human body model (HBM) 2kV
Charged-device model (CDM) 750V

Recommended Operating Conditions [3]

Input voltage (V_{IN}) ....6V to 40V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance [4]

	θ_{JA}	θ_{JC}	
QFN-32 (5mmx5mm)	36	8	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 14V, T_J = -40° to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		6		40	V
VG low-dropout (LDO) output voltage	V_G	I_{LDO} ≤ 5mA, V_{IN} > 13V	11	12	13	V
VG LDO resistance	R_{LDO}	V_{IN} < V_G		80		Ω
Quiescent current	I_Q	nSLEEP = 1, not switching		6	10	mA
	I_{SLEEP}	nSLEEP = 0			10	µA
Control Logic						
Input logic low threshold	V_{IL}				0.6	V
Input logic high threshold	V_{IH}		2.2			V
Logic input current	I_{IN_H}	V_{IH} = 5V	-20		+20	µA
	I_{IN_L}	V_{IL} = 0.8V	-20		+20	µA
Internal pull-down resistance	R_{PD}			500		kΩ
Fault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
V_{IN} under-voltage lockout (UVLO) falling threshold	$V_{IN\_UVLO\_FALLING}$		3.9	4.45	5	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			150		mV
V_{IN} under-voltage (UV) warning	$V_{IN\_UV\_WARN}$		7.3	8	8.7	V
Bootstrap (BST) voltage (V_{BST}) UVLO threshold	V_{BST_UVLO}	Voltage between the SHx and BSTx pins	1.8	2.95	4	V
VG voltage (V_G) UVLO rising threshold	$V_{G\_UVLO\_RISING}$		5.1	5.4	5.7	V
V_G UVLO falling threshold	$V_{G\_UVLO\_FALLING}$		4.7	5	5.3	V
Short-circuit threshold (voltage across each external low-side MOSFET)	V_{SCP_LS}	xSC2~xSC0 = 000	80	110	140	mV
		xSC2~xSC0 = 100	450	510	570	
		xSC2~xSC0 = 111	730	810	890	
Short-circuit threshold (voltage across each external high-side MOSFET)	V_{SCP_HS}	xSC2~xSC0 = 000	90	120	150	mV
		xSC2~xSC0 = 100	460	520	580	
		xSC2~xSC0 = 111	740	820	900	
Open-load detection threshold	V_{OLD}	Lower threshold	0.45	0.5	0.55	V
		Upper threshold	1.15	1.25	1.35	
Sleep wake-up time	t_{SLEEP}		0.8	1.2	1.6	ms
Over-temperature (OT) warning (5)	T_{OT_W}			125		°C
Thermal shutdown (5)	T_{TSD}			165		°C
Gate Drive						
BST diode forward voltage	V_{FWD_BST}	I_D = 10mA		0.77	0.9	V
		I_D = 100mA		1	1.3	V
Gate drive pull-up resistance	R_{DS_UP}	xSR1~xSR0 = 00		175	350	Ω
		xSR1~xSR0 = 11		7.5	15	
Gate drive pull-down resistance	R_{DS_DOWN}	xSR1~xSR0 = 00		90	190	Ω
		xSR1~xSR0 = 11		2.5	6	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 14V, T_J = -40° to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Dead time [5]	t_{DEAD}	xDT2~xDT0 = 000		50		ns
		xDT2~xDT0 = 100		800		ns
		xDT2~xDT0 = 111		6.4		µs
Current-Sense Amplifier						
Amplifier output offset	V_{OFS}	V_{SHx} or V_{LSS} = 0V, A_{CS} = 100	-10	0	+10	mV
Input common-mode drift	CMDF	LSS = GND + 30mV, GND = 0V, and GND = 2V	-3		3	%
Amplifier gain	A_{CS}	xGN2~xGN0 = 000	18	20	22	V/V
		xGN2~xGN0 = 100	93	100	107	
		xGN2~xGN0 = 111	233	250	267	
Settling time	t_S	From LS-FET on, ΔV_{CS} = 100mV		3		µs

TIMING CHARACTERISTICS [5]

V_{IN} = 14V, T_A = -40° to +125°C, unless otherwise noted.

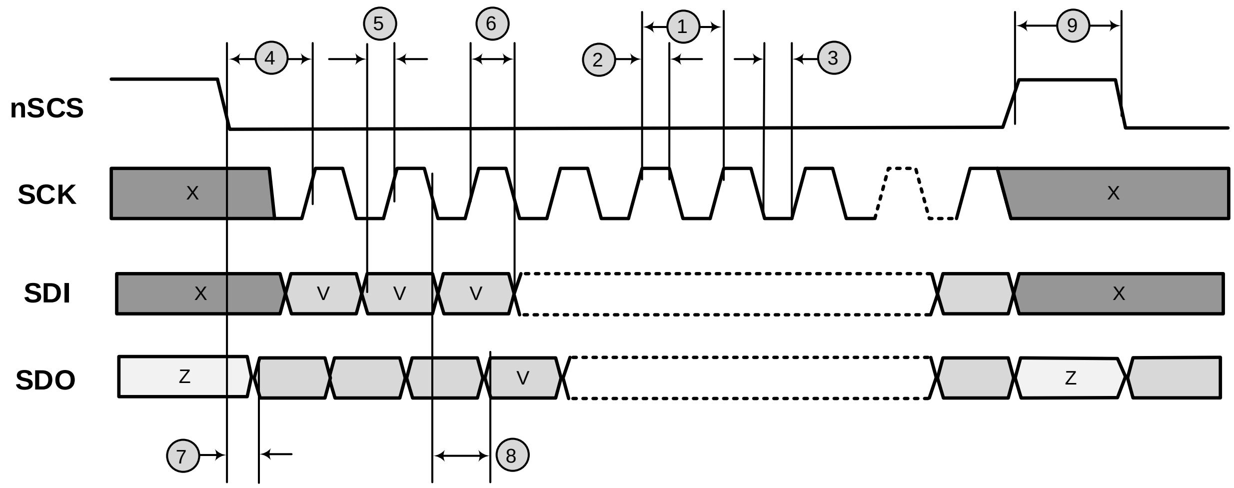


Figure 1: Serial Interface Timing Diagram

Table 1: Timing Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCK cycle time	t_1		100			ns
SCK frequency	-		0.1		10	MHz
SCK high time	t_2		50			ns
SCK low time	t_3		50			ns
SCK rising/falling time	-				50	ns
Set-up time (nSCS low to SCK rising)	t_4		30			ns
Set-up time (SDI valid to SCK rising)	t_5		15			ns
Holding time (SCK rising to SDI invalid)	t_6		10			ns
nSCS low to SDO enabled	t_7		40			ns
SCK falling to SDO valid	t_8	C_L < 100pF			10	ns
nSCS inactive time	t_9		100			ns

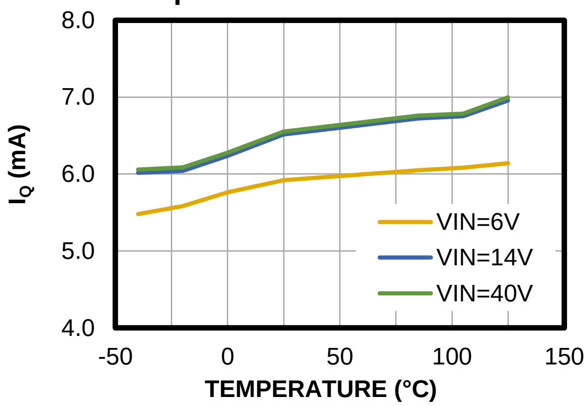
Note:

5) Not subject to production testing. Specified by design.

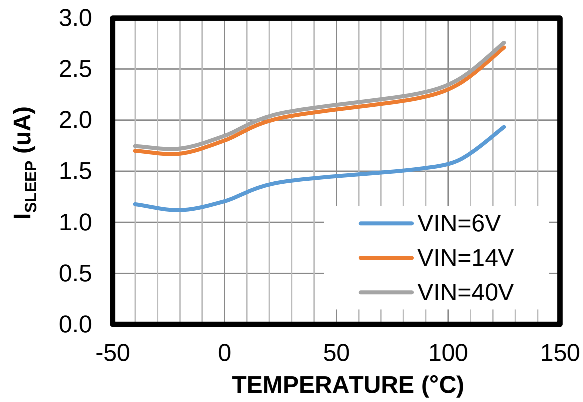
TYPICAL CHARACTERISTICS

V_{IN} = 14V, T_A = -40° to +125°C, unless otherwise noted.

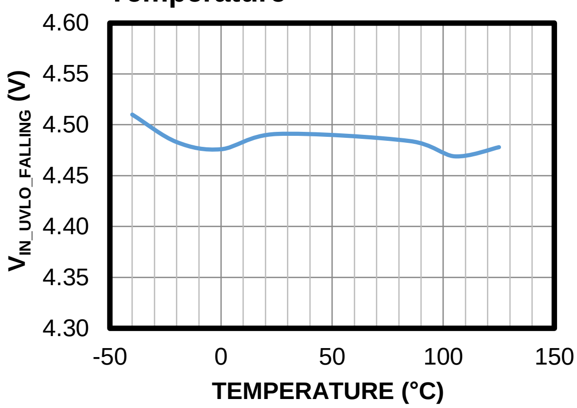
Quiescent Current vs. Temperature



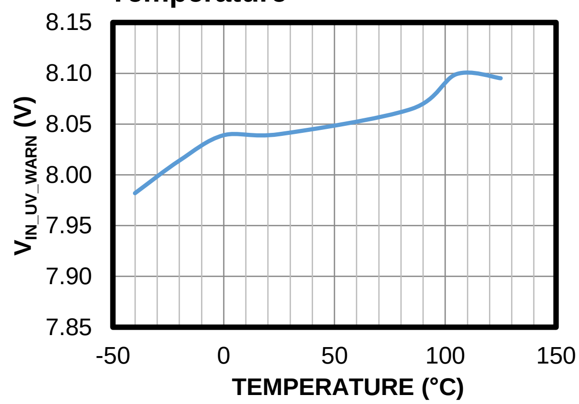
Sleep Current vs. Temperature



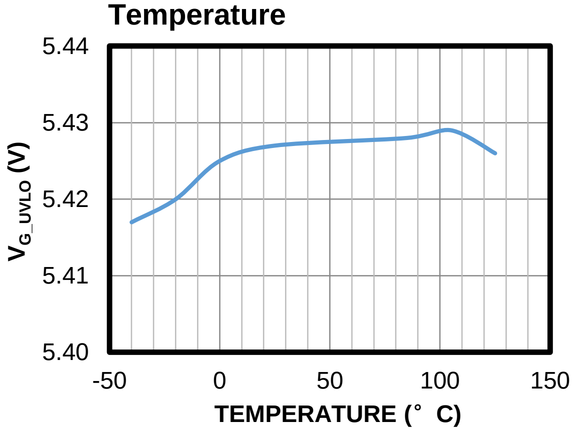
V_{IN} UVLO Falling Threshold vs. Temperature



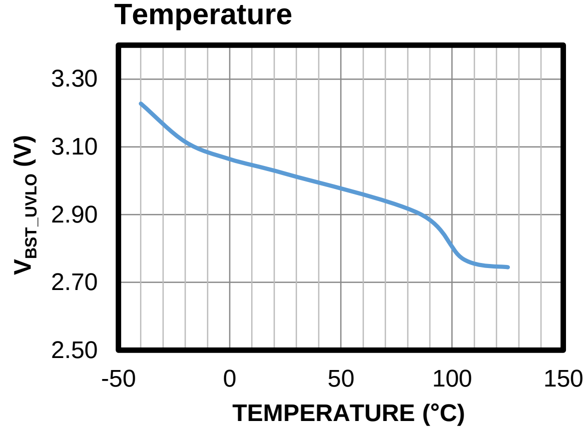
V_{IN} UV Warning Threshold vs. Temperature



V_G UVLO Threshold vs. Temperature



BST UVLO Threshold vs. Temperature

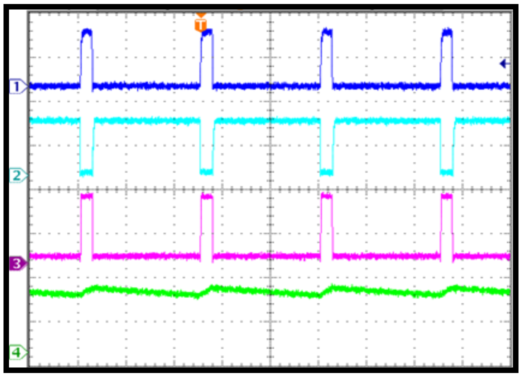


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 14V, T_A = 25°C, resistor + inductor load: R = 2Ω, L = 700µH, unless otherwise noted.

Normal Operation
20kHz, 10% duty cycle

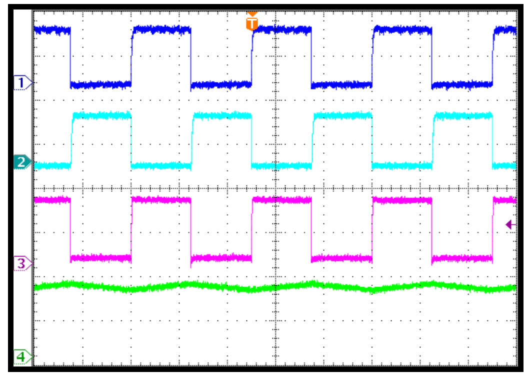
CH1: V_{GHA} 20V/div.
CH2: V_{GLA} 10V/div.
CH3: V_{SHA} 10V/div.
CH4: I_{OUT} 500mA/div.



20µs/div.

Normal Operation
20kHz, 50% duty cycle

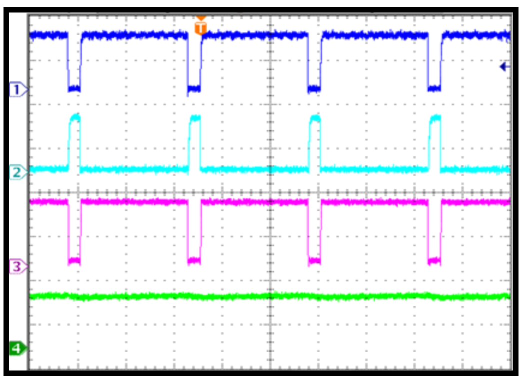
CH1: V_{GHA} 20V/div.
CH2: V_{GLA} 10V/div.
CH3: V_{SHA} 10V/div.
CH4: I_{OUT} 2A/div.



20µs/div.

Normal Operation
20kHz, 90% duty cycle

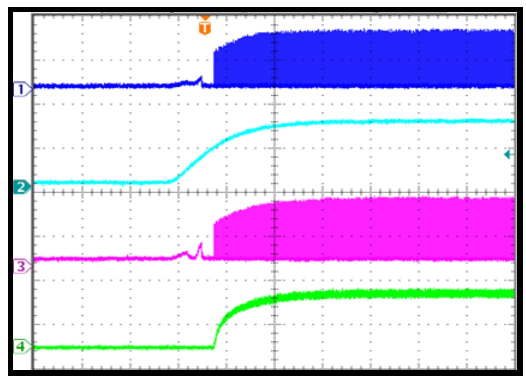
CH1: V_{GHA} 20V/div.
CH2: V_{GLA} 10V/div.
CH3: V_{SHA} 10V/div.
CH4: I_{OUT} 5A/div.



20µs/div.

Start-Up through VIN
20kHz, 50% duty cycle

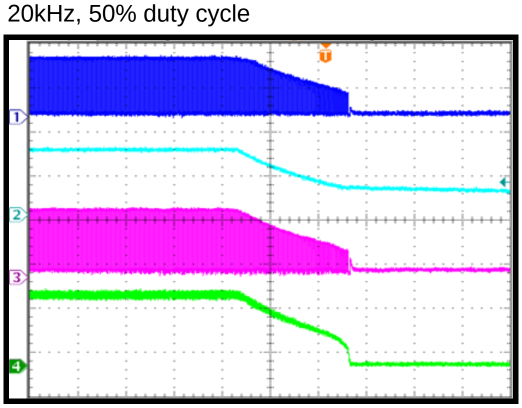
CH1: V_{GHA} 20V/div.
CH2: V_{IN} 10V/div.
CH3: V_{SHA} 10V/div.
CH4: I_{OUT} 2A/div.



4ms/div.

Shutdown through VIN
20kHz, 50% duty cycle

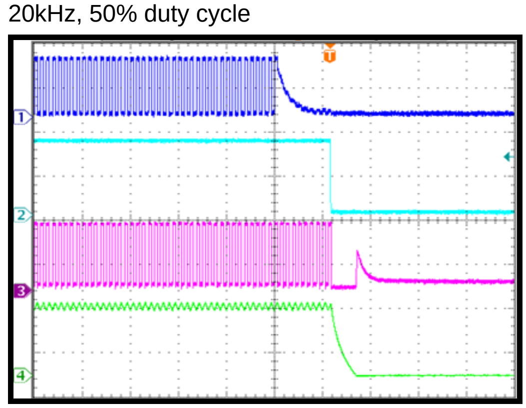
CH1: V_{GHA} 20V/div.
CH2: V_{IN} 10V/div.
CH3: V_{SHA} 10V/div.
CH4: I_{OUT} 2A/div.



4ms/div.

Sleep Mode Entry
20kHz, 50% duty cycle

CH1: V_{GHA} 20V/div.
CH2: nSLEEP 2V/div.
CH3: V_{SHA} 10V/div.
CH4: I_{OUT} 2A/div.



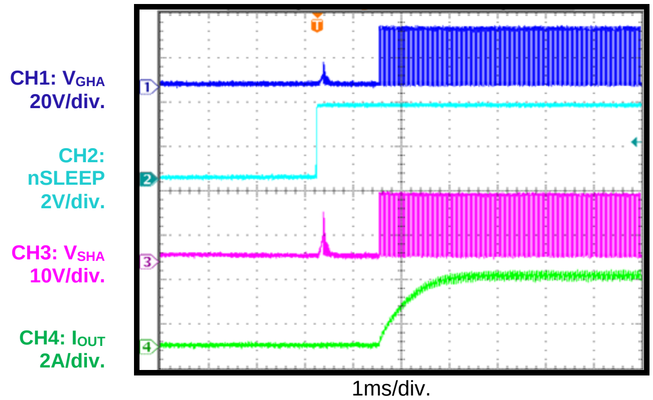
400µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 14V, T_A = 25°C, resistor + inductor load: R = 2Ω, L = 700µH, unless otherwise noted.

Sleep Mode Exit

20kHz, 50% duty cycle



FUNCTIONAL BLOCK DIAGRAM

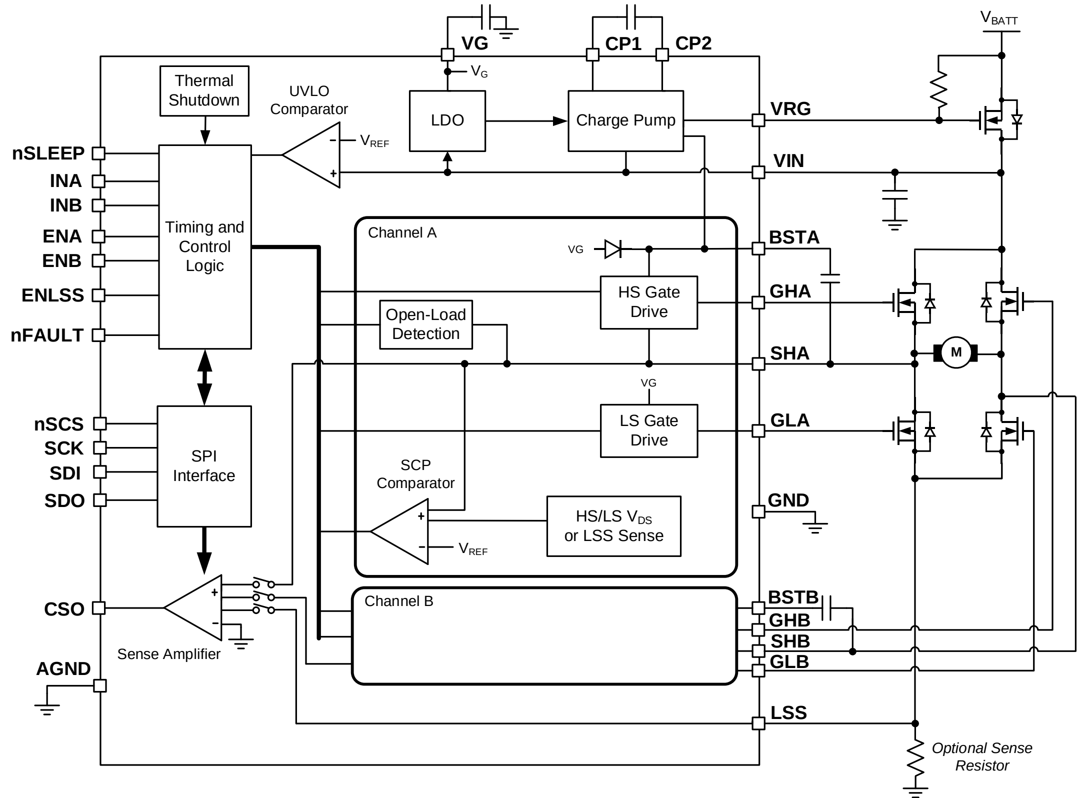


Figure 2: Functional Block Diagram

OPERATION

The MPQ6641 is a two-channel motor pre-driver that drives four N-channel MOSFETs with 0.8A source current and 1A sink current capability. It can operate across an input voltage (V_{IN}) range up to 40V. The MPQ6641 is suitable for driving DC motors or other loads in automotive applications.

Start-Up Sequence

To initiate the start-up sequence, V_{IN} and the VG pin voltage (V_G) must exceed their under-voltage lockout (UVLO) thresholds (V_{IN_UVLO} and V_{G_UVLO}, respectively). After V_{IN} and V_G are ready, the MPQ6641 sequentially turns on each low-side MOSFET (LS-FET) in succession to charge the bootstrap (BST) capacitors (C_{BST}).

The start-up sequence takes between 1ms and 2ms. Once start-up is complete, the MPQ6641 responds to logic inputs and drives the outputs.

If V_{IN} drops below V_{IN_UVLO}, or V_G drops below V_{G_UVLO}, the start-up sequence is initiated again.

Sleep Mode

Pull the nSLEEP pin low to put the device into a low-power sleep state. In this state, all internal circuits are disabled, including the reverse battery protection charge pump, and all inputs are ignored. Once the MPQ6641 exits sleep mode, wait 1ms before sending a pulse-width modulation (PWM) command. This stabilizes the internal circuitry.

Input Logic

The MPQ6641 can be controlled via the input pins (ENx and INx), by writing to the BENx and BINx bits in the OUT register via the serial peripheral interface (SPI), or a combination of both methods.

The enable function uses the level on the input pins, or it works with the state of the corresponding register bits in the OUT register. Enable control can be achieved either via the SPI or the ENx and INx pins. To invert the input state, set the BENx or BINx bit to 1.

The ENx pin or the BENx bit enables the gate drive outputs of each channel. When both the pin and bit are at the same level (both low or high), the gate drive outputs are disabled, and the INx pin and the BINx bit on that channel are ignored.

When enabled, the INx input pin and the BINx bit are recognized. Table 2 shows the logic of the ENx and INx pins, and the BENx and BINx bits.

Table 2: Input Logic Truth Table

ENx	BENx	INx	BINx	SHx
L	L	-	-	Hi-Z
L	H	L	L	GND
L	H	L	H	VIN
L	H	H	L	VIN
L	H	H	H	GND
H	L	L	L	GND
H	L	L	H	VIN
H	L	H	L	VIN
H	L	H	H	GND
H	H	-	-	Hi-Z

To control the MPQ6641 only via the SPI, connect the INx and ENx pins to ground. Then the BENx bit enables the output, and the BINx bit controls the device.

Gate Drive Voltage Regulator

The MPQ6641 provides an integrated linear regulator to generate a voltage to drive the external MOSFET gates. This voltage is supplied to VG.

A 10µF ceramic capacitor must be connected between VG and ground.

Charge Pump and Bootstrap (BST)

The high-side (HS) gate drive voltage is typically generated from C_{BST}. These capacitors are connected between the SHx and BSTx pins. When the LS-FET turns on, C_{BST} is charged.

If the output is held in a high state for an extended period, C_{BST} slowly discharges. This results in gate drive loss for the high-side MOSFET (HS-FET).

The BST voltage (V_{BST}) is monitored by an under-voltage (UV) detection circuit. If V_{BST} drops below its UVLO threshold (V_{BST_UVLO}), the device initiates a new start-up sequence.

Reverse Battery Protection Charge Pump

An internal charge pump generates a VRG pin voltage (V_{RG}) that exceeds V_{IN} by about 12V. V_{RG} drives the gate of an external N-channel MOSFET to provide reverse battery protection (see Figure 2 on page 9).

Connect a resistor between the gate and source of the external MOSFET to maintain the reverse battery conditions. It is recommended to use a 100kΩ resistor.

The charge pump uses an external capacitor connected between the CP1 and CP2 pins. It is recommended to use a 0.22µF ceramic capacitor.

The charge pump is disabled during the initial start-up sequence, and when the MPQ6641 is in sleep mode. In these scenarios, the input current (I_{IN}) flows through the MOSFET body diode.

After start-up, the charge pump is enabled by writing 1 to the ENVRG bit in the FAULT register. The ENVRG bit is toggled each time it is set to 1, and writing 0 to this bit has no effect. If the ENVRG bit is set to 1, the charge pump is enabled.

Dead-Time (DT) Adjustment

Shoot-through refers to simultaneous conduction through the HS-FET and LS-FET. To prevent shoot-through, a dead time (t_{DEAD}) is inserted between the HS-FET turning off and the LS-FET turning on, or vice versa.

t_{DEAD} for both channels is set via the xDT2~xDT0 bits in the CTRLA and CTRLB registers (for channel A and channel B, respectively). Table 3 lists the t_{DEAD} configurations.

Table 3: Dead Time Adjustment

xDT2	xDT1	xDT0	t_{DEAD}
0	0	0	50ns
0	0	1	100ns
0	1	0	200ns
0	1	1	400ns
1	0	0	800ns
1	0	1	1.6µs
1	1	0	3.2µs
1	1	1	6.4µs

Slew Rate Adjustment

To minimize EMI, the output slew rate can be controlled by changing the resistance of the gate drive's pull-up and pull-down switches (R_{DS_UP} and R_{DS_DOWN}, respectively). This resistance and the resulting slew rate are set via the xSR1~xSR0 bits in the CTRLx registers. Table 4 shows the gate drive resistances.

Table 4: Slew Rate Adjustment

xSR1	xSR0	R_{DS_UP}	R_{DS_DOWN}
0	0	200Ω	100Ω
0	1	100Ω	50Ω
1	0	50Ω	20Ω
1	1	10Ω	5Ω

When a MOSFET turns on, the other MOSFET remains off with a strong Miller clamp to prevent any parasitic start-up caused by the gate-to-drain capacitance.

Current-Sense Amplifiers

An integrated current-sense amplifier amplifies the voltage present across the LS-FETs when they turn on, or the voltage across an external sense resistor connected to the LSS pin. This voltage is output to the CSO pin. The MUX1~MUX0 bits in the CTRLD register select which of the three sources are measured and output to the CSO pin (see Table 5).

Table 5: CSO MUX Settings

MUX1	MUX0	Source
0	0	Channel A
0	1	LSS
1	0	Channel B
1	1	None

The current-sense amplifier is only active when the LS-FET turns on, and channel A or channel B is selected to be output to CSO. To enable current sense from LSS, either the ENLSS pin must be pulled logic high, or the BELSS bit must be set to 1.

If an external sense resistor is connected to LSS, and the CSO source selects channel A or channel B, the current-sense amplifier amplifies the total voltages present across the LS-FET and the sense resistor.

The current-sense amplifier gain (A_{CS}) for each channel or LSS can be configured by writing to the xGN2~xGN0 bits in the CTRLx or LSS registers. Table 6 shows A_{CS} for xGN0, xGN1, and xGN2.

Table 6: Current-Sense Amplifier Gain

xGN2	xGN1	xGN0	A_{CS}
0	0	0	20
0	0	1	40
0	1	0	60
0	1	1	80
1	0	0	100
1	0	1	150
1	1	0	200
1	1	1	250

nFAULT

The nFAULT pin reports to the system if a fault condition, such as over-current (OC) or over-temperature (OT), is detected. nFAULT is an open-drain output, and is pulled low if a fault condition occurs. Once the fault condition is cleared, an external pull-up resistor pulls nFAULT high.

Short-Circuit Protection (SCP)

To protect the MPQ6641 from excessive currents through the MOSFETs due to a short circuit, the voltage across each MOSFET (V_{DS}) is monitored when the MOSFET turns on.

If the voltage across the HS-FET exceeds the short-circuit threshold for the voltage across each external high-side MOSFET (V_{SCP_HS}), a short to ground condition is detected, and the corresponding SCHx bit in the FAULT register is set.

If the voltage across the LS-FET exceeds the short-circuit threshold for the voltage across each external low-side MOSFET (V_{SCP_LS}), a short to supply condition is detected, and the SCLx bit in the FAULT register is set.

Short-circuit protection (SCP) can be disabled or enabled via the ENSCx bits in the CTRLx registers.

V_{SCP_HS} and V_{SCP_LS} can be adjusted via the xSC2~xSC0 bits in the CTRLD register for each channel. Table 7 shows the short-circuit thresholds for the LS-FET and LSS OC detection.

Table 7: Short-Circuit Thresholds for the LS-FET and LSS

xSC2	xSC1	xSC0	V_{SCP_LS}
0	0	0	110mV
0	0	1	210mV
0	1	0	310mV
0	1	1	410mV
1	0	0	510mV
1	0	1	610mV
1	1	0	710mV
1	1	1	810mV

Table 8 shows the short-circuit thresholds for the HS-FET.

Table 8: Short-Circuit Thresholds for the HS-FET

xSC2	xSC1	xSC0	V_{SCP_HS}
0	0	0	120mV
0	0	1	220mV
0	1	0	320mV
0	1	1	420mV
1	0	0	520mV
1	0	1	620mV
1	1	0	720mV
1	1	1	820mV

It takes time to fully turn on a MOSFET. To prevent the device from falsely detecting a short-circuit condition, an adjustable blanking time (t_{BLANK}) starts from when switching starts until V_{DS} is measured. t_{BLANK} is controlled by the xBT2~xBT0 bits in the CTRLx registers (see Table 9).

Table 9: Blanking Time

xBT2	xBT1	xBT0	t_{BLANK}
0	0	0	1µs
0	0	1	2µs
0	1	0	5µs
0	1	1	10µs
1	0	0	25µs
1	0	1	100µs
1	1	0	500µs
1	1	1	1ms

If a short-circuit fault occurs, the FAULT bit is set, and the nFAULT pin is pulled active low. The OCLx or OCHx bit is set and is not cleared until it is set to 1.

If the OCMD bit in the FAULT register is set to 0, then the channel is automatically enabled again after a delay of about 1ms. If the OCMD bit is set to 1, the channel remains latched off until the corresponding OCHx, OCLx, or SCLSS bit is cleared.

LSS Over-Current Protection (OCP)

In addition to sensing V_{DS}, the voltage across a shunt resistor connected to LSS can be monitored for an OC condition. This function is similar to sensing V_{DS} for the MOSFETs.

LSS sensing must be enabled by pulling the ENLSS pin high, or by setting the BELSS bit. Then LSS OCP can be initiated.

The LSCx bits set the detection threshold (see Table 7 on page 12). When the LSS pin voltage (V_{LSS}) exceeds the detection threshold, an LSS OC condition is detected.

When an LSS OC condition is detected, the SCLSS and FAULT bits in the FAULT register are set, and nFAULT asserts.

After the fault is detected, the current-sense amplifier is disconnected from LSS. To enable the current-sense amplifier again and clear the fault, the SCLSS bit must be written to 1.

Open and Short Load Detection

The MPQ6641 integrates a circuit to detect open loads and shorts to ground or VIN. Figure 3 shows the open and load detection circuit.

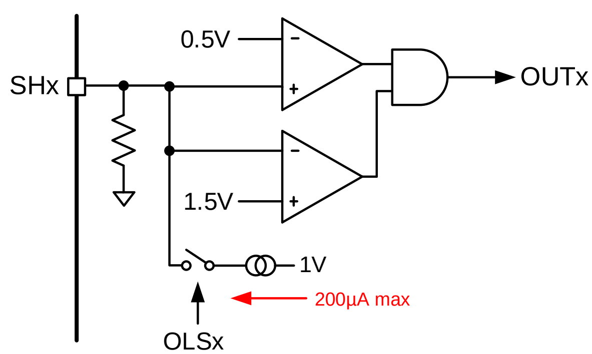


Figure 3: Open and Short Load Detection

To detect shorts to the ground or supply, the two outputs are disabled (ENx = 0). Then a limited current voltage source (1V) is enabled on an output by setting the corresponding OLSx bit in the OUTPUT register to 1.

Read the corresponding OUTx bit in the OUT register to determine whether the output is shorted to ground or VIN. If there is no short, the driven output is weakly biased to 1V, and the OUTx bit is set to 1.

If there is a load connected between the outputs, the OUTx bit that corresponds to the load's other side is biased to 1V through the connected load. As a result, this OUTx bit is set to 1. If there is no load or the load is open, the OUTx bit is pulled to ground via a weak pull-down resistor and read as 0.

If a load is connected from an output directly to VIN or ground after setting the OLSx bit, the corresponding OUTx bit is read as 0, unless the load is open.

Input Under-Voltage (UV) Warning and Under-Voltage Lockout (UVLO)

If V_{IN} drops below its UV warning threshold ($V_{IN\_UV\_WARN}$), the UVW bit in the FAULT register is set, and nFAULT is pulled active low.

If V_{IN} drops below V_{IN_UVLO}, all circuitry in the MPQ6641 is disabled, and the internal logic resets. Operation resumes once V_{IN} exceeds V_{IN_UVLO}.

VG and Bootstrap (BST) Under-Voltage (UV) Conditions

If V_G drops below V_{G_UVLO}, the VGUV bit in the FAULT2 register is set, and nFAULT is pulled low.

If either of the two BST supplies drops below the BSTUV threshold, the corresponding BSUVx bit in the FAULT2 register is set, and nFAULT is pulled active low. Then the MPQ6641 initiates a BST refresh cycle (see the Start-Up Sequence section on page 10).

Thermal Shutdown and Warning

If the die temperature exceeds safe limits, the MPQ6641 enters a fault state. The OTS and FAULT bits are set, and nFAULT is pulled active low. The MPQ6641 remains disabled until the temperature falls to a safe level, and 1 is written to the OTS bit.

If the die temperature exceeds the OT warning threshold, the OTW bit in the FAULT register is set. The bit remains set until the temperature drops below the OTW threshold.

Serial Peripheral Interface (SPI)

The SPI configures the MPQ6641's parameters, and reads status and fault information.

The SPI uses a standard 16-bit serial data packet that is composed of three address bits, one read/write (R/W) bit (1 = write, 0 = read), and 12 data bits.

Serial data is clocked into the SDI pin by the rising edges on the SCK pin, and the nSCS pin remains active low. SDO is pulled to a value according to the last SDI while nSCS is active low. SDO has a high impedance when nSCS is high.

The first three bits are the address bits that are sent to one of the registers inside the MPQ6641. These bits select the source of the data to be shifted out the SDO pin, as well as the destination of the new data.

Figure 4 shows the SPI logic diagram.

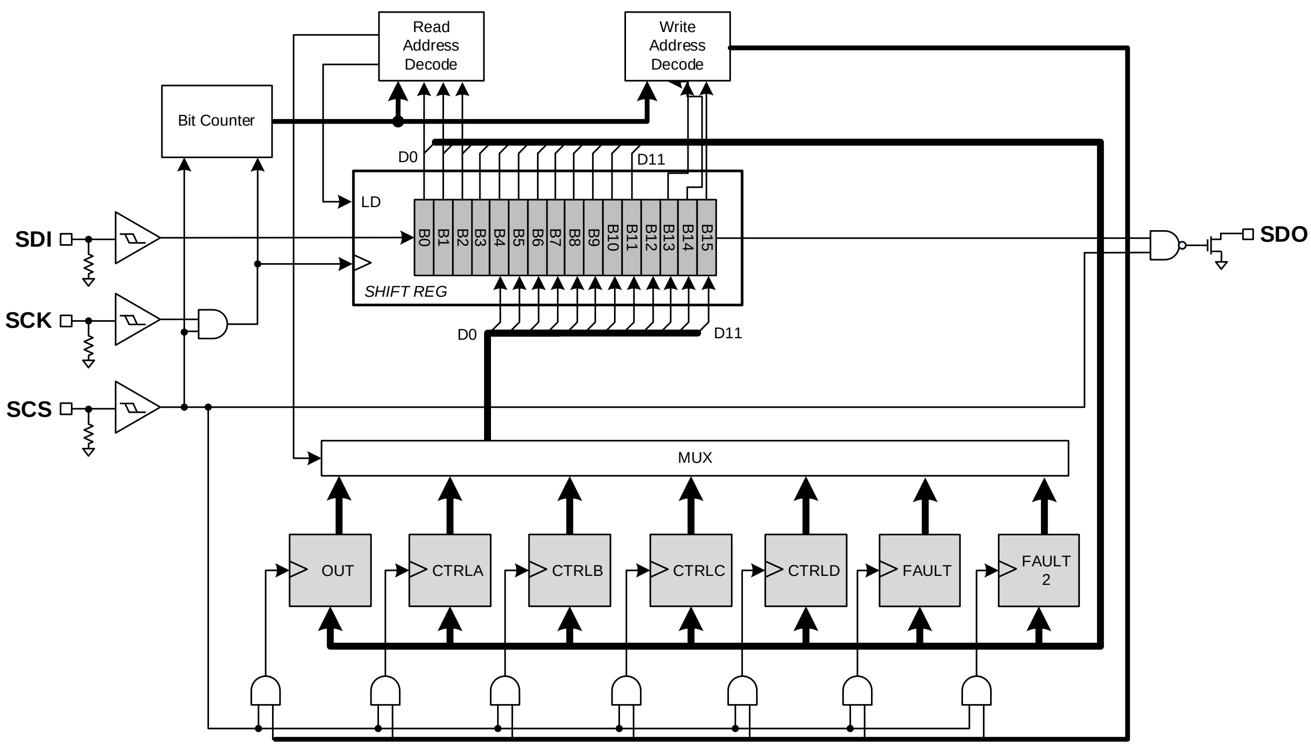


Figure 4: SPI Logic

Figure 5 shows the waveform for SPI data transfers.

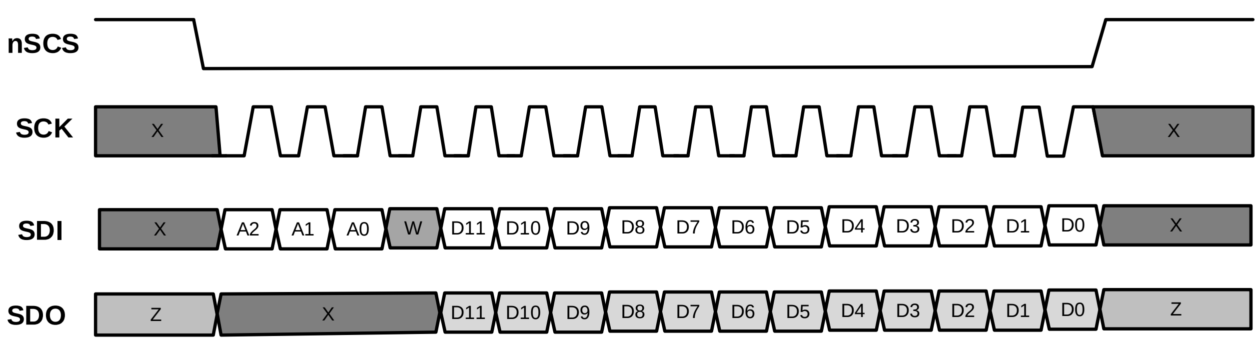


Figure 5: SPI Timing

DIAGNOSTIC AND FAULT SUMMARY

Table 10: Diagnostic and Fault Summary

Fault	Device Action	Bits Set	Bits Cleared By	nFAULT Active
Short circuit	If OCMD = 1, the output with the over-current (OC) condition latches off	SCxx, FAULT	Write 1 to SCxx	Until SCxx is cleared
	If OCMD = 0, the output with the OC condition turns off for 1ms before being re-enabled	SCxx, FAULT	Write 1 to SCxx	Until SCxx is cleared
LSS overcurrent	CSAMP disconnected from LSS (if enabled)	SCLSS, FAULT	Write 1 to SCLSS	Until SCLSS cleared
V_{IN} under-voltage (UV) warning	N/A	UVW, FAULT	Write 1 to UVW	Until UVW is cleared
V_{IN} UV shutdown	Outputs are disabled until V_{IN} exceeds the under-voltage lockout (UVLO) threshold.	UVLO, FAULT	Write 1 to UVLO	Until UVLO is cleared
Thermal shutdown	Outputs remain latched off until the temperature falls to a safe level, and the TSD bit is cleared	TSD, FAULT	Write 1 to TSD	Until TSD is cleared
Over-temperature (OT) warning	N/A	OTW	The temperature drops below T_{OT_W}	N/A
V_G UV condition	Bootstrap (BST) refresh	VGUV, FAULT	Write 1 to VGUV	Until VGUV is cleared
V_{BST} UV condition	BST refresh	BSUVx, FAULT	Write 1 to BSUVx	Until BSUVx is cleared

REGISTER MAP

OUT (00h)

The OUT command sets the serial peripheral interface (SPI) control to enable channel A and channel B. It also enables open-load detection and indicates whether there is an open-load condition on channel A and channel B.

Bits	Access	Bit Name	Reset Value	Description
11	R	OUTB	1'b 0	Indicates an open-load condition on the SHB pin.
10	R	RS0	1'b 0	Write 0 to this bit.
9	R	OUTA	1'b 0	Indicates an open-load condition on the SHA pin.
8	R/W	OLSB	1'b 0	Enables open-load detection for the voltage source on channel B. 1'b 0: Disabled 1'b 1: Enabled
7	R/W	RS0	1'b 0	Write 0 to this bit.
6	R/W	OLSA	1'b 0	Enables open-load detection for the voltage source on channel A. 1'b 0: Disabled 1'b 1: Enabled
5	R/W	BINB	1'b 0	Sets the serial peripheral interface (SPI) control for the input of channel B. This bit is XOR'd with the INB pin value.
4	R/W	BENB	1'b 0	Sets the SPI control to enable channel B. This bit is XOR'd with the ENB pin value.
3	R/W	RS0	1'b 0	Write 0 to this bit.
2	R/W	BELSS	1'b 0	Sets the SPI control to enable LSS current sensing. This bit is XOR'd with the ENLSS pin.
1	R/W	BINA	1'b 0	Sets the SPI control for channel A's input. This bit is XOR'd with the INA pin value.
0	R/W	BENA	1'b 0	Sets the SPI control to enable channel A. This bit is XOR'd with the ENA pin value.

CTRLA (01h)

The CTRLA command sets the current-sense amplifier gain, blanking time, dead time (DT), and slew rate for channel A. It also enables short-circuit protection (SCP) for channel A.

Bits	Access	Bit Name	Reset Value	Description
11	R/W	ENSCA	1'b 0	Enables SCP for channel A. 1'b 0: Disabled 1'b 1: Enabled
10:8	R/W	AGN	3'b 000	Sets the current-sense amplifier gain for channel A. 3'b 000: 20x 3'b 001: 40x 3'b 010: 60x 3'b 011: 80x 3'b 100: 100x 3'b 101: 150x 3'b 110: 200x 3'b 111: 250x

7:5	R/W	ABT	3'b 000	Adjusts channel A's blanking time. 3'b 000: 1µs 3'b 001: 2µs 3'b 010: 5µs 3'b 011: 10µs 3'b 100: 25µs 3'b 101: 100µs 3'b 110: 500µs 3'b 111: 1ms
4:2	R/W	ADT	3'b 111	Adjusts channel A's dead time. 3'b 000: 50ns 3'b 001: 100ns 3'b 010: 200ns 3'b 011: 400ns 3'b 100: 800ns 3'b 101: 1.6µs 3'b 110: 3.2µs 3'b 111: 6.4µs
1:0	R/W	ASR	2'b 00	Adjusts channel A's slew rate. 2'b 00: 200Ω pull-up resistance, 100Ω pull-down resistance 2'b 01: 100Ω pull-up resistance, 50Ω pull-down resistance 2'b 10: 50Ω pull-up resistance, 20Ω pull-down resistance 2'b 11: 10Ω pull-up resistance, 5Ω pull-down resistance

LSS (02h)

The LSS command sets the LSS current-sense amplifier gain and enables LSS SCP.

Bits	Access	Bit Name	Reset Value	Description
11	R/W	ENSCL	1'b 0	Enables LSS SCP. 1'b 0: Disabled 1'b 1: Enabled
10:8	R/W	LGN	3'b 000	Sets the current-sense amplifier gain for LSS current sensing. 3'b 000: 20x 3'b 001: 40x 3'b 010: 60x 3'b 011: 80x 3'b 100: 100x 3'b 101: 150x 3'b 110: 200x 3'b 111: 250x
7:0	R/W	RESERVED	8'b 00011100	Reserved.

CTRLB (03h)

The CTRLB command sets the current-sense amplifier gain, blanking time, DT, and slew rate for channel B. It also enables SCP for channel B.

Bits	Access	Bit Name	Reset Value	Description
11	R/W	ENSCB	1'b 0	Enables SCP for channel B. 1'b 0: Disabled 1'b 1: Enabled

10:8	R/W	BGN	3'b 000	Sets the current-sense amplifier gain for channel B. 3'b 000: 20x 3'b 001: 40x 3'b 010: 60x 3'b 011: 80x 3'b 100: 100x 3'b 101: 150x 3'b 110: 200x 3'b 111: 250x
7:5	R/W	BBT	3'b 000	Adjusts channel B's blanking time. 3'b 000: 1µs 3'b 001: 2µs 3'b 010: 5µs 3'b 011: 10µs 3'b 100: 25µs 3'b 101: 100µs 3'b 110: 500µs 3'b 111: 1ms
4:2	R/W	BDT	3'b 111	Adjusts channel B's dead time. 3'b 000: 50ns 3'b 001: 100ns 3'b 010: 200ns 3'b 011: 400ns 3'b 100: 800ns 3'b 101: 1.6µs 3'b 110: 3.2µs 3'b 111: 6.4µs
1:0	R/W	BSR	2'b 00	Adjusts channel B's slew rate. 2'b 00: 200Ω pull-up resistance, 100Ω pull-down resistance 2'b 01: 100Ω pull-up resistance, 50Ω pull-down resistance 2'b 10: 50Ω pull-up resistance, 20Ω pull-down resistance 2'b 11: 10Ω pull-up resistance, 5Ω pull-down resistance

CTRLD (04h)

The CTRLD command sets the SCP threshold for channel A, channel B and LSS, respectively, over-current protection (OCP) mode, and which channel is sensed by the current-sense amplifier and output to the CSO pin.

Bits	Access	Bit Name	Reset Value	Description
11:9	R/W	BSC	3'b 000	Sets the SCP threshold for channel B.
8:6	R/W	LSC	3'b 000	Sets the SCP threshold for LSS.
5:3	R/W	ASC	3'b 000	Sets the SCP threshold for channel A.
2	R/W	OCMD	1'b 0	Sets OCP mode. 0: The device automatically attempts to restart 1: The device latches off
1:0	R/W	MUX	2'b 00	Sets which channel is sensed by the current-sense amplifier and output to the CSO pin. 2'b 00: Channel A 2'b 01: LSS 2'b 10: Channel B 2'b 11: N/A

FAULT (05h)

The FAULT command indicates whether any fault occurs. Writing 1 to the relevant bit can clear the corresponding fault and enable the reverse battery protection charge pump.

Bits	Access	Bit Name	Reset Value	Description
11	R/W	ENVRG	1'b 0	If this bit is set to 1, the reverse battery protection charge pump is enabled. Write 1 to ENVRG to toggle this bit.
10	R	OTW	1'b 0	Indicates whether there is an over-temperature (OT) warning. 1'b 0: No OT warning 1'b 1: OT warning is reported
9	R/W	UVLO	1'b 0	Indicates whether V_{IN} under-voltage lockout (UVLO) has occurred. 1'b 0: No V_{IN} UVLO 1'b 1: V_{IN} UVLO is reported
8	R/W	UVW	1'b 0	Indicates whether there is a V_{IN} under-voltage (UV) warning. 1'b 0: No V_{IN} UV warning 1'b 1: V_{IN} UV warning is reported
7	R/W	SCHB	1'b 0	Indicates whether there is a high-side (HS) short-circuit condition on channel B. 1'b 0: No HS short-circuit on channel B 1'b 1: HS short-circuit is reported on channel B
6	R/W	RESERVED	1'b 0	Reserved.
5	R/W	SCHA	1'b 0	Indicates whether there is a HS short-circuit condition on channel A. 1'b 0: No HS short-circuit on channel A 1'b 1: HS short-circuit is reported on channel A
4	R/W	SCLB	1'b 0	Indicates whether there is a low-side (LS) short-circuit condition on channel B. 1'b 0: No LS short-circuit on channel B 1'b 1: LS short-circuit is reported on channel B
3	R/W	SCLSS	1'b 0	Indicates whether there is an over-current (OC) condition on LSS. 1'b 0: No OC condition on LSS 1'b 1: OC condition is reported on LSS
2	R/W	SCLA	1'b 0	Indicates whether there is a LS short-circuit condition on channel A. 1'b 0: No LS short-circuit on channel A 1'b 1: LS short-circuit is reported
1	R/W	OTS	1'b 0	Indicates whether OT shutdown has occurred. 1'b 0: No OT shutdown 1'b 1: OT shutdown has occurred
0	R	FAULT	1'b 0	Indicates logical 'OR' for all the other fault bits. 1'b 0: No fault has occurred 1'b 1: At least one fault has occurred

FAULT2 (06h)

The FAULT2 command indicates whether there is a bootstrap (BST) UV or V_G UV condition.

Bits	Access	Bit Name	Reset Value	Description
11:4	R/W	RESERVED	8'b 00000000	Reserved.
3	R/W	BSUVB	1'b 0	Indicates whether there is a BST UV condition on channel B. 1'b 0: No BST UV condition on channel B 1'b 1: BST UV is reported on channel B
2	R/W	RESERVED	1'b 0	Reserved.
1	R/W	BSUVA	1'b 0	Indicates whether there is a BST UV condition on channel A. 1'b 0: No BST UV condition on channel A 1'b 1: BST UV is reported on channel A
0	R/W	VGUV	1'b 0	Indicates whether there is a V_G UV condition. 1'b 0: No V_G UV condition 1'b 1: V_G UV condition is reported

APPLICATION INFORMATION

Input Voltage

The VIN pin supplies all power to the device, and must be properly bypassed with a capacitor connected to ground. The normal V_{IN} operating range is between 6V and 40V.

To protect the device, V_{IN} must never exceed the absolute maximum ratings, even under short-term transient conditions. In some cases when mechanical energy can transform a motor into a generator, it is recommended to use some additional form of over-voltage protection (OVP), such as a TVS diode placed between VIN and ground.

Reverse Battery Protection

The MPQ6641 integrates a charge pump to implement reverse battery protection using an external N-channel MOSFET. A gate-to-source resistor is required to ensure that the MOSFET remains off under reverse battery conditions.

Component Selection

Selecting the MOSFET

Correctly selecting the power MOSFETs for driving the motor is crucial.

The MOSFET must have a breakdown voltage (V_{BR}) that exceeds the supply voltage. It is recommended to add a 10V to 15V margin to prevent damage to the MOSFET from transient voltages, which are caused by parasitic inductance in the PCB layout and wiring.

For example, MOSFETs in 24V power supply applications should have a 40V to 60V V_{BR}. Additional margin is recommended for high-current applications since the transients caused by parasitic inductance may be larger. Conditions such as regenerative braking can inject current back into the power supply. Care must be taken to ensure that such conditions do not increase the power supply voltage enough to damage components.

The MOSFETs must be able to safely handle the current required to run the motor. The motor's stall current is the highest current condition (typically when the motor is first started or stalled) that must be supported by the MOSFET.

$R_{DS(ON)}$ is the MOSFET's on resistance ($R_{DS(ON)}$) when it is fully on. The power (P) dissipated by the MOSFET is proportional to $R_{DS(ON)}$ and the motor current. P can be calculated with Equation (1):

$$P = I^2 \times R \tag{1}$$

Select $R_{DS(ON)}$ to ensure that the heat generated by the power can be safely dissipated. In some cases, this may require special PCB design considerations, or implementing external heatsinks for the MOSFETs.

Consider the safe operating area (SOA) of the MOSFETs under fault conditions, such as a short circuit. The MPQ6641 acts quickly in the event of a short. However, large currents can flow in the MOSFETs for a short period (about 3µs), while the protection circuits recognize the fault and disable the outputs.

Selecting the External Capacitor

Connect the charge pump flying capacitor (C_{CP}) to the CP1 and CP2 pins. C_{CP} should have a capacitance of 220nF, and it must be rated to withstand the maximum V_{IN} power supply. An X7R or X5R ceramic capacitor is recommended.

Use C_{BST} to provide the large peak currents required to turn on the HS-FET. These capacitors are charged when the output is pulled low, then the C_{BST} charge turns on the HS-FET when the output is pulled high. An internal charge pump keeps C_{BST} charged when the output is held high for an extended period.

Select C_{BST} based on the MOSFET's total gate charge (Q_G). When the HS-FET turns on, the charge stored in C_{BST} is transferred to the HS-FET's gate. For simplification, the minimum C_{BST} can be estimated using Equation (2):

$$C_{BST} > 8 \times Q_G \tag{2}$$

Where Q_G is in nC, and the minimum C_{BST} is in nF.

C_{BST} should not exceed 1µF, or it may cause improper start-up.

For most applications, it is recommended to use ceramic capacitors for C_{BST} with X5R or X7R dielectrics. These capacitors should be between 0.1µF and 1µF, and rated for at least 25V.

The VG pin is the output of the gate drive's voltage regulator. Connect a 10µF bypass capacitor between VG and ground. It is recommended to use a X7R or X5R ceramic capacitor rated for at least 16V.

Connect a bypass capacitor between VIN and ground, placed as close to the device as possible. It is recommended to use a minimum 0.1µF ceramic capacitor with X5R or X7R dielectrics. The capacitor should be rated for V_{IN}.

Depending on the power supply impedance, the distance between the MOSFETs, and the power supply, additional bulk capacitance may be required. Low-ESR electrolytic capacitors between 47µF and 470µF are recommended.

Gate Drive Considerations

The selected MOSFETs' gate characteristics affect how quickly the MOSFETs switch on and off. Connect the MPQ6641's gate drive outputs directly to the gates of the power MOSFETs.

Slew Rate Selection

The strength of the gate drive outputs can be set via the xSR bits in the CTRLx registers. A fast slew rate reduces switching loss but may result in increased EMI. This tradeoff is also affected by the external MOSFET, which means that the slew rate must be optimized using experiments.

Figure 6 shows a waveform representing the LS-FET and HS-FET gates, and the phase node (output) with the fastest slew rate setting and minimum gate drive resistance. The scale is 100ns/div. The gates transition quickly, meaning the rising time on the phase node is fast.

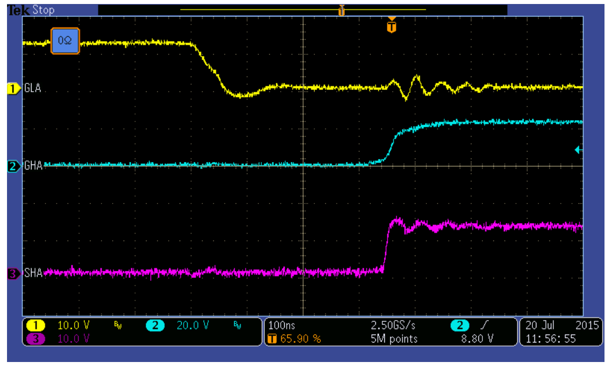


Figure 6: LS-FET and HS-FET Gates

Figure 7 shows the waveform when the slew rate is set for a 100Ω gate drive resistance. The phase node's rising time is slowed significantly. The scale is 200ns/div.

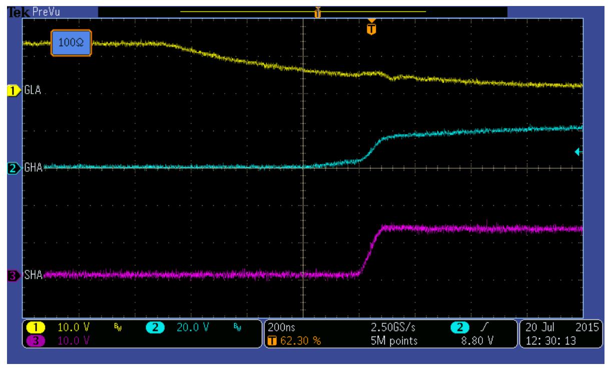


Figure 7: 100Ω Gate Drive Resistance

Dead Time Selection

During the transition between driving an output low and high, t_{DEAD} is the short period during which neither the HS-FET nor LS-FET turn on. t_{DEAD} is necessary to prevent shoot-through, a condition in which the HS-FET and LS-FET being on simultaneously can create a short circuit between the power supply and ground. Shoot-through causes large transient currents and can damage the MOSFETs.

Since motors are naturally inductive, once current is flowing in the motor, it cannot stop immediately, even if the MOSFETs are turned off. This recirculation current continues to flow in the original direction until the magnetic field decays. When the MOSFETs turn off, the current flows through the MOSFET's integrated body diode.

MOSFET body diodes have a significantly greater voltage drop than the MOSFET during conduction, meaning more power is dissipated during body diode conduction than during the MOSFET's on time. Therefore, it is ideal to minimize t_{DEAD} while ensuring it is long enough to guarantee that the HS-FET and LS-FET never turn on at the same time.

t_{DEAD} is selected via the xDT bits in the CTRLx registers. It is recommended to set t_{DEAD} to about 1µs. If faster switching or a high PWM frequency (f_{PWM}) (exceeding 30kHz) is used, a shorter t_{DEAD} may be required.

Figure 8 shows a waveform with a t_{DEAD} of 300ns between the LS-FET gate turn-off and the HS-FET gate turn-on.

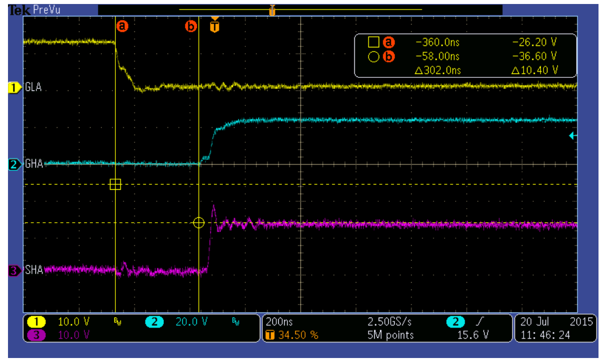


Figure 8: 200ns Dead Time

PCB Layout Guidelines

Efficient PCB layout is critical for optimal MOSFET gate driver performance. The connection between the HS-FET source and LS-FET drain must be as direct as possible to avoid negative undershoot on the phase node due to parasitic inductance. The MPQ6641 is designed to accommodate a negative undershoot, but an excessive undershoot can damage the device.

Using Surface-Mounted MOSFETs

The first PCB layout example uses surface-mounted MOSFETs. For the best results, refer to Figure 9 and follow the guidelines below:

1. Use wide copper areas for the high-current paths.
2. Place the charge pump and supply bypass capacitors close to the IC.
3. Connect the grounded side of these capacitors to a ground plane, which is connected to the device's ground pin and exposed pad.

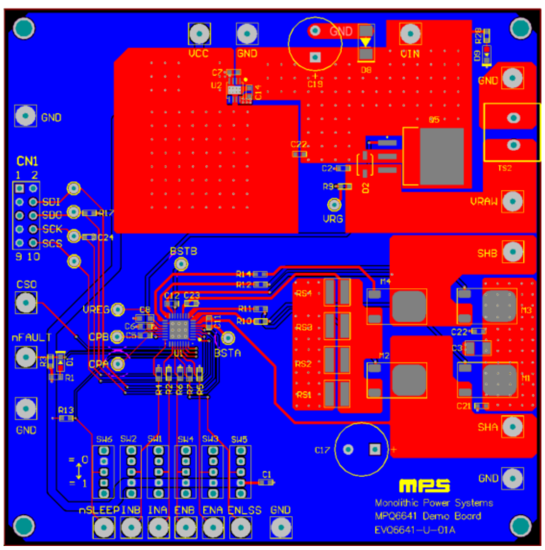


Figure 9: Recommended PCB Layout with Surface-Mounted MOSFETs

Using a Power Plane

The second PCB layout example uses a power plane. The four layers provide solid planes for the ground and supply voltage. For the best results, refer to Figure 10 and Figure 11, and follow the guidelines below:

1. Route VIN on the right portion of the plane, and connect it to the MOSFET's input power and bulk capacitors. The left portion of the plane is used as a redundant ground plane (see Figure 10).

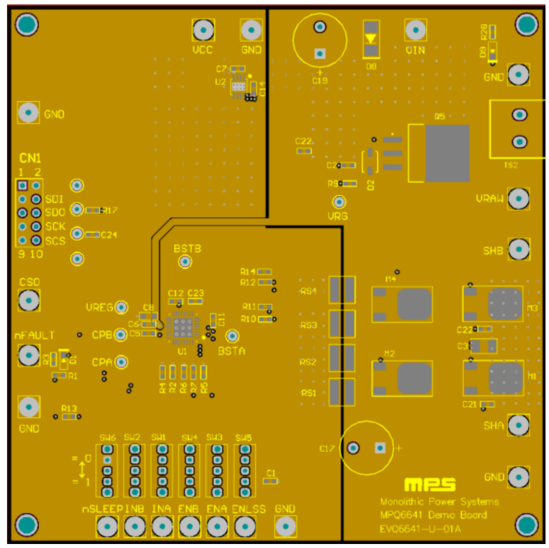


Figure 10: Recommended PCB Layout with a Power Plane

2. Use a split solid ground plane for the high-current path between the bulk capacitors.
3. Route the MOSFETs away from the rest of the circuitry. The two planes meet underneath the IC (see Figure 11).

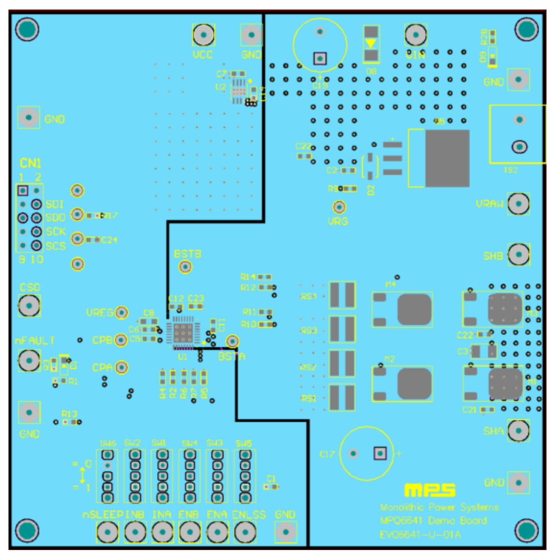


Figure 11: Recommended PCB Layout with a Power Plane

TYPICAL APPLICATION CIRCUIT

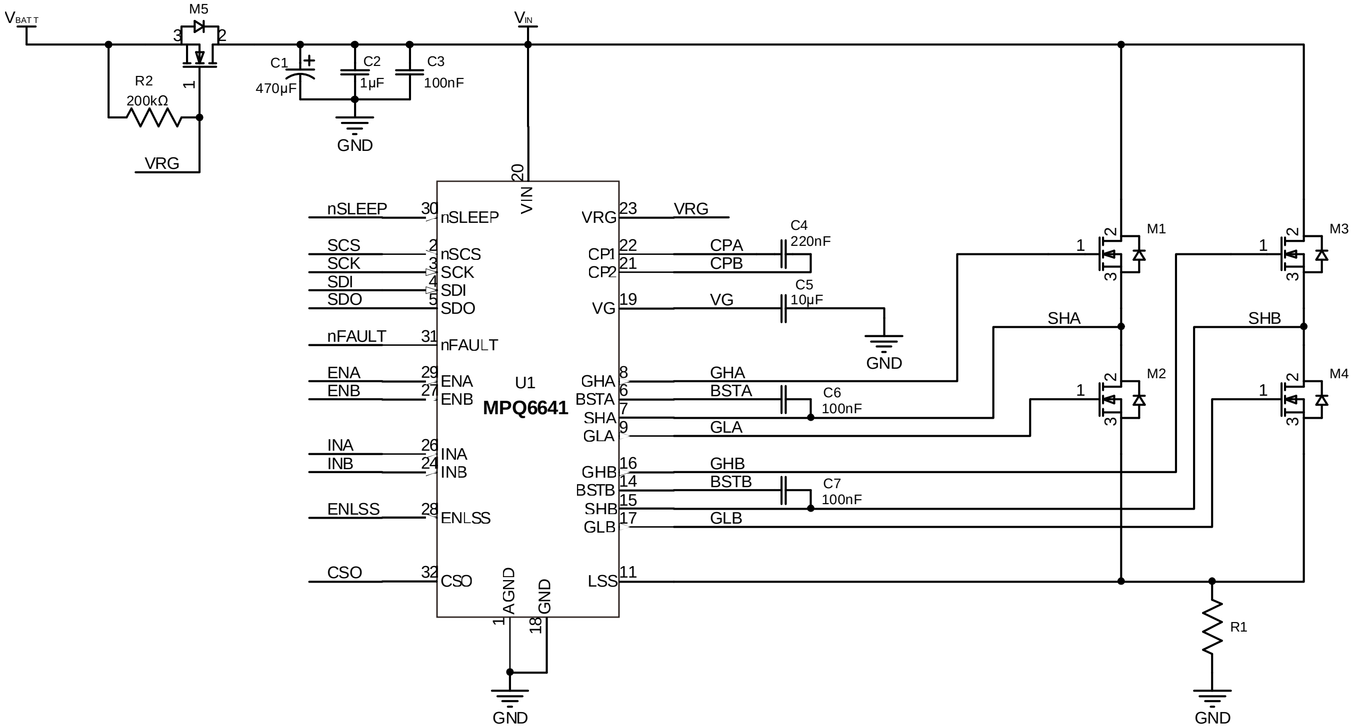
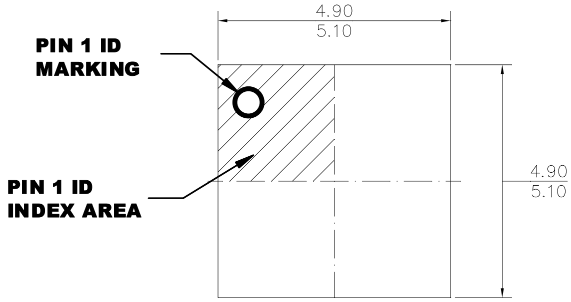


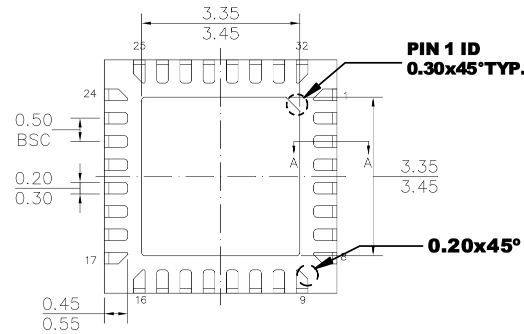
Figure 12: Typical Application Circuit

PACKAGE INFORMATION

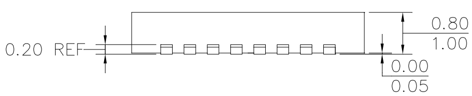
QFN-32 (5mmx5mm)



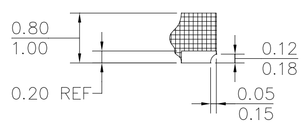
TOP VIEW



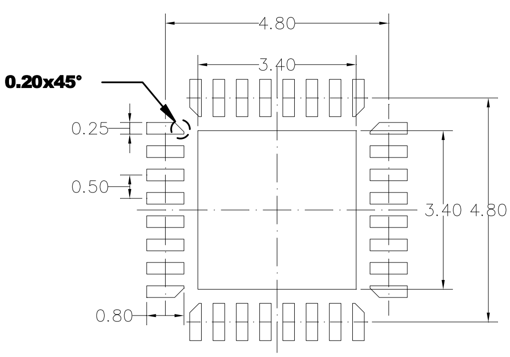
BOTTOM VIEW



SIDE VIEW



SECTION A-A

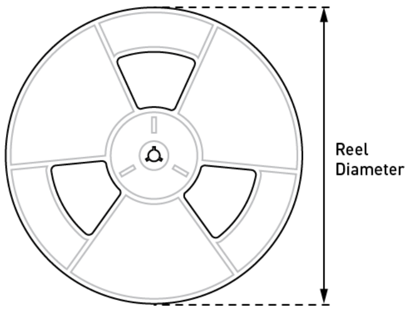


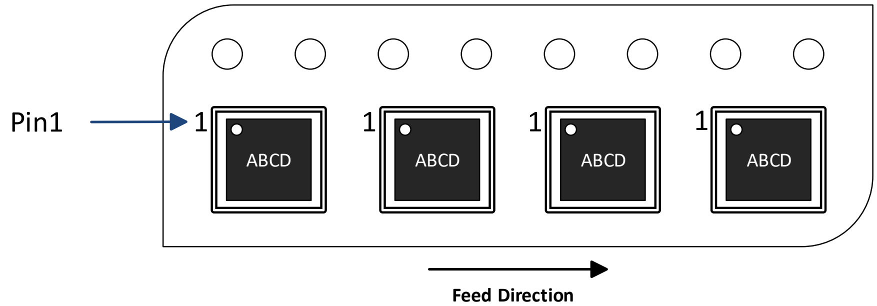
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6641GUE-AEC1-Z	QFN-32 (5mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/7/2024	Initial Release	-