MPQ6609

32V, 1A, Stepper Motor Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6609 is a stepper motor driver with current regulation and a built-in translator. The device provides internal current sensing, which does not require any external sense resistors. With high integration and a small package size, the MPQ6609 is a space-saving, cost-effective solution for stepper motor drives.

The MPQ6609 operates across a 4V to 32V input voltage (V_{IN}) range. It can deliver an output current (I_{OUT}) up to 1A per phase, based on the PCB design and thermal conditions. The device can operate a bipolar stepper motor in full-, half-, quarter-, eighth-, 1/16-, and 1/32-step modes.

Internal safety and diagnostic features include rotor stall detection, open load detection, low-temperature detection (LTD), over-current protection (OCP), over-voltage protection (OVP), under-voltage lockout (UVLO), over-temperature warning (OTW), and over-temperature shutdown (OTS).

Automatic hold current mode can reduce winding current to save power automatically when full current is not required, such as when the motor is stopped or lightly loaded.

The motor's back electromotive force (BEMF) is measured and available via the serial interface, for advanced diagnostic and control functions.

A serial interface sets the control modes such as step mode, direction, and I_{OUT}. It also reads the diagnostic registers. The STEP and DIR input pins are available to allow motor motion without serial bus transactions.

The MPQ6609 is available in a QFN-18 (3mmx4mm) package.

FEATURES

- 4V to 32V Operating Supply Input Voltage (V_{IN})
- Two Internal Full-Bridge Drivers
- Up to 1/32-Step Microstepping
- Internal Current-Sensing and Regulation
- Low On Resistance ($R_{DS(ON)}$): 350mΩ High-Side MOSFET (HS-FET), 230mΩ Low-Side MOSFET (LS-FET)
- Serial Control Interface
- Enable (EN) and Step Input (STEP) Pins
- 3.3V and 5V Compatible Logic Input
- 1A Configurable Peak Current
- Automatic Hold Current
- Automatic Current Decay
- Controlled Slew Rate
- Diagnostic Functions, Including:
  - Rotor Stall Detection
  - Back Electromotive Force (BEMF) Measurement
  - Open Load Detection
  - Over-Current Protection (OCP)
  - Over-Voltage Protection (OVP) and Under-Voltage Lockout (UVLO)
  - Over-Temperature Warning (OTW) and Over-Temperature Shutdown (OTS)
  - Low-Temperature Detection (LTD)
  - Fault Indication Output
- Available in a Space-Saving QFN-18 (3mmx4mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Stepper Motors
- Headlight Position Adjustment
- Electronic Expansion Valve (EXV) and Electrical Control Valve (ECV) Stepper Motors

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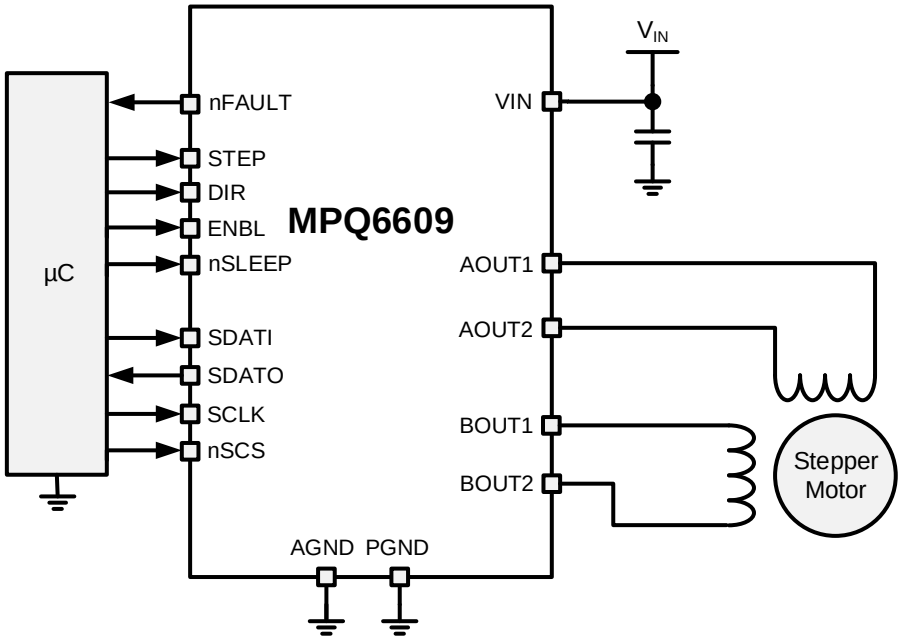
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6609GLE-AEC1	QFN-18 (3mmx4mm)	*See Below*	1

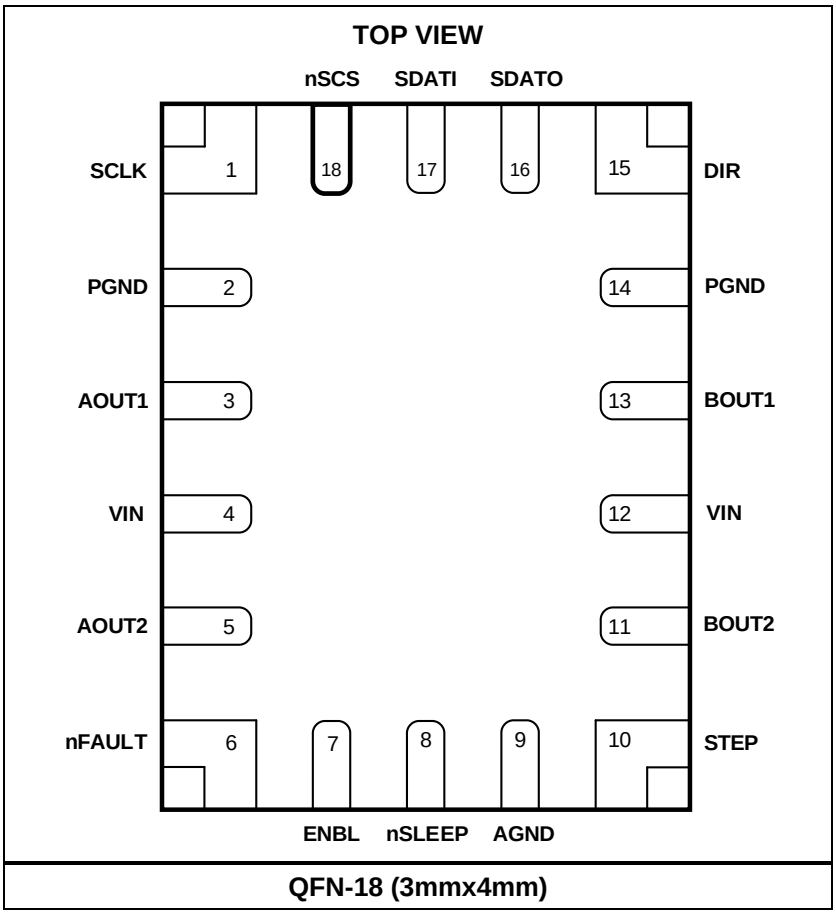
* For Tape & Reel, add suffix -Z (e.g. MPQ6609GLE-AEC1-Z).

TOP MARKING

MPYW
6609
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
6609: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-18 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	SCLK	**Serial clock.** Data is shifted on the SCLK pin's rising edge. SCLK has an internal pull-down resistor.
2, 14	PGND	**Power ground for H-bridge outputs**.
3	AOUT1	**Bridge A output terminal 1.**
4, 12	VIN	**Input supply voltage.** All VIN pins must be connected to the same supply. Decouple VIN to ground using minimum 100nF ceramic capacitors for each pin. Additional bulk capacitance may also be required based on system specifications.
5	AOUT2	**Bridge A output terminal 2.**
6	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. If there is a fault condition, pull nFAULT logic low. If this pin is used, an external pull-up resistor is required.
7	ENBL	**Enable input.** The ENBL pin works in conjunction with the EN bit (CTRL, bit[0]) (see the CTRL section on page 22). If the exclusive OR (XOR) result of ENBL and the EN bit is 1, then the outputs are enabled, and the rising edge of the step signal can be identified. ENBL has an internal pull-down resistor.
8	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin logic low to enter low-power sleep mode; pull nSLEEP logic high to enter normal operation. nSLEEP has an internal pull-down resistor.
9	AGND	**Signal ground.**
10	STEP	**Step input.** The rising edge advances the motor by one increment. The STEP pin has an internal pull-down resistor.
11	BOUT2	**Bridge B output terminal 2.**
13	BOUT1	**Bridge B output terminal 1.**
15	DIR	**Direction Input.** The DIR pin works in conjunction with the DIR bit (CTRL, bit[2]) to set the step direction (see the CTRL section on page 22). DIR has an internal pull-down resistor.
16	SDATO	**Serial data output.** The SDATO pin has an internal pull-down resistor.
17	SDATI	**Serial data input.** The SDATI pin has an internal pull-down resistor.
18	nSCS	**Serial chip selection input.** The nSCS pin is pulled up internally.

ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN}).....-0.3V to +40V
AOUT1/2, BOUT1/2 voltage ($V_{A/BOUT1/2}$).....
.....-0.7V to +40V
$V_{A/BOUT1/2}$ (<100ns transient).....-2V to +40V
All other pins to ground.....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-18 (3mmx4mm)… 2.6W
Storage temperature..... -65°C to +150°C
Junction temperature (T_J) .....175°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM).....±2kV
Charged-device model (CDM).....±750V

Recommended Operating Conditions (3)

Input supply voltage (V_{IN}).....4V to 32V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-18 (3mmx4mm)..... 48 ..... 11... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, a 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4		32	V
Quiescent current	I_{IN_Q}	XOR result of ENBL and EN (CTRL, bit[0] = 0, nSLEEP = 1, no load, power stage off		2.5	3.5	mA
	I_{IN_SLEEP}	nSLEEP = 0, T_J = 25°C			1	µA
		nSLEEP = 0, T_J = -40°C to +150°C			10	µA
Internal MOSFETs						
Output on resistance	$R_{DS(ON)_HS}$	I_{OUT} = 100mA, T_J = 25°C		350	420	mΩ
		I_{OUT} = 100mA, T_J = 150°C		570		mΩ
	$R_{DS(ON)_LS}$	I_{OUT} = 100mA, T_J = 25°C		230	270	mΩ
		I_{OUT} = 100mA, T_J = 150°C		350		mΩ
Body diode forward voltage	V_F	I_{OUT} = 500mA			1.1	V
Control Logic Inputs						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		1.6			V
Logic input current	I_{IN_H}	V_{IH} = 5V	-20		+20	µA
	I_{IN_L}	V_{IL} = 0V	-20		+20	µA
Internal pull-down resistance	R_{PD}	To ground		530		kΩ
Internal pull-up resistance	R_{PU}	To internal VCC		530		kΩ
nFault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	V_{IN_RISE}		3.3	3.6	3.9	V
V_{IN} UVLO hysteresis	ΔV_{IN_RISE}			460		mV
V_{IN} over-voltage protection (OVP) rising threshold	V_{OVP}		37	38	39	V
V_{IN} OVP hysteresis	ΔV_{OVP}			2.1		V
Open load detection current	I_{OL}			100		µA
Over-current (OC) trip level	I_{OCP1}	Sinking	1.5	2.5	3.5	A
	I_{OCP2}	Sourcing	1.5	2.5	3.5	A
OC deglitch time (5)	t_{OCP}			1		µs
Over-temperature shutdown (OTS) (5)	T_{OTS}			165		°C
OTS hysteresis (5)	ΔT_{OTS}			20		°C
Over-temperature warning (OTW) (5)	T_{OTW}			155		°C
OTW hysteresis (5)	ΔT_{OTW}			10		°C

Note:

5) Not tested in production, guaranteed by design.

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to 150°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Bridge Output						
Rising/falling time	t_{RF}	SR1~SR0 (TSTP, bits[8:7]) = 00b		150		ns
		SR1~SR0 = 01b		300		ns
		SR1~SR0 = 10b		1		µs
		SR1~SR0 = 11b		2		µs
Current Control						
Constant off time	t_{OFF}	OT2~OT0 (CTRL, bits[8:6]) = 010b	27	30	33	µs
Blanking time	t_{BLANK}	BT2~BT0 (CTRL2, bits[2:0]) = 100b		2		µs
Dead time	t_{DT}	HS-FET off to LS-FET on or LS-FET off to HS-FET on for one bridge, SR1~SR0 = 00b		650		ns
Current trip accuracy	ΔI_{TRIP}	I_{OUT} = 71% to 100% of I_{PEAK}, T_J = -40°C to +85°C	-5		+5	% of I_{PEAK}
		I_{OUT} = 38% to 67% of I_{PEAK}, T_J = -40°C to +85°C	-7		+7	% of I_{PEAK}
		I_{OUT} < 34% of I_{PEAK}, T_J = -40°C to +85°C	-15		+15	% of I_{PEAK}
Back Electromotive Force (BEMF) Measurement						
BEMF gain	A_{BEMF}	BEG2~BEG0 (BEMFA, bits[10:8]) = 001b	0.235	0.25	0.265	V/V
		BEG2~BEG0 = 010b	0.475	0.5	0.525	
		BEG2~BEG0 = 011b	0.96	1	1.04	
		BEG2~BEG0 = 100b	1.9	2	2.1	
		BEG2~BEG0 = 101b	4.7	5	5.3	
BEMF analog-to-digital converter (ADC) accuracy	ΔADC	BEG2~BEG0 = 011b, V_{BEMF} = 0.3V	-7		+7	LSB
		BEG2~BEG0 = 011b, V_{BEMF} = 2.7V	-9		+9	

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TIMING CHARACTERISTICS (6)

T_J = -40°C to 150°C, unless otherwise noted.

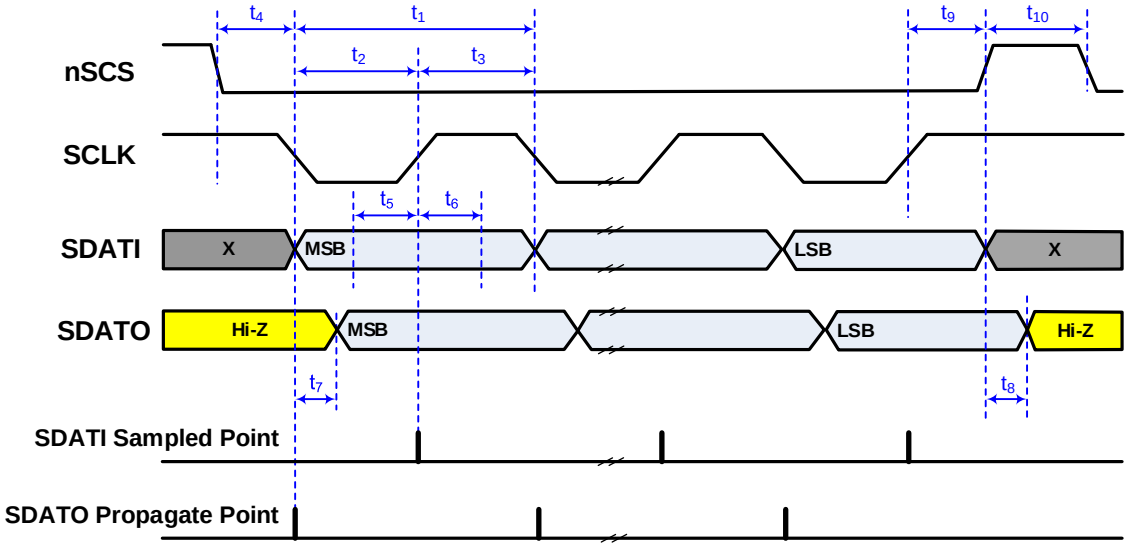

Figure 1: SPI Timing Characteristics

Table 1: Timing Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCLK cycle time	t_1		100			ns
SCLK frequency			0.1		10	MHz
SCLK low time	t_2		50			ns
SCLK high time	t_3		50			ns
nSCS input set-up time (nSCS low to SCLK falling)	t_4		30			ns
SDATI input set-up time (SDATI valid to SCLK rising)	t_5		15			ns
SDATI input hold time (SCLK rising to SDATI valid)	t_6		10			ns
SDATO output delay time (SCLK falling to SDATO valid)	t_7	C_L = 20pF			50	ns
nSCS disable delay time (nSCS high to SDATO high impedance)	t_8				50	ns
nSCS input hold time (SCLK rising to nSCS inactive)	t_9		30			ns
nSCS inactive time	t_{10}		100			ns

Note:

6) Not tested in production, guaranteed by design.

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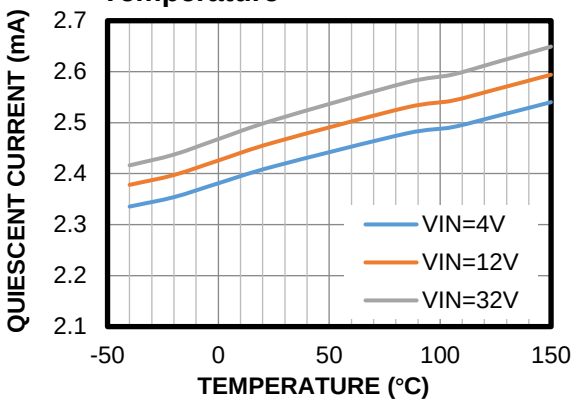
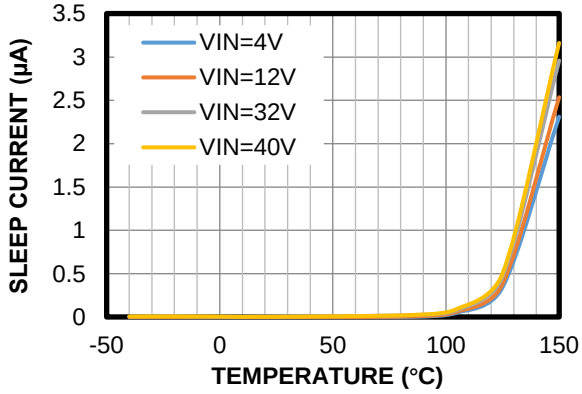
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 150°C, unless otherwise noted.

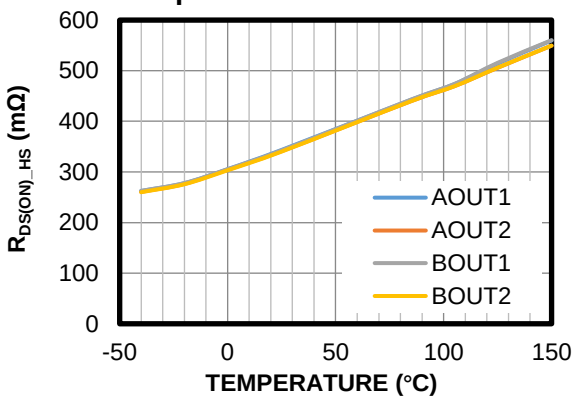
Quiescent Current vs. Temperature



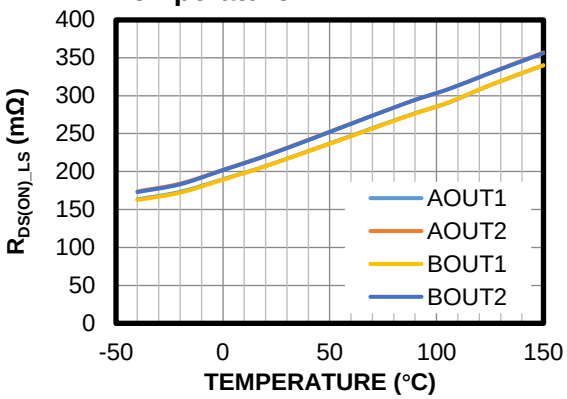
Sleep Current vs. Temperature



HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature



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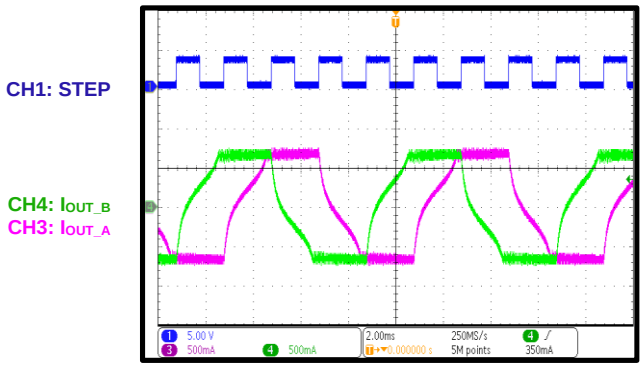
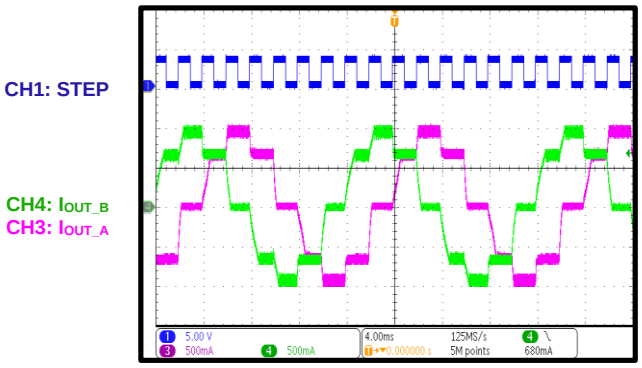
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, I_{PEAK} = 1A, T_A = 25°C, bipolar stepper motor (R = 5.9Ω, L = 13.5mH/phase), unless otherwise noted.

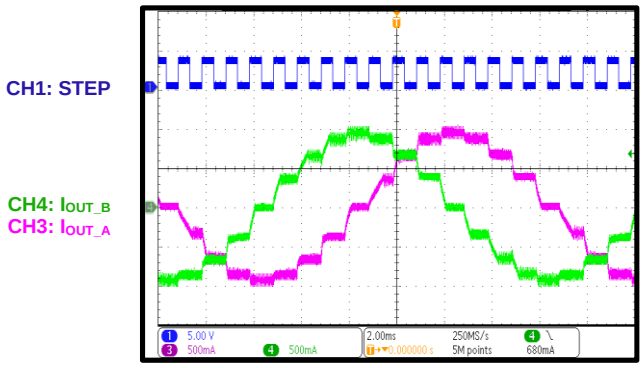
Full Step



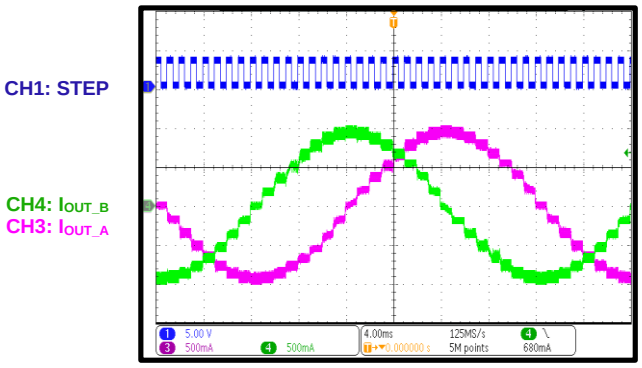
Half-Step



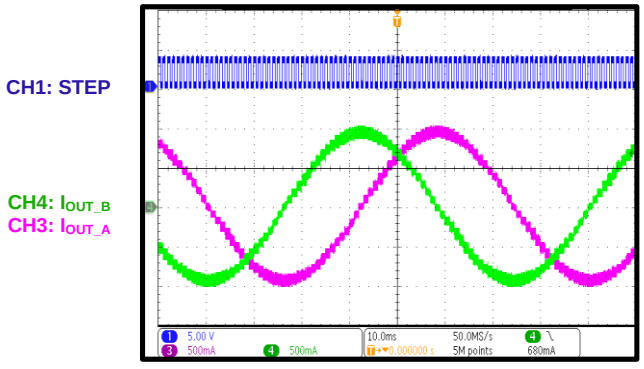
1/4-Step Microstepping



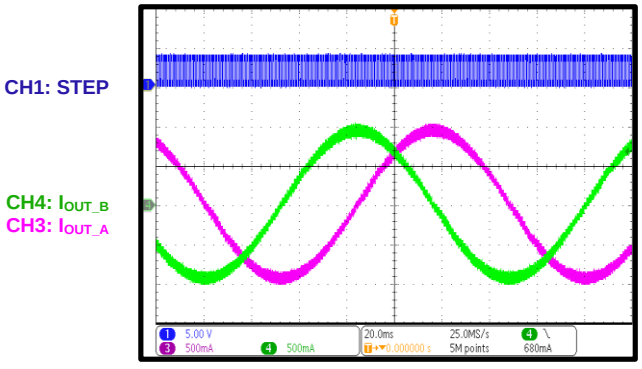
1/8-Step Microstepping



1/16-Step Microstepping



1/32-Step Microstepping



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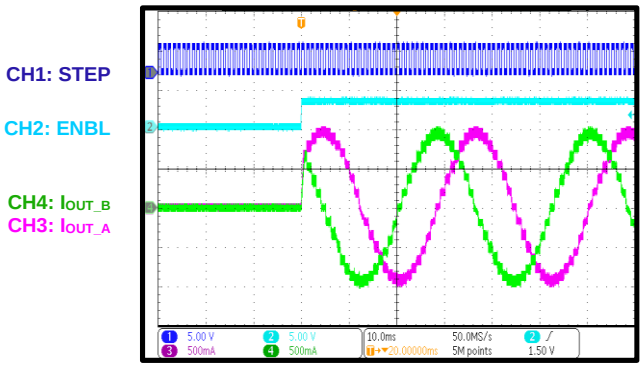
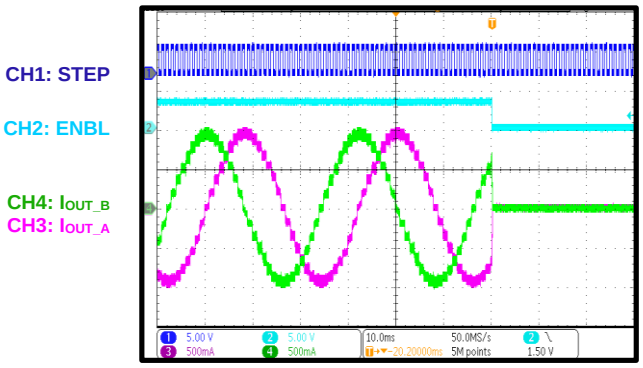
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, I_{PEAK} = 1A, T_A = 25°C, bipolar stepper motor (R = 5.9Ω, L = 13.5mH/phase), unless otherwise noted.

Output Enabled

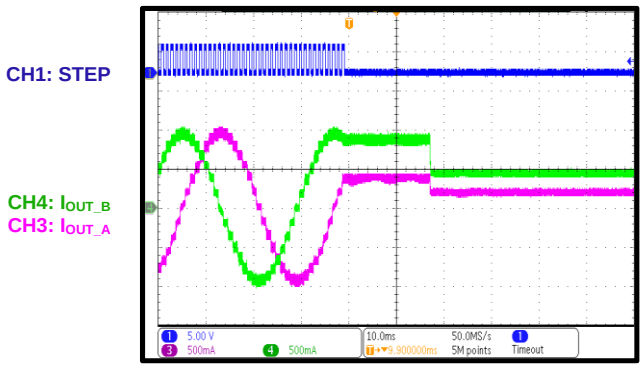


Output Disabled



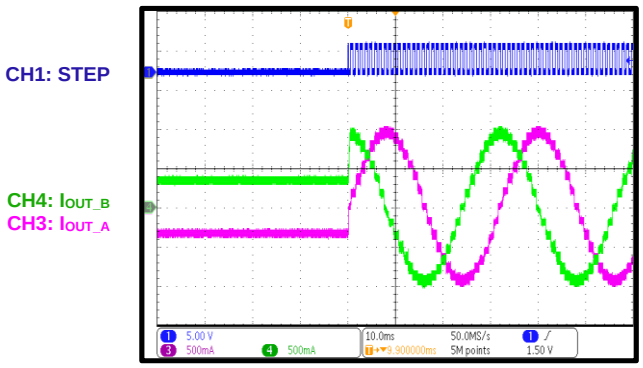
Automatic Hold Current Entry

Peak hold current = 500mA



Automatic Hold Current Exit

Peak hold current = 500mA



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FUNCTIONAL BLOCK DIAGRAM

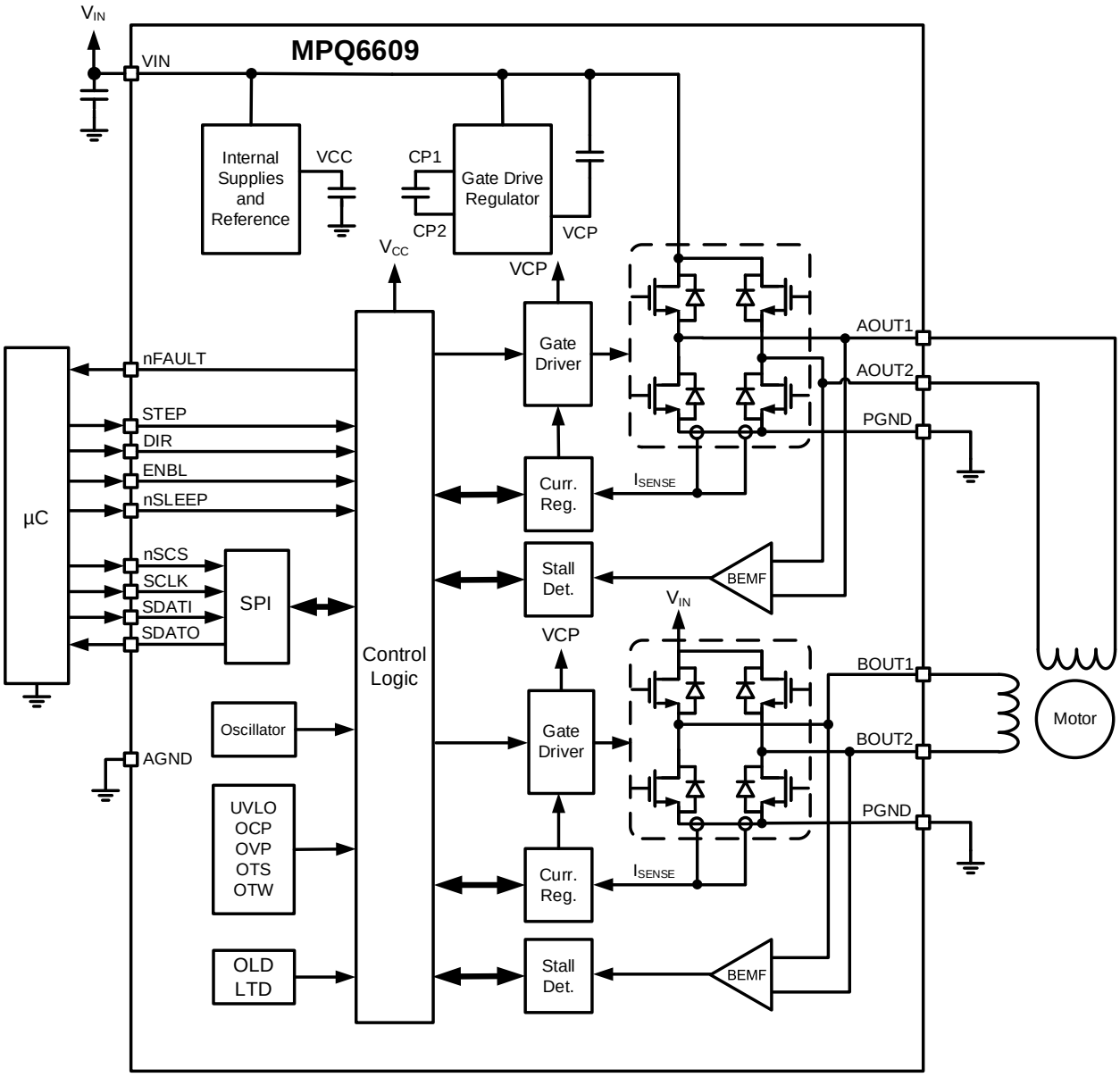

Figure 2: Functional Block Diagram

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OPERATION

The MPQ6609 is a microstepping stepper motor driver for bipolar stepper motors. It integrates eight N-channel power MOSFETs connected as two full H-bridges.

A serial peripheral interface (SPI) control interface is used to configure device operation, as well as to read back the device status and access diagnostic information. In addition, the motor may be stepped by logic signals applied to the STEP and DIR input pins.

The MPQ6609 is designed to operate bipolar stepper motors in full-, half-, quarter-, eighth-, 1/16-, and 1/32-step modes. At each step, the current of each full bridge is set by the output voltage (V_{OUT}) of a digital-to-analog converter (DAC), which is controlled by the translator's output.

The currents in each of the two outputs are regulated with configurable, constant-off-time (COT) pulse width modulation (PWM) control circuitry.

The MPQ6609 does not require external sense resistors due to its integrated internal current-sensing. The peak motor current is set by writing to the SPI.

nSLEEP and ENBL Operation

Pulling the nSLEEP pin low makes the MPQ6609 enter a low-power sleep state. In this state, all the internal circuits and H-bridge outputs are disabled. In addition, all inputs are ignored and all register contents are reset to their power-up values. The indexer is reset, and all faults are cleared when nSLEEP is active low.

When the device wakes up from sleep mode, about 1ms must pass before a STEP command can be issued, which allows the internal circuitry to stabilize. nSLEEP has an internal pull-down resistor.

The ENBL pin works in conjunction with the EN bit (CTRL, bit[0]) to control the output drivers. The value from ENBL pin is exclusive-ORed with the value of the EN bit. If the result is 1, then the H-bridge outputs are enabled, and the rising edge on the STEP pin can be identified. If the result is 0, then the H-bridge outputs are disabled, and the step input is ignored.

If ENBL is low and the EN bit is set, then the outputs are enabled; if ENBL is high and the EN bit is low, then the outputs are enabled. Otherwise, the outputs are disabled. ENBL has an internal pull-down resistor.

Stepping

To increment or decrement the contents of the TSTP command, one of the following is required: a rising edge on the step input, or writing 1 to the STEP bit (CTRL, bit[1]). The state of the DIR pin, exclusive-ORed with the DIR bit (CTRL, bit[2]), determines if the register is incremented or decremented.

The translator uses the value in the TSTP command to control the magnitude and direction of the current driven in each winding.

In addition to moving the motor using the STEP bit or input pin, the TSTP command can be accessed directly (read and written) via the SPI. This allows for readback of the current position, and immediately jumping to any spot in the step table.

Step Mode Selection

The MPQ6609 supports full-, half-, quarter-, eighth-, 1/16-, and 1/32-step modes for progressively finer step resolution and control.

The step mode is selected via the MS2, M21, and MS0 bits (CTRL, bits[5:3]). Table 2 shows the step mode settings.

Table 2: Step Mode Settings

MS2~MS0	Step Mode
000b	Full step
001b	Half step
010b	Quarter step
011b (reset value)	Eighth step
100b	1/16 step
101b	1/32 step

Current Control Operation

The winding current is regulated by a COT PWM current control circuit, which uses an automatic decay mode to accurately regulate winding current.

At the beginning of a PWM cycle, a diagonal pair of MOSFETs turns on and drives current through the motor winding. The current increases in the motor winding, which is sensed

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by an internal current-sense circuit. During the initial blanking time (t_{BLANK}), the MOSFETs always turn on.

When the current reaches the current trip threshold (I_{TRIP}), the internal current comparator turns off the high-side MOSFET (HS-FET) and turns on the low-side MOSFET (LS-FET). This allows the winding current to freewheel through the two LS-FETs (slow decay). The current decays for the constant off time (t_{OFF}).

At the end of t_{OFF}, if the current is below I_{TRIP}, then a new PWM cycle begins. If the current exceeds I_{TRIP}, then fast decay mode is initiated by reversing the state of the H-bridge outputs. Once the current level during this fast decay period drops below I_{TRIP}, slow decay is engaged again for t_{OFF}. After this second fixed t_{OFF} completes, a new PWM cycle begins.

Figure 3 shows automatic decay mode during a current reduction as a result of a step input.

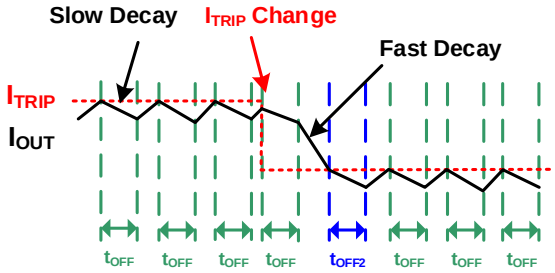

Figure 3: Automatic Decay Mode during t_{OFF} (when $I_{OUT} > I_{TRIP}$ at the End of t_{OFF})

In the case of high voltage and low inductance, or the regulation of small currents, the minimum on time (t_{ON_MIN}) of the PWM cycle (set by t_{BLANK}) can cause the current to significantly exceed the desired I_{TRIP} level. In this scenario, slow and fast decay alternate (see Figure 4).

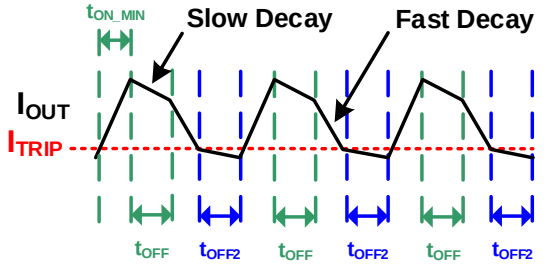

Figure 4: Current Regulation of Slow and Fast Decay Mode

The constant t_{OFF} is determined via the OT2, OT1, and OT0 bit settings (CTRL, bits[8:6]). Table 3 shows the t_{OFF} settings.

Table 3: t_{OFF} Settings

OT2~OT0	t_{OFF}
000b	20µs
001b	25µs
010b (reset value)	30µs
011b	35µs
100b	40µs
101b	45µs
110b	50µs
111b	55µs

Blanking Time

There is typically a current spike during PWM turn-on due to the body diode's reverse-recovery current or the motor winding's distributed capacitance. This current spike requires filtering to prevent current regulation at an insufficient level.

After the PWM cycle begins, the output of the current-sense comparator is ignored for a fixed t_{BLANK}. This fixed t_{BLANK} also results in a t_{ON_MIN} for the PWM cycle.

t_{BLANK} is configurable via the BT2, BT1, and BT0 bits (CTRL2, bits[2:0]). Table 4 shows the t_{BLANK} settings.

Table 4: t_{BLANK} Settings

BT2~BT0	t_{BLANK}
000b	250ns
001b	500ns
010b	1µs
011b	1.5µs
100b (reset value)	2µs
101b	2.5µs
110b	3µs
111b	3.5µs

Current Setting

The full-scale (100%) regulation current ($I_{100\%}$) is set via the IS5, IS4, IS3, IS2, IS1, and IS0 bits (ISET, bits[5:0]). Table 5 on page 14 shows the full-scale current settings, where bits IS5~IS0 are for the current setting during normal operation, and the IL5, IL4, IL3, IL2, IL1, and IL0 bits (ISET, bits[11:6]) are for the hold current setting.

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Table 5: Full-Scale Current Settings

IS5~IS0, IL5~IL0	Peak Current ($I_{100\%}$)	IS5~IS0, IL5~IL0	Peak Current ($I_{100\%}$)
0x00	50mA	0x10	450mA
0x01	75mA	0x11	475mA
0x02	100mA	0x12	500mA
0x03	125mA	0x13	525mA
0x04	150mA	0x14	550mA
0x05	175mA	0x15	575mA
0x06	200mA	0x16	600mA
0x07	225mA	0x17	625mA
0x08 (Reset Value)	250mA	0x18	650mA
0x09	275mA	0x19	700mA
0x0A	300mA	0x1A	750mA
0x0B	325mA	0x1B	800mA
0x0C	350mA	0x1C	850mA
0x0D	375mA	0x1D	900mA
0x0E	400mA	0x1E	950mA
0x0F	425mA	0x1F	1A

The translator output controls two DACs, one for each motor phase. This sets I_{TRIP} according to the value in the TSTP command and a fixed sine/cosine function. I_{TRIP} can be calculated with Equation (1):

$$I_{TRIP} = \%I_{PEAK} \times I_{100\%} \quad (1)$$

See the Appendix 1: Microstepping section on page 28 for more details regarding the $\%I_{PEAK}$ values for each value of the TSTP command.

Slew Rate (SR) Control

The MPQ6609 integrates configurable slew rate control to quickly reduce electromagnetic interference (EMI) generated by the output switching action. The slew rate is configurable via the SR1 and SR0 bits (TSTP, bits[8:7]). Table 6 shows the slew rate adjustment.

Table 6: Slew Rate Adjustment

SR1~SR0	Rising/Falling Time (t_{RF})
00b (reset value)	150ns
01b	300ns
10b	1µs
11b	2µs

Charge Pump

An internal charge pump generates the gate drive for the HS-FETs. The charge pump frequency can be set to four selections via the CPF1 and CPF0 bits (TSTP, bits[10:9]). Table 7 shows the charge pump frequency settings.

Table 7: Charge Pump Frequency Settings

CPF1~CPF0	Charge Pump Frequency
00b	4MHz
01b (reset value)	2MHz
10b	1MHz
11b	500kHz

Automatic Hold Current

The current required in the windings of a stepper motor is dependent on the load torque applied to the motor. When the motor is stopped, the current can be reduced, saving energy and reducing power dissipation. The MPQ6609 has automatic hold current circuitry to provide an automatic means to reduce the winding current when full current is not needed.

When automatic hold is enabled, if there are no edges on the step input or register for a period of time, then the winding current is changed to the value set via bits IL5~IL0, scaled by the $\%I_{PEAK}$ value of the current step.

As soon as activity resumes on the step input, the current immediately increases to the value set via the IS5, IS4, IS3, IS2, IS1, and IS0 bits, scaled by the $\%I_{PEAK}$ value of the current step.

The automatic hold function is controlled via the AH2, AH1, and AH0 bits (CTRL, bits[11:9]). The setting of the AH2~AH0 bits sets the amount of time that passes with no STEP activity until the automatic hold current is activated. If the AH2~AH0 bits are set to 0, then the automatic hold is disabled (see Table 8).

Table 8: Automatic Hold Time Settings

AH2~AH0	Auto Hold Time	Min. Steps/Sec
000b (reset value)	Disabled	-
001b	15.6ms	64
010b	31.3ms	32
011b	62.5ms	16
100b	125ms	8
101b	250ms	4
110b	500ms	2
111b	1000ms	1

When the MPQ6609 enters automatic hold state, stall detection is disabled.

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Figure 5 shows the current control circuitry diagram.

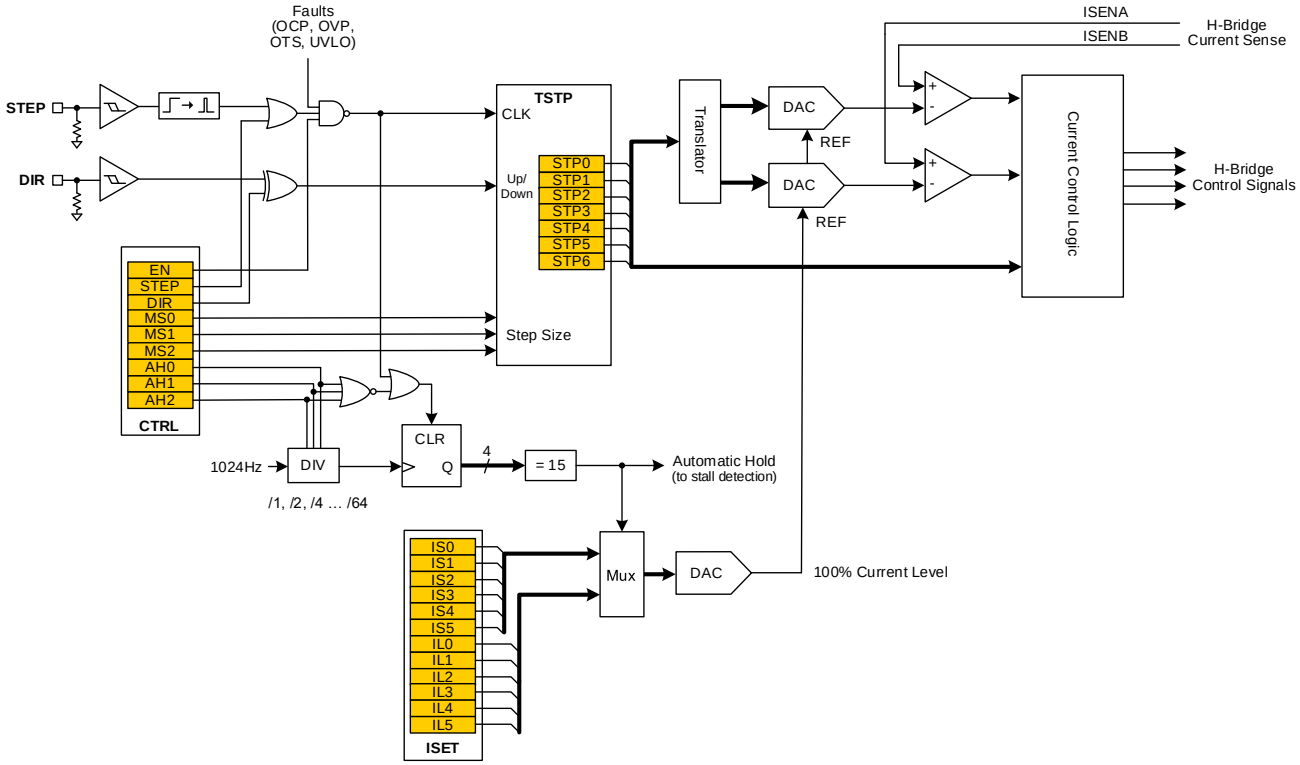

Figure 5: Current Control Circuitry Diagram

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DIAGNOSTIC AND PROTECTION FUNCTIONS

Fault Pin (nFAULT)

The MPQ6609 provides a fault pin (nFAULT) that reports fault conditions. nFAULT is an open-drain output and is pulled low if a fault condition occurs. Once the fault condition is removed and the set bit is cleared, then nFAULT is pulled high via an external pull-up resistor.

The fault source can be determined by reading the FAULT command via the serial peripheral interface (SPI).

Over-Current Protection (OCP)

If the current though a MOSFET exceeds the over-current (OC) limit threshold, and lasts for longer than the OC deglitch time (t_{OCP}), then over-current protection (OCP) is triggered. All MOSFETs in both H-bridges are disabled. The corresponding OCA bit (FAULT, bit[6]), OCB bit (FAULT, bit[7]), and FLT bit (FAULT, bit[0]) are set. nFAULT is pulled low. The MPQ6609 stays in this state until the FLT bit is cleared by writing 1 to the OCA or OCB bit.

OC conditions are detected independently on both the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET), e.g. excessive current from an output to ground, supply, or to another output all result in an OC shutdown.

The OCA and OCB bits can be read to determine if the fault is detected on H-bridge A or H-bridge B.

Over-Voltage Protection (OVP)

If the input voltage (V_{IN}) on the VIN pin exceeds the over-voltage protection (OVP) rising threshold (typically 38V), then the H-bridge outputs are disabled. The OVP bit (FAULT, bit[2]) and FLT bit (FAULT, bit[0]) are set, and nFAULT is pulled low. This protection is released, and the H-bridges are automatically re-enabled when V_{IN} drops below the OVP falling threshold (typically 35.9V). The OVP and FLT bits remain set, and nFAULT is pulled low until the FLT bit is cleared by writing 1 to the OVP bit.

V_{IN} Under-Voltage Lockout (UVLO) Protection

If V_{IN} drops below its under-voltage lockout (UVLO) threshold, then the H-bridge outputs are disabled. The VINUV bit (FAULT, bit[1]) and the FLT bit are set, and nFAULT is pulled low. Once V_{IN} exceeds its UVLO threshold, nFAULT is automatically pulled high via an external pull-up resistor, and the H-bridges are automatically re-enabled. The VINUV bit remains set until the FLT bit is cleared by writing 1 to the VINUV bit.

The VINUV bit may be set at power-up, and nFAULT may be pulled active low momentarily.

Over-Temperature Warning (OTW)

If the die temperature exceeds the thermal warning threshold, then the OTW bit (FAULT, bit[3]) and FLT bit are set, and nFAULT is pulled active low. All device functions remain operational. The OTW and FLT bits remain set, and nFAULT is pulled low until the FLT bit is cleared by writing 1 to the OTW bit.

Over-Temperature Shutdown (OTS)

If the die temperature exceeds the safe limits (typically 165°C), then all MOSFETs in the H-bridge are disabled. The OTS bit (FAULT, bit[5]) and FLT bit are set, and nFAULT is pulled low. This protection is released, and the H-bridges are automatically re-enabled once the temperature drops below the over-temperature shutdown falling threshold (typically 145°C). The OTS bit remains set, and nFAULT is pulled low until the FLT bit is cleared by writing 1 to the OTS bit.

Low Temperature Detection

If the die temperature drops below the low temperature threshold (40°C), then only the LTD bit (FAULT, bit[4]) is set. All device functions remain operational, and nFAULT is not pulled low. The die temperature is sampled and digitized during this period (see Table 9 on page 17). The LTD bit is automatically cleared once the die temperature exceeds 40°C. Table 9 on page 17 shows the low temperature indication settings via the LT3, LT2, LT1, and LT1 bits (CTRL2, bits[10:7]).

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Table 9: Low-Temperature Indication

LT3~LT0	Temperature Range
0x00	-40°C to -35°C
0x01	-35°C to -30°C
0x02	-30°C to -25°C
0x03	-25°C to -20°C
0x04	-20°C to -15°C
0x05	-15°C to -10°C
0x06	-10°C to -5°C
0x07	-5°C to 0°C
0x08	0°C to 5°C
0x09	5°C to 10°C
0x0A	10°C to 15°C
0x0B	15°C to 20°C
0x0C	20°C to 25°C
0x0D	25°C to 30°C
0x0E	30°C to 35°C
0x0F	35°C to 40°C

Open-Load Detection

If open-load detection is enabled, the MPQ6609 can detect an open load condition on the outputs. Open load is only sensed when the output current (I_{OUT}) flows from xOUT2 to xOUT1 (where x = A or B).

If the winding current does not reach the configured current trip threshold (I_{TRIP}) within open load detection timeout, then the xOUT1 output is turned off to allow the current to recirculate.

If an inductive load is present, the winding current freewheels and passes through the high-side body diodes, causing the xOUT1 pin to be pulled slightly above V_{IN}. If there is no load connected, the output floats, similar to when the motor winding is open. Once the xOUT1 pin voltage is near 0V (between -0.3V and +1.5V), an open load error is detected.

If an open load is detected, the OLA bit (FAULT, bit[9]) or OLB bit (FAULT, bit[10]) and the FLT bit are set, and nFAULT is pulled active low. All device functions remain operational. The OLA, OLB, and FLT bits remain set, and nFAULT is pulled low until the fault is cleared by writing 1 to the set OLA or OLB bit. Open-load detection can be disabled by setting the OLDIS bit (CTRL2, bit[6]) to 1.

Stall Detection

Stall detection in the MPQ6609 works by sensing the back electromotive force (BEMF) of each phase when there is zero current being driven through the winding. The differential voltage between the xOUT1 and xOUT2 pins is sampled just before current is once again driven though the winding.

The BEMF voltage indicates the motor's BEMF, which is a function of the motor speed and the applied torque. When the motor is stalled, there is no BEMF, meaning the sampled voltage is near 0V.

Since stall detection relies on measuring the BEMF at a zero-current step, it does not work in full-step mode. This function also does not work at very slow step rates, as there is not enough BEMF to reliably detect a stall.

The BEMF voltage is sampled and digitized. If the BEMFSEL bit (BEMFA, bit[11]) is set to 1, then the real-time value from the analog-to-digital converter (ADC) is used for stall detection. If the BEMFSEL bit is set to 0, then an average of the last 16 readings is used. This value is compared to a configurable stall threshold. If the BEMF is below the configured stall threshold for a configurable number of steps, then a stall is reported.

The time point at which the BEMF is sampled can be configured via the BES1 and BES0 bits (CTRL2, bits[5:4]). Table 10 shows the BEMF sample point settings.

Table 10: BEMF Sample Point Settings

BES1~BES0	BEMF Sample Point
00b	100µs after zero current
01b	200µs after zero current
10b	400µs after zero current
11b (reset value)	End of zero current

The BEMF measurement can also be read directly in the BEMF command. This information can be utilized by a processor to implement advanced diagnostic and control features.

The BEMF and STALL commands contain several settings that relate to the stall detect function. To make stall detection work correctly, these commands must be set correctly for the application and motor characteristics.

The BEG2, BEG1, and BEG0 bits (BEMF, bits[10:8]) set the gain or attenuation of the BEMF measurement. The full-scale input level

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applied to the ADC is 3V. The BEG bits are set to allow the ADC to accurately measure the BEMF at the target stall detection point. This BEMF level depends on motor construction and speed, and is always below the supply voltage. Table 11 shows the BEMF gain.

Table 11: BEMF Gain

BEG2~BEG0	BEMF Gain	Full-Scale BEMF
000b	0.125	24V
001b	0.25	12V
010b	0.5	6V
011b (reset value)	1	3V
100b	2	1.5V
101b	5	600mV
110b	10	300mV
111b	20	150mV

The STH7, STH6, STH5, STH4, STH4, STH3, STH2, STH1, and STH0 bits (STALL, bits[11:0]) set the BEMF threshold of a stall. If the BEMF is below the threshold, then the stall counter is incremented; if the BEMF exceeds the threshold, then the counter is cleared. The BEMF threshold is a percentage of the maximum BEMF (see Table 12).

Table 12: BEMF Threshold Settings

STH7~STH0	% Max BEMF Voltage
0x00	No stall detected
0x01	0.4%
0x02	0.8%
•	•
•	•
0x7F	49.8%
0x80 (reset value)	50.2%
0x81	50.6%
•	•
•	•
0xFE	99.6%
0xFF	100%

The STD3, STD2, STD1, and STD0 bits (STALL, bits[3:0]) set the count that the stall counter must reach to report a stall condition. Table 13 shows the steps to report a stall.

Table 13: Steps to Report a Stall

STD3~STD0	Steps Required to Report Stall
0x00 (reset value)	Stall detect disabled
0x01	1
0x02	2
•	•
•	•
0x0D	13
0x0E	14
0x0F	15

If the stall counter reaches the count set in the STD3~STD0 bits, then a stall condition is reported. The STALL bit (FAULT, bit[8]) and FLT bit are set, and nFAULT is pulled active low. All device functions remain operational.

The STALL and FLT bits remain set, and nFAULT is pulled low until the fault is cleared by writing 1 to the STALL bit.

Figure 6 on page 19 shows the stall detection circuitry diagram. Table 14 on page 20 shows the diagnostic and fault summary.

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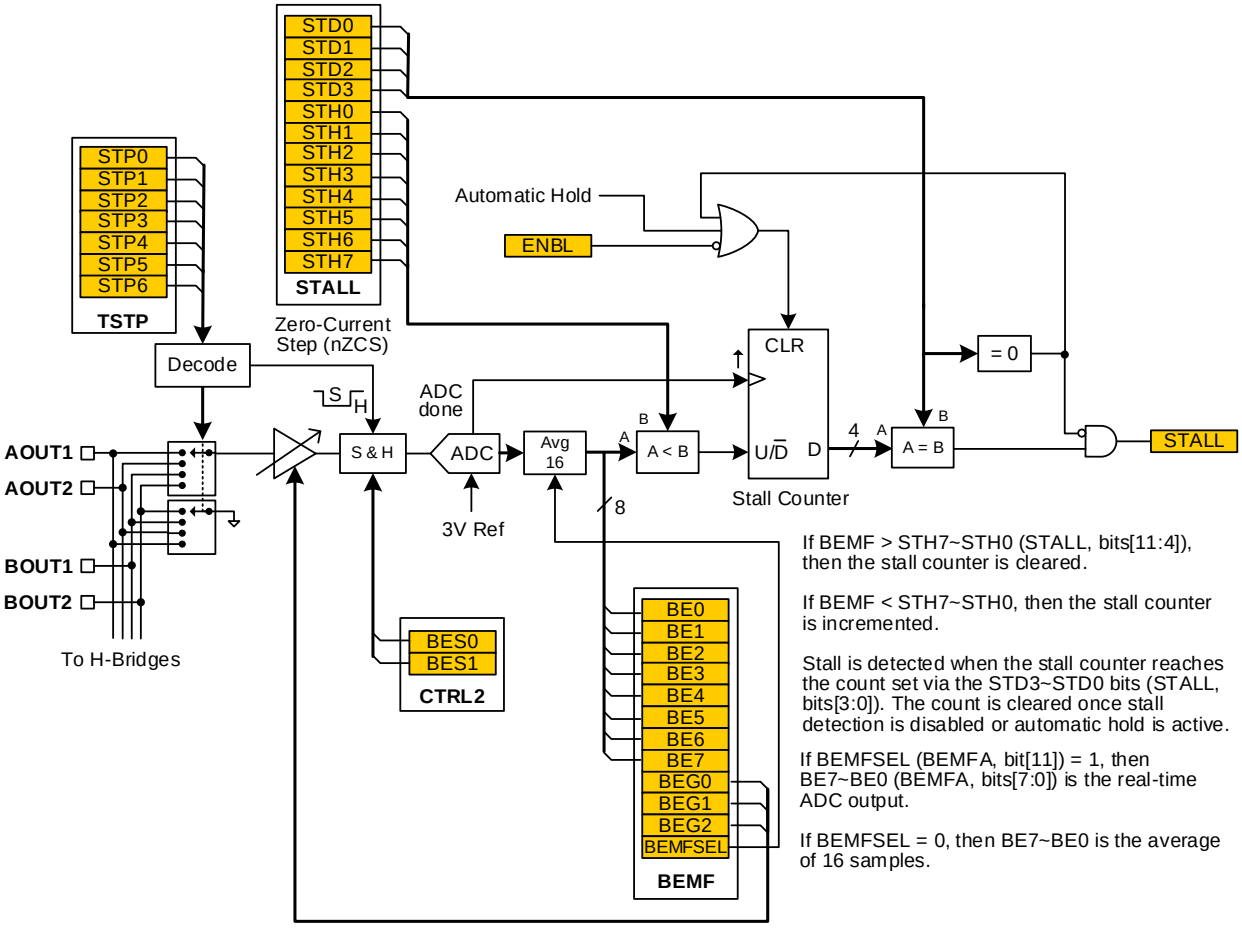

Figure 6: Stall Detection Circuitry Diagram

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Table 14: Diagnostic and Fault Summary

Fault	Device Action	Bits Set	Fault Clearing Action	nFAULT Active
Over-current protection (OCP)	Outputs are latched off, stepping disabled, and nFAULT is pulled low	OCA (FAULT, bit[6]) or OCB (FAULT, bit[7]), and FLT (FAULT, bit[0])	Write 1 to OCA or OCB	Until OCA and OCB cleared
V_{IN} over-voltage protection (OVP)	Outputs and stepping disabled until V_{IN} is below OVP threshold, and nFAULT is pulled low	OVP (FAULT, bit[2]) and FLT	Write 1 to OVP	Until OVP is cleared
V_{IN} under-voltage lockout (UVLO)	Outputs and stepping disabled, and nFAULT is pulled low until V_{IN} exceeds its UVLO threshold	VINUV (FAULT, bit[1]) and FLT	Write 1 to VINUV	Until V_{IN} exceeds its UVLO threshold
Over-temperature warning (OTW)	nFAULT is pulled low	OTW (FAULT, bit[3]) and FLT	Write 1 to OTW	Until OTW is cleared
Over-temperature shutdown (OTS)	Outputs and stepping disabled until the temperature is below T_{OTS}, and nFAULT is pulled low	OTS (FAULT, bit[5]) and FLT	Write 1 to OTS	Until OTS is cleared
Low temperature	None	LTD (FAULT, bit[4])	Until the temperature exceeds 40°C	Always inactive
Open load	nFAULT is pulled low	OLA (FAULT, bit[9]) or OLB (FAULT, bit[10]), and FLT	Write 1 to OLA or OLB	Until OLA and OLB are cleared
Stall	nFAULT is pulled low	STALL (FAULT, bit[8]) and FLT	Write 1 to STALL	Until STALL is cleared

Serial Peripheral Interface (SPI) Control

The SPI uses a standard 16-bit serial data packet, composed of 3 address bits, one read/write (R/W) bit (where 1 is write, and 0 is read), and 12 data bits. Serial data is clocked into the SDATI pin by the rising edges on the SCLK pin, while the nSCS pin is held active low.

The first 3 bits sent are the address bits, which address one of eight registers inside the MPQ6609. These bits select the source of data to be shifted out the SDATO pin, as well as the destination of the new data being shifted in.

The 4th bit is a R/W bit. If this bit is cleared, the data sent is ignored, and register data is read out on the SDATO pin. If this bit is set, the next 12 bits sent are latched into the selected register at the end of the transfer.

The addressed register is updated on the 16th rising edge of the SCLK.

Figure 7 on page 21 shows the SPI diagram. Figure 8 on page 21 shows the SPI timing diagram for SPI data transfers.

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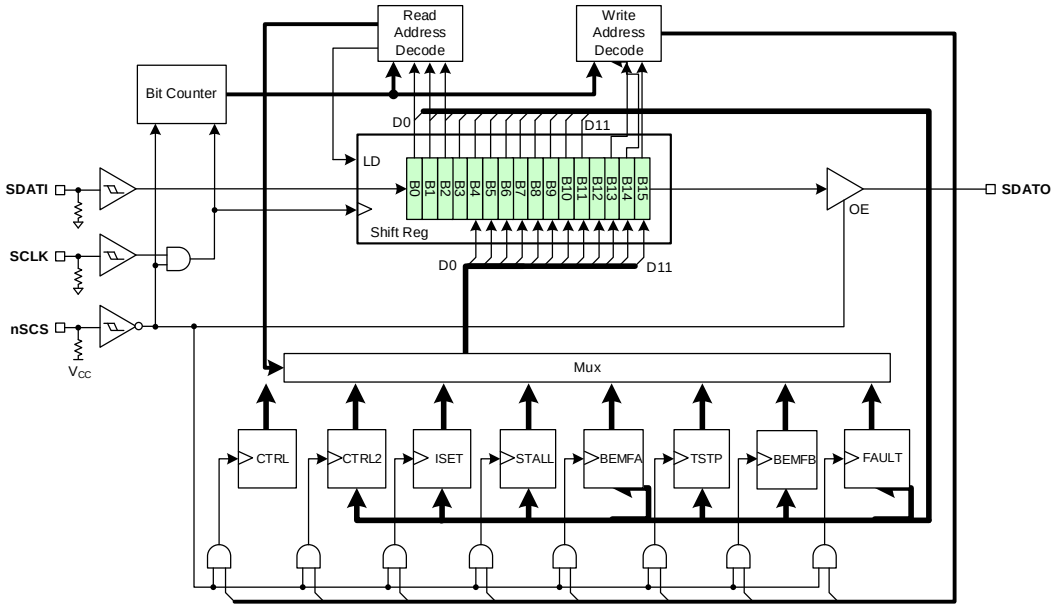

Figure 7: SPI Diagram

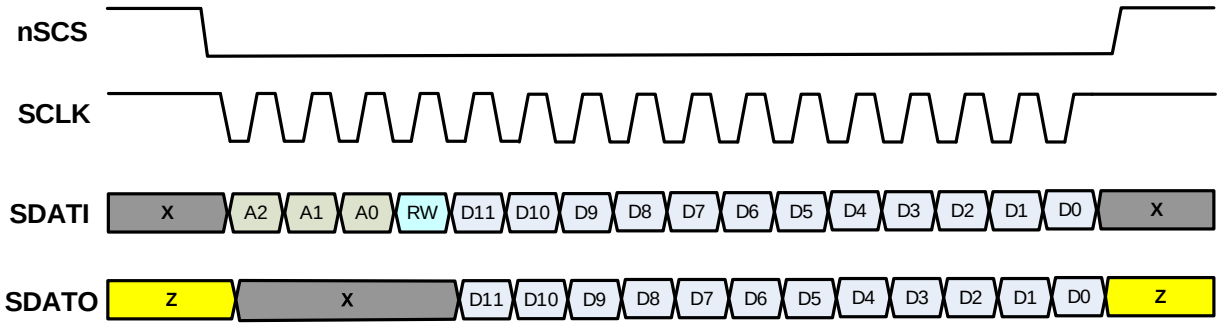

Figure 8: SPI Timing Diagram

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REGISTER MAP

CTRL

Address: 0x00 read, 0x01 write

The CTRL command sets the automatic hold time, fixed off time (t_{OFF}), step mode, step direction, enables the motor driver outputs, and the indexer increases by one step.

Bits	Access	Bit Name	Default	Description
11	R/W	AH2	0b	Sets the automatic hold time.
10	R/W	AH1	0b	
9	R/W	AH0	0b	
8	R/W	OT2	0b	Sets the fixed t_{OFF}.
7	R/W	OT1	1b	
6	R/W	OT0	0b	
5	R/W	MS2	0b	Sets the step mode.
4	R/W	MS1	1b	
3	R/W	MS0	1b	
2	R/W	DIR	0b	This bit works in conjunction with the DIR input pin to set the step direction.
1	R/W	STEP	0b	If this bit is written to 1, the indexer increases by one step. This bit is automatically reset to 0.
0	R/W	EN	0b	This bit works in conjunction with the ENBL input pin, and enables the motor drive outputs.

CTRL2

Address: 0x02 read, 0x03 write

The CTRL2 command sets the back electromotive force (BEMF) sample point time, blanking time (t_{BLANK}), enables the open load detection, and indicates the die temperature.

Bits	Access	Bit Name	Default	Description
11	R	RESERVED	0b	Reserved.
10	R	LT3	-	The measured value of the die temperature when it is below 40°C.
9	R	LT2	-	
8	R	LT1	-	
7	R	LT0	-	
6	R/W	OLDIS	0b	If this bit is written to 1, then open-load detection is disabled.
5	R/W	BES1	1b	Sets the BEMF sample point time.
4	R/W	BES0	1b	
3	R	RESERVED	0b	Reserved.
2	R/W	BT2	1b	Sets the blanking time.
1	R/W	BT1	0b	
0	R/W	BT0	0b	

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ISET

Address: 0x04 read, 0x05 write

The ISET command sets the peak current level in normal operation and automatic hold mode.

Bits	Access	Bit Name	Default	Description
11	R/W	IL5	0b	Sets the peak (100%) current level in automatic hold mode.
10	R/W	IL4	0b	
9	R/W	IL3	1b	
8	R/W	IL2	0b	
7	R/W	IL1	0b	
6	R/W	IL0	0b	
5	R/W	IS5	0b	Sets the peak (100%) current level in normal operation.
4	R/W	IS4	0b	
3	R/W	IS3	1b	
2	R/W	IS2	0b	
1	R/W	IS1	0b	
0	R/W	IS0	0b	

STALL

Address: 0x06 read, 0x07 write

The STALL command sets the stall detection BEMF threshold, and the number of cycles required to detect a stall.

Bits	Access	Bit Name	Default	Description
11	R/W	STH7	1b	Sets the stall detection BEMF threshold.
10	R/W	STH6	0b	
9	R/W	STH5	0b	
8	R/W	STH4	0b	
7	R/W	STH3	0b	
6	R/W	STH2	0b	
5	R/W	STH1	0b	
4	R/W	STH0	0b	
3	R/W	STD3	0b	Sets the number of cycles required to detect a stall. If this bit is written to 0, then stall detection is disabled.
2	R/W	STD2	0b	
1	R/W	STD1	0b	
0	R/W	STD0	0b	

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BEMFA

Address: 0x08 read, 0x09 write

The BEMFA command sets the BEMF measurement gain, real-time sample or average of 16 samples, and indicates the phase A BEMF at the zero-current step.

Bits	Access	Bit Name	Default	Description
11	R/W	BEMFSEL	0b	If this bit is written to 1, then the BE7~BE0 bits (BEMFA/B, bits[7:0]) are the real-time BEMF data; if this bit is written to 0, then the BE7~BE0 bits are the average of 16 samples.
10	R/W	BEG2	0b	Sets the BEMF measurement gain.
9	R/W	BEG1	1b	
8	R/W	BEG0	1b	
7	R	BE7	-	The measured value of the BEMFA at the last zero-current step.
6	R	BE6	-	
5	R	BE5	-	
4	R	BE4	-	
3	R	BE3	-	
2	R	BE2	-	
1	R	BE1	-	
0	R	BE0	-	

TSTP

Address: 0x0A read, 0x0B write

The TSTP command sets the charge pump frequency, slew rate, and indicates the indexer's current position.

Bits	Access	Bit Name	Default	Description
11	R	RESERVED	0b	Reserved.
10	R/W	CPF1	0b	Sets the charge pump frequency.
9	R/W	CPF0	1b	
8	R/W	SR1	0b	Sets the slew rate of the rising and falling output.
7	R/W	SR0	0b	
6	R/W	STP6	0b	The current position in the indexer's step table.
5	R/W	STP5	0b	
4	R/W	STP4	1b	
3	R/W	STP3	0b	
2	R/W	STP2	0b	
1	R/W	STP1	0b	
0	R/W	STP0	0b	

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BEMFB

Address: = 0x0C read, 0x0D write

The BEMFB command indicates the phase B BEMF at the zero-current step.

Bits	Access	Bit Name	Default	Description
11	R	RESERVED	0b	Reserved.
10	R	RESERVED	0b	
9	R	RESERVED	0b	
8	R	RESERVED	0b	
7	R	BE7	-	The measured value of the BEMFB at the last zero-current step.
6	R	BE6	-	
5	R	BE5	-	
4	R	BE4	-	
3	R	BE3	-	
2	R	BE2	-	
1	R	BE1	-	
0	R	BE0	-	

FAULT

Address: = 0x0E read, 0x0F write

The FAULT command sets open-load detection timeout, and reports warning and fault conditions. Write 1 to clear any bits in the FAULT command. Writing 0 to any of the bits in this command has no effect.

Bits	Access	Bit Name	Default	Description
11	R/W	OLDT	0b	If this bit is written to 1, then the open load detection timeout is 256µs; if this bit is written to 0, then the detection timeout is 1ms.
10	R/W	OLB	0b	This bit is set if an open load is detected on bridge B.
9	R/W	OLA	0b	This bit is set if an open load is detected on bridge A.
8	R/W	STALL	0b	This bit is set if a rotor stall is detected.
7	R/W	OCB	0b	This bit is set if over-current protection (OCP) is detected on bridge B.
6	R/W	OCA	0b	This bit is set if OCP is detected on bridge A.
5	R/W	OTS	0b	This bit is set if over-temperature shutdown (OTS) occurs.
4	R/W	LTD	0b	This bit is set if the die temperature is below 40°C.
3	R/W	OTW	0b	This bit is set if the die temperature exceeds the over-temperature warning (OTW) threshold.
2	R/W	OVP	0b	This bit is set if over-voltage protection (OVP) is detected.
1	R/W	VINUV	0b	This bit is set if the input voltage (V_{IN}) drops below the under-voltage lockout (UVLO) threshold. Depends on the power-up sequence, where this bit can be set at power-up.
0	R	FLT	-	Logical OR of the bits in the FAULT command except for the OLDT bit (FAULT, bit[11]) and LTD bit (FAULT, bit[4]). This bit also reflects the nFAULT pin state, and is read only.

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APPLICATION INFORMATION

Selecting External Components

The MPQ6609 only requires VIN capacitors since it integrates charge pump capacitors and VG capacitors internally.

The bypass capacitors must be placed as close as possible to the VIN pin. At minimum, it is recommended to use a 100nF ceramic capacitor (X5R or X7R) rated for the input voltage (V_{IN}).

Depending on the distance between the power supply and the device, an additional 100µF, bulk electrolytic capacitor is typically required.

PCB Layout Guidelines

The MPQ6609 relies on thermal conduction to dissipate power. A multi-layer PCB with a solid ground plane provides the most optimal power dissipation and lowest operating temperature.

On a well-designed 2-layer PCB, the temperature rise is only 31° above the ambient temperature (T_A). Figure 9 shows the thermal results at 1A, 12V, 1/8-step operation with the fastest slew rate.

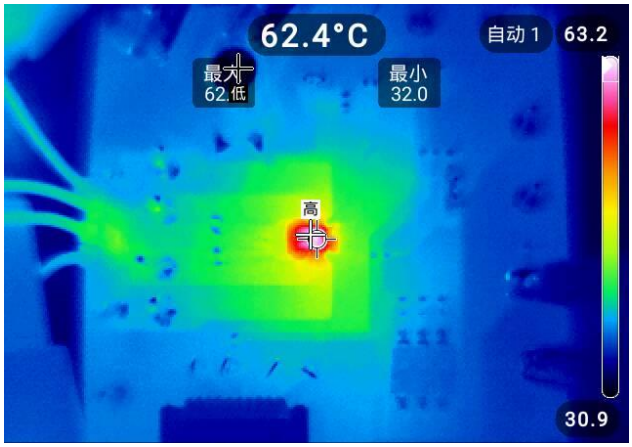


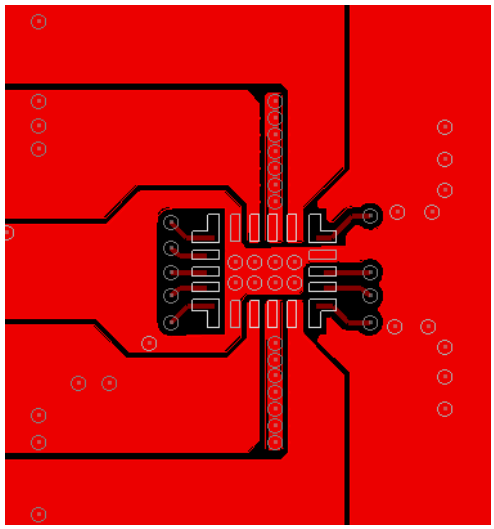
Figure 9: Thermal Results

The top layer is vital because it removes heat from the device. Many vias are used (especially on ground) to move heat from the top layer to the bottom layer plane.

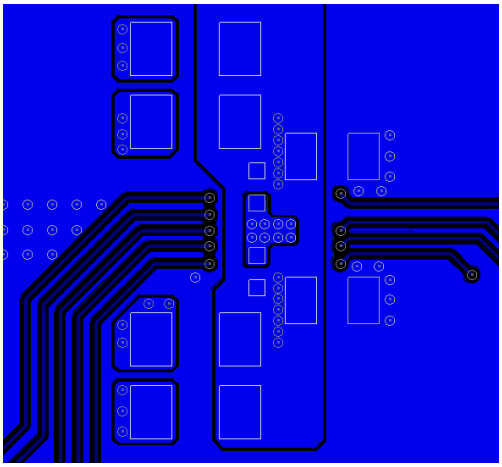
Figure 10 uses a solid ground plane to route the power and signals. The bottom layer is mostly ground, while the VIN bypass capacitors are mounted on the PCB's backside.

For the best thermal results, refer to Figure 10 and follow the guidelines below:

1. To remove heat from the device, add additional copper areas on the top and bottom layers connected to the power pins.
2. Place the VIN bypass capacitors on the PCB's backside.
3. Use multiple vias to connect the VIN and PGND pins.
4. Connect PGND and AGND together on the same layer.



Top Layer



Bottom Layer

Figure 10: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

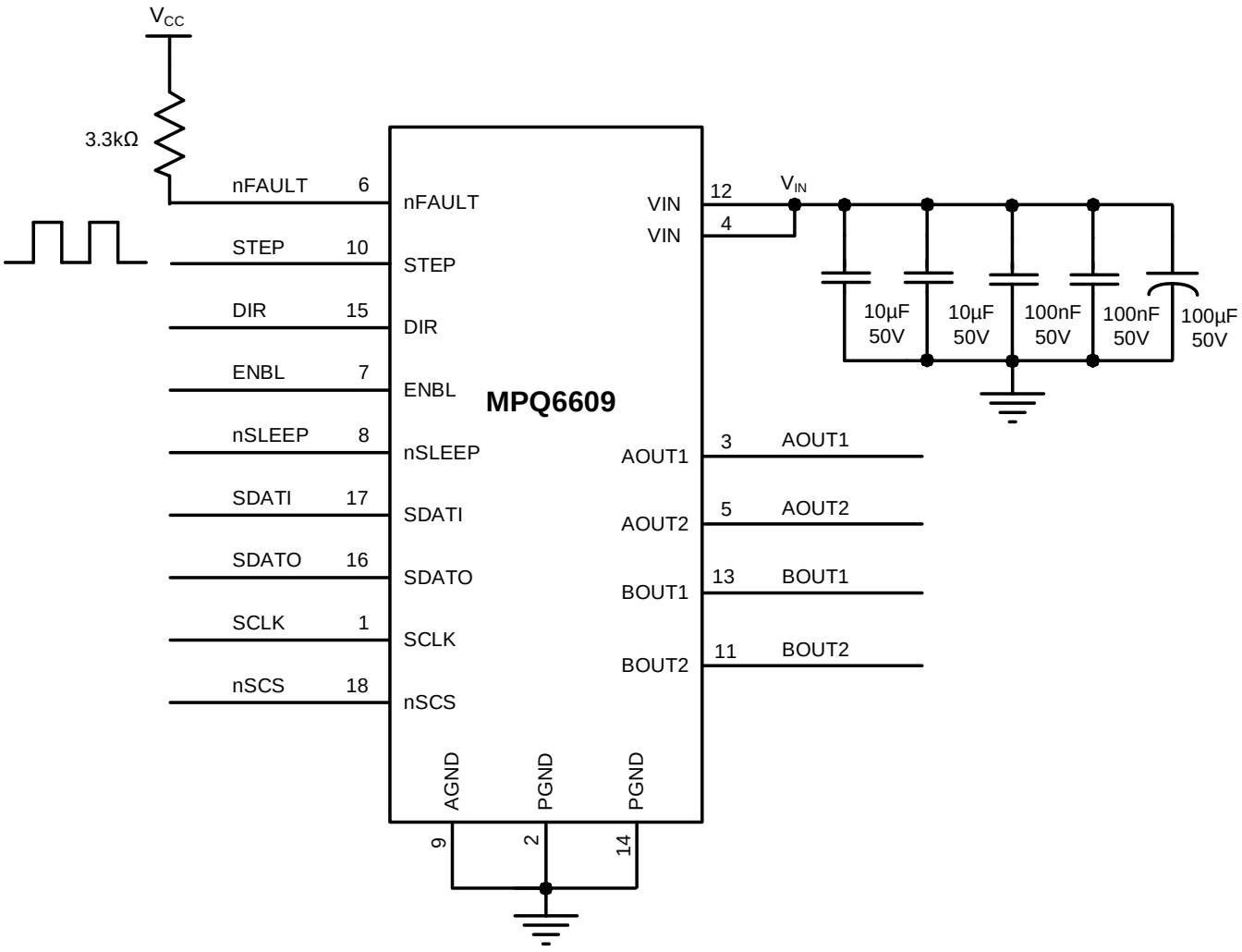

Figure 11: Typical Application Circuit

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APPENDIX 1: MICROSTEPPING

Table 15: Relative Current Level Sequence (DIR = 1) (7)

1/32 Step #	1/16 Step #	1/8 Step #	1/4 Step #	Half Step #	Full Step #	Phase A Current $\%I_{PEAK}$ (%)	Phase B Current $\%I_{PEAK}$ (%)	Step Angle (°)	TSTP Command Value
1	1	1	1	1		100.00	0.00	0.0	0x00
2	-	-	-	-	-	99.88	4.91	2.8	0x01
3	2	-	-	-	-	99.52	9.80	5.6	0x02
4	-	-	-	-	-	98.92	14.67	8.4	0x03
5	3	2	-	-	-	98.08	19.51	11.3	0x04
6	-	-	-	-	-	97.00	24.30	14.1	0x05
7	4	-	-	-	-	95.69	29.03	16.9	0x06
8	-	-	-	-	-	94.15	33.69	19.7	0x07
9	5	3	2	-	-	92.39	38.27	22.5	0x08
10	-	-	-	-	-	90.40	42.76	25.3	0x09
11	6	-	-	-	-	88.19	47.14	28.1	0x0A
12	-	-	-	-	-	85.77	51.41	30.9	0x0B
13	7	4	-	-	-	83.15	55.56	33.8	0x0C
14	-	-	-	-	-	80.32	59.57	36.6	0x0D
15	8	-	-	-	-	77.30	63.44	39.4	0x0E
16	-	-	-	-	-	74.10	67.16	42.2	0x0F
17	9	5	3	2	1	70.71	70.71	45.0	0x10 (reset position)
18	-	-	-	-	-	67.16	74.10	47.8	0x11
19	10	-	-	-	-	63.44	77.30	50.6	0x12
20	-	-	-	-	-	59.57	80.32	53.4	0x13
21	11	6	-	-	-	55.56	83.15	56.3	0x14
22	-	-	-	-	-	51.41	85.77	59.1	0x15
23	12	-	-	-	-	47.14	88.19	61.9	0x16
24	-	-	-	-	-	42.76	90.40	64.7	0x17
25	13	7	4	-	-	38.27	92.39	67.5	0x18
26	-	-	-	-	-	33.69	94.15	70.3	0x19
27	14	-	-	-	-	29.03	95.69	73.1	0x1A
28	-	-	-	-	-	24.30	97.00	75.9	0x1B
29	15	8	-	-	-	19.51	98.08	78.8	0x1C
30	-	-	-	-	-	14.67	98.92	81.6	0x1D
31	16	-	-	-	-	9.80	99.52	84.4	0x1E
32	-	-	-	-	-	4.91	99.88	87.2	0x1F
33	17	9	5	3	-	0.00	100.00	90.0	0x20
34	-	-	-	-	-	-4.91	99.88	92.8	0x21
35	18	-	-	-	-	-9.80	99.52	95.6	0x22
36	-	-	-	-	-	-14.67	98.92	98.4	0x23
37	19	10	-	-	-	-19.51	98.08	101.3	0x24
38	-	-	-	-	-	-24.30	97.00	104.1	0x25
39	20	-	-	-	-	-29.03	95.69	106.9	0x26
40	-	-	-	-	-	-33.69	94.15	109.7	0x27
41	21	11	6	-	-	-38.27	92.39	112.5	0x28
42	-	-	-	-	-	-42.76	90.40	115.3	0x29
43	22	-	-	-	-	-47.14	88.19	118.1	0x2A
44	-	-	-	-	-	-51.41	85.77	120.9	0x2B
45	23	12	-	-	-	-55.56	83.15	123.8	0x2C
46	-	-	-	-	-	-59.57	80.32	126.6	0x2D
47	24	-	-	-	-	-63.44	77.30	129.4	0x2E
48	-	-	-	-	-	-67.16	74.10	132.2	0x2F
49	25	13	7	4	2	-70.71	70.71	135.0	0x30
50	-	-	-	-	-	-74.10	67.16	137.8	0x31
51	26	-	-	-	-	-77.30	63.44	140.6	0x32

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1/32 Step #	1/16 Step #	1/8 Step #	1/4 Step #	Half Step #	Full Step #	Phase A Current %I_{PEAK} (%)	Phase B Current %I_{PEAK} (%)	Step Angle (°)	TSTP Command Value
52	-	-	-	-	-	-80.32	59.57	143.4	0x33
53	27	14	-	-	-	-83.15	55.56	146.3	0x34
54	-	-	-	-	-	-85.77	51.41	149.1	0x35
55	28	-	-	-	-	-88.19	47.14	151.9	0x36
56	-	-	-	-	-	-90.40	42.76	154.7	0x37
57	29	15	8	-	-	-92.39	38.27	157.5	0x38
58	-	-	-	-	-	-94.15	33.69	160.3	0x39
59	30	-	-	-	-	-95.69	29.03	163.1	0x3A
60	-	-	-	-	-	-97.00	24.30	165.9	0x3B
61	31	16	-	-	-	-98.08	19.51	168.8	0x3C
62	-	-	-	-	-	-98.92	14.67	171.6	0x3D
63	32	-	-	-	-	-99.52	9.80	174.4	0x3E
64	-	-	-	-	-	-99.88	4.91	177.2	0x3F
65	33	17	9	5	-	-100.00	0.00	180.0	0x40
66	-	-	-	-	-	-99.88	-4.91	182.8	0x41
67	34	-	-	-	-	-99.52	-9.80	185.6	0x42
68	-	-	-	-	-	-98.92	-14.67	188.4	0x43
69	35	18	-	-	-	-98.08	-19.51	191.3	0x44
70	-	-	-	-	-	-97.00	-24.30	194.1	0x45
71	36		-	-	-	-95.69	-29.03	196.9	0x46
72			-	-	-	-94.15	-33.69	199.7	0x47
73	37	19	10	-	-	-92.39	-38.27	202.5	0x48
74	-	-	-	-	-	-90.40	-42.76	205.3	0x49
75	38	-	-	-	-	-88.19	-47.14	208.1	0x4A
76	-	-	-	-	-	-85.77	-51.41	210.9	0x4B
77	39	20	-	-	-	-83.15	-55.56	213.8	0x4C
78	-	-	-	-	-	-80.32	-59.57	216.6	0x4D
79	40	-	-	-	-	-77.30	-63.44	219.4	0x4E
80	-	-	-	-	-	-74.10	-67.16	222.2	0x4F
81	41	21	11	6	3	-70.71	-70.71	225.0	0x50
82	-	-	-	-	-	-67.16	-74.10	227.8	0x51
83	42	-	-	-	-	-63.44	-77.30	230.6	0x52
84	-	-	-	-	-	-59.57	-80.32	233.4	0x53
85	43	22	-	-	-	-55.56	-83.15	236.3	0x54
86	-	-	-	-	-	-51.41	-85.77	239.1	0x55
87	44	-	-	-	-	-47.14	-88.19	241.9	0x56
88	-	-	-	-	-	-42.76	-90.40	244.7	0x57
89	45	23	12	-	-	-38.27	-92.39	247.5	0x58
90	-	-	-	-	-	-33.69	-94.15	250.3	0x59
91	46	-	-	-	-	-29.03	-95.69	253.1	0x5A
92	-	-	-	-	-	-24.30	-97.00	255.9	0x5B
93	47	24	-	-	-	-19.51	-98.08	258.8	0x5C
94	-	-	-	-	-	-14.67	-98.92	261.6	0x5D
95	48	-	-	-	-	-9.80	-99.52	264.4	0x5E
96	-	-	-	-	-	-4.91	-99.88	267.2	0x5F
97	49	25	13	7	-	0.00	-100.00	270.0	0x60
98	-	-	-	-	-	4.91	-99.88	272.8	0x61
99	50	-	-	-	-	9.80	-99.52	275.6	0x62
100	-	-	-	-	-	14.67	-98.92	278.4	0x63
101	51	26	-	-	-	19.51	-98.08	281.3	0x64
102	-	-	-	-	-	24.30	-97.00	284.1	0x65
103	52	-	-	-	-	29.03	-95.69	286.9	0x66
104	-	-	-	-	-	33.69	-94.15	289.7	0x67
105	53	27	14	-	-	38.27	-92.39	292.5	0x68
106	-	-	-	-	-	42.76	-90.40	295.3	0x69
107	54	-	-	-	-	47.14	-88.19	298.1	0x6A
108	-	-	-	-	-	51.41	-85.77	300.9	0x6B
109	55	28	-	-	-	55.56	-83.15	303.8	0x6C

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1/32 Step #	1/16 Step #	1/8 Step #	1/4 Step #	Half Step #	Full Step #	Phase A Current $\%I_{PEAK}$ (%)	Phase B Current $\%I_{PEAK}$ (%)	Step Angle (°)	TSTP Command Value
110	-	-	-	-	-	59.57	-80.32	306.6	0x6D
111	56	-	-	-	-	63.44	-77.30	309.4	0x6E
112	-	-	-	-	-	67.16	-74.10	312.2	0x6F
113	57	29	15	8	4	70.71	-70.71	315.0	0x70
114	-	-	-	-	-	74.10	-67.16	317.8	0x71
115	58	-	-	-	-	77.30	-63.44	320.6	0x72
116	-	-	-	-	-	80.32	-59.57	323.4	0x73
117	59	30	-	-	-	83.15	-55.56	326.3	0x74
118	-	-	-	-	-	85.77	-51.41	329.1	0x75
119	60	-	-	-	-	88.19	-47.14	331.9	0x76
120	-	-	-	-	-	90.40	-42.76	334.7	0x77
121	61	31	16	-	-	92.39	-38.27	337.5	0x78
122	-	-	-	-	-	94.15	-33.69	340.3	0x79
123	62	-	-	-	-	95.69	-29.03	343.1	0x7A
124	-	-	-	-	-	97.00	-24.30	345.9	0x7B
125	63	32	-	-	-	98.08	-19.51	348.8	0x7C
126	-	-	-	-	-	98.92	-14.67	351.6	0x7D
127	64	-	-	-	-	99.52	-9.80	354.4	0x7E
128	-	-	-	-	-	99.88	-4.91	357.2	0x7F

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APPENDIX 1: MICROSTEPPING *(continued)*

Table 16: Relative Current Level Sequence (DIR = 0) (7)

1/32 Step #	1/16 Step #	1/8 Step #	1/4 Step #	Half Step #	Full Step #	Phase A Current $\%I_{PEAK}$ (%)	Phase B Current $\%I_{PEAK}$ (%)	Step Angle (°)	TSTP Command Value
1	1	1	1	1	-	100.00	0.00	0.0	0x00
2	-	-	-	-	-	99.88	-4.91	357.2	0x7F
3	2	-	-	-	-	99.52	-9.80	354.4	0x7E
4	-	-	-	-	-	98.92	-14.67	351.6	0x7D
5	3	2	-	-	-	98.08	-19.51	348.8	0x7C
6	-	-	-	-	-	97.00	-24.30	345.9	0x7B
7	4	-	-	-	-	95.69	-29.03	343.1	0x7A
8	-	-	-	-	-	94.15	-33.69	340.3	0x79
9	5	3	2	-	-	92.39	-38.27	337.5	0x78
10	-	-	-	-	-	90.40	-42.76	334.7	0x77
11	6	-	-	-	-	88.19	-47.14	331.9	0x76
12	-	-	-	-	-	85.77	-51.41	329.1	0x75
13	7	4	-	-	-	83.15	-55.56	326.3	0x74
14	-	-	-	-	-	80.32	-59.57	323.4	0x73
15	8	-	-	-	-	77.30	-63.44	320.6	0x72
16	-	-	-	-	-	74.10	-67.16	317.8	0x71
17	9	5	3	2	1	70.71	-70.71	315.0	0x70
18	-	-	-	-	-	67.16	-74.10	312.2	0x6F
19	10	-	-	-	-	63.44	-77.30	309.4	0x6E
20	-	-	-	-	-	59.57	-80.32	306.6	0x6D
21	11	6	-	-	-	55.56	-83.15	303.8	0x6C
22	-	-	-	-	-	51.41	-85.77	300.9	0x6B
23	12	-	-	-	-	47.14	-88.19	298.1	0x6A
24	-	-	-	-	-	42.76	-90.40	295.3	0x69
25	13	7	4	-	-	38.27	-92.39	292.5	0x68
26	-	-	-	-	-	33.69	-94.15	289.7	0x67
27	14	-	-	-	-	29.03	-95.69	286.9	0x66
28	-	-	-	-	-	24.30	-97.00	284.1	0x65
29	15	8	-	-	-	19.51	-98.08	281.3	0x64
30	-	-	-	-	-	14.67	-98.92	278.4	0x63
31	16		-	-	-	9.80	-99.52	275.6	0x62
32	-	-	-	-	-	4.91	-99.88	272.8	0x61
33	17	9	5	3	-	0.00	-100.00	270.0	0x60
34	-	-	-	-	-	-4.91	-99.88	267.2	0x5F
35	18	-	-	-	-	-9.80	-99.52	264.4	0x5E
36	-	-	-	-	-	-14.67	-98.92	261.6	0x5D
37	19	10	-	-	-	-19.51	-98.08	258.8	0x5C
38	-	-	-	-	-	-24.30	-97.00	255.9	0x5B
39	20	-	-	-	-	-29.03	-95.69	253.1	0x5A
40	-	-	-	-	-	-33.69	-94.15	250.3	0x59
41	21	11	6	-	-	-38.27	-92.39	247.5	0x58
42	-	-	-	-	-	-42.76	-90.40	244.7	0x57
43	22	-	-	-	-	-47.14	-88.19	241.9	0x56
44	-	-	-	-	-	-51.41	-85.77	239.1	0x55
45	23	12	-	-	-	-55.56	-83.15	236.3	0x54
46	-	-	-	-	-	-59.57	-80.32	233.4	0x53
47	24	-	-	-	-	-63.44	-77.30	230.6	0x52
48	-	-	-	-	-	-67.16	-74.10	227.8	0x51
49	25	13	7	4	2	-70.71	-70.71	225.0	0x50
50	-	-	-	-	-	-74.10	-67.16	222.2	0x4F
51	26	-	-	-	-	-77.30	-63.44	219.4	0x4E
52	-	-	-	-	-	-80.32	-59.57	216.6	0x4D
53	27	14	-	-	-	-83.15	-55.56	213.8	0x4C
54	-	-	-	-	-	-85.77	-51.41	210.9	0x4B
55	28	-	-	-	-	-88.19	-47.14	208.1	0x4A

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1/32 Step #	1/16 Step #	1/8 Step #	1/4 Step #	Half Step #	Full Step #	Phase A Current %I_{PEAK} (%)	Phase B Current %I_{PEAK} (%)	Step Angle (°)	TSTP Command Value
56	-	-	-	-	-	-90.40	-42.76	205.3	0x49
57	29	15	8	-	-	-92.39	-38.27	202.5	0x48
58	-	-	-	-	-	-94.15	-33.69	199.7	0x47
59	30	-	-	-	-	-95.69	-29.03	196.9	0x46
60	-	-	-	-	-	-97.00	-24.30	194.1	0x45
61	31	16	-	-	-	-98.08	-19.51	191.3	0x44
62	-	-	-	-	-	-98.92	-14.67	188.4	0x43
63	32	-	-	-	-	-99.52	-9.80	185.6	0x42
64	-	-	-	-	-	-99.88	-4.91	182.8	0x41
65	33	17	9	5	-	-100.00	0.00	180.0	0x40
66	-	-	-	-	-	-99.88	4.91	177.2	0x3F
67	34	-	-	-	-	-99.52	9.80	174.4	0x3E
68	-	-	-	-	-	-98.92	14.67	171.6	0x3D
69	35	18	-	-	-	-98.08	19.51	168.8	0x3C
70	-	-	-	-	-	-97.00	24.30	165.9	0x3B
71	36	-	-	-	-	-95.69	29.03	163.1	0x3A
72	-	-	-	-	-	-94.15	33.69	160.3	0x39
73	37	19	10	-	-	-92.39	38.27	157.5	0x38
74	-	-	-	-	-	-90.40	42.76	154.7	0x37
75	38	-	-	-	-	-88.19	47.14	151.9	0x36
76	-	-	-	-	-	-85.77	51.41	149.1	0x35
77	39	20	-	-	-	-83.15	55.56	146.3	0x34
78	-	-	-	-	-	-80.32	59.57	143.4	0x33
79	40	-	-	-	-	-77.30	63.44	140.6	0x32
80	-	-	-	-	-	-74.10	67.16	137.8	0x31
81	41	21	11	6	3	-70.71	70.71	135.0	0x30
82	-	-	-	-	-	-67.16	74.10	132.2	0x2F
83	42	-	-	-	-	-63.44	77.30	129.4	0x2E
84		-	-	-	-	-59.57	80.32	126.6	0x2D
85	43	22	-	-	-	-55.56	83.15	123.8	0x2C
86	-	-	-	-	-	-51.41	85.77	120.9	0x2B
87	44	-	-	-	-	-47.14	88.19	118.1	0x2A
88	-	-	-	-	-	-42.76	90.40	115.3	0x29
89	45	23	12	-	-	-38.27	92.39	112.5	0x28
90	-	-	-	-	-	-33.69	94.15	109.7	0x27
91	46	-	-	-	-	-29.03	95.69	106.9	0x26
92	-	-	-	-	-	-24.30	97.00	104.1	0x25
93	47	24	-	-	-	-19.51	98.08	101.3	0x24
94	-	-	-	-	-	-14.67	98.92	98.4	0x23
95	48	-	-	-	-	-9.80	99.52	95.6	0x22
96	-	-	-	-	-	-4.91	99.88	92.8	0x21
97	49	25	13	7		0.00	100.00	90.0	0x20
98	-	-	-	-	-	4.91	99.88	87.2	0x1F
99	50	-	-	-	-	9.80	99.52	84.4	0x1E
100	-	-	-	-	-	14.67	98.92	81.6	0x1D
101	51	26	-	-	-	19.51	98.08	78.8	0x1C
102	-	-	-	-	-	24.30	97.00	75.9	0x1B
103	52	-	-	-	-	29.03	95.69	73.1	0x1A
104	-	-	-	-	-	33.69	94.15	70.3	0x19
105	53	27	14	-	-	38.27	92.39	67.5	0x18
106	-	-	-	-	-	42.76	90.40	64.7	0x17
107	54	-	-	-	-	47.14	88.19	61.9	0x16
108	-	-	-	-	-	51.41	85.77	59.1	0x15
109	55	28	-	-	-	55.56	83.15	56.3	0x14
110	-	-	-	-	-	59.57	80.32	53.4	0x13
111	56	-	-	-	-	63.44	77.30	50.6	0x12
112	-	-	-	-	-	67.16	74.10	47.8	0x11

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1/32 Step #	1/16 Step #	1/8 Step #	1/4 Step #	Half Step #	Full Step #	Phase A Current $\%I_{PEAK}$ (%)	Phase B Current $\%I_{PEAK}$ (%)	Step Angle (°)	TSTP Command Value
113	57	29	15	8	4	70.71	70.71	45.0	0x10 (reset position)
114	-	-	-	-	-	74.10	67.16	42.2	0x0F
115	58	-	-	-	-	77.30	63.44	39.4	0x0E
116	-	-	-	-	-	80.32	59.57	36.6	0x0D
117	59	30	-	-	-	83.15	55.56	33.8	0x0C
118	-	-	-	-	-	85.77	51.41	30.9	0x0B
119	60	-	-	-	-	88.19	47.14	28.1	0x0A
120	-	-	-	-	-	90.40	42.76	25.3	0x09
121	61	31	16	-	-	92.39	38.27	22.5	0x08
122	-	-	-	-	-	94.15	33.69	19.7	0x07
123	62	-	-	-	-	95.69	29.03	16.9	0x06
124	-	-	-	-	-	97.00	24.30	14.1	0x05
125	63	32	-	-	-	98.08	19.51	11.3	0x04
126	-	-	-	-	-	98.92	14.67	8.4	0x03
127	64	-	-	-	-	99.52	9.80	5.6	0x02
128	-	-	-	-	-	99.88	4.91	2.8	0x01

Note:

7) The reset position is at TSTP = 0x10.

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APPENDIX 2: STEP MODE ILLUSTRATION FOR BIPOLAR MODE (8)

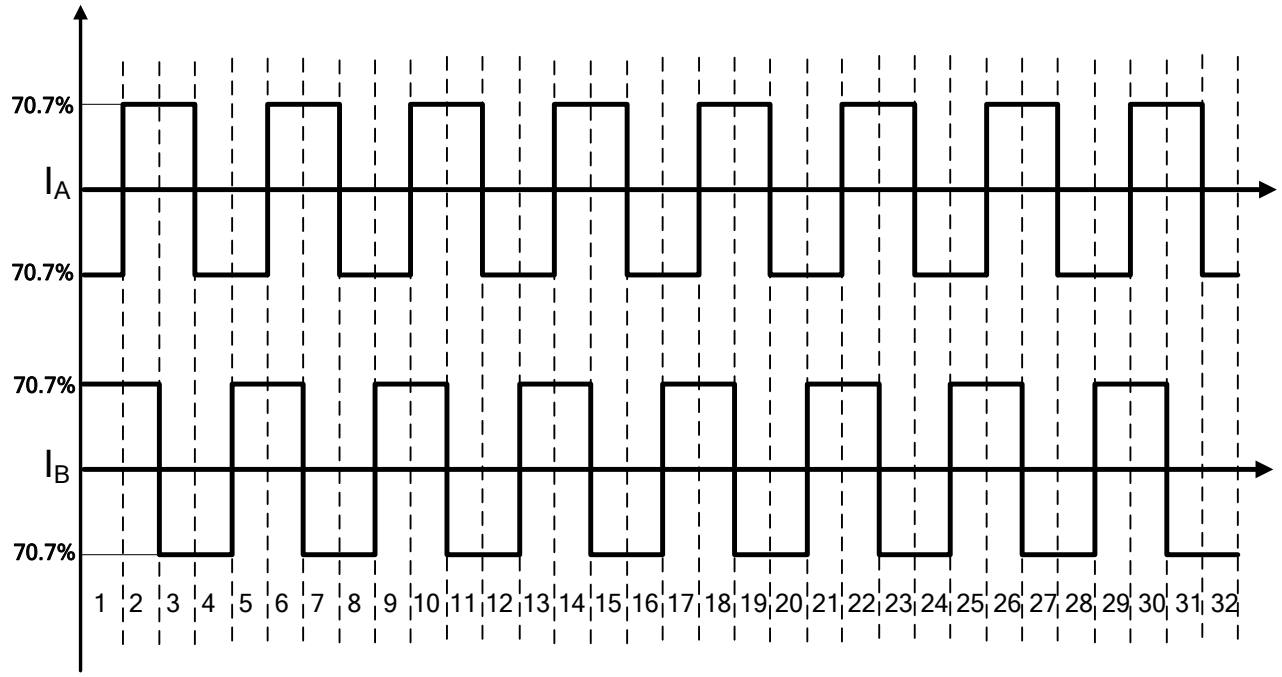

Figure 12: Full Step (4 Step Sequences, DIR = 0)

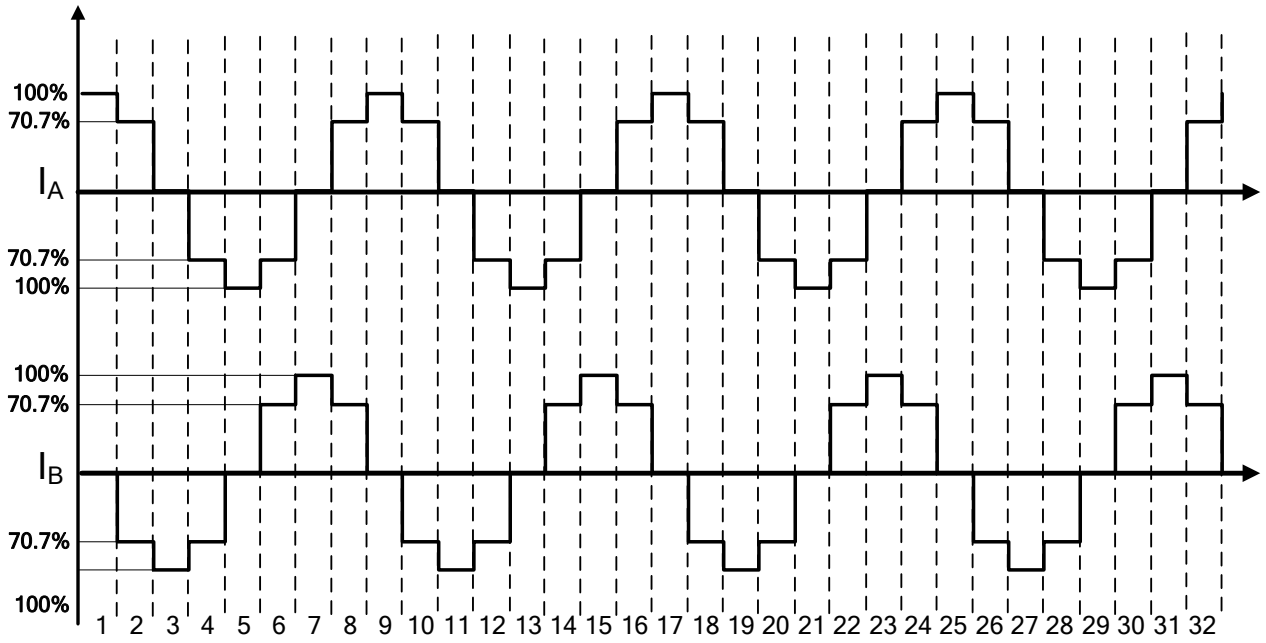

Figure 13: Half Step (8 Step Sequences, DIR = 0)

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APPENDIX 2: STEP MODE ILLUSTRATION FOR BIPOLAR MODE *(continued)*

(8)

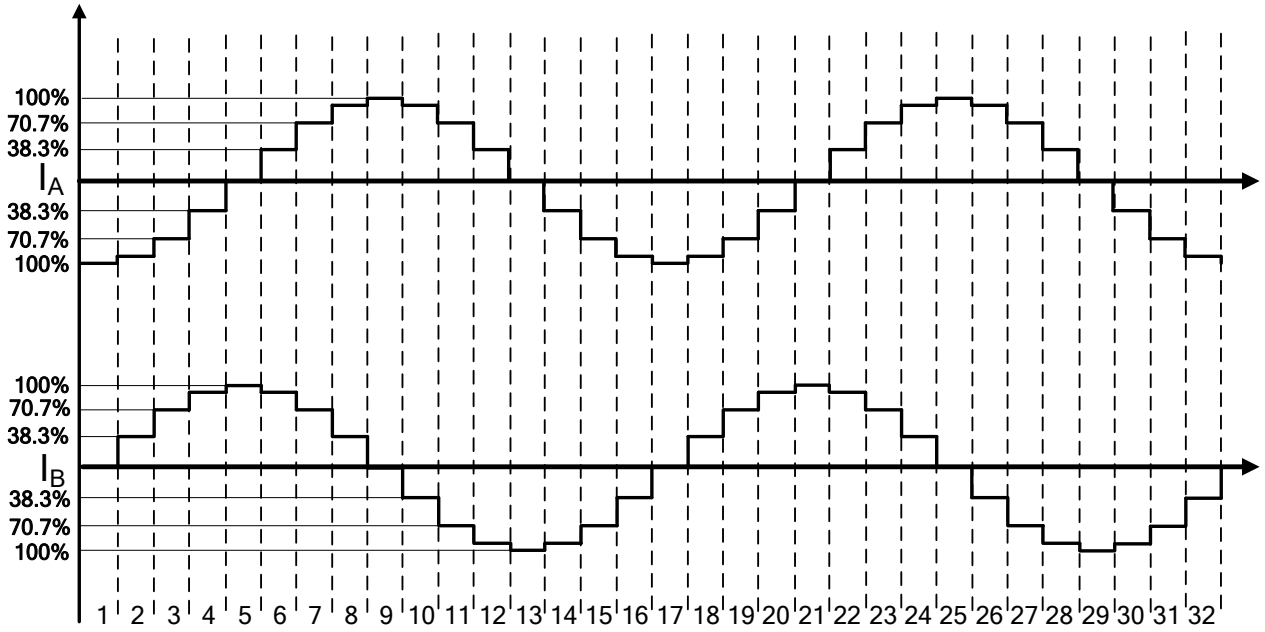

Figure 14: Quarter Step (16 Step Sequences, DIR = 0)

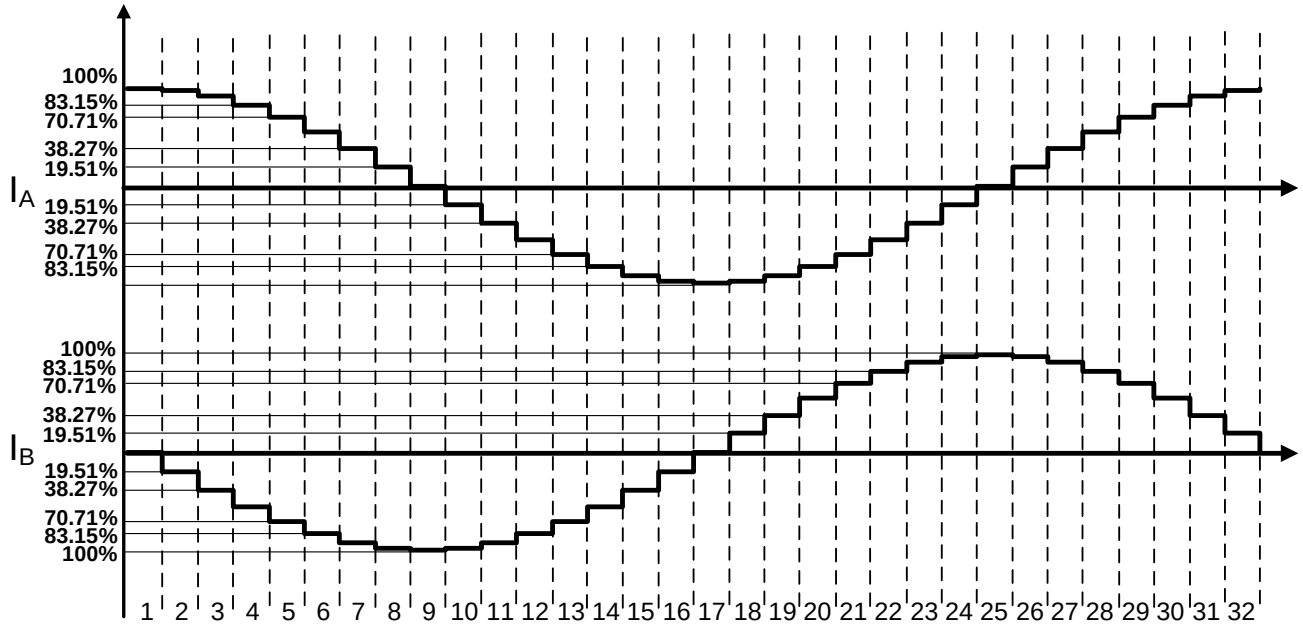

Figure 15: Eighth Step (32 Step Sequences, DIR = 0)

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APPENDIX 2: STEP MODE ILLUSTRATION FOR BIPOLAR MODE *(continued)*

(8)

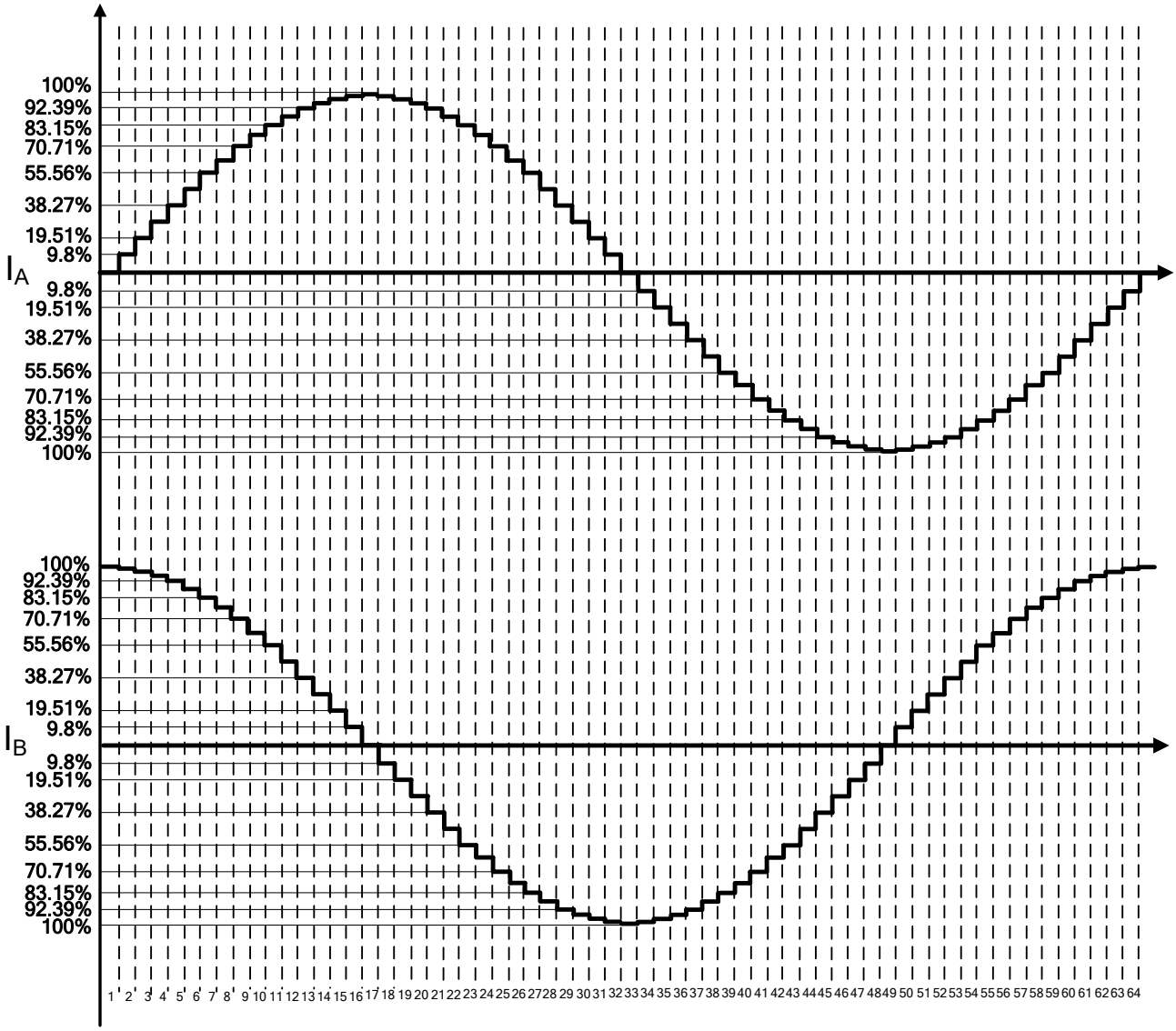

Figure 16: Sixteenth Step (64 Step Sequences, DIR = 0)

Note:

8) 1/32-step not shown due to complexity.

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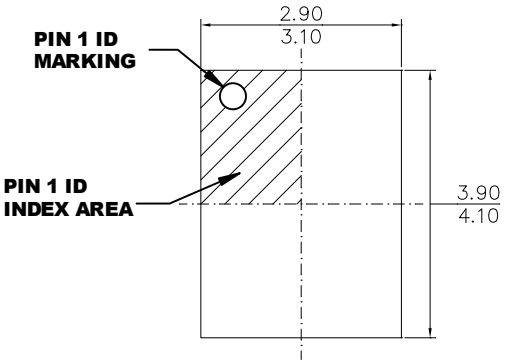
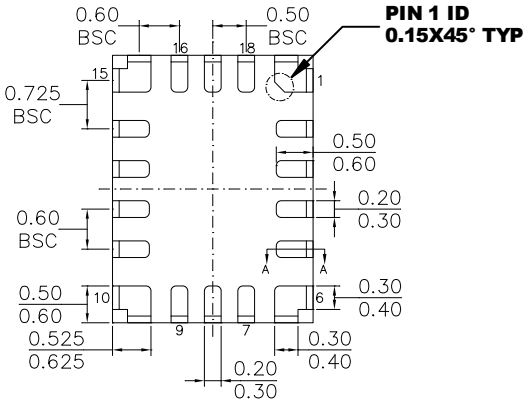
PACKAGE INFORMATION

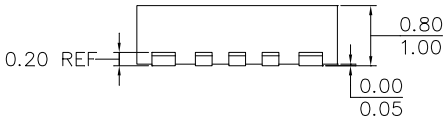
QFN-18 (3mmx4mm)



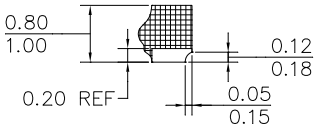
TOP VIEW



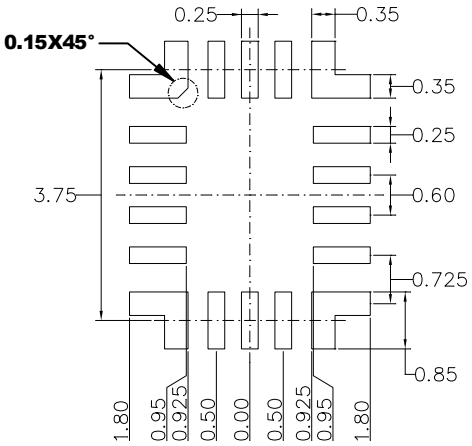
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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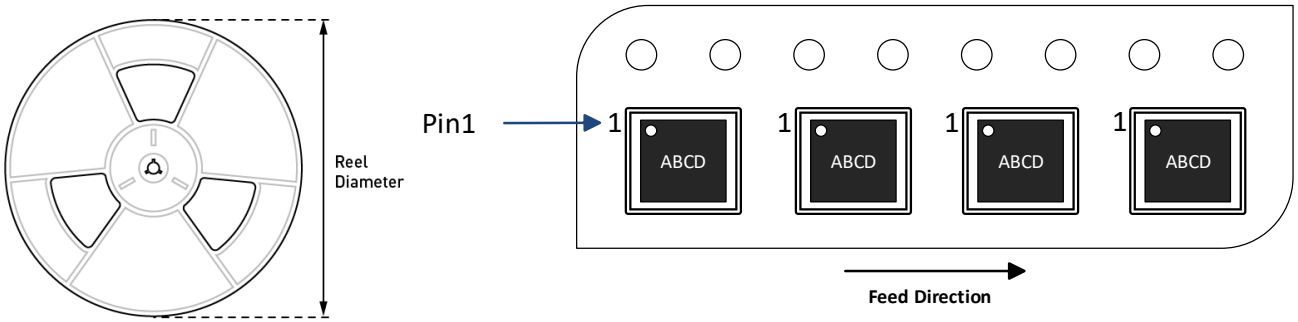
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6609GLE-AEC1-Z	QFN-18 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/18/2025	Initial Release	-

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