MPQ6590A

80V High-Side MOSFET Driver, AEC-100 Qualified

DESCRIPTON

The MPQ6590A is a high-side N-channel power MOSFET driver. It generates a gate drive voltage above the input supply voltage (V_{IN}) to drive an N-channel gate. It can source and sink 1A of current to quickly enable and disable large power MOSFETs. The MPQ6590A can operate from supply voltages up to 80V.

Internal safety features include over-current protection (OCP), under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6590A is available in a QFN-11 (3mmx4mm) package with wettable flanks, and is AEC-Q100 qualified.

FEATURES

- 7.5V to 80V Operating Input Voltage (V_{IN}) Range
- Gate Drive Charge Pump Generates Voltage 12V Above V_{IN}
- Low-Power Sleep Mode (<1µA)
- Output Tolerant to -70V
- Under-Voltage Lockout (UVLO)
- Adjustable Drain-to-Source Voltage (V_{DS}) Desaturation Detection
- Thermal Shutdown
- Fault Indication Output
- Available in a QFN-11 (3mmx4mm) Package
- Available in AEC-100 Grade 1

APPLICATIONS

- Battery Power Tools
- Automotive High-Side Switches

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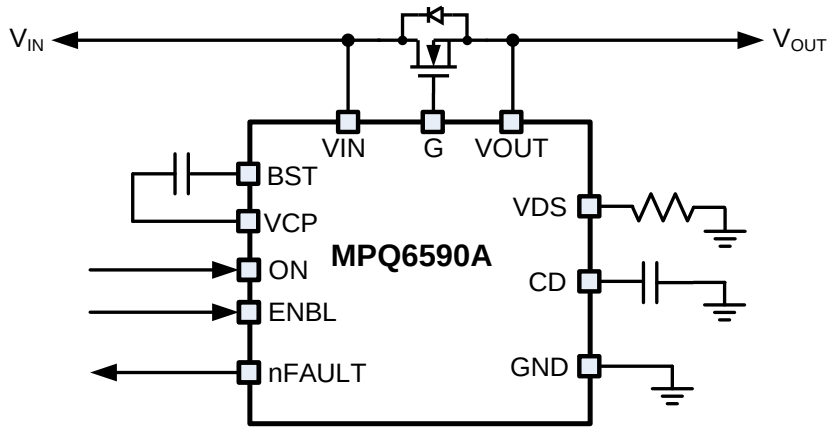
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package**	Top Marking	MSL Rating
MPQ6590AGLE-AEC1	QFN-11 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ6590AGLE-AEC1-Z).

** Wettable flank package

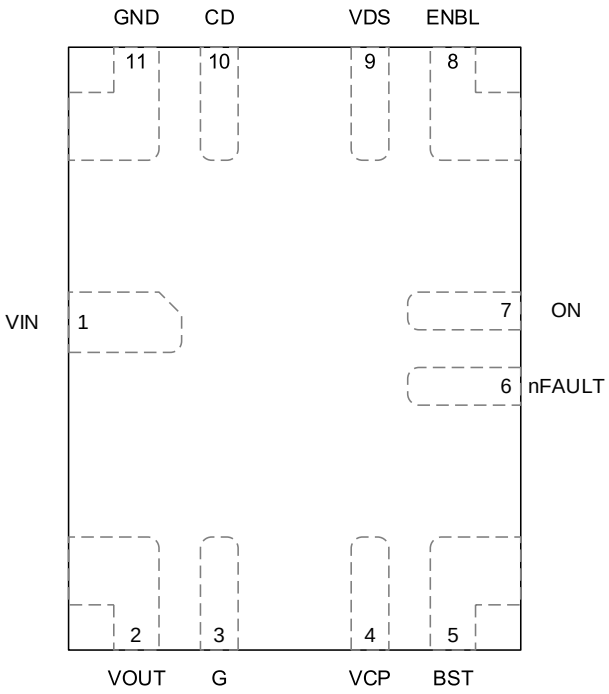
TOP MARKING

MPYW
6590
ALLL
E

MP: MPS prefix
Y: Year code
W: Week code
6590A: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-11 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
7	ON	**Input pin.** Pull the ON pin high to drive G to the input voltage (V_{IN}) + 12V; pull it low to drive G to the output voltage (V_{OUT}). This pin has an internal pull-down resistor.
8	ENBL	**Enable input.** Pull the ENBL pin low to shut down the device and drive G to V_{OUT}.
6	nFAULT	**Fault indication.** The nFAULT pin has an open-drain output. It is pulled logic low during any in fault condition (e.g. V_{DS} detection, over-temperature protection [OTP], under-voltage lockout [UVLO]).
2	VOUT	**Output feedback.** Connect the VOUT pin to the MOSFET's output to sense the VDS voltage (V_{DS}).
3	G	**Gate drive output.** Connect the G pin to the MOSFET gate.
5	BST	**Gate drive power supply.** Connect a 100nF capacitor (C_{BST}) rated for at least 16V between the BST and VCP pins.
4	VCP	**Charge pump output**. Connect a 100nF capacitor (C_{VCP}) rated for at least 16V between the VCP and BST pins.
1	VIN	**Input supply voltage.** Decouple with a minimum 100nF ceramic capacitor (C_{IN}) to GND. Additional bulk capacitance may be desirable.
9	VDS	**VDS threshold configuration.** Connect a resistor to GND to set the drain-to-source (DS) voltage (V_{DS}) threshold.
10	CD	**VDS blanking time configuration.** Connect a capacitor (C_{CD}) between the CD pin and GND to set the blanking time. Connect this pin to GND to disable V_{DS} sensing.
11	GND	**System ground connection.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +90V
Output voltage (V_{OUT}), G voltage (V_G)……
……..-70V to +100V
VCP voltage (V_{CP})……-0.7V to +100V
BST voltage (V_{BST})……-0.7V to +100V
V_G - V_{OUT} ……-0.7V to +20V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
……..2.4W
Storage temperature ..... -55°C to +150°C
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) ..... ±1500V (4)
Charged-device model (CDM)…… ±750V (5)

Recommended Operating Conditions

Supply voltage (V_{IN}) .....7.5V to 80V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Metrics (3)

θ_{JA} (junction-to-ambient).....53.2°C/W
θ_{JC_TOP} (junction-to-case top).....49.1°C/W
θ_{JC_BOTTOM} (junction-to-case bottom).....6.1°C/W
θ_{JB} (junction-to-board).....8.3°C/W
Ψ_{JT} (junction-to-top).....3.1°C/W
Ψ_{JB} (junction-to-board).....8°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on a JESD51-7, 4-layer PCB.
4) Per AECQ100-002.
5) Per AECQ100-011.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 14V, T_J = -40 to +150°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		7.5		80	V
Quiescent current	I_Q	No load current, ENBL = 1		1.1	1.5	mA
Shutdown current	I_{SHDN}	Shutdown mode, ENBL = 0, 25°C			10	µA
Gate Drive Output						
Output pull-up resistance	R_{PU}			400		Ω
Output pull-down resistance	R_{PD}			10		Ω
Peak output current (6)	I_{OUTP}			1		A
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		+20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		+20	µA
Internal pull-down resistance	R_{PD}			500		kΩ
nFault (Open-Drain Output)						
Output low voltage	V_{OL}	Output current (I_{OUT}) = 5mA			0.5	V
Output high leakage current	I_{OH}	Output voltage (V_{OUT}) = 3.3V			2	µA
Protections						
Under-voltage lockout (UVLO) rising threshold	V_{UV}		6.6	7	7.4	V
UVLO hysteresis	ΔV_{UV}			500		mV
VDS voltage (V_{DS}) detection threshold	V_{VDST}	VDS resistor (R_{VDS}) = 100kΩ	60	100	200	mV
		R_{VDS} = 5kΩ	1.5	2	2.5	V
V_{DS} detection blanking time	t_{VDSB}	CD capacitor (C_{CD}) = 1nF	5	8	11	µs
UVLO blanking time (6)	t_{UVB}	From ON = 1		5		µs
VCP threshold voltage	V_{VCPMIN}		5.8	6.5	7.2	V
Thermal shutdown	T_{TSD}			170		°C
Thermal shutdown hysteresis	ΔT_{TSD}			25		°C
Charge Pump						
Gate drive output voltage	V_{CP}		V_{IN} + 9.5	V_{IN} + 11	V_{IN} + 13.5	V

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TIMING CHARACTERISTICS

V_{IN} = 14V, T_J = -40 to +150°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Enable (wake-up) time	t_{WAKE}	From ENBL = low to high		50		µs
Disable (sleep) time	t_{SLEEP}	From ENBL = high to low		200		ns
Start-up time (6)	t_{PUP}	From $V_{VCP} > V_{VCPMIN}$		200		ns
Propagation delay	t_{PD}	IN to G = 10V, C_L = 10nF		200		ns

Note:

6) Not tested in production; guaranteed by design.

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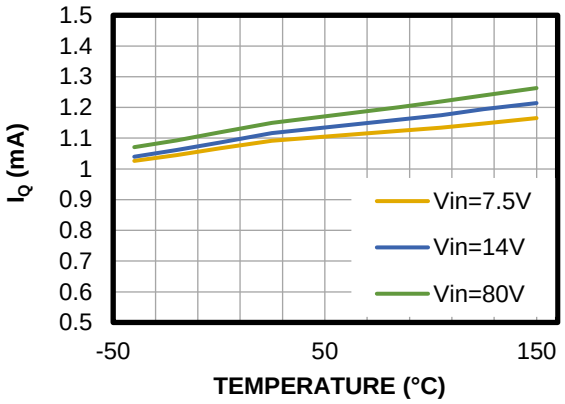
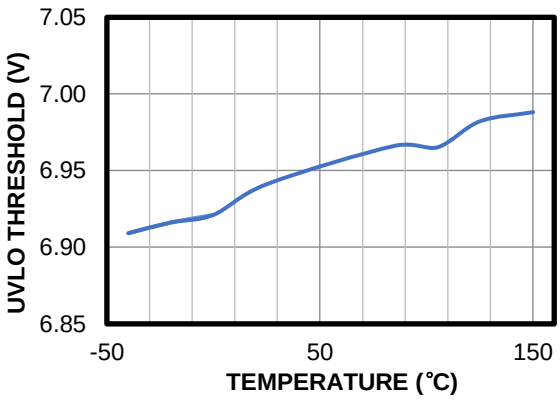
TYPICAL CHARACTERISTICS

V_{IN} = 14V, T_J = -40 to +150°C, unless otherwise noted.

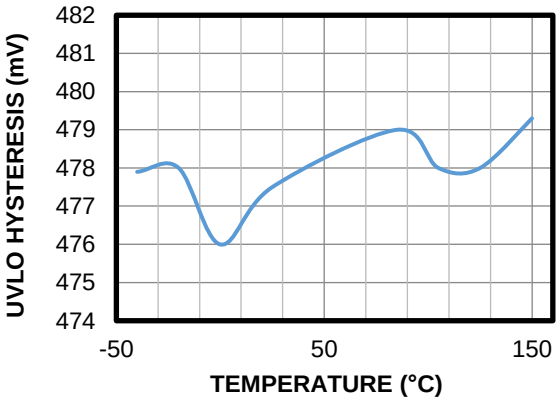
Quiescent Current vs. Temperature



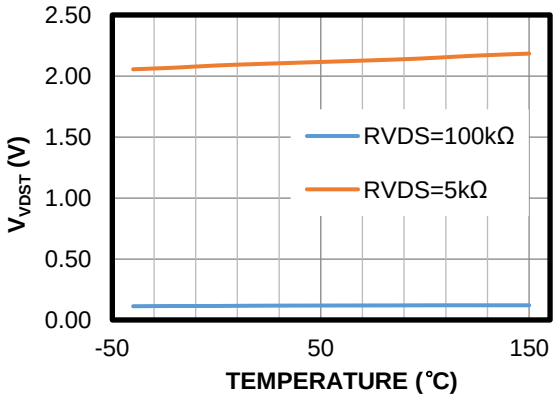
UVLO Threshold vs. Temperature



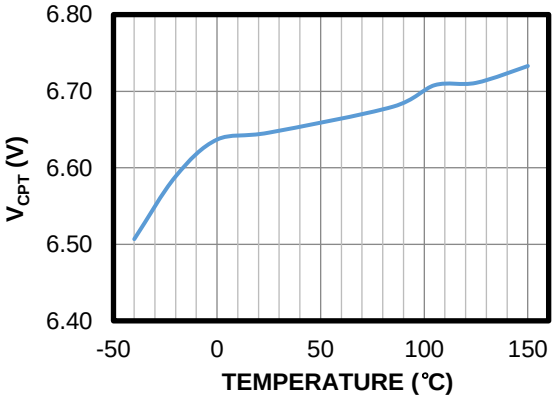
UVLO Hysteresis vs. Temperature



V_{DS} Detection Threshold vs. Temperature



VCP Voltage Threshold vs. Temperature



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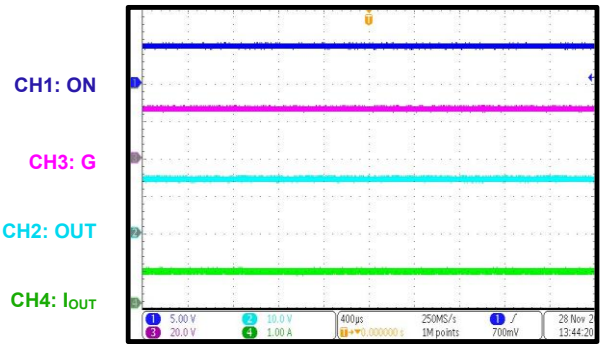
TYPICAL PERFORMANCE CHARACTERISTICS

V_{ON} = 5V, V_{ENBL} = 5V, T_A = 25°C, unless otherwise noted.

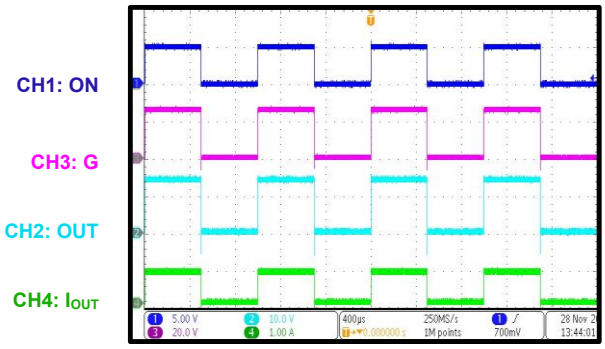
High-Side Fully On

V_{IN} = 14V, ON = ENBL = high, load = 17Ω



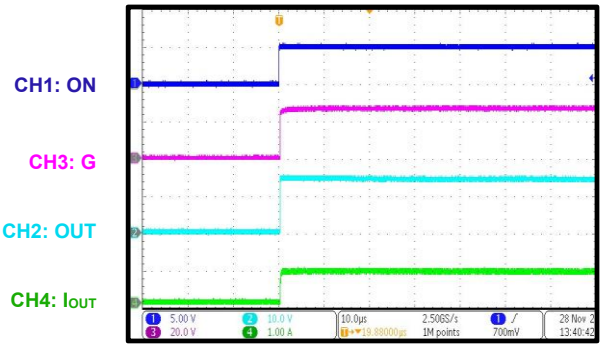
Switching Operation

V_{IN} = 14V, ENBL = high, ON = 1kHz/50%, load = 17Ω



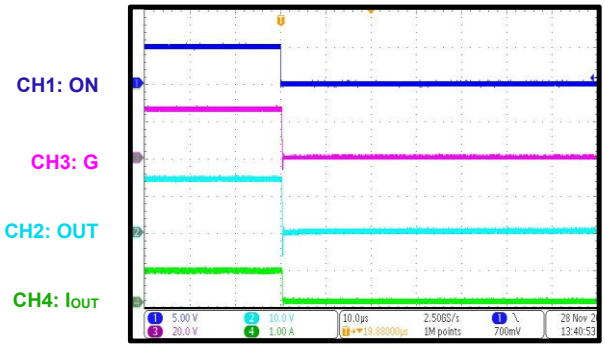
MOSFET Turning On

V_{IN} = 14V, ENBL = high, ON = from low to high, load = 17Ω



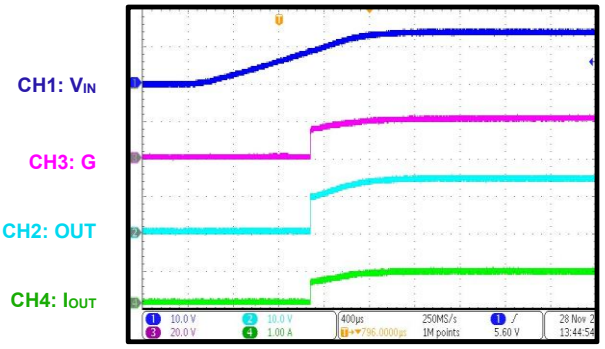
MOSFET Turning Off

V_{IN} = 14V, ENBL = high, ON = from high to low, load = 17Ω



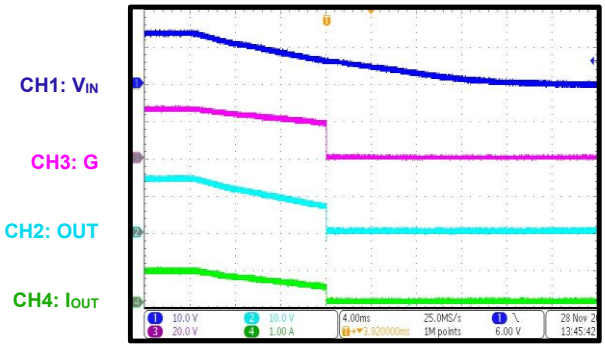
Start-Up through VIN

V_{IN} = 14V, ON = ENBL = high, load = 17Ω



Shutdown through VIN

V_{IN} = 14V, ON = ENBL = high, load = 17Ω



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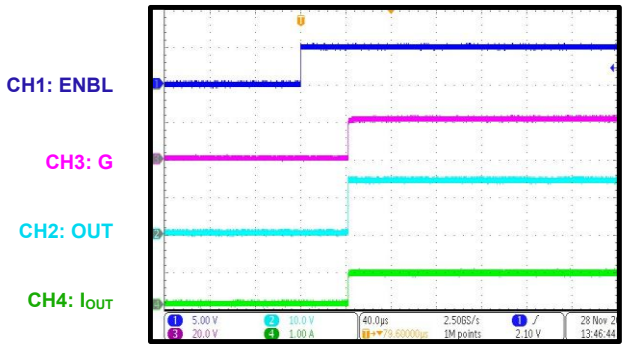
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{ON} = 5V, V_{ENBL} = 5V, T_A = 25°C, unless otherwise noted.

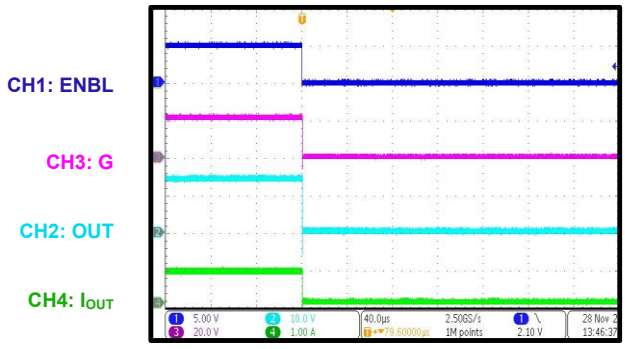
IC Enable

V_{IN} = 14V, ON = high, ENBL from low to high, load = 17Ω



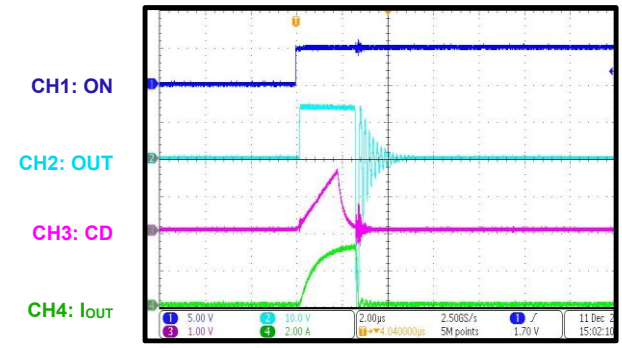
IC Disable

V_{IN} = 14V, ON = high, ENBL from high to low, load = 17Ω



OCP

V_{IN} = 14V, ENBL = high, ON from low to high, MOSFET $R_{DS(ON)}$ = 60mΩ, OCP threshold = 100mV, load = 4Ω



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FUNCTIONAL BLOCK DIAGRAM

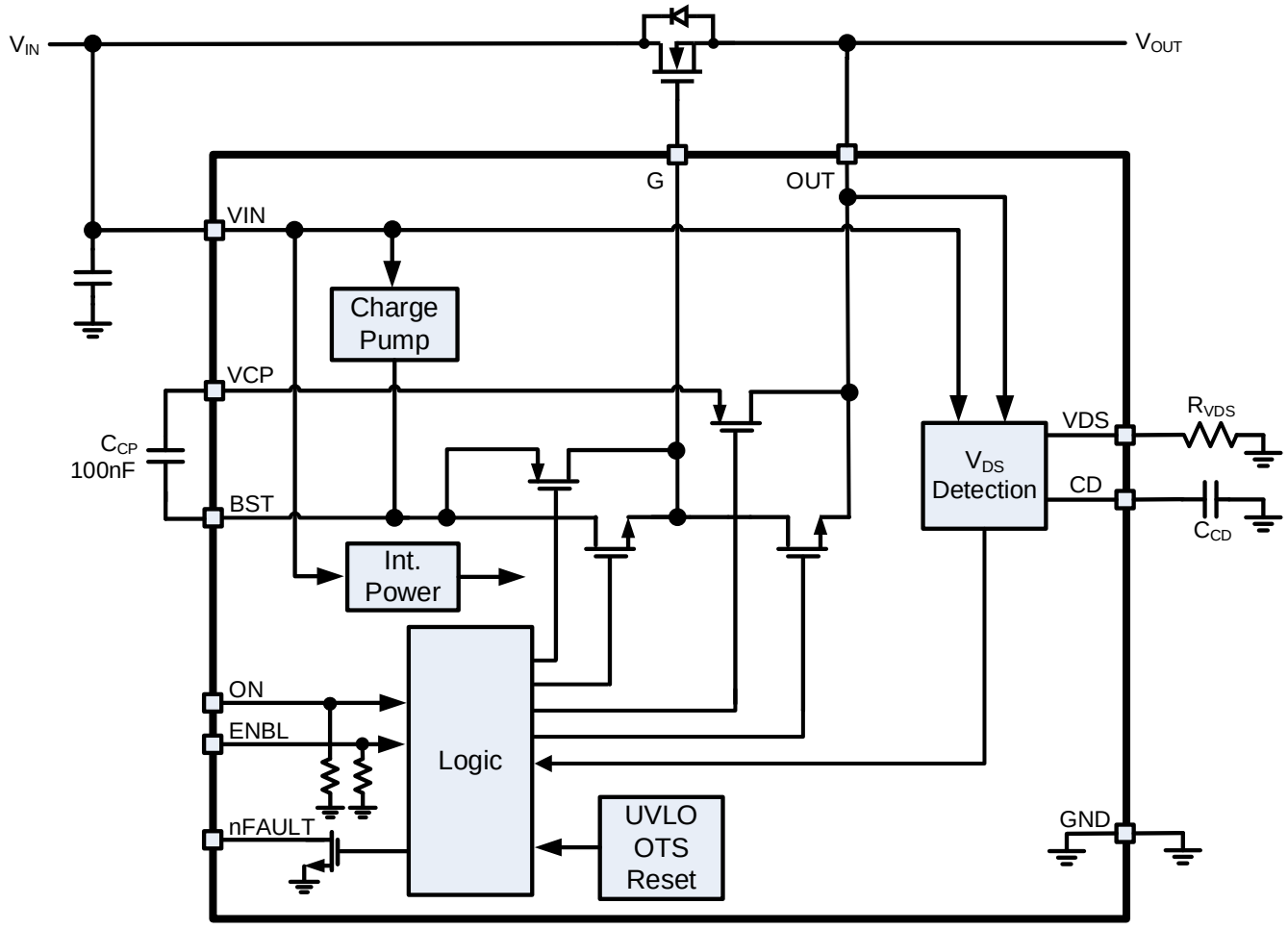

Figure 1: Functional Block Diagram

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OPERATION

The MPQ6590A, in combination with an external N-channel power MOSFET, is used to implement a high-side switch. It generates the required gate drive voltage to fully enhance the external MOSFET, and provides control and protection functions.

Start-Up

Once the VCP voltage exceeds V_{VCPMIN} and the ENBL pin is logic high, the MPQ6590A starts up. The external MOSFET cannot turn on until the input voltage (V_{IN}) exceeds its under-voltage lockout (UVLO) threshold (V_{IN_UVLO}) and the VCP voltage (V_{CP}) has exceeded its minimum threshold (V_{VCPMIN}). There is a minimum 200ns delay (t_{PUP}) before the MOSFET can be enabled to prevent rapid cycling during a fault condition.

Input Logic

The MPQ6590A has two input pins: ON and ENBL.

The ENBL pin enables and disables the part. When ENBL is logic low, the internal charge pump is disabled and internal circuitry is put into a low-power state. The G pin is pulled to the VOUT pin to keep the external MOSFET disabled.

When ENBL is pulled to logic high, the part is enabled and the charge pump runs.

The ON pin is used to turn the external MOSFET on. Pulling the ON pin logic high drives G to V_{IN} + 12V and turns the MOSFET on. Pulling it logic low drives G to the output voltage (V_{OUT}) to turn the MOSFET off.

Charge Pump/Bootstrap

An external capacitor (C_{BST}) is used as a bootstrap to initially turn on the external MOSFET. Once the MOSFET is on, a weak charge pump is used to overcome leakages to allow 100% duty cycle operation indefinitely.

There must be some load at the OUT pin (MOSFET source) to return the current (approximately 10µA) required to charge C_{BST} when the MOSFET is turned off. The load resistance (R_{LOAD}) must be less than (V_{IN} - 6.5V) / 10µA. This equates to 750kΩ when V_{IN} = 14V.

The gate drive voltage is regulated at a nominal 12V for the standard MPQ6590A. If the charge pump voltage drops to below the charge pump threshold voltage (V_{VCPMIN}), the external MOSFET turns off.

Gate Driver

N-channel and P-channel MOSFETs are used to drive the external MOSFET's gate either to the charge pump voltage or to the output, which is the source terminal for the external MOSFET.

The output terminal can be subject to negative voltages when the switch is turned off. The MPQ6590A's VOUT pin can tolerate negative voltages to -70V.

Drain-to-Source Voltage (V_{DS}) Desaturation Detection

To provide some protection against short circuits, the MPQ6590A monitors the voltage drop across the external MOSFET.

When the MOSFET is turned on, the voltage difference between V_{IN} and V_{OUT} is monitored. When the MOSFET is first turned on, V_{DS} detection is disabled until after a set blanking time (t_{VDSB}, typically 8µs when C_{CD} = 1nF). If the voltage exceeds the V_{DS} threshold (V_{DST}), the MOSFET turns off and the nFAULT pin is pulled active low. The part remains in this state until either the ON or ENBL pin is made inactive and then active again, or until power is removed and re-applied.

V_{DST} is set by an external resistor (R_{VDS}) placed between the VDS pin and ground. It can be calculated using Equation (1):

$$V_{VDST}(V) = 10/R_{VDS}\ (k\Omega) \quad (1)$$

For example, a 100kΩ R_{VDS} gives a threshold of 100mV; a 5kΩ R_{VDS} gives a threshold of 2V.

t_{VDSB} is used after the MOSFET is turned on to allow for inrush current. The time is set by a capacitor (C_{CD}) connected between the CD pin and ground. A 200µA current is sourced to the pin, and the desaturation detection is blanked until the CD pin's voltage (V_{CD}) reaches 1.22V. The time can be calculated with Equation (2):

$$t_{VDSB} = 1.22V \times C_{CD} / 200\mu A \quad (2)$$

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V_{IN} Under-Voltage Lockout (UVLO) Protection

If at any time V_{IN} falls below V_{IN_UVLO}, the external MOSFET turns off, and the device turns off most internal circuitry and enters a low power state. Once V_{IN} again exceeds V_{IN_UVLO}, the device resumes normal operation.

UVLO protection is disabled (blanked) for a short time (t_{UVB}) after the external MOSFET turns on. This delay is longer than t_{VDSB}, so that during a turn-on into a short circuit that causes V_{IN} to droop, V_{DS} protection can still detect the event.

Over-Temperature Protection (OTP)

If the die temperature exceeds safe limits (the thermal shutdown temperature, typically 170°C), the G pin is pulled to the VOUT pin to turn the MOSFET off, and the nFAULT pin is pulled low. Once the die temperature has fallen to a safe level (below the OTP falling threshold, typically 145°C), the device resumes normal operation automatically.

nFAULT Output

The MPQ6590A provides an nFAULT pin that is driven active low if any of the protection circuits are activated. These fault conditions include a V_{DS} fault, V_{CP} UVLO, V_{IN} UVLO, and OTP. nFAULT is an open-drain output and requires an external pull-up resistor. Once the fault condition is removed, the nFAULT pin is pulled inactive high by the pull-up resistor.

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APPLICATION INFORMATION

PCB Layout Guidelines

Proper PCB layout is critical for optimal performance. The MPQ6590A is designed to accommodate a negative undershoot, but excessive undershoot can damage the device. For the best results, refer to Figure 2 and follow the guidelines below:

1. Make the connection between the OUT pin and the MOSFET source as direct as possible to avoid excessive undershoot on OUT due to inductive load or parasitic inductance.
2. Place the C_{BST}, C_{CD}, and supply bypass capacitors as close to the IC as possible.
3. Use wide copper areas for all the high-current paths.

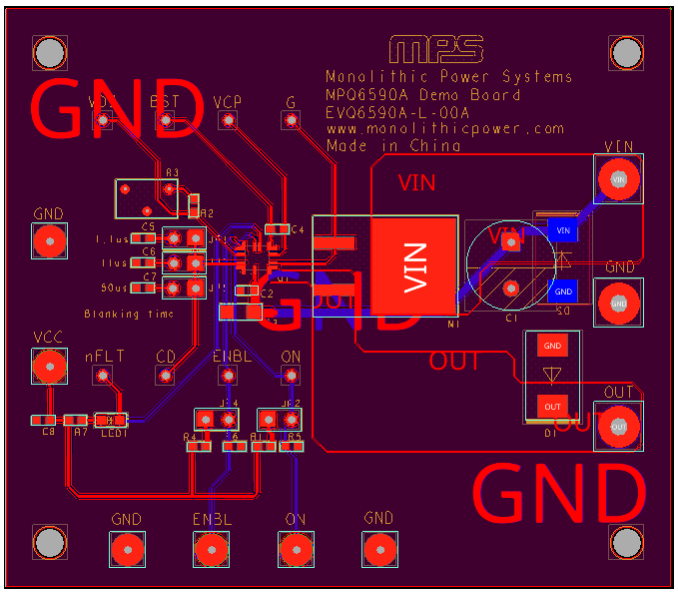

Figure 2: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

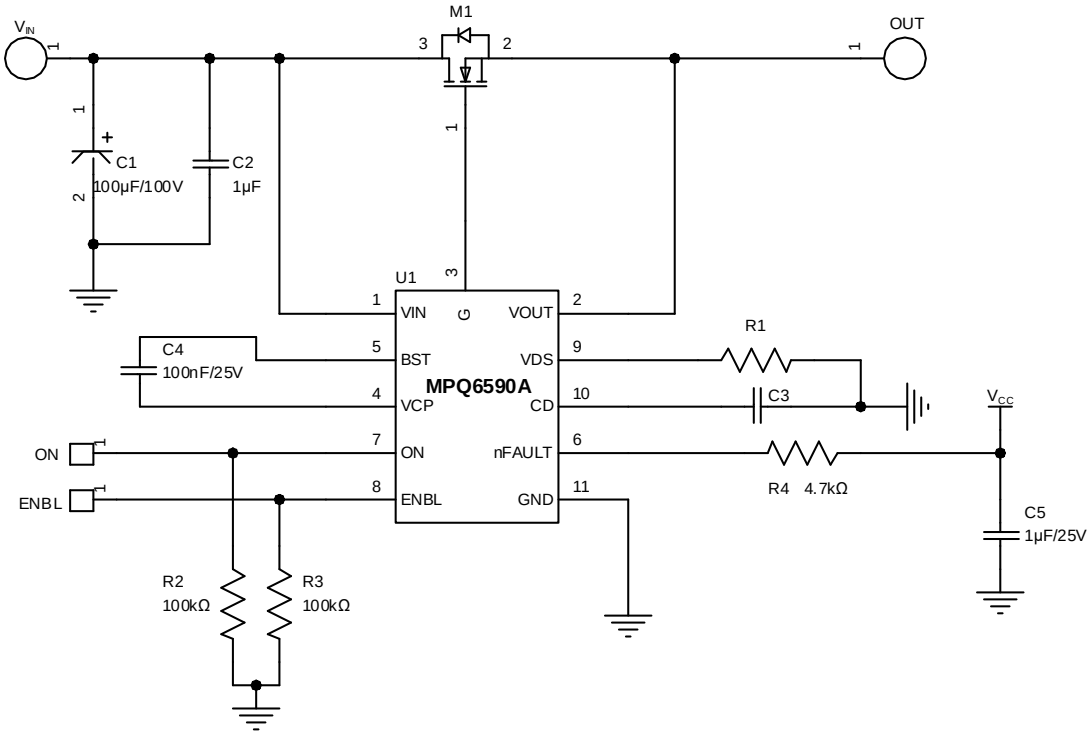

Figure 3: Typical Application Circuit

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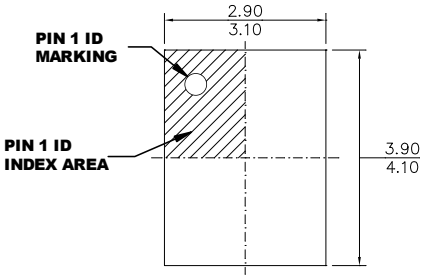
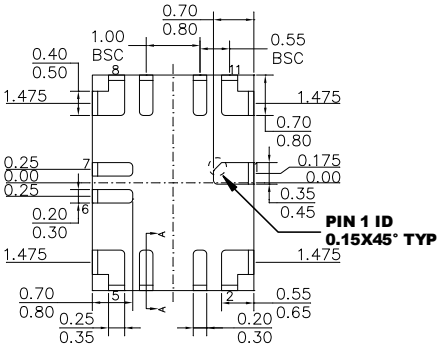
PACKAGE INFORMATION

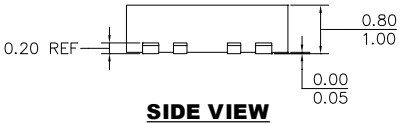
QFN-11 (3mmx4mm)
Wettable Flanks



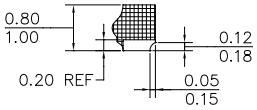
TOP VIEW



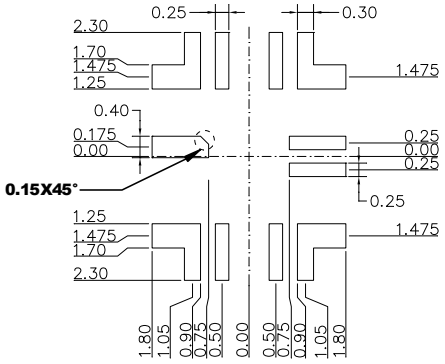
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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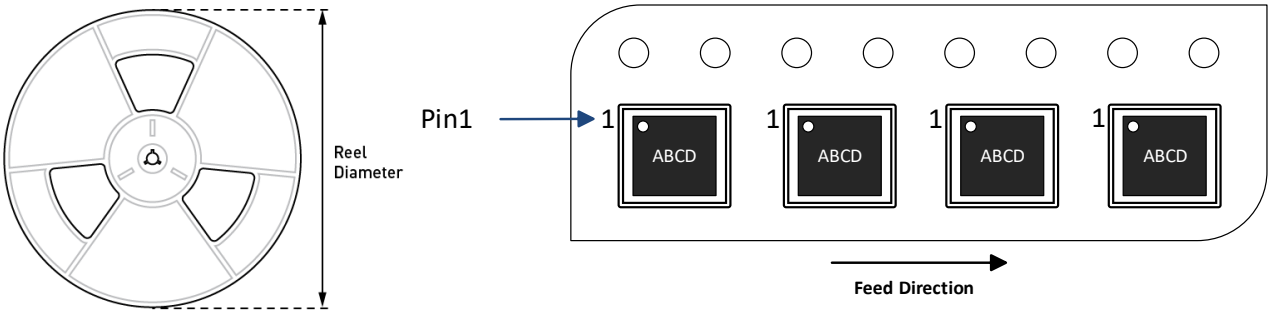
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6590AGLE -AEC1-Z	QFN-11 (3mmx4mm) with wettable flanks	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/14/2026	Initial Release	-

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