MPQ4570

3A, 4.5V-55V Input, Frequency Programmable, Fully Integrated Synchronous, Step-Down Converter

AEC-Q100 Qualified

The Future of Analog IC Technology

DESCRIPTION

The MPQ4570 is a frequency programmable step-down switching converter with integrated internal high-side and low side power MOSFETs. It can provide 3A continuous output current with peak current control for excellent transient response and efficiency performance.

The wide 4.5V to 55V input voltage range accommodates a variety of step down applications, including those applications in industrial, PoE, automotive and printer with DC high voltage bus.

The MPQ4570 uses peak current mode control to regulate the output voltage. The chip provides over current protection with valley current detection which is used to avoid current running way. Also it has accurate and reliable over voltage protection, and auto recovery thermal protection. In addition, the optional external soft start is available. Enable and power good indication function can be used to power track easily. In order to increase the efficiency, MPQ4570 will automatically scaling down the switching frequency when load is light. Meanwhile, the low side MOSFET will be turned off to reduce driver loss when zero inductor current is detected. MPQ4570 also features as a fully integrated solution with both high side and low side power MOSFETs. Synchronous operation mode with integrated low side MOSFET is much helpful to reduce the conduction loss and also beneficial to reduce external components space and save the cost.

The MPQ4570 is available in a TSSOP-20 EP with exposed pad package.

FEATURES

- Wide Input Voltage Range: 4.5V to 55V
- 90mΩ and 70mΩ Internal High and Low Power MOSFETs
- Peak Current Mode Control
- Programmable Switching Frequency
- Stable Independent on Output Capacitors
- Optional External Soft Start
- OCP Protection with Valley Current Detection
- Support External SYNC Clock
- OVP Protection
- Current Limit Decreasing during Output Short for Better Thermal Performance
- Power Good Indication
- Thermal Shutdown Protection
- Available in a TSSOP-20 EP Package.
- Available in AEC-Q100 Grade 1

APPLICATIONS

- PoE Input Non-isolated Buck
- Industrial Power Systems
- Printers and Scanners
- Automotive Power Systems
- Distributed Power Systems

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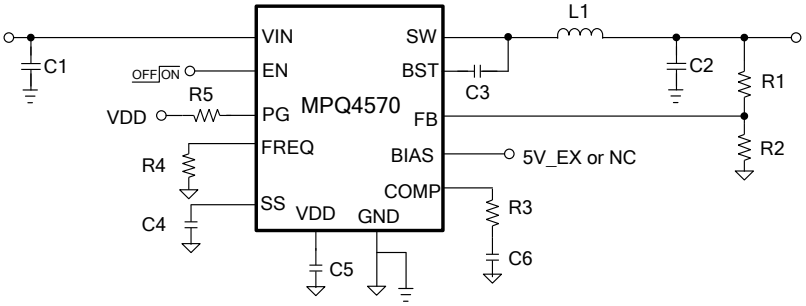
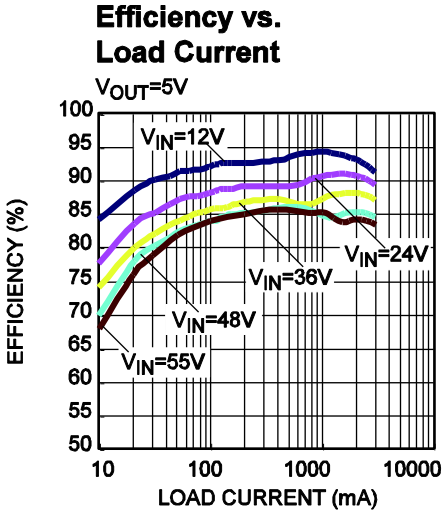
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ4570GF*	TSSOP-20 EP	*See Below*
MPQ4570GF-AEC1	TSSOP-20 EP	*See Below*

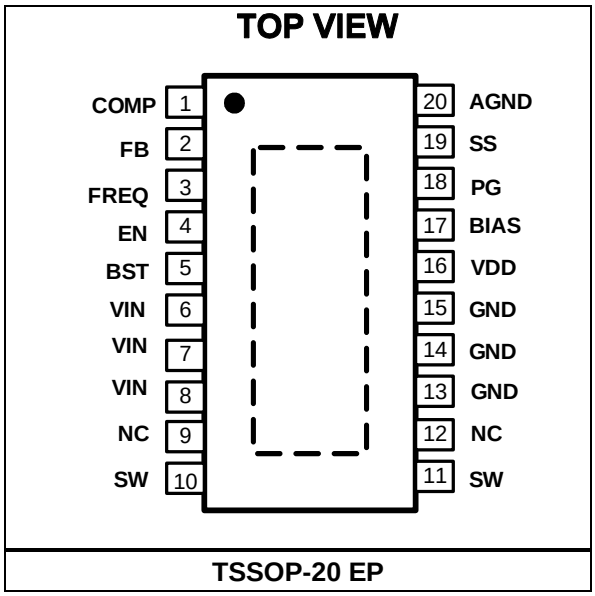
* For Tape & Reel, add suffix –Z (e.g. MPQ4570GF–Z);

TOP MARKING

MPSYYWW
MP4570
LLLLLLLLL

MP4570: product code of MPQ4570GF and MPQ4570GF-AEC1;
MPS: MPS prefix:
YY: year code;
WW: week code:
LLLLLLLLL: lot number;

PACKAGE REFERENCE



TSSOP-20 EP

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ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 60V
V_{SW} ..... –0.5V to (VIN+0.5V)
V_{BS} ..... V_{SW} + 6V
All Other Pins ..... –0.3V to +6V
EN Sink Current 150µA
Continuous Power Dissipation (T_A = 25°C) (2)
TSSOP-20 EP 2.78W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions

Supply Voltage V_{IN} ..... 4.5V to 55V
Output Voltage V_{OUT} ..... 1V to 0.9·V_{IN}
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (3) θ_{JA} θ_{JC}

TSSOP-20 EP	45	10	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 48V, V_{EN} = 3.3V, T_J= -40°C to +125°C, unless otherwise noted. Typical values are at T_J= 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Error Amplifier						
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 55V	0.98	1	1.02	V
FB Current	I_{FB}	V_{FB}=1.07V		10	50	nA
Error AMP Transconductance			430	630	730	μA/V
COMP Sink/Source Current	I_{COMP}		13	30	52	μA
Switch Characteristic						
Upper Switch On Resistance	R_{ON_HS}			90	160	mΩ
Lower Switch On Resistance	R_{ON_LS}			70	120	mΩ
Upper Switch Leakage	I_{LKG_SW}	V_{EN} = 0V, V_{SW} = 0V		10	300	nA
Current Limit						
Peak Current Limit	I_{LIMIT}	10% Duty Cycle	3.9	5.7	7.5	A
Quiescent Supply						
Quiescent Supply Current	I_Q	No load, Without Switching		450	670	μA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V		7	18	μA
VDD Regulator						
VDD Regulator Output Voltage	V_{DD}	BIAS = NC	3.4	3.6	3.8	V
VDD Regulator Output Voltage	V_{DD}	BIAS = External 5V Power	4.6	4.8		V
Threshold Voltage						
EN Rising Threshold	V_{EN_R}		1.4	1.6	1.8	V
EN Falling Threshold	V_{EN_F}		1.1	1.3	1.5	V
EN Threshold Hysteresis	V_{EN_HYS}			300		mV
VIN UVLO Rising Threshold	V_{INUV_R}		3.7	3.9	4.1	V
VIN UVLO Falling Threshold	V_{INUV_F}		3.3	3.5	3.7	V
VIN UVLO Threshold Hysteresis	V_{INUV_HYS}			400		mV
Soft Start						
External Soft Start Capacitor Charging Current	I_{SS}	V_{SS}=1V	2.5	4	5.5	μA
PWM Comparator						
Minimum Off Time (4)	t_{OFF_MIN}			100		ns
Minimum On Time (4)	t_{ON_MIN}			90		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{EN} = 3.3V, T_J= -40°C to +125°C, unless otherwise noted. Typical values are at T_J= 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillator Frequency						
Switching Frequency	f_{SW}	R_{FREQ}=100k	400	520	640	kHz
OVP Protection						
Output OVP Threshold	V_{OVP}	$V_{FB(OVP)}/V_{FB}$	108	115	122	%
Power Good						
Power Good Threshold	V_{PG_TH}	V_{OUT} Rising, $V_{FB(PG)}/V_{FB}$	86	90	94	%
		V_{OUT} Falling, $V_{FB(PG)}/V_{FB}$	81	85	89	
Power Good Hysteresis	V_{PG_HYS}	$\Delta V_{FB(PG)}/V_{FB}$		5		%
Power Good Delay	t_{PG_DL}	V_{OUT} Rising	8	22	37	µs
		V_{OUT} Falling	8	21	33	µs
Frequency SYNC						
SYNC Leakage Current	I_{LKG_SYNC}			10	100	nA
SYNC Frequency Range	f_{SYNC}		100		1000	kHz
Thermal						
Thermal Shutdown (4)	T_{SD}		150	170		°C
Thermal Shutdown Hysteresis (4)	T_{SD_HYS}			10		°C

Note:

4) Derived from bench characterization. Not tested in production.

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PIN FUNCTIONS

Pin #	Name	Description
1	COMP	Compensation Networks Setting. Please connect an external resistor series with a capacitor between this pin and GND.
2	FB	Feedback. This is the input to the PWM comparator. Please put an external resistive divider connected between the output and GND.
3	FREQ	Switching frequency setting pin. Connect a resistor from this pin to GND to set the switching frequency. If external SYNC clock is applied to this pin, the converter will follow this SYNC clock frequency.
4	EN	Enable Input. Pulling this pin below the specified threshold shuts the chip down. There is no internal pull-up or pull-down circuit, so do not float the pin.
5	BST	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a capacitor between this pin and SW pin.
6,7,8	VIN	Input Supply. This supplies power to all the internal control circuitry, VDD regulator. A decoupling capacitor to ground must be placed close to this pin to minimize switching spikes.
9,12	NC	Not connected pin. Please float this pin in the application.
10,11	SW	Switch Node. This is the output node from the internal high-side MOSFET source.
13,14, 15, Exposed Pad	GND	Power ground pin for internal power MOSFETs.
16	VDD	Power for internal MOSFET driver and BST charging circuit.
17	BIAS	For better thermal performance, please connect this pin to external 5V source, VDD and internal circuit will be powered by BIAS. Since there is a diode inside between the BIAS pin and the internal circuit, please float this pin or connected to GND if not used.
18	PG	Power good indication. Please connect a resistor to a pull up power source if used.
19	SS	Optional external soft-start time setting. Connect an external capacitor between this pin and GND to set soft-start time externally. Floating the pin will activate the internal 0.5ms soft-start setting.
20	ANGD	Ground for internal logic and signal circuit.

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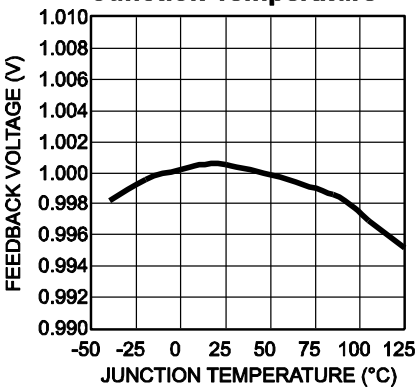
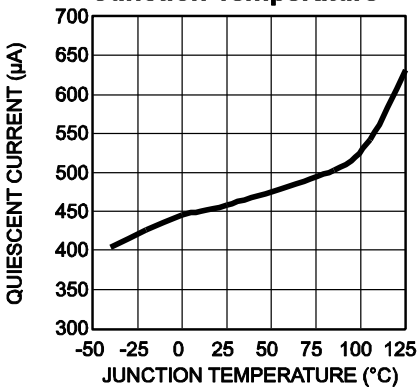
TYPICAL CHARACTERISTICS

V_{IN}=48V, unless otherwise noted.

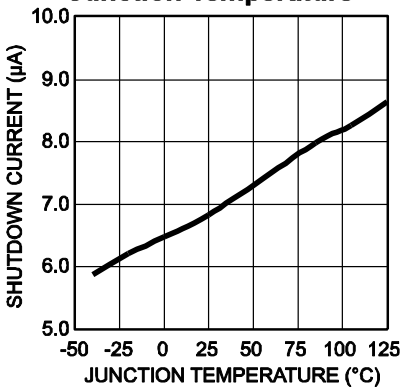
Feedback Voltage vs. Junction Temperature



Quiescent Current vs. Junction Temperature

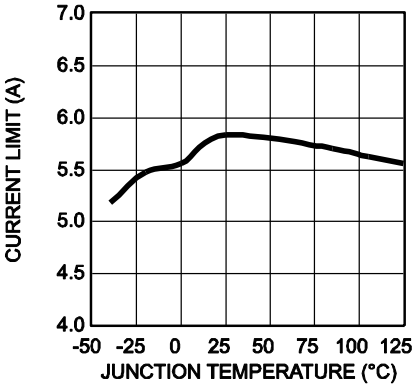


Shutdown Current vs. Junction Temperature

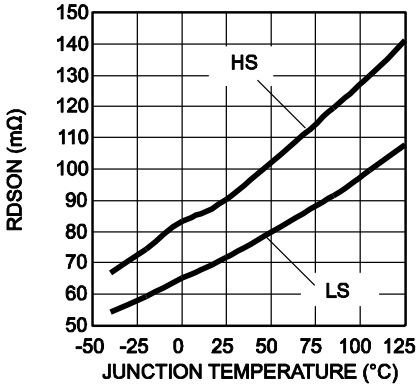


Current Limit vs. Junction Temperature

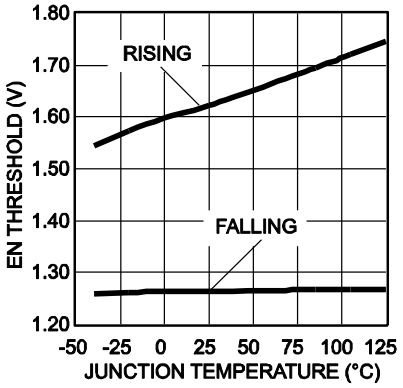
Duty Cycle=10%



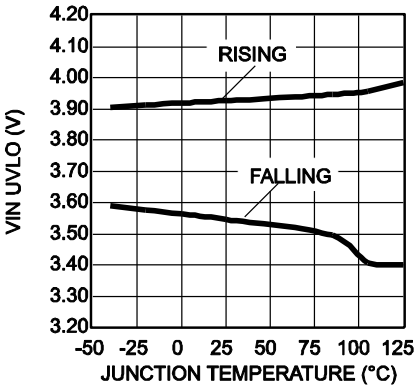
Switch ON Resistance vs. Junction Temperature



EN Threshold vs. Junction Temperature

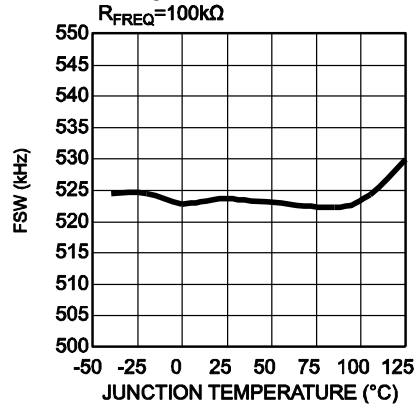


V_{IN} UVLO vs. Junction Temperature



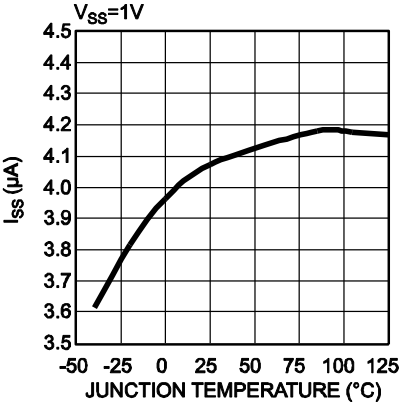
f_{SW} vs. Junction Temperature

R_{FREQ}=100kΩ



I_{SS} vs. Junction Temperature

V_{SS}=1V



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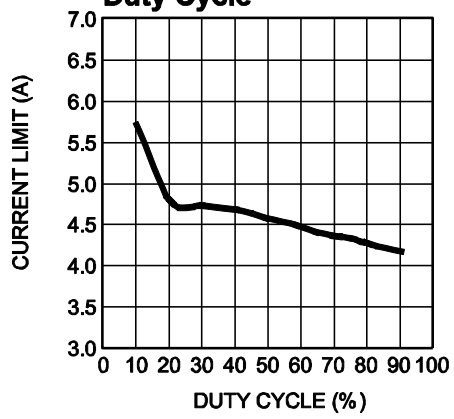
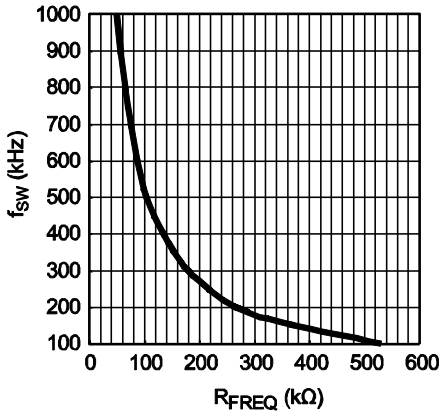
TYPICAL CHARACTERISTICS

V_{IN}=48V, unless otherwise noted.

Current Limit vs. Duty Cycle



f_{SW} vs. R_{FREQ}



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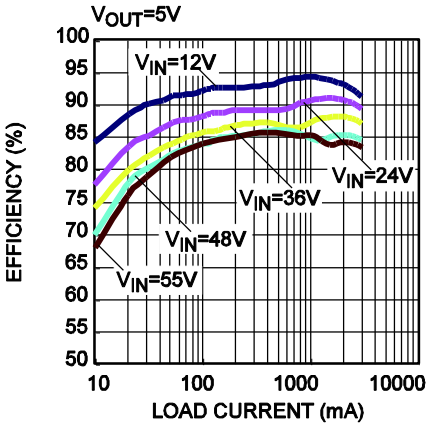
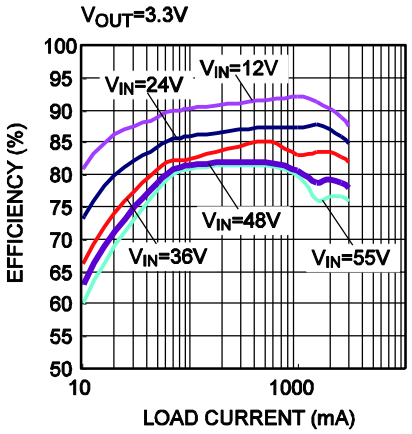
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} =3.3V, C_{OUT} = 2x22µF, L = 10µH, f_{SW}=500kHz, T_A = +25°C, unless otherwise noted.

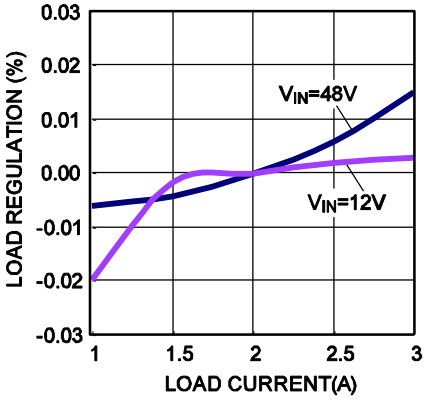
Efficiency vs. Load Current



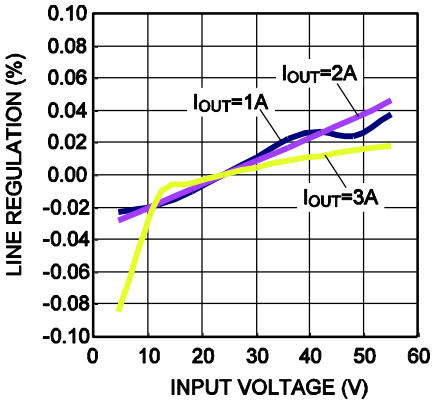
Efficiency vs. Load Current



Load Regulation



Line Regulation



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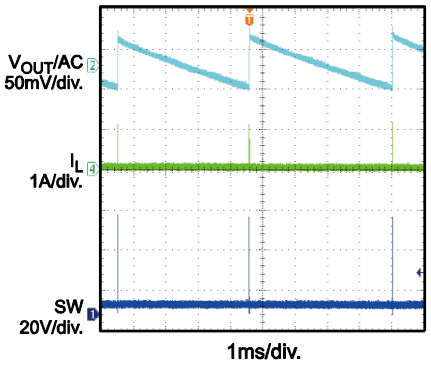
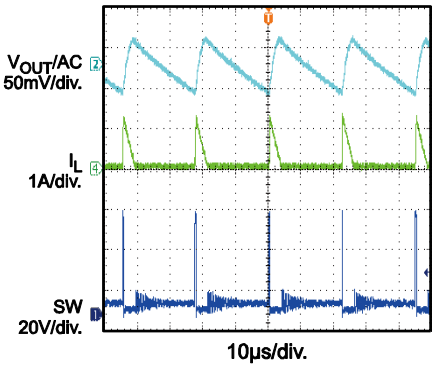
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} =3.3V, C_{OUT} = 2x22µF, L = 10µH, f_{SW}=500kHz, T_A = +25°C, unless otherwise noted.

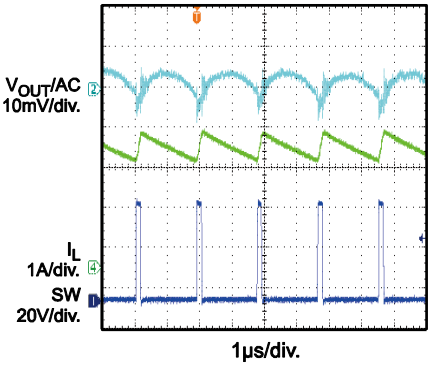
Steady State
I_{OUT}=0A



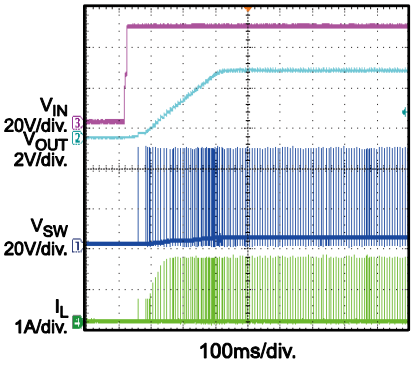
Steady State
I_{OUT}=0.1A



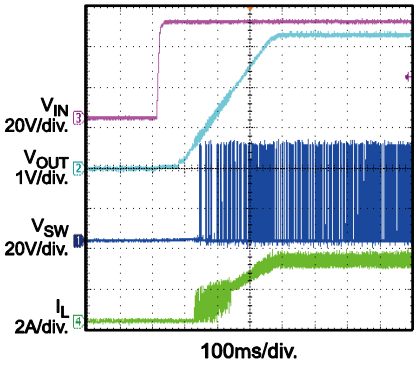
Steady State
I_{OUT}=3A



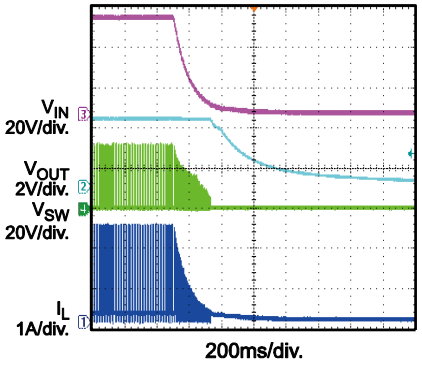
Startup Through V_{IN}
I_{OUT} = 0A



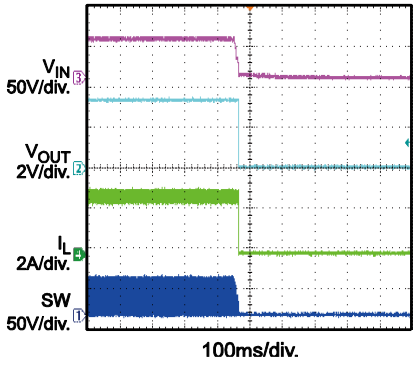
Startup Through V_{IN}
I_{OUT} = 3A



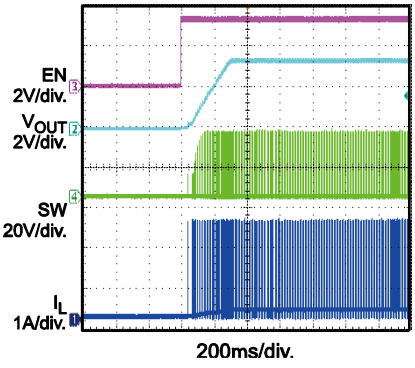
Shutdown Through V_{IN}
I_{OUT} = 0A



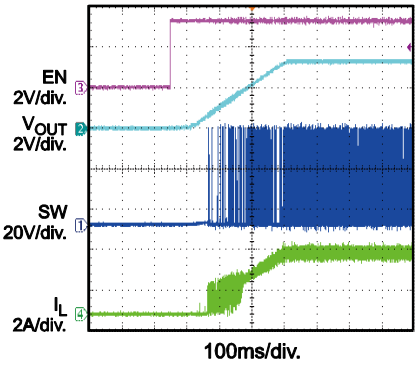
Shutdonw Through V_{IN}
I_{OUT} = 3A



Startup Through EN
I_{OUT} = 0A



Startup Through EN
I_{OUT} = 3A



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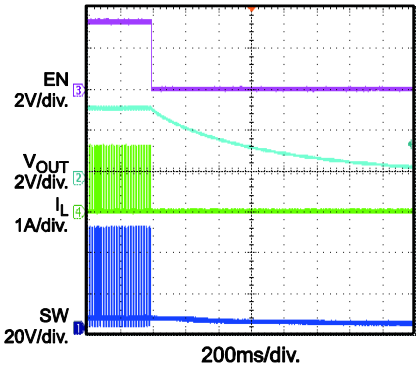
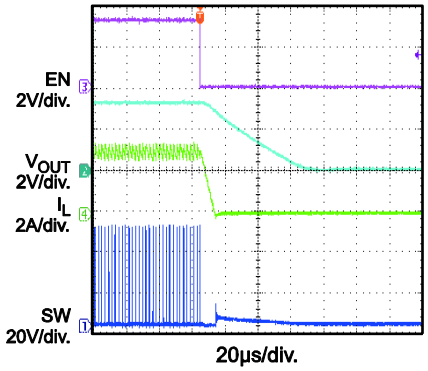
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} =3.3V, C_{OUT} = 2x22µF, L = 10µH, f_{SW}=500kHz, T_A = +25°C, unless otherwise noted.

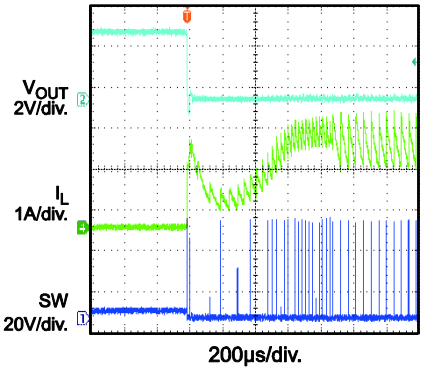
Shutdown Through EN
I_{OUT}=0A



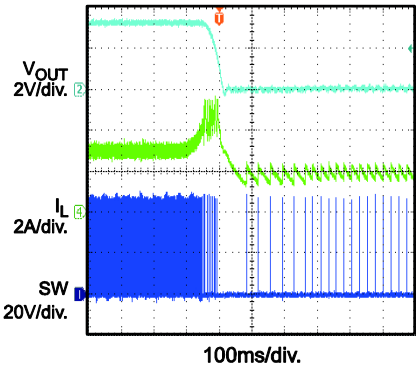
Shutdown Through EN
I_{OUT}=3A



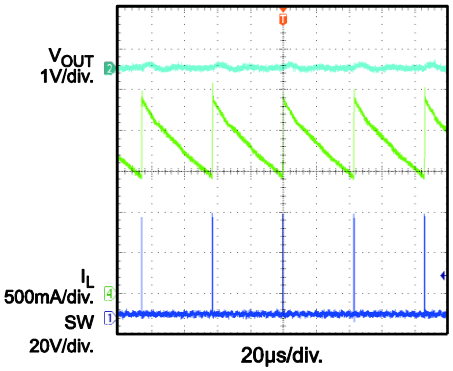
SCP Entry
I_{OUT}=0A to Short Circuit



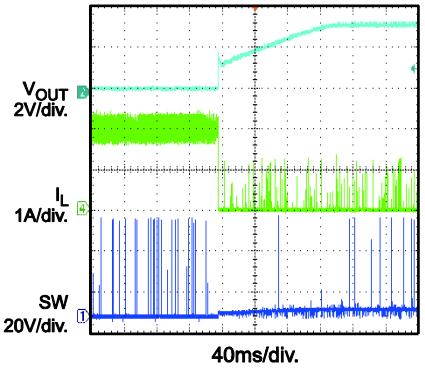
SCP Entry
I_{OUT}=3A to Short Circuit



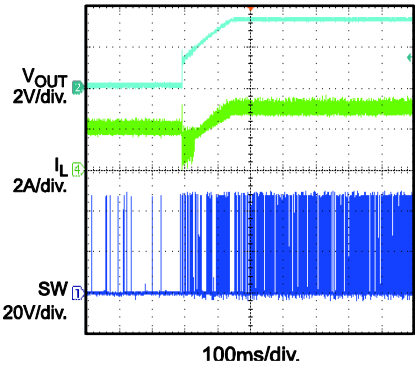
SCP Steady State



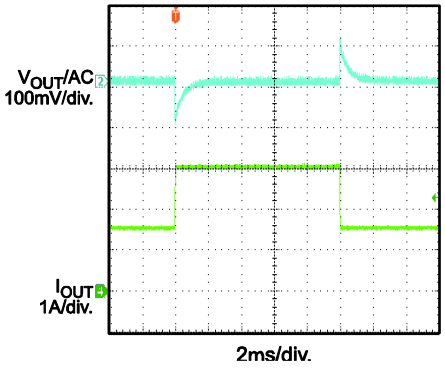
SCP Recovery
Short Circuit to I_{OUT}=0A



SCP Recovery
Short Circuit to I_{OUT}=3A



Load Transient
I_{OUT} =1.5A <-> 3A, 1.6A/µs



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FUNCTIONAL BLOCK DIAGRAM

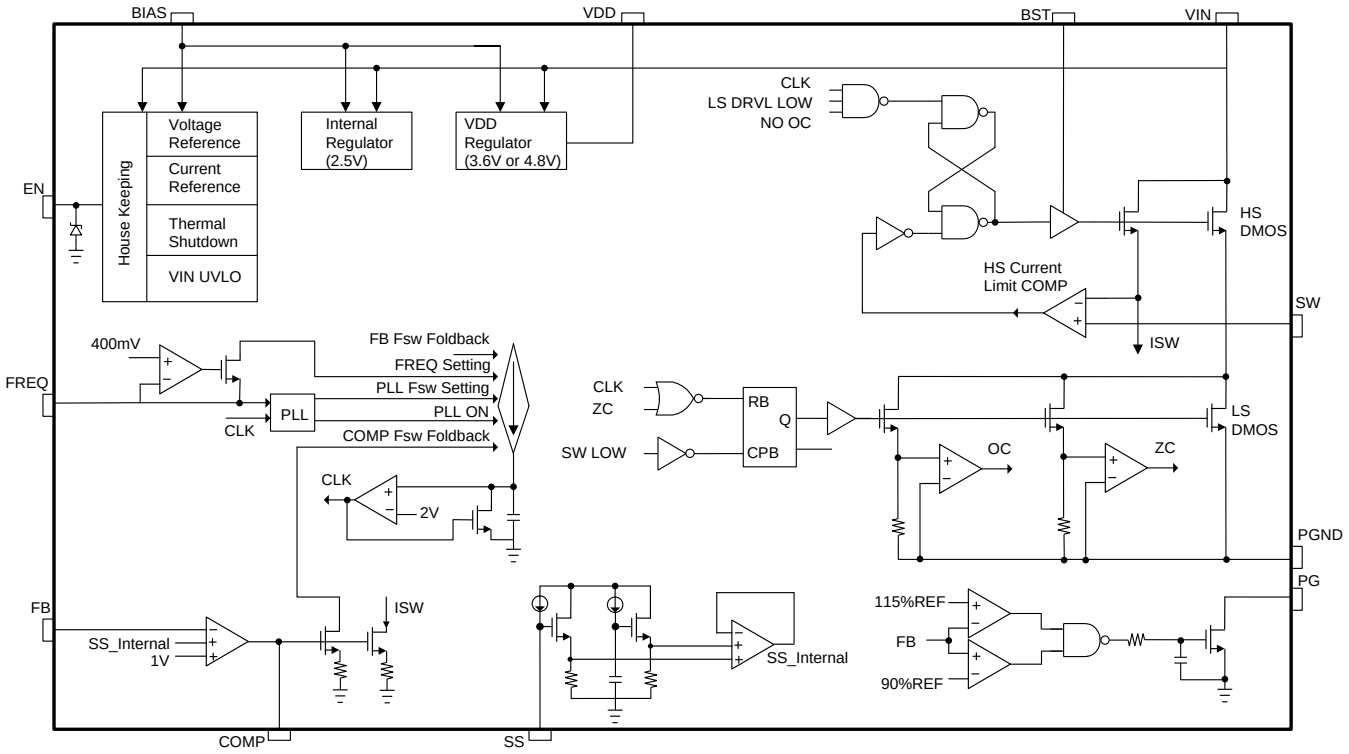

Figure 1 — Functional Block Diagram

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OPERATION

The MPQ4570 is a step-down switching regulator with integrated high-side high voltage power MOSFETs. It features as wide input voltage range, high efficiency, external internal soft-start, frequency programmable and comprehensive protection mode, i.e. OVP, OCP, OTP.

PWM Control

The MPQ4570 uses peak current mode control to regulate the output voltage.

A PWM cycle is initiated by the internal clock at the beginning of every cycle. After the high side MOSFET turns on, the inductor current will rise linearly to provide the energy to the load. The high side MOSFET remains on until its current hits the COMP voltage which is the output of the internal error amplifier (EA). The output voltage of error amplifier depends on the difference of output feedback voltage and the internal high precision reference and it will decide how much energy should be transferred to the load. The higher load current, the higher COMP voltage. After the high switch is off, the low side switch is on and the inductor current will flow through the low side switch. In order to avoid shoo-through issue, the dead time is inserted to avoid the high side and low side MOSFETS to turn on at the same time. For each turn on and off in a switching cycle, the high side MOSFET will keep on and off with minimum on and off time limit.

Light Load Operation

In order to get high efficiency, MPQ4570 has two features during light load: 1).When the load current decreases, the inductor current will drop at same time. The low side MOSFET will turn off in order to save driver loss when inductor current drops to zero. 2) When the load decreases, the switching frequency will be scaled down in order to reduce switching loss after COMP voltage drops down lower than certain threshold.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal reference and outputs a current proportional to the difference between the two. This current is used to charge the external compensation networks to form the COMP voltage, which is used to control the high side MOSFET peak current and to regulate the output voltage.

Oscillator and SYNC Function

The internal oscillator frequency is set by a single external resistor (R_{FREQ}) connected between FREQ pin and GND. The frequency setting resistor should be located close to the device. The relationship between oscillator frequency and R_{FREQ} refer to table 1 in APPLICATION INFORMATION section.

During light load, the switching frequency will be scalded down according to the COMP voltage. The switching frequency will start to decrease when the COMP voltage is lower than around 0.8V. And the switching will be disabled when the COMP voltage drops lower than around 0.7V.

In order to reduce the switching loss and the thermal dissipation, the switching frequency will be decreased according to the FB voltage. When the FB is lower than 25%xRFE, the switching frequency starts to decrease from the normal value, and finally drops to 5% of the normal value when the FB is zero.

The FREQ pin can be used to synchronize the internal oscillator rising edge to an external clock falling edge. Make sure the HIGH amplitude of SYNC clock is higher than 1.5V and LOW amplitude is lower than 1V to drive the internal logic. The recommended external SYNC frequency is in the range of 100kHz and 1MHz. There is no pulse width requirement but please note that there is always parasitic capacitance of the pad there, so, if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. The pulse longer than 100ns is recommended in application.

EN Control

EN is a control pin that turns the regulator on and off: Drive EN higher than 1.6V to turn on the regulator, drive it lower than 1.3V to turn off. There is no internal pull-up or pull-down at EN, so when it is floating, the EN status is uncertain.

The EN pin is clamped internally using a 6.5V zener diode between EN and GND, as shown in the functional block diagram. Connecting the EN pin directly to a voltage source without any pull-up resistor requires limiting voltage amplitude to ≤6V to prevent damage to the zener diode. EN pin can be connected to higher voltage (e.g. VIN) through pull-up resistor if the system doesn't

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have another logic signal acting as enable signal. Just make sure the pull-up resistor is high enough to make sure the sink current into EN pin less than 150uA to avoid damaging the zener diode. For example, when connecting EN to V_{IN}=12V, $R_{PULL-UP}$ ≥ (12V – 6.5V) ÷ 150μA = 37kΩ.

Soft Start

The soft start is implemented to ensure the smooth up output voltage during the power on and off. In addition, the soft start function also helps to reduce the inrush current value at the startup.

The soft start function is achieved by ramping SS up slowly and using SS to override the internal reference (REF) when SS-900mV is lower than REF. When SS-900mV is higher than REF, REF regains the control. The 900mV above is the offset voltage of SS which means SS is detected as 0 internally when it is lower than 900mV. To minimize the delay for SS to reach 0.9V, an internal pull-up circuit with about 30uA average current pulls SS up to 600mV first. Then use 4uA constant current to charge SS until it reaches to 2.5V. When SS is in the range of 0.9V to 1.9V, it overrides the REF as reference voltage of the error amplifier. During this period, output voltage ramps up from 0 to the regulated value following SS rising. The soft start time (t_{SS}) set by the external SS capacitor can be calculated by below formula:

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)}$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (1V), and I_{SS} is the $4\mu A$ SS charge current.

The delay time for SS reaches to 900mV can be estimated as below:

$$t_{SS_delay}(ms) = \frac{C_{SS}(nF) \times 0.6V}{30\mu A} + \frac{C_{SS}(nF) \times 0.3V}{4\mu A}$$

There is also an internal fixed 500us soft start. The final SS time is determined by the longer time between 500μs and external SS setting time.

When output voltage is shorted to GND, feedback voltage is pulled to low then the SS will be discharged. The part will soft start again when the short at output is removed.

Internal Regulator and BIAS

There is an internal 2.5V regulator powers all the internal control circuits. The 2.5V regulator takes VIN as power supply when BIAS pin is lower than 3.2V while supplies from BIAS when BIAS is higher than 3.2V.

VDD regulator powers LS driver and also BST regulator when it is higher than 4.5V. VDD is powered from VIN when BIAS is floating and regulated at 3.6V. When BIAS is higher than 4.2V, it starts to power VDD. VDD will increases as BIAS rising with 600mV voltage drop and regulated at 4.8V when BIAS is higher than 5.4V. A 1μF decoupling capacitor is needed at the pin and make the capacitor as close to the pin as possible.

Using BIAS to power internal regulator can improve the efficiency. It is recommended to connect BIAS to an external power supply that is in the range of 3.3V to 5.5V. Output voltage is a good choice for this power supply if it is in above range. A 0.1μF to 1μF decoupling capacitor at the pin is recommended.

Over Voltage Protection

The MPQ4570 monitors the feedback output voltage to achieve the over voltage protection. If the FB voltage is higher than the 115%xREF, the high side and low side MOSFET will be turned off immediately, the PG signal will be asserted to inform the fault status. High side and low side MOSFET will resume switching following close loop operation after FB voltage drops back to lower than 103%xREF.

Over Current Protection

The MPQ4570 has cycle-by-cycle peak current limit protection and valley current detection protection. The inductor current is monitored during the high side MOSFET on state. If the inductor current exceeds the current limit value set by COMP voltage, the high side MOSFET turns off immediately. Then, the low side MOSFET will be turned on to discharge the energy and inductor current will decrease. The high side MOSFET will not be on again unless the inductor valley current is lower than a certain current threshold which is called the valley current limit. It is very useful to avoid the inductor current to run away. Also, both the peak current limit and the valley current limit value are

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dependent on the FB voltage. If the feedback output voltage is higher than the 50%xREF, the current limit value is as the normal value. If the feedback output voltage is lower than 50%xRFF, the current limit will decrease and drop to the half normal value when the feedback output voltage is zero. This feature is very helpful to reduce the OCP thermal dissipation which may especially get worse when the output voltage is shorted. Also, it is very helpful to reduce the high inrush current during the startup.

UVLO Protection

The MPQ4570 has input under voltage lockout protection (UVLO). Assuming the EN is active, the MPQ4570 is powered on when the input voltage is higher than the UVLO rising threshold and is powered off when input voltage drops below the UVLO falling threshold.

Thermal Shutdown Protection

The thermal shutdown is employed in MPQ4570 by monitoring the IC temperature internally. If the junction temperature exceeds the threshold (typically 170°C), the regulator shuts off and it will turns on again when the temperature drops below 160°C. There is a ~10°C hysteresis.

Power Good

MPQ4570 has one power good (PG) pin out to indicate the normal operation after soft start time. The PG pin is the open drain of an internal MOSFET. It should be connected to VDD or external voltage source through a resistor (i.e. 100kohm). After the input voltage is applied, the MOSFET is turned on and the PG pin is pulled to GND before SS is ready. After the FB voltage reaches 90% REF voltage, the MOSFET turns off and PG pin is pulled to high by external voltage source. When the FB voltage drops to 85% REF voltage, the PG voltage is pulled to GND to indicate a failure output status.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor (0.1μF typically) between BST pin and SW pin powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.3V with a hysteresis of 300mV. The driver's UVLO is soft-start related: When the bootstrap voltage hits its UVLO threshold, the soft-start circuit resets. When bootstrap UVLO is gone, the reset is off and then the soft-start process resumes.

The dedicated internal bootstrap regulator regulates and charges the bootstrap capacitor to 4.2V. When the voltage between the BST and SW nodes is less than its regulation, a PMOS pass transistor from VIN to BST turns ON. The charging current path is from VIN, BST and then to SW.

As long as V_{IN} is sufficiently higher than V_{SW}, the bootstrap capacitor can be charged. When the high side MOSFET is ON, $V_{IN} \approx V_{SW}$ so the bootstrap capacitor can't be charged. When low side MOSFET is ON, the difference between V_{IN} and V_{SW} is at its largest, thus making it the best period to charge. When there is no current in the inductor, $V_{SW}=V_{OUT}$ so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

At higher duty cycles, the time period available for bootstrap charging is shorter so the bootstrap capacitor may not be sufficiently charged. If the internal circuit does not have sufficient voltage and the bootstrap capacitor is not charged, extra external circuitry can be used to ensure the bootstrap voltage is within the normal operational region.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Switching Frequency

The MPQ4570 has an externally adjustable frequency. The switching frequency (f_{SW}) can be set using a resistor at FREQ pin (R_{FREQ}). The recommended R_{FREQ} values for various f_{SW} see table1. Refer to f_{SW} vs. R_{FREQ} curve in TYPICAL CHARACTERISTICS section for more detailed values.

Table 1 — f_{SW} vs. R_{FREQ}

f_{SW} (kHz)	R_{FREQ} (kΩ)
1000	47.5
900	56
800	63.4
700	73.2
600	84.5
500	102
400	133
300	178
200	261
100	523

Setting the Output Voltage

A resistive voltage divider from the output voltage to FB pin sets the output voltage. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB}=V_{OUT}\times\frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT}=V_{FB}\times\frac{R1+R2}{R2}$$

For example, the value for R1 can be 10kΩ. With this value, R2 is:

$$R2=\frac{10}{V_{OUT}-1}k\Omega$$

So for a 3.3V output voltage, R1 is 10kΩ, and R1 is 4.32kΩ.

Inductor

The inductor provides constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in lower ripple current that will lower the output ripple voltage. However, a larger inductor value will be physically larger, have higher series resistance, or lower saturation current.

To determine the inductance, allow the inductor's peak-to-peak ripple current to approximately equal 30% of the maximum switch current limit. Make sure that the peak inductor current is less than the maximum switch current limit. The inductance value can be calculated by:

$$L1=\frac{V_{OUT}}{f_{SW}\times\Delta I_L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated by:

$$I_{LP}=I_{LOAD}+\frac{V_{OUT}}{2\times f_{SW}\times L1}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Input Capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use capacitors with low equivalent series resistances (ESR) for the best performance. Ceramic capacitors are best, but tantalum or low-ESR electrolytic capacitors may also suffice.

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor (C1) can be electrolytic, tantalum, or ceramic.

When using electrolytic or tantal

um capacitors, place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance is approximately:

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$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Low-ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the ESR value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and contributes the most to the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple is approximately:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4570 can be optimized for a wide range of capacitances and ESR values.

Compensation Components

MPQ4570 employs current-mode control for easy compensation and fast transient response. The COMP pin controls the system stability and transient response. The COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the control system's characteristics. The DC gain of the voltage feedback loop is:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where A_{VEA} is the error-amplifier voltage gain, 1000V/V; G_{CS} is the current-sense transconductance, 12A/V; R_{LOAD} is the load resistor value.

The system has two important poles: One from the compensation capacitor (C3) and the output resistor of error amplifier, and the other due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where, G_{EA} is the error-amplifier transconductance, 630μA/V.

The system has one important zero due to the compensation capacitor and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C4) and the compensation resistor can compensate for the effect of the ESR zero. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C4 \times R3}$$

The goal of compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important: Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies lead to system instability. Generally, set the crossover frequency to ~0.1×f_{SW}.

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Follow these steps to design the compensation:

1. Choose R3 to set the desired crossover frequency:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency.

2. Choose C3 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero (f_{Z1}) <0.25 ×f_C to provide sufficient phase margin. C3 is then:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

3. C4 is required if the ESR zero of the output capacitor is located at <0.5×f_{SW}, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_{SW}}{2}$$

If this is the case, use C4 to set the pole (f_{P3}) at the location of the ESR zero. Determine the C4:

$$C4 = \frac{C2 \times R_{ESR}}{R3}$$

External Bootstrap Diode

For high duty-cycle operation (when V_{OUT}/V_{IN} > 65%), the time period available to the bootstrap charging is less so the bootstrap capacitor may not be charged sufficiently. This affects the efficiency, even the normal operation of the part. An external bootstrap diode from 3V-5V rail to the BST pin can help to charge the bootstrap capacitor and enhance the efficiency. Output voltage is the good choice of this power supply if it is in above range. The bootstrap diode can be a low cost one such as IN4148.

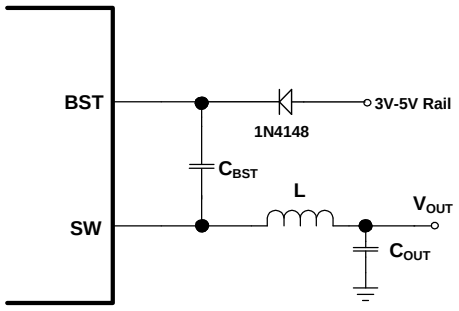

Figure 2 — External Bootstrap Diode

At no-load or light-load, the converter may operate in pulse-skipping mode in order to maintain output-voltage regulation. Under this condition, V_{SW}= V_{OUT} in most time period, so the diode from V_{OUT} to BST can't charge the bootstrap capacitor. For sufficient gate voltage during pulse-skipping, V_{IN}–V_{OUT} should be no less than 3V. For example, if the V_{OUT}=3.3V, V_{IN} must exceed 3.3V+3V=6.3V to maintain sufficient bootstrap voltage at no-load or light-load. To meet this requirement, the EN pin can program the input UVLO voltage to V_{OUT}+3V

PCB Layout Guide

PCB layout is very important to stable operation. Please follow below guidelines and use figure 3 as reference.

1) Place the ceramic input capacitor as close to IN and GND pins as possible, especially the small package size (0603) input bypass capacitor. Keep the connection of input capacitor and IN pin as short and wide as possible.

2) Place the VDD capacitor to VDD pin and GND pin as close as possible.

3) Use large ground plane directly connect to GND pin. Add vias near the GND pin if bottom layer is ground plane.

4) Route SW, BST away from sensitive analog areas such as FB.

5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.

6) Connect IN, SW, and especially GND and exposed pad to large copper areas to cool the chip for improved thermal performance and long-term reliability.

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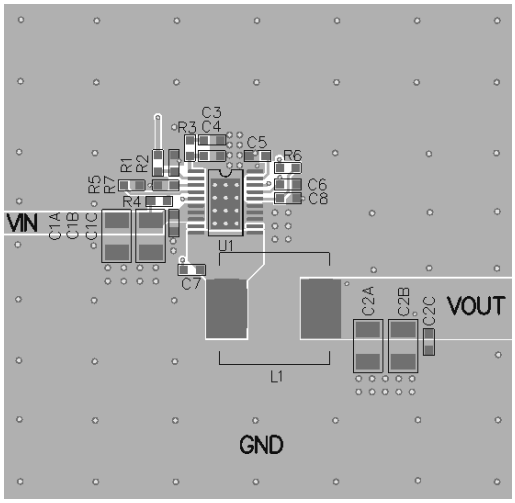
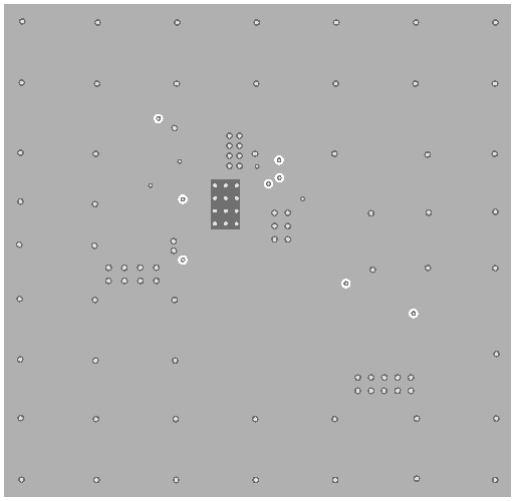
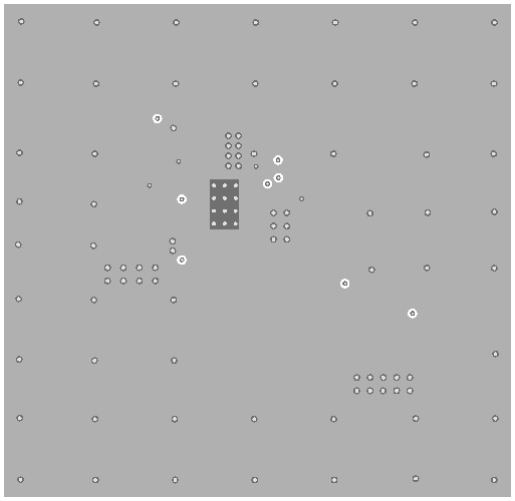


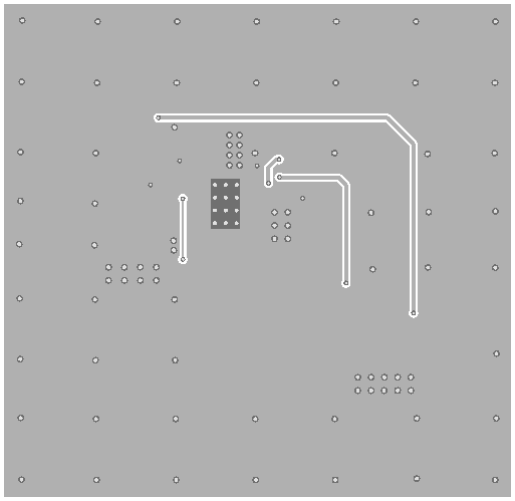
Top Layer



Bottom Layer



Inner 1 Layer



Inner 2 Layer

Figure 3 – Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

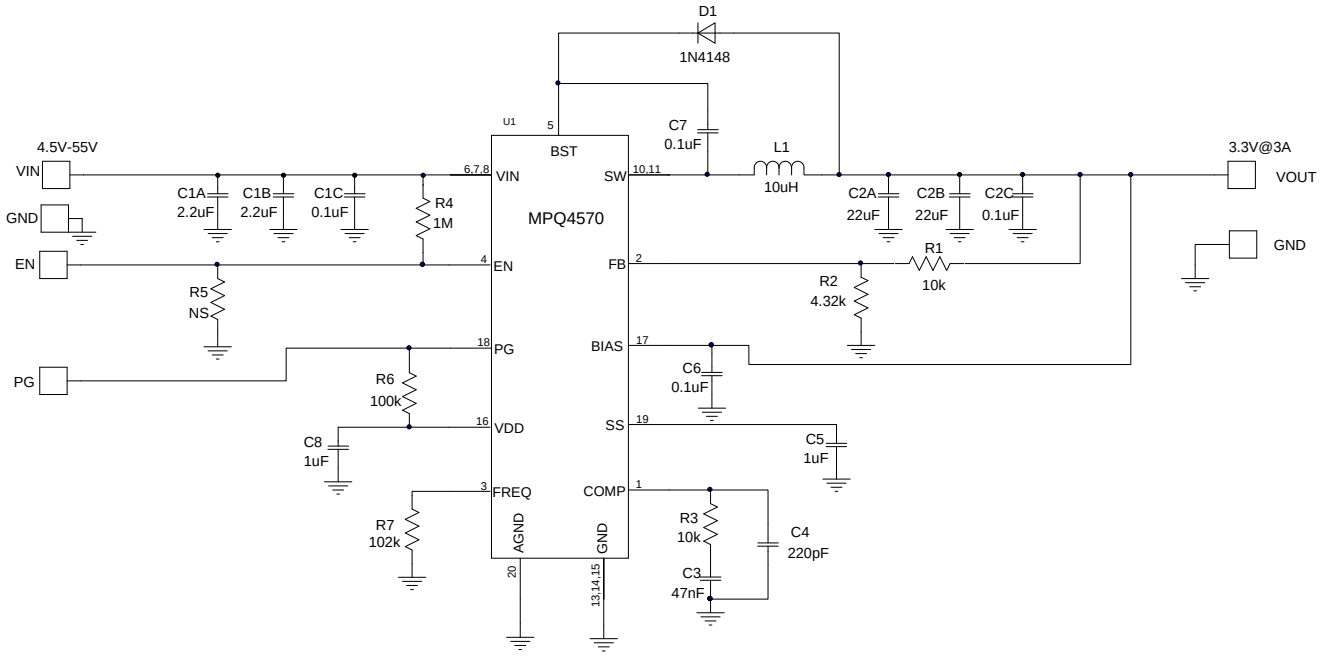

Figure 4 – 3.3V Output Typical Application Circuit

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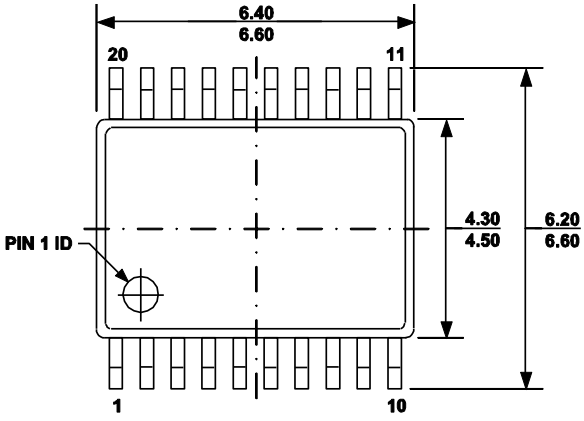
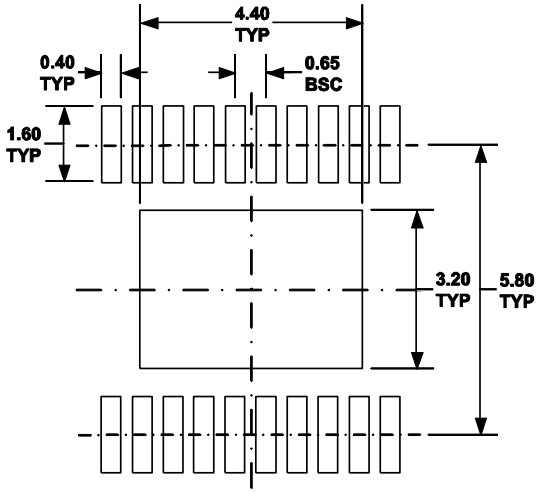
PACKAGE INFORMATION

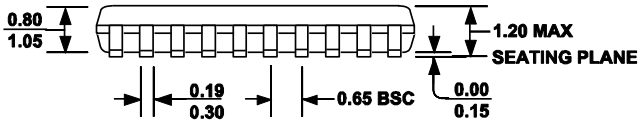
TSSOP-20 EP
(EXPOSED PAD)



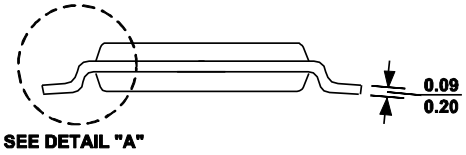
TOP VIEW



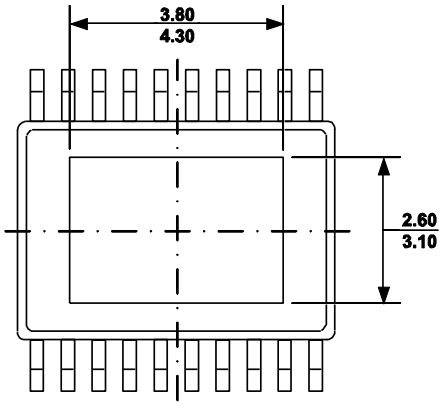
RECOMMENDED LAND PATTERN



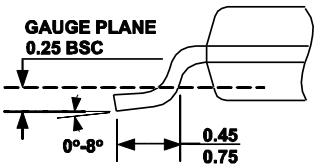
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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