MPQ4569A

75V, 0.3A, Synchronous, Step-Down Converter AEC-Q100 Qualified

DESCRIPTION

The MPQ4569A is a step-down, switching regulator with integrated high-side and low-side, high-voltage power MOSFETs. The MPQ4569A provides a highly efficient output of up to 0.3A.

The wide 4.5V to 75V input range accommodates a variety of step-down applications in automotive environment. The 5μA shutdown mode quiescent current in full temperature range is sufficient for battery-powered applications.

The MPQ4569A allows for high-power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driver losses.

The switching frequency during start-up and short circuit also can be scaled down to prevent inductor current runaway. Thermal shutdown provides reliable and fault-tolerant operation.

The MPQ4569A is available in a QFN-10 (3mmx3mm) package.

FEATURES

- 20μA Quiescent Current (Active Mode)
- Wide 4.5V to 75V Operating Input Range
- 1.2Ω/0.5Ω Internal Power MOSFETs
- Programmable Soft Start (SS)
- FB Tolerance: 1% at Room Temperature, 2% at Full Temperature
- Adjustable Output
- 1V Reference Voltage Output
- Low Shutdown Mode Current: 5μA
- Internal EN Pull-Up
- Available in a QFN-10 (3mmx3mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery-Powered Systems

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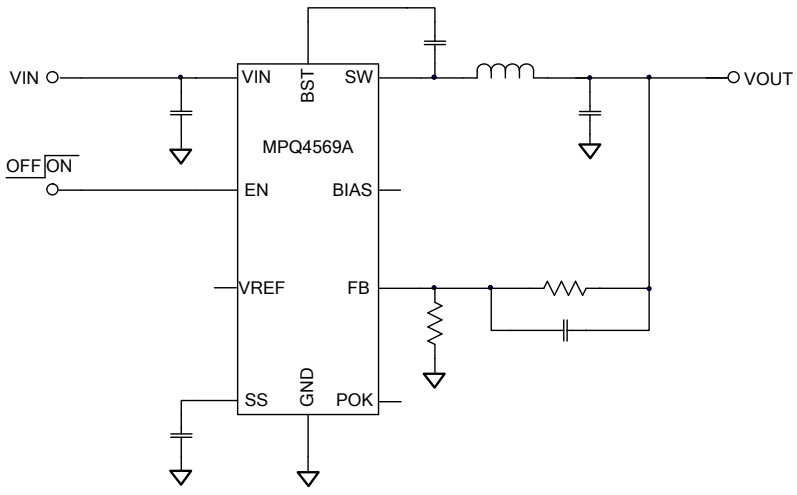
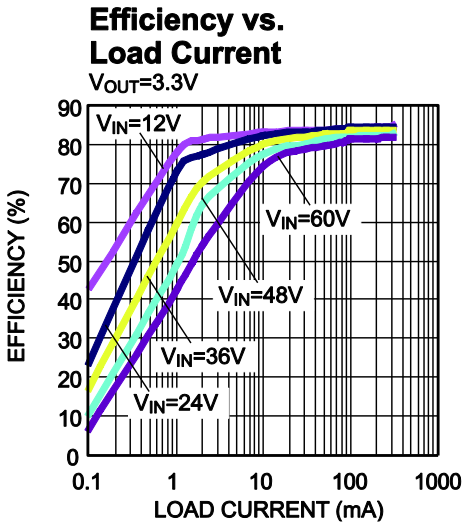
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ4569AGQ	QFN-10 (3mmx3mm)	*See Below*
MPQ4569AGQ-AEC1		

* For Tape & Reel, add suffix –Z (e.g. MPQ4569AGQ–Z)

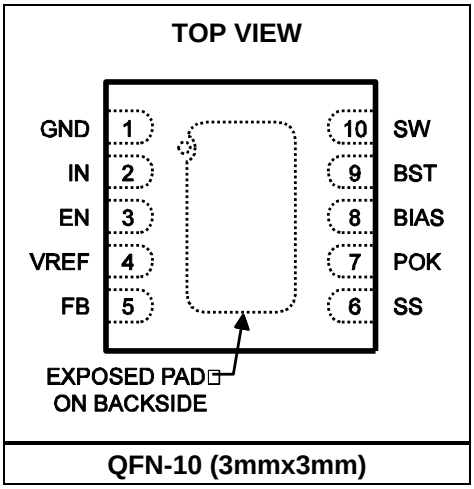
TOP MARKING

ANEY

LLL

ANE: Product code of MPQ4569AGQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-10 (3mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +80V
Switch voltage (V_{SW}) .....-0.3V to V_{IN} + 1V
BST to SW .....-0.3 to +6.0V
All other pins .....-0.3V to +6.0V
EN sink current 150µA
Continuous power dissipation (T_A = +25°C) (2)
QFN-10 (3mmx3mm) 2.5W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature .....150°C

Recommended Operating Conditions

Supply voltage (V_{IN}) .....4.5V to 75V
Output voltage (V_{OUT}) .....1V to 0.9xV_{IN}
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (3) θ_{JA} θ_{JC}

QFN-10 (3mmx3mm)..... 50..... 12... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C, unless otherwise noted, typical values at T_J = +25°C.

Parameter	Condition	Min	Typ	Max	Units
Supply quiescent current	No load, V_{FB} = 1.2V		20	30	µA
Shutdown supply current	V_{EN} < 0.3V		2.2	5	µA
V_{IN} UVLO rising threshold		3.9	4.2	4.4	V
V_{IN} UVLO falling threshold		3.45	3.75	3.95	V
V_{IN} UVLO hysteresis			0.45		V
Feedback voltage	V_{IN} = 4.5V to 75V, T_J = 25°C	0.99	1	1.01	V
	V_{IN} = 4.5V to 75V	0.98		1.02	V
Feedback current	V_{FB} = 1.2V	-50	2	50	nA
VREF voltage	V_{IN} = 4.5V to 75V, I_{REF} = 100µA	0.965	1	1.035	V
Upper switch on resistance	V_{BST} - V_{SW} = 5V, T_J = 25°C	0.9	1.2	1.5	Ω
	V_{BST}-V_{SW} = 5V	0.7		2.5	Ω
Lower switch on resistance	V_{BIAS} = 5V, T_J = 25°C	0.375	0.5	0.625	Ω
	V_{BIAS} = 5V	0.3		1	Ω
Lower switch leakage	V_{EN} = 0V, V_{SW} = 75V			1	µA
Peak current limit		640	720	800	mA
Minimum switch on time (4)			115		ns
Enable rising threshold		1.4	1.55	1.7	V
Enable falling threshold		1.152	1.2	1.248	V
Enable threshold hysteresis			0.35		V
Enable current	V_{EN} = 2.4V, source current		0.75	2	µA
Soft start current		4	5	6	µA
POK upper trip threshold	FB with respect to the nominal value	86	90	94	%
POK lower trip threshold	FB with respect to the nominal value	81	85	89	%
POK threshold hysteresis	FB with respect to the nominal value		5		%
POK deglitch timer			40		µs
POK output voltage low	I_{SINK} = 1mA			0.4	V
FB OVP rising threshold			1.05	1.1	V
FB OVP hysteresis			50		mV
Thermal shutdown (4)			175		°C
Thermal shutdown hysteresis (4)			20		°C

NOTE:

4) Derived from bench characterization, not tested in production.

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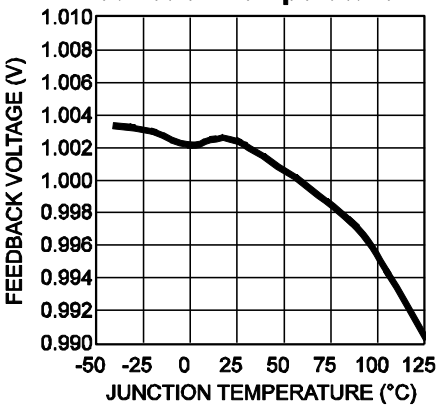
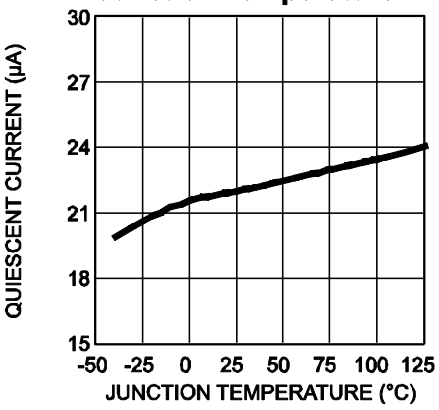
TYPICAL CHARACTERISTICS

V_{IN} = 12V, unless otherwise noted.

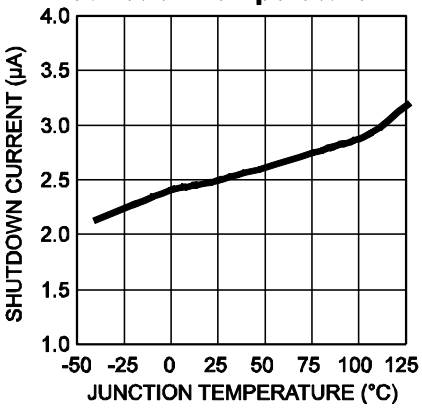
Feedback Voltage vs. Junction Temperature



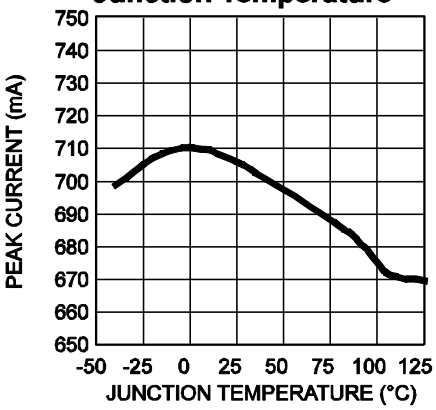
Quiescent Current vs. Junction Temperature



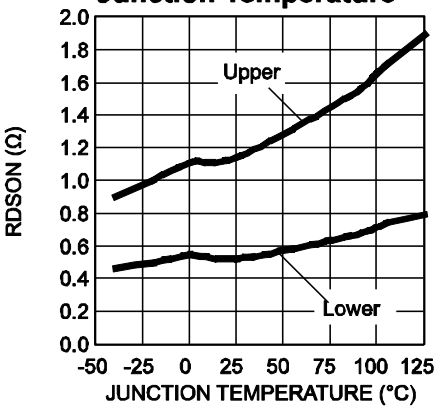
Shutdown Current vs. Junction Temperature



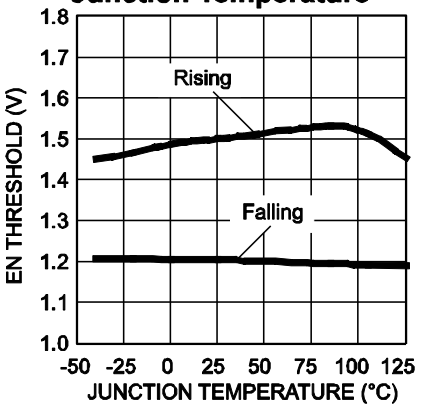
Current Limit vs. Junction Temperature



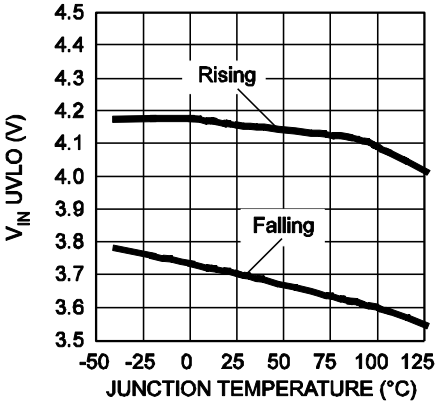
Switch On Resistance vs. Junction Temperature



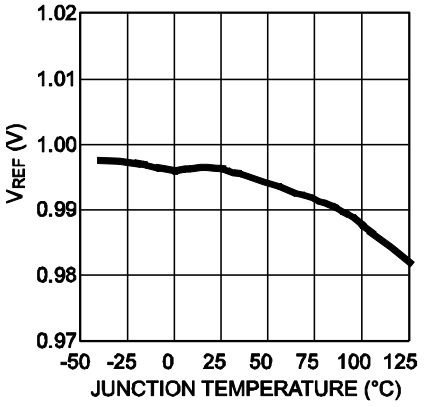
EN Threshold vs. Junction Temperature



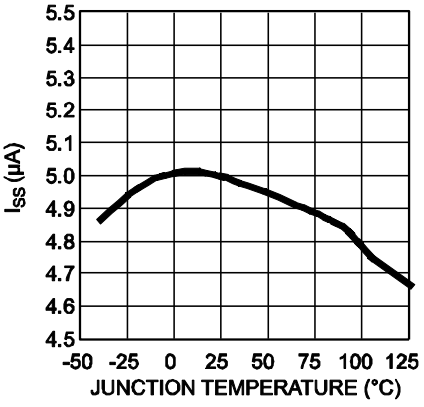
V_{IN} UVLO vs. Junction Temperature



V_{REF} vs. Junction Temperature



I_{SS} vs. Junction Temperature



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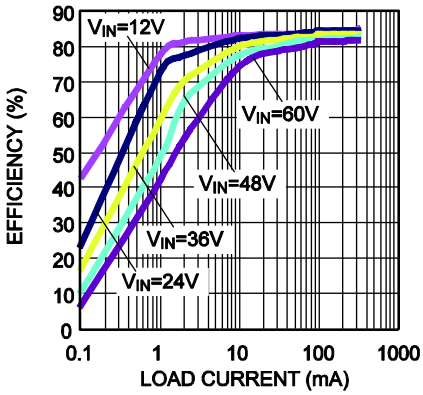
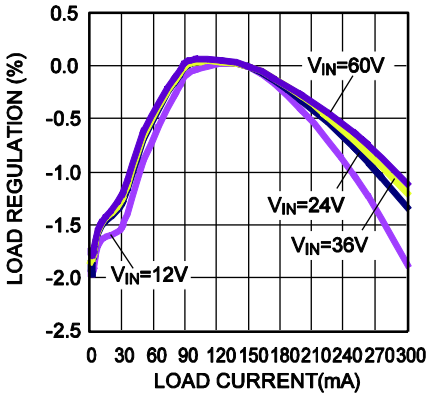
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 33µH, C_{OUT} = 2 x 22µF, T_A = +25°C, unless otherwise noted.

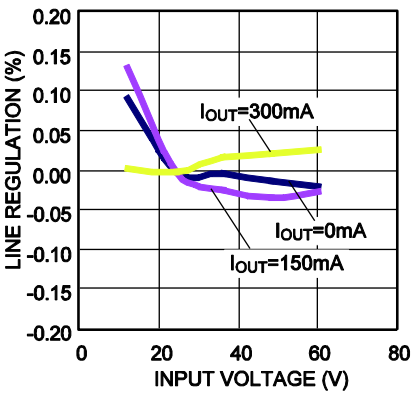
Efficiency vs. Load Current



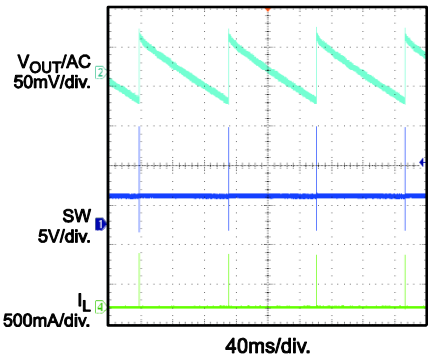
Load Regulation



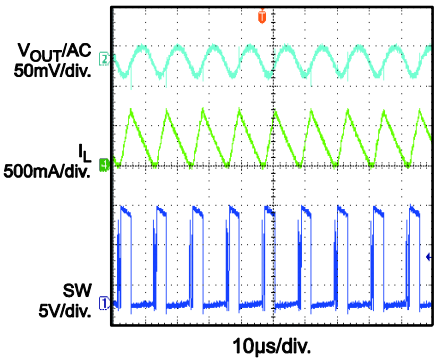
Line Regulation



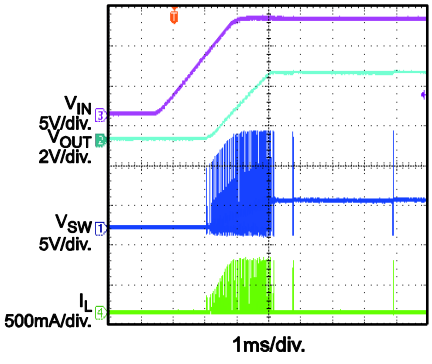
Steady State
I_{OUT}=0A



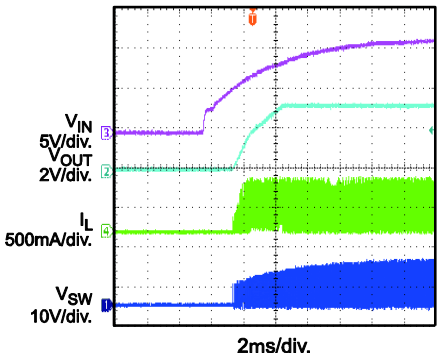
Steady State
I_{OUT}=0.3A



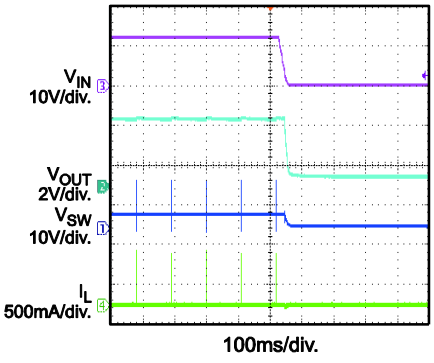
Start-Up Through V_{IN}
I_{OUT} = 0A



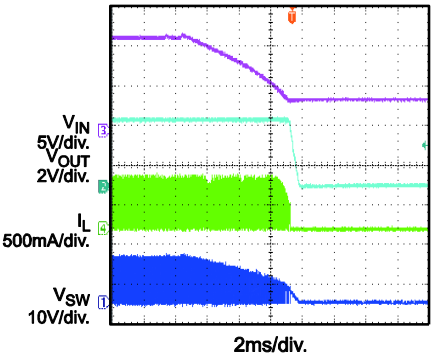
Start-Up Through V_{IN}
I_{OUT} = 0.3A



Shutdown Through V_{IN}
I_{OUT} = 0A



Shutdown Through V_{IN}
I_{OUT} = 0.3A



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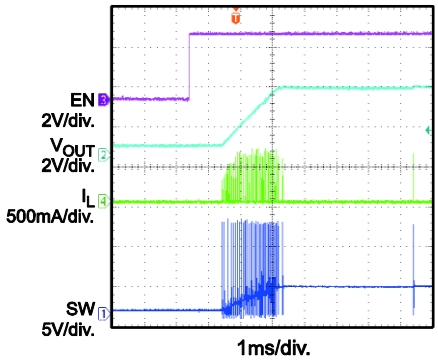
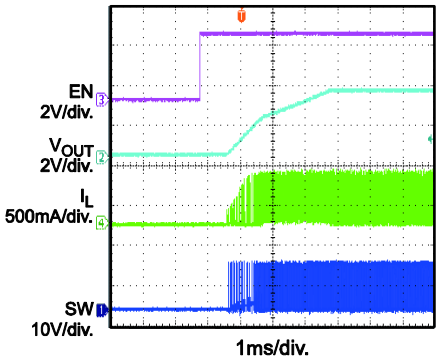
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 33µH, C_{OUT} = 2 x 22µF, T_A = +25°C, unless otherwise noted.

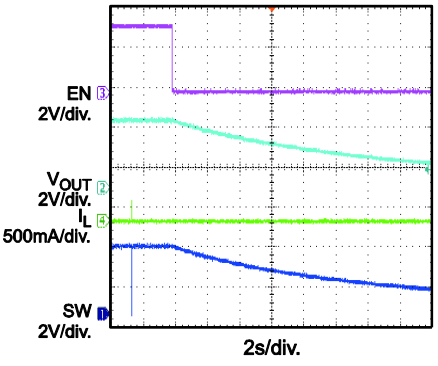
Start-Up Through EN
I_{OUT} = 0A



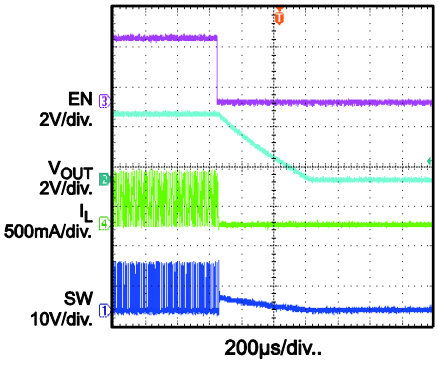
Start-Up Through EN
I_{OUT} = 0.3A



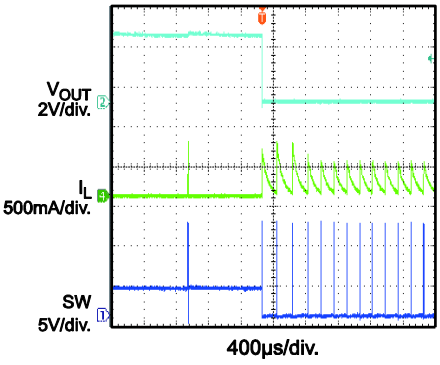
Shutdown Through EN
I_{OUT}=0A



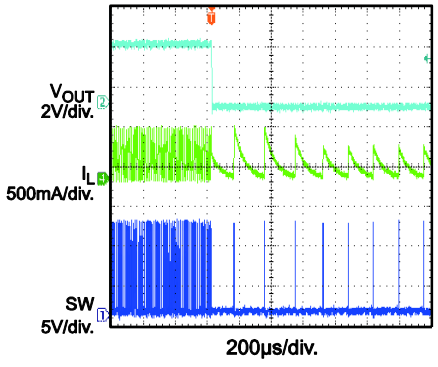
Shutdown Through EN
I_{OUT}=0.3A



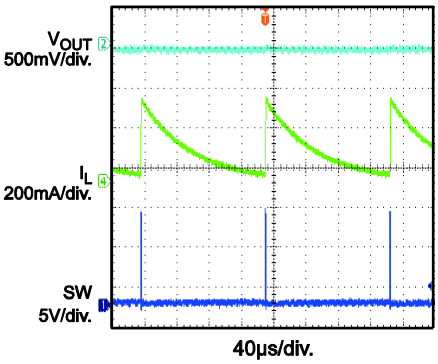
SCP Entry
I_{OUT}=0A to Short Circuit



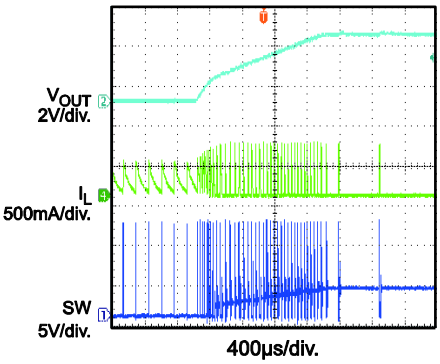
SCP Entry
I_{OUT}=0.3A to Short Circuit



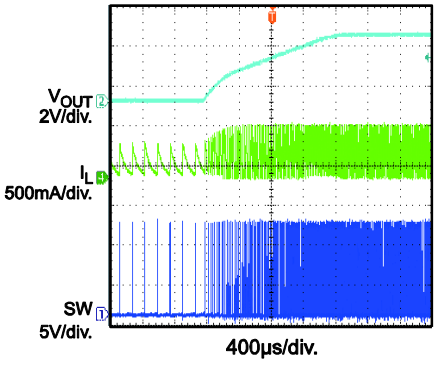
SCP Steady State



SCP Recovery
Short Circuit to I_{OUT}=0A



SCP Recovery
Short Circuit to I_{OUT}=0.3A



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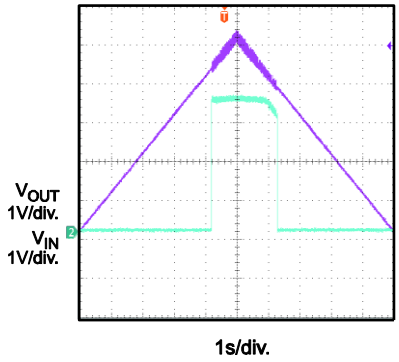
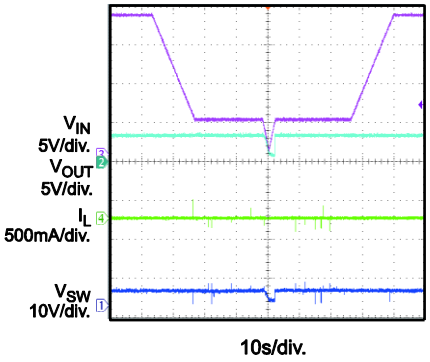
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 33µH, C_{OUT} = 2 x 22µF, T_A = +25°C, unless otherwise noted.

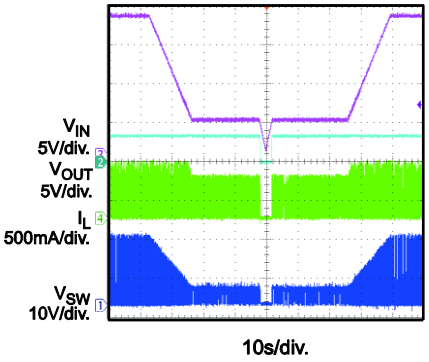
V_{IN} Ramp Up and Down
I_{OUT}=0.3A



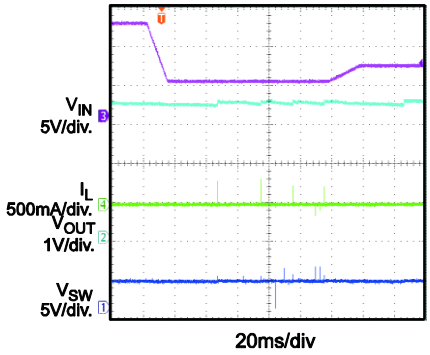
V_{IN} Ramp Up and Down
V_{IN}=18V->4.5V->0V->4.5V->18V,I_{OUT}=0A



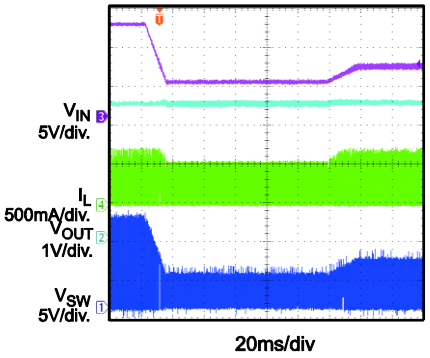
V_{IN} Ramp Up and Down
V_{IN}=18V->4.5V->0V->4.5V->18V,I_{OUT}=0.3A



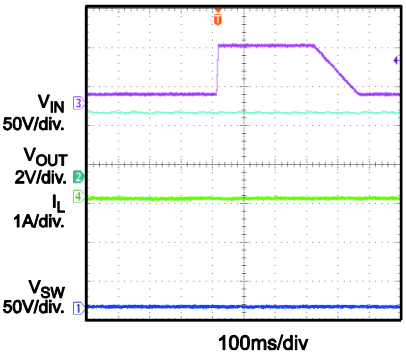
Cold Crank
V_{IN}=12V->4.5V->6.5V,I_{OUT}=0A



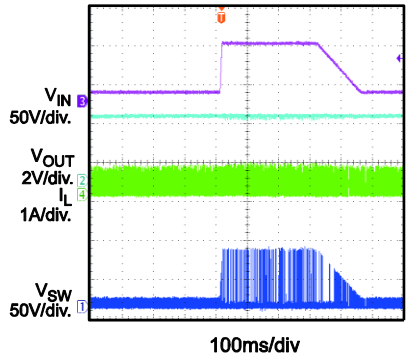
Cold Crank
V_{IN}=12V->4.5V->6.5V,I_{OUT}=0.3A



Load Dump
V_{IN}=12<->75V, V_{OUT}=3.3V,I_{OUT}=0A



Load Dump
V_{IN}=12<->75V, V_{OUT}=3.3V, I_{OUT}=0.3A



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PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.** Connect the output capacitor as close to GND as possible to avoid high-current switch paths.
2	IN	**Input supply.** A decoupling capacitor to ground is required to reduce switching spikes.
3	EN	**Enable input.** Pull EN below the low threshold to shut down the MPQ4569A. Pull EN above the high threshold or leave EN floating to enable the chip.
4	VREF	**Reference voltage output.**
5	FB	**Feedback.** FB is connected to the tap of an external resistive divider between the output and GND. FB sets the regulation voltage when compared to the internal 1V reference.
6	SS	**Soft-start control input.** Connect a capacitor from SS to GND to set the soft-start period.
7	POK	**Open-drain power good output.** POK at a high output indicates that V_{OUT} is higher than 90% of reference. POK is pulled down during shutdown.
8	BIAS	**Controller bias input.** BIAS supplies current to the internal circuit when V_{BIAS} is larger than 2.9V.
9	BST	**Bootstrap.** BST is the positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
10	SW	**Switch node.**

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BLOCK DIAGRAM

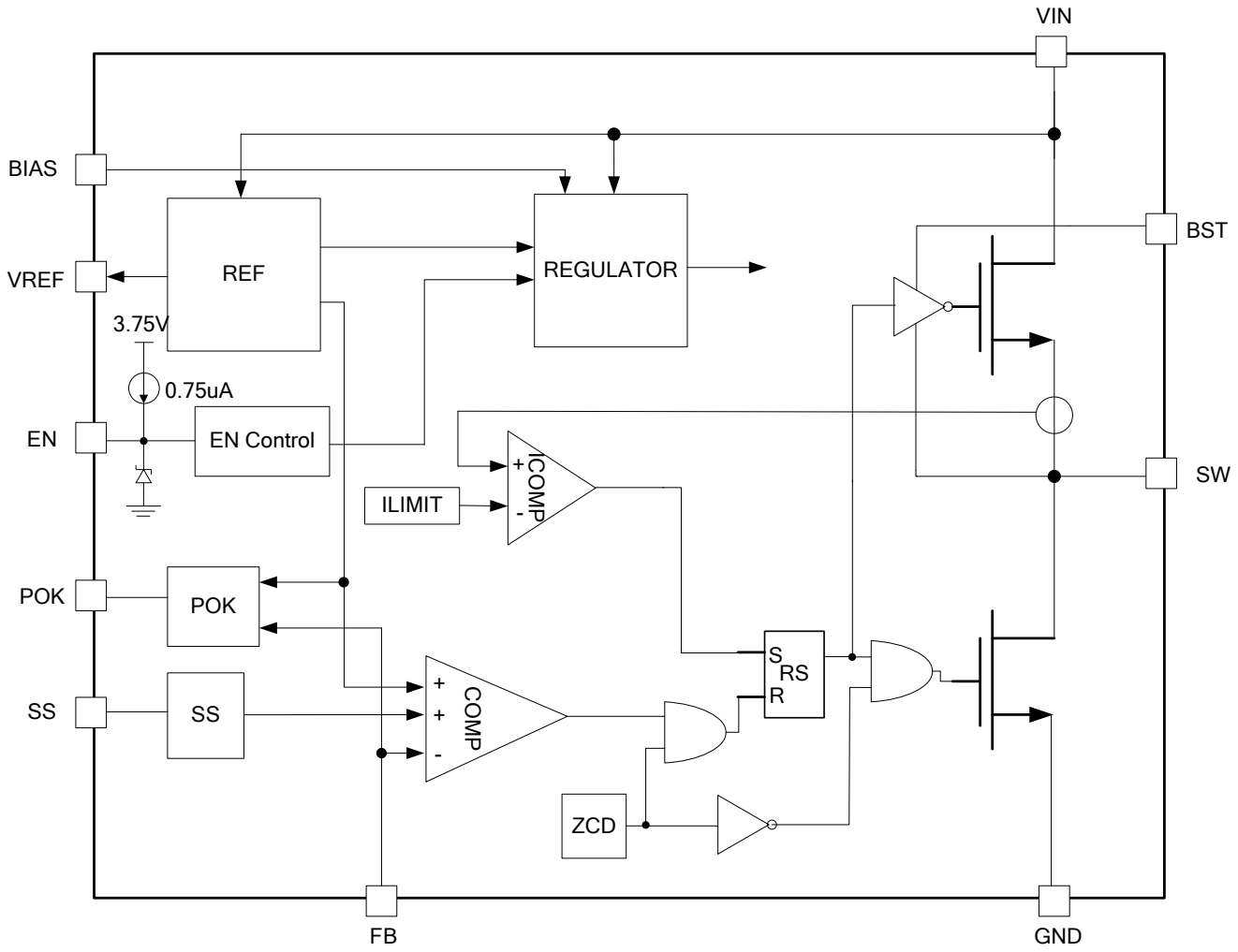

Figure 1: Functional Block Diagram

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OPERATION

The MPQ4569A is a 75V, 0.3A, synchronous, step-down, switching regulator with integrated high-side and low-side, high-voltage, power MOSFETs (HS-FET, LS-FET). The MPQ4569A has a highly efficient 0.3A output and features a wide input voltage range, external soft-start control, and precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

Control Scheme

The ILIM comparator, FB comparator, and zero current detector (ZCD) block control the pulse-width modulation (PWM). If the FB voltage (V_{FB}) is below the 1V reference and the inductor current drops to zero, the HS-FET turns on, and the ILIM comparator starts to sense the HS-FET current: When the HS-FET current reaches the limit, the HS-FET turns off, and the LS-FET turns on with the ZCD block. Meanwhile, the ILIM comparator is turned off to reduce the quiescent current. The LS-FET turns off with the ZCD block after the inductor current drops to zero. If V_{FB} is less than the 1V reference at this time, the HS_FET turns on immediately and begins another cycle. If V_{FB} is still higher than the 1V reference, the HS-FET does not turn on until V_{FB} drops below 1V (see Figure 2).

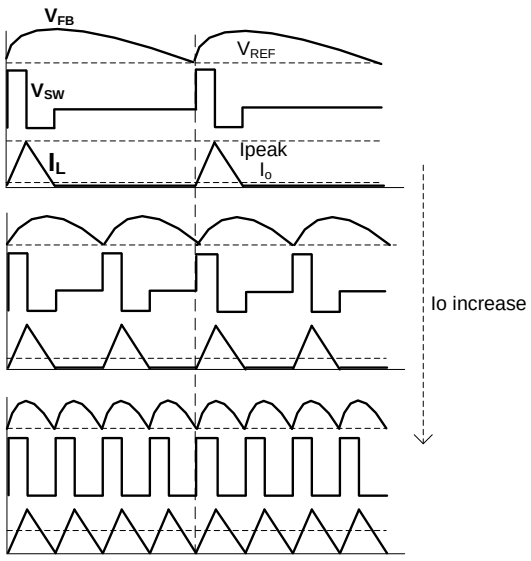

Figure 2: Control Scheme

Internal Regulator and BIAS

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} is greater than 3.0V, the output of the regulator is in full regulation. Lower values of V_{IN} result in lower output voltages. When V_{BIAS} is larger than 2.9V, the bias supply overrides the input voltage and supplies power to the internal regulator. When V_{BIAS} is larger than 4.5V, it can power the LS-FET driver. Using BIAS to power the internal regulator can improve efficiency. It is recommended to connect BIAS to the regulated output voltage when it is in the range of 2.9V to 5.5V. When output voltage is out of this range, an external supply (>2.9V, ideally >4.5V) can be used to power BIAS.

Enable Control (EN)

The MPQ4569A has a dedicated enable control pin (EN). When V_{IN} goes high, EN enables and disables the chip (high logic). Its trailing threshold is a consistent 1.2V, and its rising threshold is about 350mV higher.

When floating, EN is pulled up to about 3.75V by an internal 0.75µA current source and is enabled. To pull EN down, a 0.75µA current capability is needed. When EN is 0V, the chip goes into the lowest shutdown-current mode. When EN is higher than zero but lower than its rising threshold, the chip remains in shutdown mode with a slightly larger shutdown current.

Under-Voltage Lockout (UVLO)

V_{IN} under-voltage lockout (UVLO) protects the chip from operating below the operational supply voltage range. The UVLO rising threshold is about 4.2V, while its trailing threshold is about 3.75V.

Soft Start (SS)

Reference-type soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a constant current to charge external SS capacitor. The soft-start voltage (V_{SS}) slowly ramps up from 0V at a slow pace set by the soft-start time. When V_{SS} is less than the V_{REF}, V_{SS} overrides V_{REF}, so the FB comparator uses V_{SS} instead of V_{REF} as the reference. When V_{SS} is higher than V_{REF}, V_{REF} resumes control.

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V_{SS} is also associated with V_{FB}. Though V_{SS} can be much smaller than V_{FB}, it can only barely exceed V_{FB}. If V_{FB} drops somehow, V_{SS} tracks V_{FB}. This function prevents output voltage overshoot in short-circuit recovery. When the short circuit is removed, SS ramps up as if it is a fresh soft-start process.

Thermal Shutdown

Thermal shutdown prevents the chip from running away thermally. When the silicon die temperature exceeds its upper threshold, the thermal shutdown feature shuts down the entire chip. When the temperature falls below its lower threshold, the chip resumes function.

Floating Driver and Bootstrap Charging

The external bootstrap capacitor powers the floating HS-FET driver. This floating driver has its own UVLO protection with a rising threshold of about 2.4V and a hysteresis of about 300mV. During this UVLO, V_{SS} resets to zero. When UVLO is disabled, the regulator follows the soft-start process.

The dedicated internal bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage difference between BST and SW falls below its working parameters, a P-channel MOSFET (P-FET) pass transistor connected from V_{IN} to BST turns on to charge the bootstrap capacitor. The current path is from V_{IN} to BST to SW. The external circuit must have enough voltage headroom to accommodate charging.

As long as V_{IN} is sufficiently higher than SW, the bootstrap capacitor can charge. When the HS_FET is ON, V_{IN} is about equal to SW so the bootstrap capacitor cannot charge. The best charging period occurs when the LS-FET is on so that V_{IN} - V_{SW} is at its largest. When there is no current in the inductor, V_{SW} is equal to V_{OUT}, so the difference between V_{IN} and V_{OUT} can charge the bootstrap capacitor.

If the internal circuit does not have sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operation region.

Start-Up and Shutdown

If both V_{IN} and V_{EN} are higher than their appropriate thresholds, the chip starts operating. The reference block starts first, generating a stable reference voltage and current and then enables the internal regulator. The regulator provides a stable supply for the rest of the device.

While the internal supply rail is high, an internal timer holds the power MOSFET off for about 50µs to blank start-up glitches. When the soft-start block is enabled, it first holds its SS output low and then ramps up slowly.

Three events can shut down the chip: V_{EN} low, V_{IN} low, and the junction temperature triggers the thermal shutdown threshold. During shutdown, the signaling path is blocked first to avoid any fault triggering. The internal supply rail is then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power OK (POK)

POK is an open-drain power good output. A high output indicates that V_{OUT} is higher than 90% of its nominal value. POK is pulled down during shutdown mode.

Reference Voltage Output (VREF)

VREF outputs a 1V reference voltage. VREF has up to 500µA of source current capability.

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APPLICATION INFORMATION

Selecting the Inductor

Since the peak current (I_{peak}) is fixed, for a given input voltage and output voltage, the inductor value can be determined with Equation (1):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{peak} \times f_s} \quad (1)$$

Where f_s is the switching frequency at the maximum output current.

A larger inductor value results in lower switching frequency and higher efficiency but also has a larger physical size, higher series resistance, lower saturation current, and slow load transient dynamic performance. There is also a lower limit of the inductor value, which is determined by the minimum on time. To ensure reliable operation, the inductor value should be chosen higher than L_{MIN}, which can be calculated with Equation (2):

$$L_{MIN} = \frac{V_{IN(MAX)} \times t_{ON(MIN)}}{I_{peak}} \quad (2)$$

Where $V_{IN(MAX)}$ is the maximum value of the input voltage, and $t_{ON(MIN)}$ is the 115ns minimum switch on time.

Switching Frequency

The switching frequency (f_s) can be estimated with Equation (3):

$$f_s = \frac{2 \times Io \times V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak}^2 \times V_{IN} \times L} \quad (3)$$

A larger inductor can achieve a lower f_s. f_s increases as Io increases. When Io increases to its maximum value (Ipeak/2), f_s also reaches its highest value and can be derived with Equation (4):

$$f_{s(max)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak} \times V_{IN} \times L} \quad (4)$$

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB.

To get the desired output voltage, a resistor divider can be chosen with Equation (5):

$$\frac{R4}{R5} = \frac{V_{OUT}}{V_{REF}} - 1 \quad (5)$$

Where V_{REF} is the FB reference voltage (1V).

The current flowing into the resistor divider increases the supply current, especially at no-load and light-load conditions. The V_{IN} supply current caused by the feedback resistors can be calculated with Equation (6):

$$I_{IN_FB} = \frac{V_{OUT}}{R4 + R5} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta} \quad (6)$$

Where η is the efficiency of the regulator.

To reduce this current, resistors in the MΩ range are recommended. The recommended values of the feedback resistors are shown in Table 1.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R4 (kΩ)	R5 (kΩ)
3.3	1200	523
5	1200	300

UVLO Point Setting

The MPQ4569A has internal, fixed, UVLO threshold. The rising threshold is about 4.2V, while the trailing threshold is about 3.75V. An external resistor divider between EN and IN can be used to achieve a higher equivalent UVLO threshold (see Figure 3).

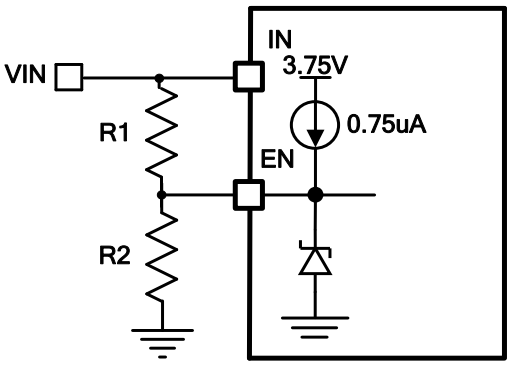

Figure 3: Adjustable UVLO using EN

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The UVLO threshold can be calculated with Equation (7) and Equation (8):

$$UVLO_{TH_Rising} = (1+\frac{R1}{R2})\times EN_{TH_Rising} - 0.75\times R1 \quad (7)$$

$$UVLO_{TH_Falling} = (1+\frac{R1}{R2})\times EN_{TH_Falling} - 0.75\times R1 \quad (8)$$

Where the R1 and R2 are in MΩ.

Soft-Start Capacitor

The soft-start time is the duration when SS is charged from zero to the FB reference voltage (1V) by an internal 5μA current source. The capacitor at SS (C_{SS}) can be chosen according to Equation (9):

$$C_{SS}(\mu F) = 5\times t_{SS}(s) \quad (9)$$

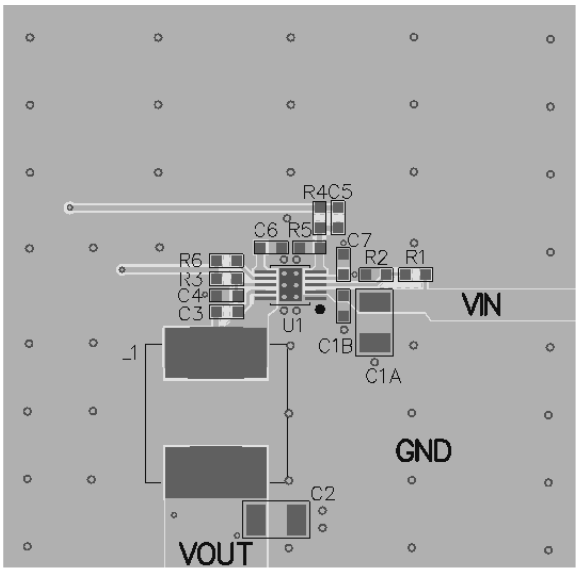
Feed-Forward Capacitor

The PWM control scheme of the MPQ4569A is very special in that the HS-FET turns on when FB drops lower than reference voltage. This results in good load transient performance, but also makes the HS-FET turn-on moment very sensitive to VFB. If there is noise on FB, the HS_FET can be affected easily the moment it turns on, and fs jitter can occur. fs jitter can occur easily, especially if the VOUT ripple is very small. To improve jitter performance, a small feed-forward capacitor between VOUT and FB can be used (39pF recommended).

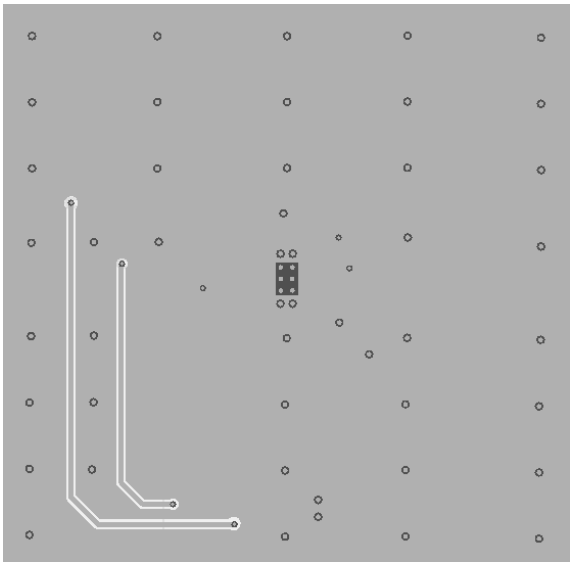
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below.

1) Keep the switching current path short.
2) Minimize the loop area formed by the input capacitor, high-side and low-side MOSFETs, and the output capacitor.
3) Place the ceramic bypass capacitors as close to IN as possible.
4) Ensure that all feedback connections are short and direct.
5) Place the feedback resistors as close to the chip as possible.
6) Keep SW away from sensitive analog areas such as FB.
7) Connect IN, SW, and GND to a large copper area to cool the chip for better thermal performance and long-term reliability consideration.



Top Layer



Bottom Layer

Figure 4: Layout Reference (5)

NOTE:

5) Based on the Typical Application Circuit in Figure 5.

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TYPICAL APPLICATION CIRCUIT

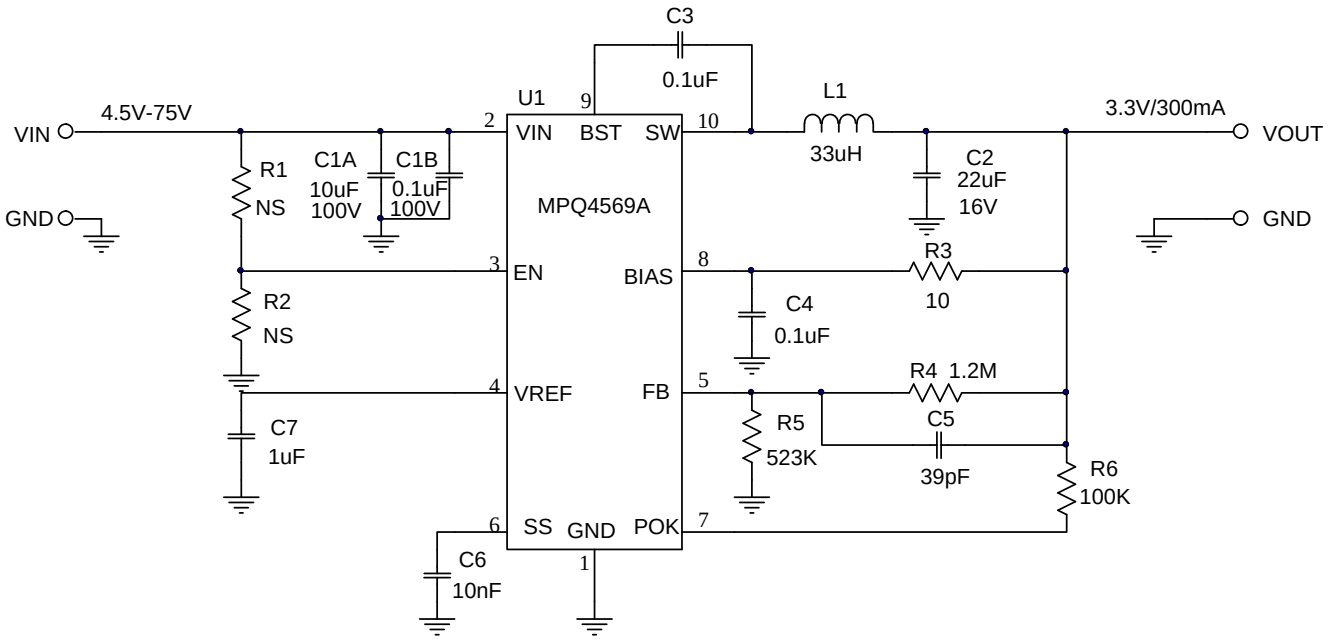

Figure 5: 3.3V Output Typical Application Circuit

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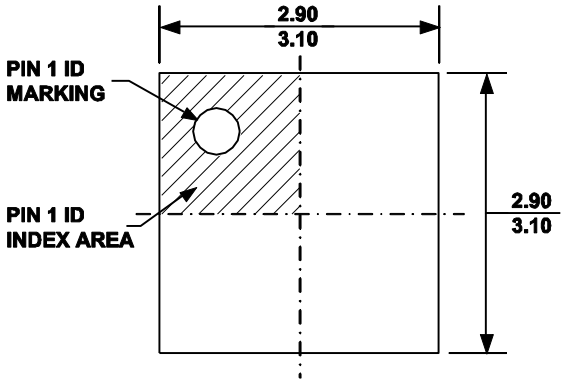
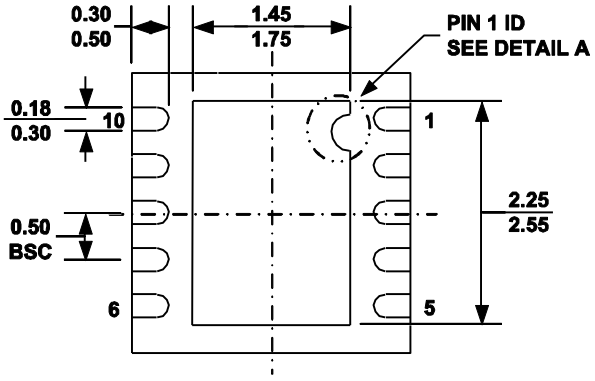
PACKAGE INFORMATION

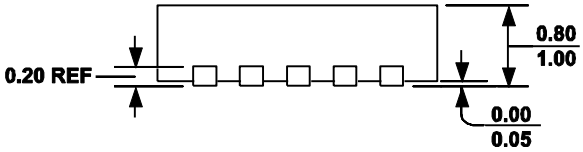
QFN-10 (3mmx3mm)



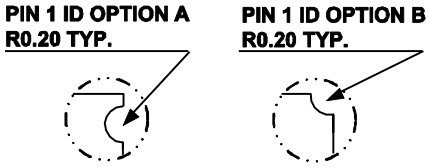
TOP VIEW



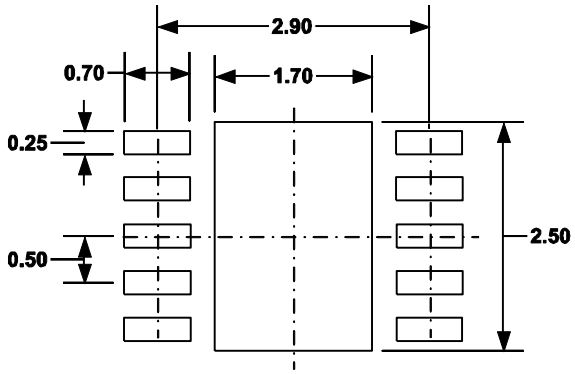
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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