MPQ4228

3A, 36V, Buck Converter with USB Charging Port Supporting DCP and Type-C 5V @ 3A DFP Mode, AEC-Q100 Qualified

DESCRIPTION

The MPQ4228 integrates a monolithic, step-down switch-mode converter with a single USB current-limit switch, as well as a Type-C 5V @ 3A mode configuration channel for USB ports. It achieves 3A of output current across a wide input supply range, with excellent load and line regulation.

The USB switch's output is current-limited. The USB port supports Apple 3A Divider mode, DCP schemes for BC1.2, and 1.2V/1.2V mode. The USB port also supports USB Type-C 5V @ 3A DFP Mode and Type-A mode (CC1 = 97.6kΩ).

Fault condition protections include hiccup current limiting, output over-voltage protection (OVP), DP/DM/CC1/CC2 short to battery protection, and thermal shutdown (TSD).

The NTC input monitors the temperature of the external PCB, as well as other components.

The MPQ4228 requires a minimal number of readily available, standard external components. The MPQ4228 is available in a QFN-22 (4mmx4mm) package.

FEATURES

- Supports Charging Only Type-C or Type-A Port
- NTC Over-Temperature Detection
- Passes Apple MFI R33 Certification Test
- USB-IF Type-C Certificated
- 145°C Internal Load Shedding Entry Temperature
- Independent USB On/Off Control Pin (EN1)
- Supports BC1.2 DCP Mode, Apple 3A Divider Mode and 1.2V/1.2V Mode
- USB_OUT, DP/DM, CC1/CC2 Pins Short to Battery Protection
- Wide 4.2V to 36V Continuous Operating Input Voltage Range
- Selectable Switching Frequency (420kHz and 2.2MHz with Spread Spectrum)
- 3A Output Current
- Integrated 20mΩ Low $R_{DS(ON)}$ USB Switch
- Line Drop Compensation
- Selectable Forced CCM Operation/Automatic PFM/PWM Operation
- EN Shutdown Discharge Function
- Fault Indication for OCP, OVP, and OTP
- Frequency Sync from 200kHz to 2.2MHz
- Hiccup Current Limit for both Buck and USB
- ±8kV IEC 61000-4-2 Contact Discharge ESD Rating for CC1 and CC2 Pins
- ±8kV IEC 61000-4-2 Contact Discharge ESD Rating with Small Resistor, Capacitor on DP and DM Pins
- ±15kV IEC 61000-4-2 Air Discharge ESD Rating for DP, DM, CC1, and CC2 Pins
- Available in a QFN-22 (4mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Dedicated Charging Ports (DCP)
- USB Type-C DFP Port

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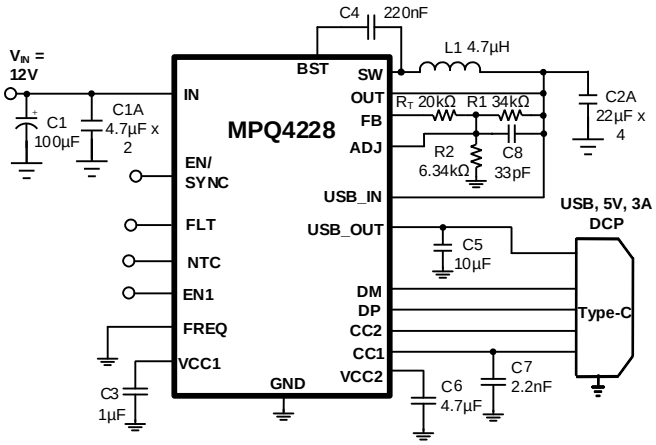
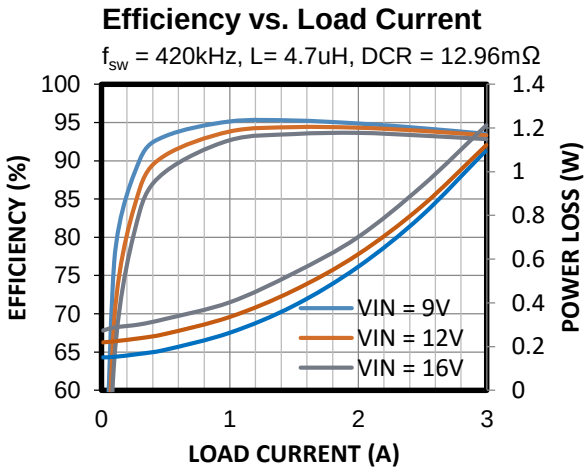
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4228GRE-AEC1	QFN-22 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4228GRE-AEC1-Z).

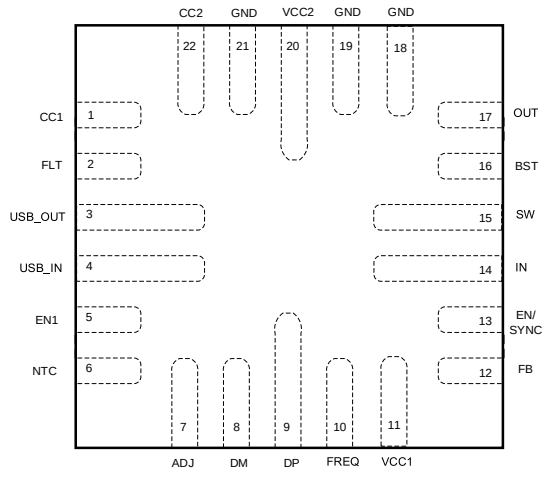
TOP MARKING

MPSYWW
MP4228
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4228: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-22 (4mmx4mm) Wettable flank

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PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 detects connections, and configures the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power to the plug's VCONN pin.
2	FLT	**Fault indicator.** The FLT pin indicates if the following protections occur: USB over-current protection (OCP) and short-circuit protection (SCP), USB_IN over-voltage protection (OVP), DP/DM/CCx short to battery protection, and thermal shutdown. FLT is an open drain under normal conditions. FLT is pulled low if a fault occurs.
3	USB_OUT	**USB bus voltage output.**
4	USB_IN	**USB bus voltage input.**
5	EN1	**USB switch enable pin.** EN1 is an active low pin. When EN1 is low, the USB is enabled. When EN1 is high, the USB is off. The buck output is still active when EN1 is high. By default, EN1 is pulled low by an internal 1MΩ resistor. Note that the maximum voltage of EN1 is 4V.
6	NTC	**Thermistor input.** Connect a thermistor from NTC to VCC2, and connect a fixed resistor from NTC to GND. Place the thermistor near the USB connector or output capacitor for temperature monitoring. The chip advertises a 1.5A load capability when NTC triggers the load-shedding threshold. The chip immediately shuts off the USB output when NTC reaches the thermal shutdown threshold, and the FLT pin is pulled low. By default, NTC is pulled low by an internal 1MΩ resistor. Connect NTC to GND (or float NTC) to disable the thermal-sense function. NTC has a maximum 4V voltage.
7	ADJ	**Line drop compensation pin.** ADJ sinks a current from the DC/DC converter's FB pin to ground to regulate the converter's output voltage.
8	DM	**D- data line to USB connector.** DM is the input/output that is used for handshaking with portable devices.
9	DP	**D+ data line to USB connector.** DP is the input/output that is used for handshaking with portable devices.
10	FREQ	**Frequency selection pin.** If FREQ = GND, the device operates at 420kHz with frequency dithering (±10% dithering) in forced continuous conduction mode (FCCM). If FREQ is floating, the device operates at 420kHz with frequency dithering (±10% dithering) in pulse frequency mode (PFM). If FREQ = VCC, the device operates at 2.2MHz with frequency dithering (±10% dithering) in FCCM.
11	VCC1	**Internal 5V LDO regulator output.** Decouple VCC1 with a 1µF capacitor.
12	FB	**Feedback.** Connect FB to the tap of an external resistor divider that is connected from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current limit runaway during a short circuit fault condition.
13	EN/SYNC	**On/off control input.** The EN pin is internally pulled to ground by a 500kΩ resistor. Apply an external CLK on this pin to synchronize the switching frequency.
14	IN	**Supply voltage.** The MPQ4228 operates from a 4.2V to 36V input rail. IN requires a capacitor (C1) to decouple the input rail. Connect IN to the input capacitor using a wide PCB trace.
15	SW	**Switch output.** Use a wide PCB trace to connect the SW pin to the inductor.
16	BST	**Bootstrap.** A 220nF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
17	OUT	**Buck output.** Connect OUT to an external power supply (5V ≤ V_{OUT} ≤ 20V) or connect to the buck converter's VOUT to reduce power dissipation and increase efficiency. Float the OUT pin or connect it to ground if not used.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
18, 19, 21	GND	**Power ground.**
20	VCC2	**Internal 3.45V LDO regulator output.** Decouple VCC2 with a 4.7µF capacitor.
22	CC2	**Configuration channel.** CC2 detects connections, and configures the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power to the plug's VCONN pin.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}, V_{OUT}) .....-0.4V to +40V
V_{SW} .....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (+43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{USB_IN}, V_{USB_OUT} .....-0.3V to +24V
V_{CC1}, V_{CC2}, V_{DM}, V_{DP} .....-0.3V to +18V
V_{FLT} .....-0.3V to +6.5V
V_{NTC}, V_{EN1} .....-0.3V to +4V
V_{FREQ}, $V_{EN/SYNC}$ .....-0.3V to +5.5V (2)
All other pins .....-0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (3) (6)
QFN-22 (4mmx4mm) 3.47W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM)
DP/DM/CC1/CC2/USB_OUT to GND ….....±8kV
All other pins……..±2kV
Charged device model (CDM)
DP/DM/CC1/CC2/USB_OUT……...±2kV
All other pins.....±750V

Recommended Operating Conditions (5)

Operation input voltage range……4.2V to 36V
Output voltage range.....5V Typical
Output current 3A
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-22 (4mmx4mm)			
EVQ4228-RE-00B (6)	36	5	°C/W
JESD51-7 (7)	46	38	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS Max rating, refer to the EN/SYNC Control section on page 16.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM with regard to GND.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on 4-layer PCB, 57.4mmx57.4mm.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JESD board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V,T_J = 25°C			1	μA
		V_{EN} = 0V,T_J = -40°C to +150°C			8	
Buck converter's supply current (quiescent)	$I_{Q_CL_VBUSDIS}$	CC pin floating, V_{FB} = 1V		0.75	1.1	mA
Overall supply current (quiescent)	I_Q	CC1 connected to ground with 5.1kΩ resistor, V_{FB} = 1V		1	1.5	mA
EN rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN_FALLING}$		1.05	1.25	1.45	V
EN input current	I_{EN1}	V_{EN} = 2V		4.5	6	μA
	I_{EN2}	V_{EN} = 0V		0	0.2	
Thermal shutdown (8)	T_{STD}			165		°C
Thermal hysteresis (8)	T_{STD_HYS}			20		°C
VCC1 regulator	V_{CC1}	I_{CC} = 0mA	4.8	5	5.2	V
VCC1 load regulation	V_{CC1_LOG}	I_{CC} = 5mA		1.5	4	%
VCC2 regulator	V_{CC2}	I_{CC} = 0mA	3.15	3.45	3.75	V
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		3.5	3.7	3.9	V
V_{IN} under-voltage lockout threshold falling	V_{UVLO_FALL}		3.05	3.25	3.45	V
HS switch on resistance	$R_{DS(ON)_HS}$			50	90	mΩ
LS switch on resistance	$R_{DS(ON)_LS}$			30	60	mΩ
Output discharge resistance	R_{DIS}			200		Ω
Feedback voltage	V_{FB}		776	792	808	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	100	nA
Sync frequency range	f_{SYNC}		0.2		2.4	MHz
Oscillator frequency	f_{SW1}	V_{FB} = 750mV, FREQ = floating	340	420	500	kHz
	f_{SW2} (8)	V_{FB} = 750mV, FREQ = VCC		2.2		MHz
Frequency spread spectrum span	f_{SW3}	FREQ = GND, based on 420kHz		±10		%
	f_{SW4} (8)	FREQ = VCC, based on 2.2MHz		±10		%
Maximum duty cycle	D_{MAX}	Based on 420kHz	94.5	96		%
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to+150°C			10	
High-side peak current limit (8)	I_{LIMIT1}	T_J = -40°C to +150°C	7	10		A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-side valley current limit (8)	I_{LIMIT2}			9		A
Low-side negative current limit (8)	I_{LSNEG}			-3		A
Minimum on time (8)	t_{ON_MIN}			60		ns
Output over-voltage protection	V_{OVP1}		112	115	118	%
Output OVP recovery	V_{OVP1_R}			105		%
Soft-start time	t_{SS}	Output from 10% to 90%		1.5		ms
USB Switch						
Under-voltage lockout threshold rising	V_{USB_UVR}		2.8	3.0	3.2	V
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}			400		mV
EN1 logic high input	V_{EN1_H}	Turn off the USB output	2			V
EN1 logic Low Input	V_{EN1_L}	Turn on the USB output			0.4	V
Switch on resistance	R_{DSON_SW}			20	40	mΩ
Input discharge resistance	R_{DIS_USB}	Turn on during IN OVP		200		Ω
USB input OVP rising	V_{USB_OV}	V_{OUT} = 5V	5.85	6.05	6.3	V
USB Input OVP recovery threshold	$V_{USB_OV_RECOVERY}$	V_{OUT} = 5V	5.5	5.75	6	V
Current Limit	I_{LIMIT1}	V_{OUT} drops to 10%, Type-C/Type-A mode, room temperature	3.2	3.55	3.9	A
USB_OUT soft-start time	t_{USB_SS}	V_{OUT} = 5V, from 10% to 90%		0.45		ms
V_{BUS} enter hiccup hold time	t_{HICP_ON}	V_{OUT} = 5V, OC, hiccup on time		2		ms
Hiccup Mode Off Time	t_{HICP_OFF}	V_{OUT} = 5V, V_{BUS} connected to GND		2		s
DM, DP pins OVP Rising	$V_{OV_DM_DP}$		3.75	4.0	4.25	V
DM, DP pins OVP hysteresis	$V_{OV_DM_DP_HYS}$			100		mV
Line drop compensate gain	G_{ADJ_SINK}	ADJ sink current/I_{OUT} current, I_{OUT} = 3A	-20%	2.05	+20%	μA/A
FLT output low voltage	I_{FLT_L}	I_{SINK} = 1mA			0.15	V
FLT leakage current	V_{FLT_LKG}	6.5V pull-up voltage			1	μA
FLT deglitch time	t_{FLT_DEG}	Over-current condition		2		ms
NTC Temperature Sensing						
Load shedding entry threshold	V_{LS_HIGH}	R_{DOWN} = 3kΩ, R_{UP} = 3kΩ (125°C)	0.47	0.5	0.53	VCC2
Load shedding exit threshold	V_{LS_LOW}	R_{DOWN} = 3kΩ, R_{UP} = 9.99kΩ (85°C)	0.21	0.24	0.27	VCC2

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal shutdown entry threshold	V_{TSD_HIGH}	R_{DOWN} = 3kΩ, R_{UP} = 1.28kΩ (160°C)	0.63	0.7	0.73	VCC2
Thermal shutdown exit threshold	V_{TSD_LOW}	R_{DOWN} = 3kΩ, R_{UP} = 2.07kΩ (140°C)	0.57	0.6	0.63	VCC2
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_SHORT}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C			40	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +150°C			50	
Divider Mode						
DP output voltage	$V_{DP_DIVIDER}$	V_{OUT} = 5V	2.5	2.7	2.85	V
DP output impedance	$R_{DP_DIVIDER}$		20	26	32	kΩ
DM output voltage	$V_{DM_DIVIDER}$	V_{OUT} = 5V		3.4		V
DM output impedance	$R_{DM_DIVIDER}$			20		kΩ
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM_1.2V}$	V_{OUT} = 5V	1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM_1.2V}$		200	300	400	kΩ
USB Type-C 5V @ 3A Mode (CC1, CC2)						
CC resistor to disable Type-C mode	R_A	CC1 pin, for Type-C mode applications add a 2.2nF capacitor on CC1	95.3	97.6	100	kΩ
CC pull-up current to detect Type-A mode	I_{PLL}		8	10	12	μA
CC voltage to enable V_{CONN}	V_{RA}				0.75	V
CC voltage to enable V_{BUS}	V_{RD}	Room temp	0.85		2.45	V
CC voltage at 5.1kΩ R_D	V_{CC_RD}	CC pin pulled down by a 5.1kΩ resistor, room temperature	1.31	1.683	2.04	V
CC detach voltage	V_{OPEN}		2.75			V
CC voltage falling debounce timer	$t_{CC_DEBOUNCE}$	V_{BUS} enable deglitch	100	150	200	ms
CC voltage rising debounce timer	$t_{PD_DEBOUNCE}$	V_{BUS} disable deglitch	0	10	20	ms
V_{CONN} output power	P_{VCONN}	V_{CONN} comes from Buck output with some series resistance	1			W
V_{BUS} to ground impedance	R_{BUS}	Type-C detach, after output discharge turn-off	72.4			kΩ

Note:

8) Guaranteed by engineering sample characterization.

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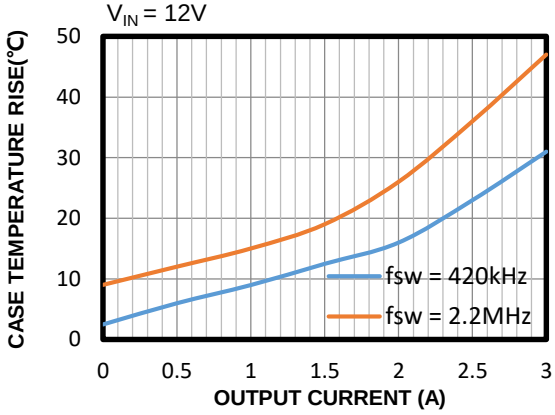
TYPICAL CHARACTERISTICS

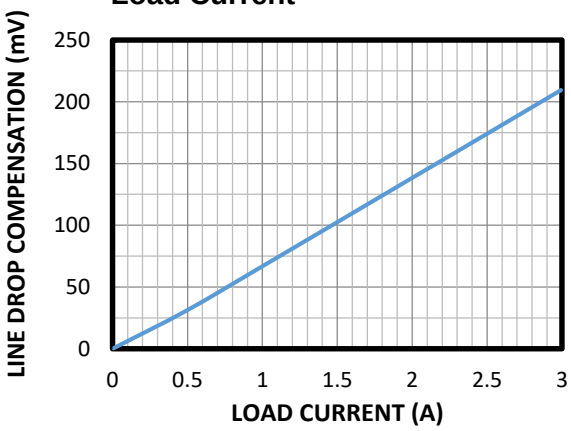
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 is connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Case Temperature Rise vs. Output Current

V_{IN} = 12V

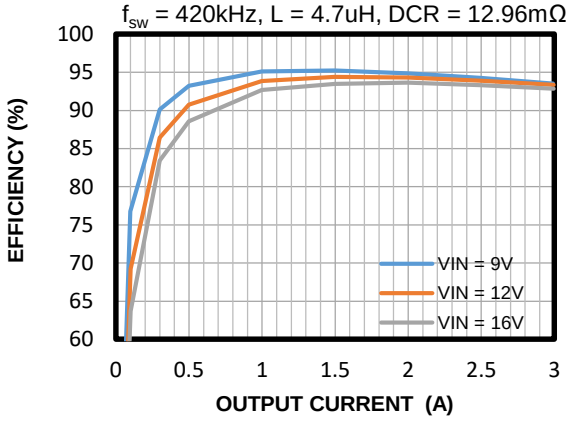


Line Drop Compensation vs. Load Current



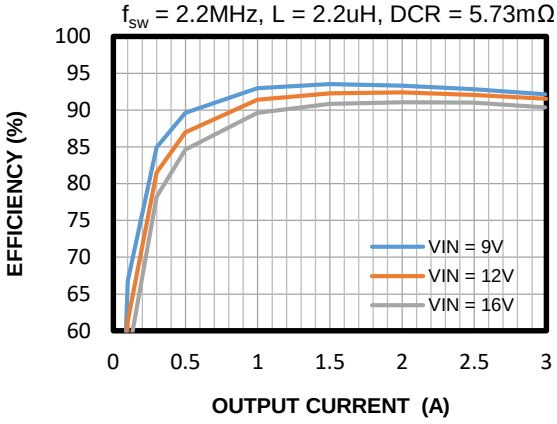
Efficiency vs. Load Current

f_{sw} = 420kHz, L = 4.7uH, DCR = 12.96mΩ



Efficiency vs. Load Current

f_{sw} = 2.2MHz, L = 2.2uH, DCR = 5.73mΩ



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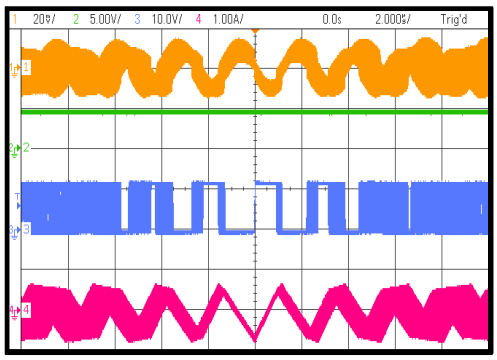
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 is connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted

Steady State

Frequency spread spectrum is enabled,
I_{OUT} = 0A

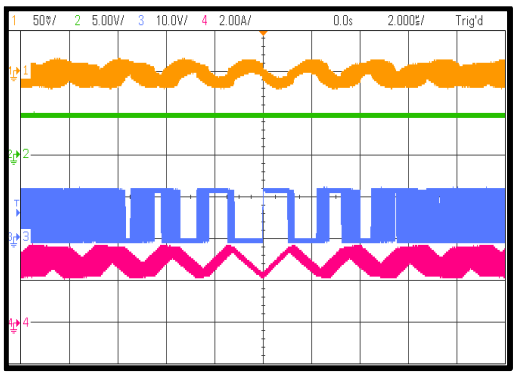
CH1: USB/AC
CH2: V_{BUCK}/ V_{OUT}
CH3: V_{SW}
CH4: I_L



Steady State

Frequency spread spectrum is enabled,
I_{OUT} = 3A

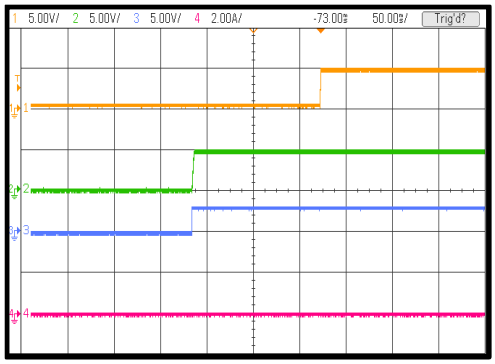
CH1: USB/AC
CH2: V_{BUCK}/ V_{OUT}
CH3: V_{SW}
CH4: I_L



Start-Up through EN

I_{OUT} = 0A

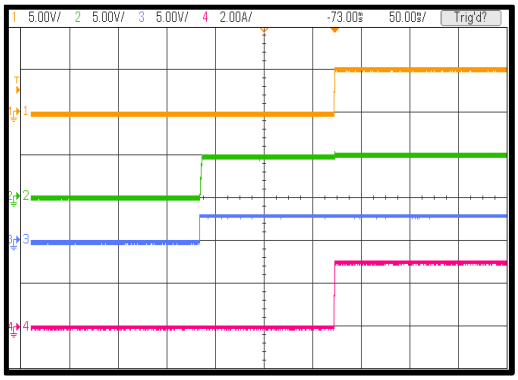
CH1: USB
CH2: V_{BUCK}/ V_{OUT}
CH3: V_{EN}
CH4: I_{OUT}



Start-Up through EN

I_{OUT} = 3A

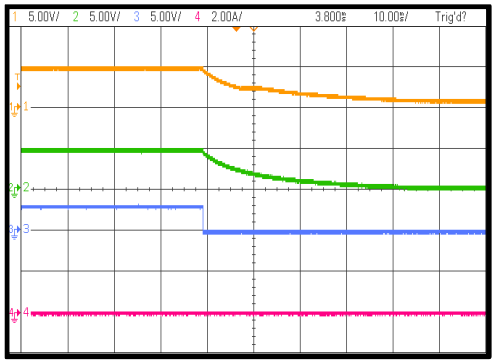
CH1: USB
CH2: V_{BUCK}/ V_{OUT}
CH3: V_{EN}
CH4: I_{OUT}



Shutdown through EN

I_{OUT} = 0A

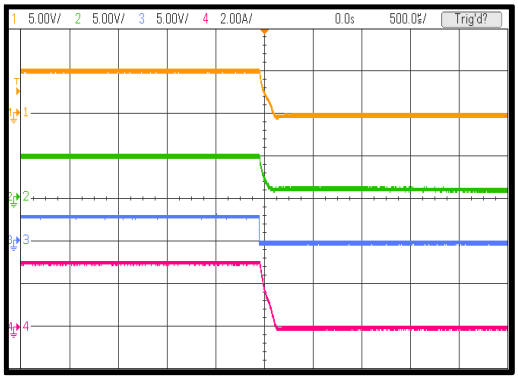
CH1: USB
CH2: V_{BUCK}/ V_{OUT}
CH3: V_{EN}
CH4: I_{OUT}



Shutdown through EN

I_{OUT} = 3A

CH1: USB
CH2: V_{BUCK}/ V_{OUT}
CH3: V_{EN}
CH4: I_{OUT}



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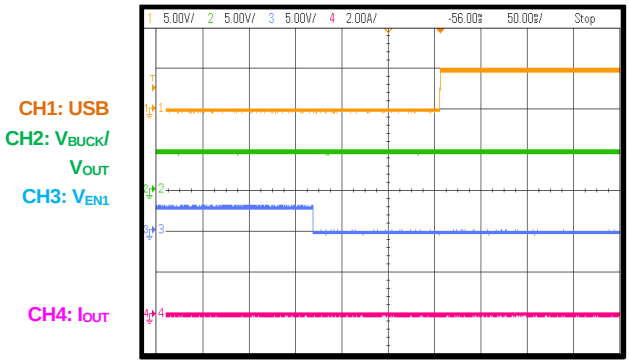
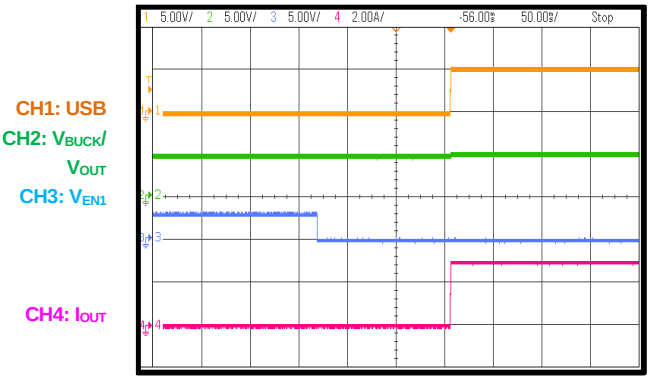
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 is connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted

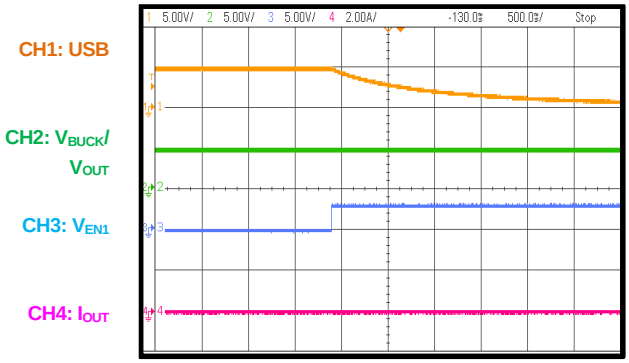
Start-Up through EN1
I_{OUT} = 0A



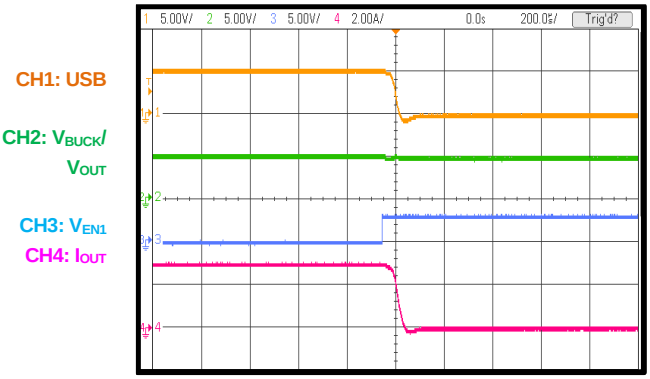
Start-Up through EN1
I_{OUT} = 3A



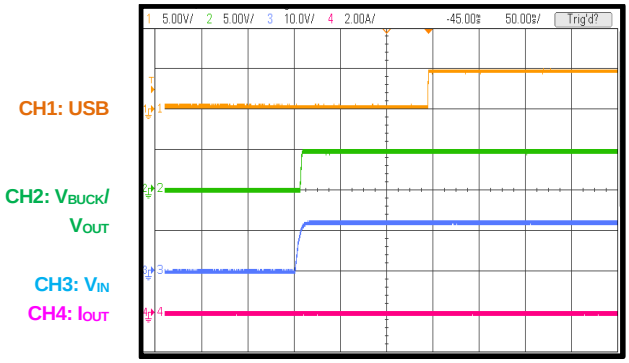
Shutdown through EN1
I_{OUT} = 0A



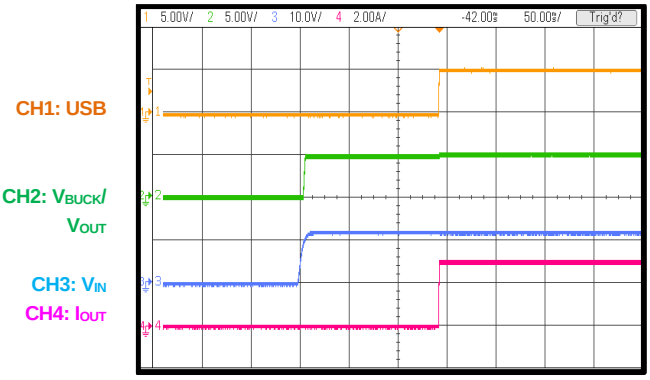
Shutdown through EN1
I_{OUT} = 3A



Start-Up
I_{OUT} = 0A



Start-Up
I_{OUT} = 3A



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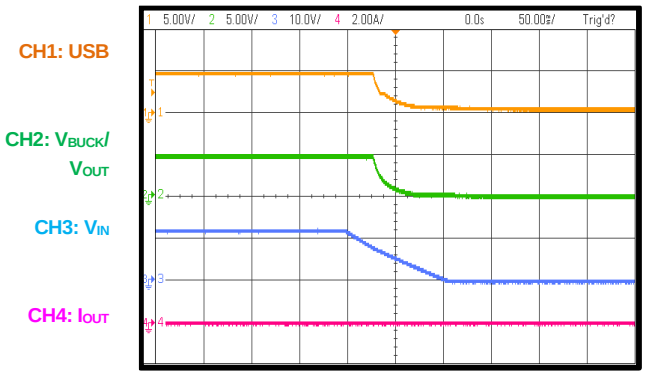
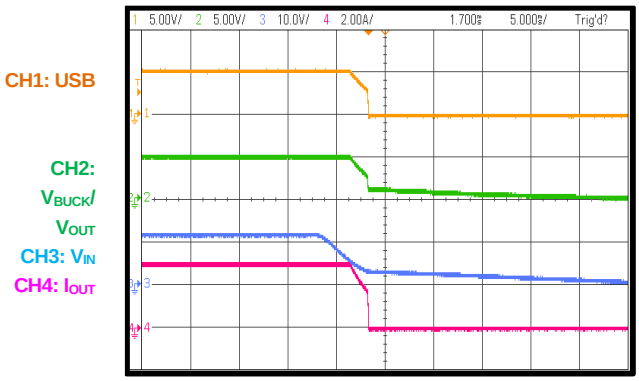
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 is connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted

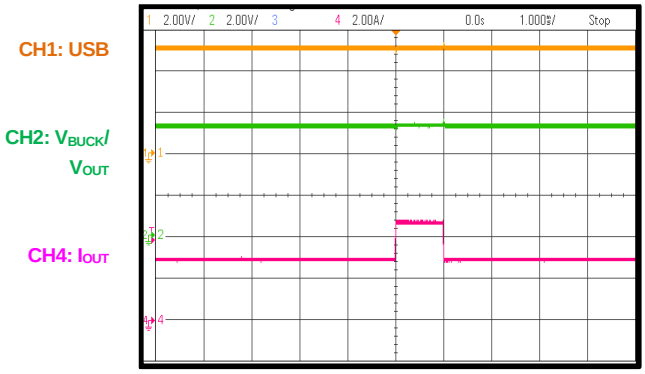
Shutdown
I_{OUT} = 0A



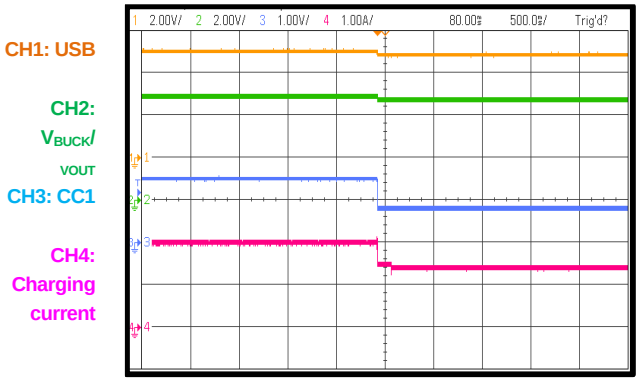
Shutdown
I_{OUT} = 3A



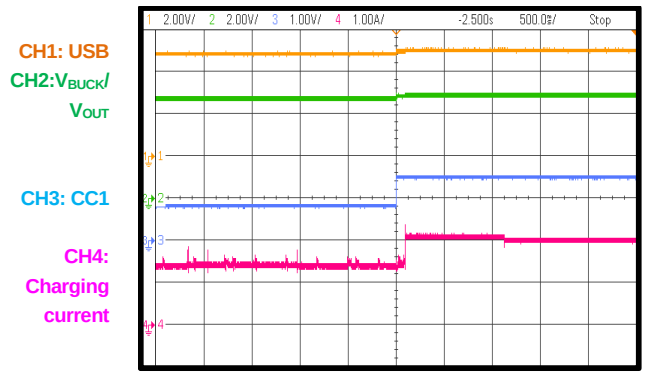
MFI Over-Current Pulse Test
I_{OUT} = 3A to 4.8A, 1ms hold time



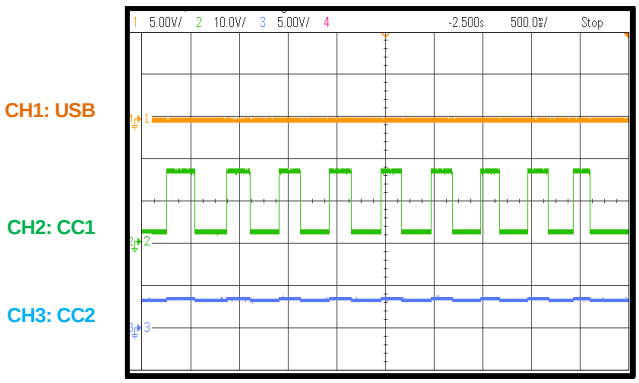
Load-Shedding Entry
Connect to mobile phone during testing



Load Shedding Recovery
Connect to mobile phone during testing



CC1 Short to Battery
$V_{BATTERY}$ = 18V, CC1 = CC2 = floating



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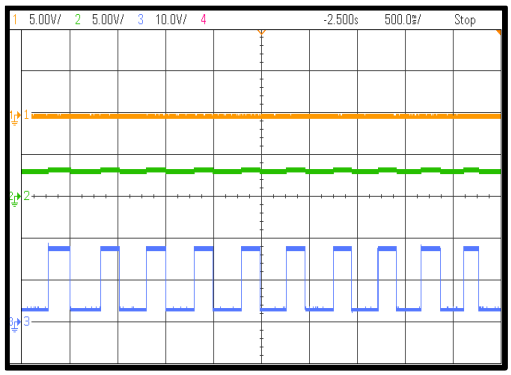
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 is connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted

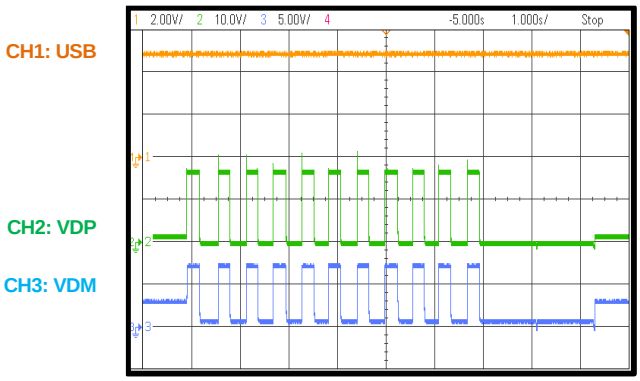
CC2 Short to Battery

$V_{BATTERY}$ = 18V, CC1 = CC2 = floating



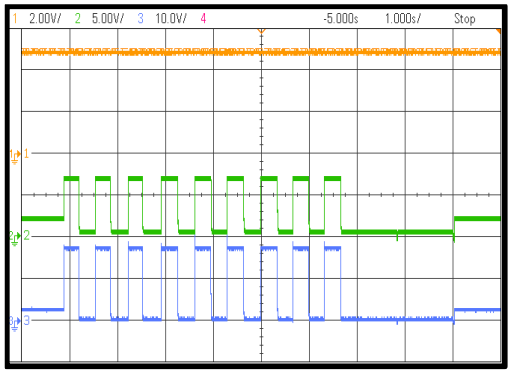
DP Short to Battery

$V_{BATTERY}$ = 18V



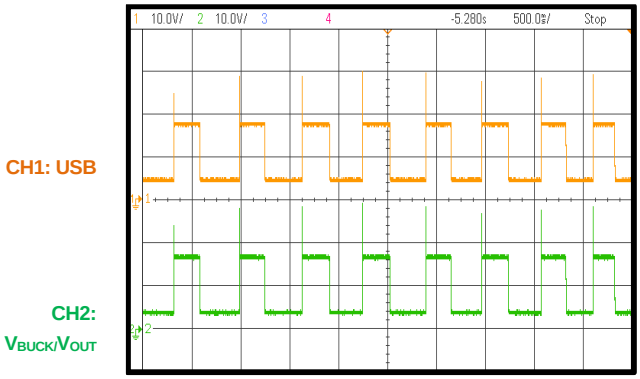
DM Short to Battery

$V_{BATTERY}$ = 18V



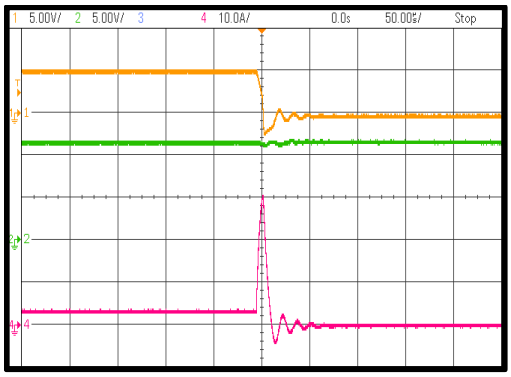
USB_OUT Short to Battery

$V_{BATTERY}$ = 18V

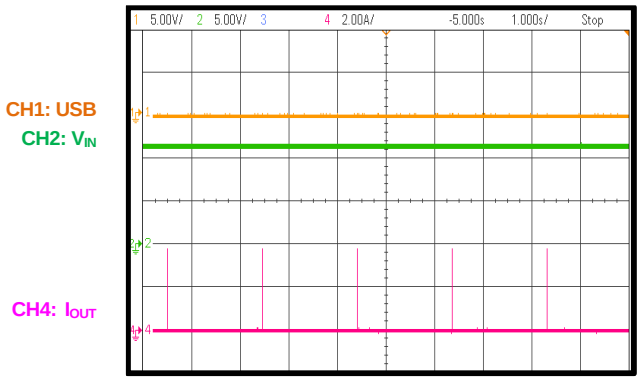


USB_OUT Short to GND Entry

I_{OUT} = 3A



USB_OUT Short to GND Steady State



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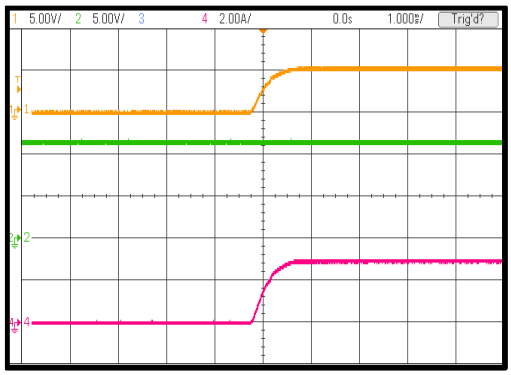
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 is connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted

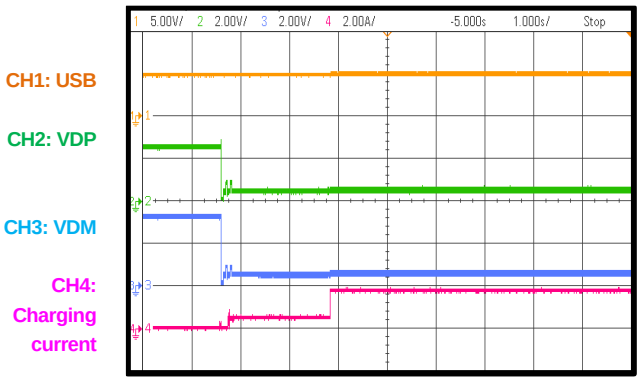
USB_OUT Short to GND Recovery

I_{OUT} = 3A



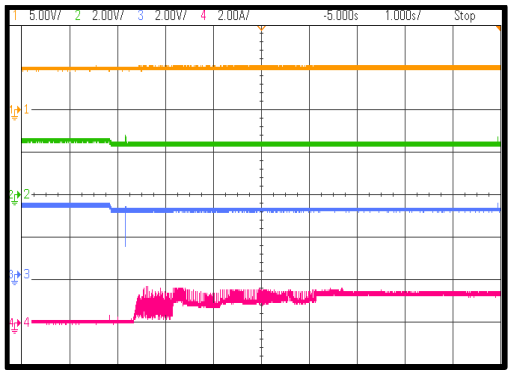
Android Device Charging Test

Mobile phone plugged in



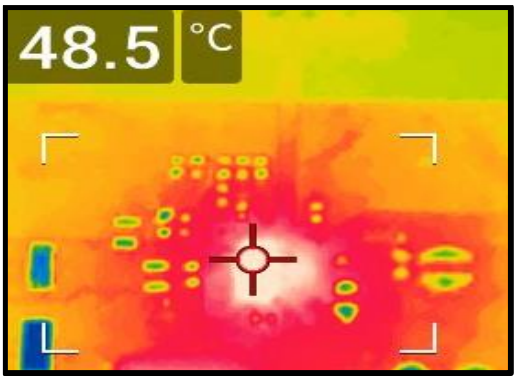
Apple Device Charging Test

Mobile phone plugged in



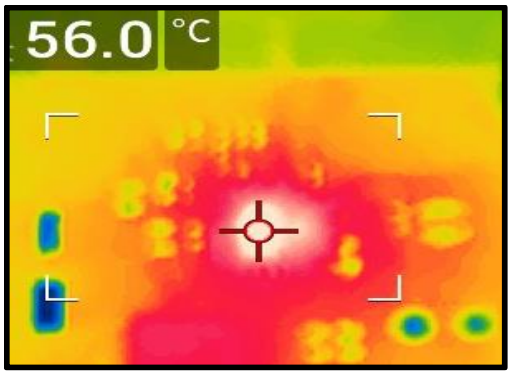
Thermal Image

V_{IN} = 12V, USB = 5V, I_{OUT} = 2.4A, measured on 4-layer PCB, 57.4mmx57.4mm, top/bottom layer: 2oz, middle layer 1 and 2: 1oz.



Thermal Image

V_{IN} = 12V, USB = 5V, I_{OUT} = 3A, measured on 4-layer PCB, 57.4mmx57.4mm, top/bottom layer: 2oz, middle layer 1 and 2: 1oz.



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FUNCTIONAL BLOCK DIAGRAM

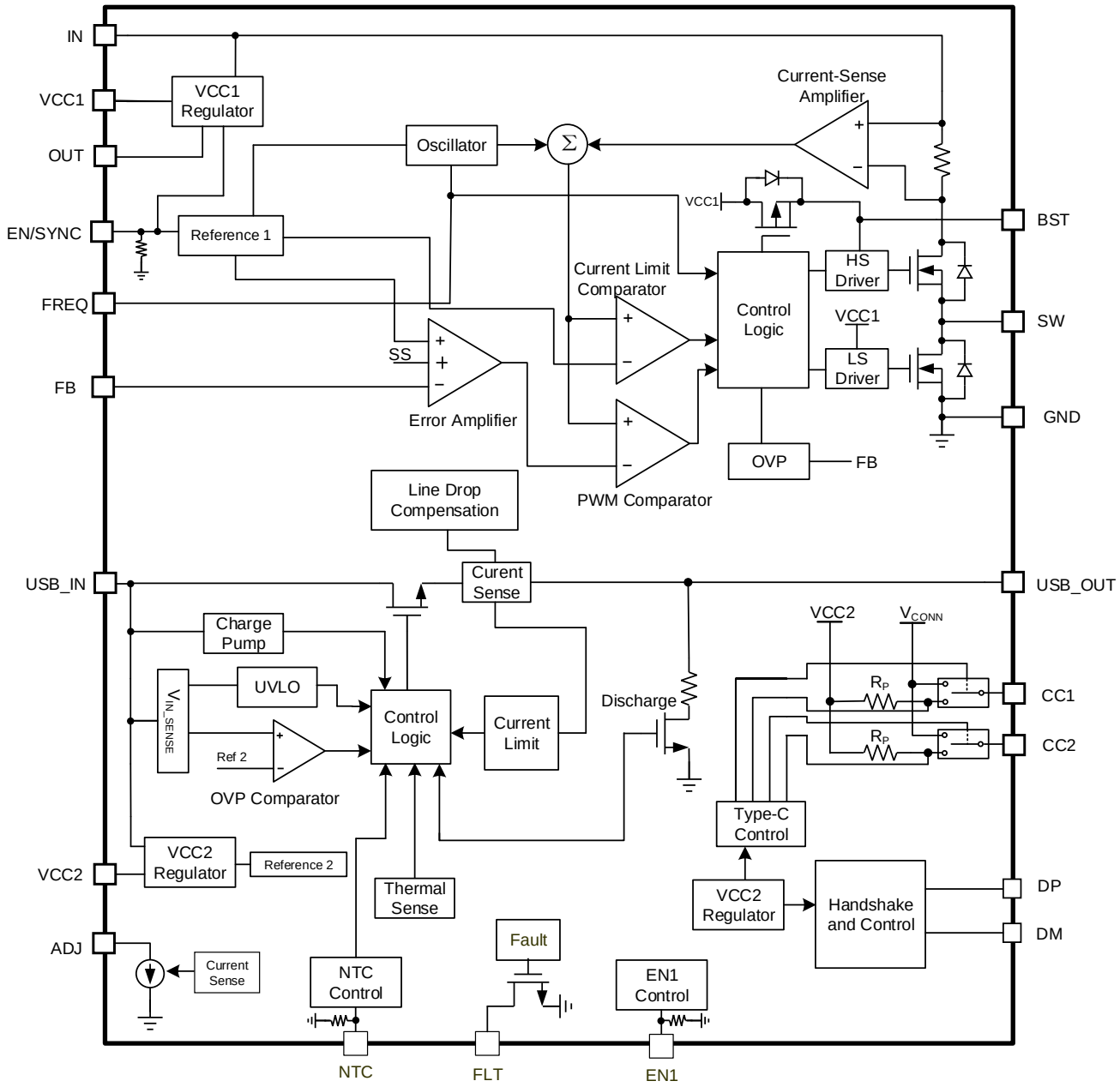

Figure 1: Functional Block Diagram

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OPERATION

BUCK CONVERTER

The MPQ4228 integrates a monolithic, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs and a USB current-limit switch with charging port auto-detection. It offers a compact solution to achieve 3A of continuous output current across a wide input supply range, with excellent load and line regulation.

The MPQ4228 operates in fixed-frequency, peak current mode control to regulate the output voltage. The internal clock initiates the PWM cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle begins. If the current value does not reach the value set by COMP within 96% of one PWM period, the power MOSET is forced off.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage to the internal 0.792V reference voltage (V_{REF}) and outputs a COMP voltage. This COMP voltage controls the power MOSFET's current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC1 Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator uses either the buck converter's V_{OUT} or V_{IN} as the supply. When V_{IN} exceeds 5V, the output of the regulator is in full regulation. If V_{IN} is below 5V, the output decreases following V_{IN}. When the output voltage is established and exceeds 4.75V, the VCC1 regulator uses the power from the buck converter's VOUT to reduce LDO power loss. VCC1 requires an external, ceramic, 0.22µF to 1µF decoupling capacitor.

EN/SYNC Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn the regulator on; drive EN low to turn it off. An internal 500kΩ resistor connected from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip

The EN pin is clamped internally using a 6.5V series Zener diode (see Figure 2). It is recommended to connect EN to VIN and GND through resistor dividers. When selecting a pull-up resistor, ensure that its resistance can limit the current flowing into EN below 100µA.

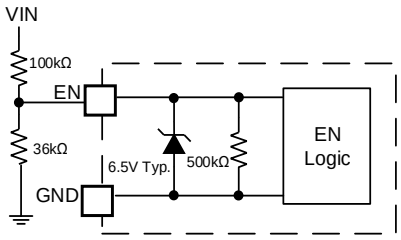

Figure 2: 6.5V Zener Diode

For example, if the EN pull-up resistor is 100kΩ, and the pull-down resistor is 36kΩ, the IC starts up when V_{IN} exceeds 6V.

If the EN pin is directly connected to a voltage source without a pull-up resistor, the voltage amplitude must be limited ≤5.5V to prevent damage to the Zener diode.

Connect an external clock that ranges between 200kHz and 2.2MHz to the EN pin. This synchronizes the internal clock. The MPQ4228 operates with a fixed frequency without spread spectrum functionality while the external clock is synchronizing. It is recommended to float FREQ when synchronizing the switching frequency to an external clock.

Setting the Frequency

The MPQ4228's switching frequency can be adjusted by the FREQ pin. If FREQ is equal to GND, the device operates at 420kHz with spread spectrum (±10% dithering) in FCCM. If FREQ is floating, the device operates at 420kHz with spread spectrum (±10% dithering) in PFM. If FREQ is equal to VCC1, the device operates at 2.2MHz with spread spectrum (±10% dithering) in FCCM (see Table 1).

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Table 1: Switching Frequency Selecting

FREQ Pin	Operation Mode	Switching Frequency
GND	FCCM with spread spectrum	420kHz
Float	PFM with spread spectrum	420kHz
VCC1	FCCM with spread spectrum	2.2MHz

Automatic PFM/PWM Operation (FREQ is Floating)

The MPQ4228 works in continuous conduction mode (CCM) under heavy loads. When the load decreases, the MPQ4228 enters discontinuous conduction mode (DCM) with a fixed frequency while the inductor current approaches 0A. If the load is further decreased (or there is no load), the inductor peak current drops below the AAM peak current threshold. Then the MPQ4228 enters pulse-skip mode to further improve light-load efficiency.

Under very light loads or no load, the FB voltage decreases slowly, and COMP ramps up until it reaches V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILSENSE}$ reaches the value set by the COMP voltage. When $V_{COMP} < V_{AAM}$, the internal clock is blocked, and the device skips some pulses for pulse-frequency modulation (PFM). This control scheme helps achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from the light-load condition, COMP increases, as well as the switching frequency. If the output current exceeds the critical level set by COMP, the MPQ4228 resumes fixed-frequency PWM control (see Figure 3).

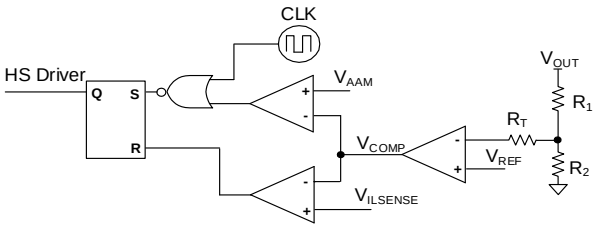

Figure 3: Auto PFM/PWM Operation Control Logic

Forced Continuous Conduction Mode (FCCM) (FREQ = GND or VCC1)

The MPQ4228 works in forced continuous conduction mode (CCM) continuously. The device operates with a fixed switching frequency, regardless of whether it is operating under light loads or full loads.

The advantage of FCCM is the controllable frequency, smaller output ripple, and sufficient bootstrap charging time. However, FCCM is less efficient under light loads. The inductance should be selected to avoid triggering the LS-FET's negative current limit (typically -3A, from SW to GND). If the negative current limit is triggered, the LS-FET turns off, and the HS-FET turns on when the internal clock begins.

Frequency Spread Spectrum

The purpose of the spread spectrum is to minimize the peak emissions at a specific frequency.

The MPQ4228 uses a 4kHz triangle wave (125μs rising, 125μs falling) to modulate the internal oscillator. The frequency span of spread spectrum operation is ±10% (see Figure 4).

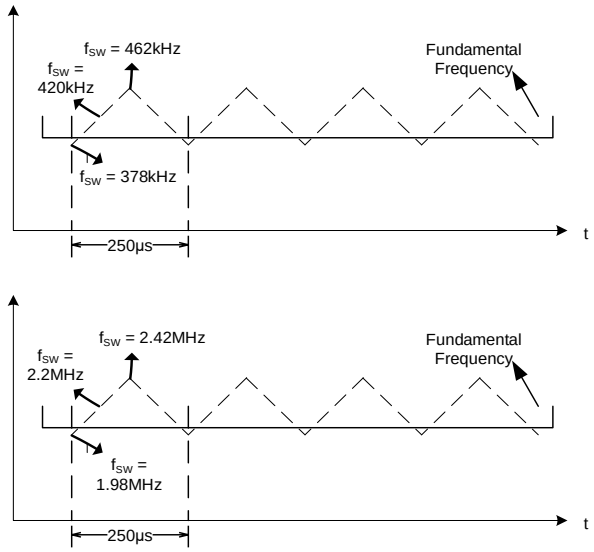

Figure 4: Frequency Spread Spectrum

Float FREQ or connect it to GND for a frequency of 420kHz with frequency spread spectrum. Connect FREQ to VCC for a frequency of 2.2MHz with frequency spread spectrum.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage.

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The UVLO comparator monitors the input voltage. The UVLO rising threshold is 3.7V, and its falling threshold is 3.25V.

Internal Soft-Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage that ramps up from 0V to 5V. When the SS voltage (V_{SS}) is below the reference voltage (V_{REF}), the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

If the device's output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side MOSFETs until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Buck Over-Current Protection (OCP)

The MPQ4228 has a cycle-by-cycle over-current (OC) limit. If the inductor's peak current exceeds the current-limit threshold, and the FB voltage drops below the under-voltage (UV) threshold (typically 50% below V_{REF}), the MPQ4228 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4228 exits hiccup mode once the OC condition is removed.

Over-Voltage Protection (OVP)

The MPQ4228 detects the output voltage through the FB pin. If V_{OUT} exceeds 115% of the target voltage, the over-voltage protection (OVP) comparator output goes high. The device stops switching and turns on the discharge resistor connected from OUT to ground until V_{OUT} falls below 105% of the target voltage.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection. The UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN and VCC through D1, M1, C4, L1, and C2 (see Figure 5). The BST capacitor's C4 voltage is quickly charged by VCC through M1. The 1μA VIN-to-BST current source can also charge the BST capacitor when the low-side MOSFET is not on.

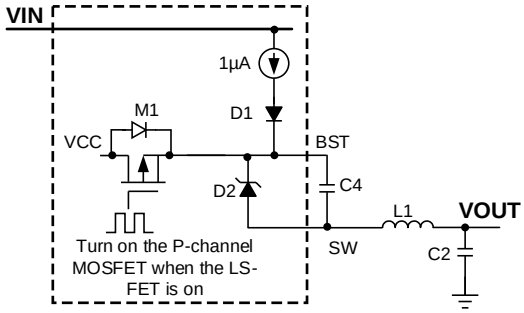

Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Discharge

The MPQ4228 has an output discharge function that provides a resistive discharge path for the external output capacitor. Three scenarios can trigger the output to discharge:

1. The input voltage falls beneath the UVLO threshold.
2. The part is enabled off.
3. An output over-voltage condition occurs.

In these scenarios, the discharge path turns off when the OUT pin's voltage drops below 0.5V, or if the maximum 200ms timer is complete.

USB CURRENT-LIMIT SWITCH

Under Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. When the input voltage exceeds the USB SW UVLO threshold, after a fixed delay, the power MOSFET starts to turn on with a controlled slew rate.

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EN1 Function

EN1 controls when the USB switch turns on and off. EN1 is an active low pin. By default, EN1 is pulled low by an internal 1MΩ resistor.

Pull EN1 high to disable the USB switch. Pull EN1 low to enable the USB switch. Note that the buck converter's output is still active even when EN1 is high.

The maximum EN1 voltage is 4V.

Internal Soft Start

Internal soft start prevents excessive inrush current, and prevents the output voltage from overshooting during start-up.

Line Drop Compensation

The MPQ4228 is capable of compensating for an output voltage drop (e.g. high impedance caused by a long trace) to maintain a fairly constant 5V load-side voltage. Line drop compensation is accomplished through the ADJ and FB pins (see Figure 6).

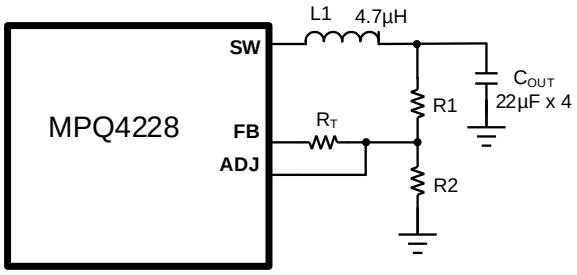

Figure 6: Line Drop Compensation

The MPQ4228 uses the sensed load current through the internal current sensing MOSFET to sink a current (I_{ADJ}) at ADJ. I_{ADJ} can be calculated with Equation (1):

$$I_{ADJ} = G_{ADJ_SINK} \times I_{USB_LOAD} \quad (1)$$

V_{BUCK_OUT} can be estimated with Equation (2):

$$V_{BUCK_OUT} = (\frac{R1}{R2} + 1) \times V_{REF} + R1 \times I_{ADJ} \quad (2)$$

This means that the line drop compensation amplitude at certain output current conditions is equal to R1 x G_{ADJ_SINK} x I_{USB_LOAD}, where G_{ADJ_SINK} is line drop compensation gain (2.05µA/A). The R1 value can also be used to adjust the line drop compensation amplitude.

For example, if the output current is 3A and R1 is 34kΩ, the line drop compensation is about 209mV.

The maximum resistance of R1 is 113kΩ (a 22kΩ resistor and 91kΩ resistor in series). When R1 is 113kΩ, the line drop compensation is about 695mV with a 3A output current.

USB Input Over-Voltage (OV) and Discharge

An accurate and fast comparator monitors the input for an over-voltage (OV) condition. If the input voltage rises above the threshold, the input-to-ground discharge path is activated, and the USB current-limit switch is still enabled. When the input voltage falls below 5.75V, the IC exits OVP.

Output Discharge

When a Type-C device is detached, both the USB_IN and USB_OUT discharge resistors are active for 30ms before turning off. After these resistors turn off, their ground resistance exceeds 72.4kΩ.

Over-Current Protection (OCP)

If the load current reaches the current-limit threshold during normal operation, the device starts a 1.7ms counter. The MPQ4228 does not limit the output current within this 1.7ms period (see Figure 7).

If the over-current (OC) condition lasts for longer than 1.7ms, the USB channel enters hiccup mode with a 2ms on time and a 2ms off time. The MPQ4228 resets the counter if the OC signal is removed during the 1.7ms timer.

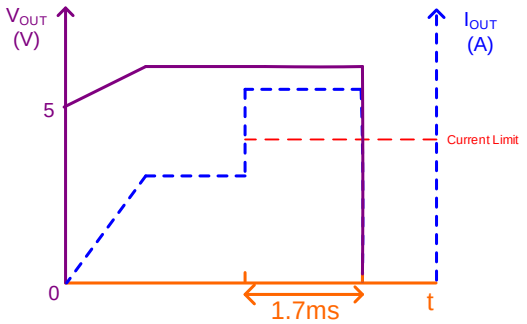

Figure 7: Over-Current Limit

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold before the control loop can respond. If the current reaches an internal

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secondary current-limit level (about 10.5A), a fast turn-off circuit activates to turn off the power FET. This limits the peak current through the switch to limit the input voltage drop.

The fast turn-off response time is about 300ns. If the fast turn off works, the power FET stays off for 80μs. After that time period, the power FET turns on again. If the part is still under a short-circuit condition, the MPQ4228 responds by entering hiccup mode or initiating thermal shutdown. After the short-circuit condition is removed, the MPQ4228 recovers automatically.

Short to Battery Protection

The MPQ4228 provides CC1, CC2, DP, DM, and USB_OUT short to battery protections when the IC is enabled and V_{BUS} is on. USB_OUT short to battery protection requires a parallel Schottky diode when V_{BUS} is off (see Figure 8).

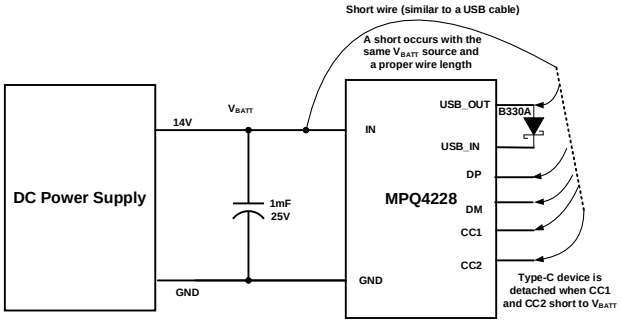

Figure 8: Short to Battery Set-Up

During USB output shorts to battery condition, the USB input will rise up to trigger OVP. The USB input discharge path will turn-on.

During a CC1/CC2 or DP/DM short to battery condition, the MPQ4228 can withstand high voltages on the internal components. Additionally, the ESD breakdown voltage exceeds the battery voltage.

A CC1 or CC2 short to battery can occur if the Type-C port is connected with a cable but has no sink (device is detached).

Fault Indication

FLT is the fault indication pin. FLT is in an open-drain state during shutdown, start-up, and normal operation. It asserts (logic low) during the following conditions: USB over-current/short circuitry, USB_IN over-voltage, DP/DM/CC1/CC2 pin over-voltage (short to battery), or over-temperature conditions.

FLT asserts low until the fault condition is removed, and the USB output voltage goes back to high. There is a 2ms deglitch time during an over-current condition to prevent a FLT false trigger. The FLT signal is not deglitched during over-voltage (short to battery) and over-temperature conditions.

Automatic Detection

The MPQ4228 integrates the USB-dedicated charging port automatic detection function. This function recognizes most mainstream portable devices. It supports the following charging schemes:

- USB Battery Charging Specification BC1.2/ Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A Divider Mode
- 1.2V/1.2V Mode
- USB Type-C 5V @ 3A Mode

The automatic detection function is a state machine that supports all of the DCP charging schemes listed above. The state machine starts in 3A divider mode. If a BC1.2 device is attached, the MPQ4228 exits 3A divider mode and enters BC1.2 short mode.

1.2V/1.2V mode turns on for a short time when the MPQ4228 enters BC1.2 short mode. The MPQ4228 returns to 3A divider mode when the downstream device releases the DP/DM line, or when the downstream device is disconnected.

USB Type-C Mode and VCONN

For the USB Type-C solution, two pins on the connector (CC1 and CC2) establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up resistor (R_P) and pull-down resistor (R_D, about 5.1kΩ) termination model is utilized (see Figure 9).

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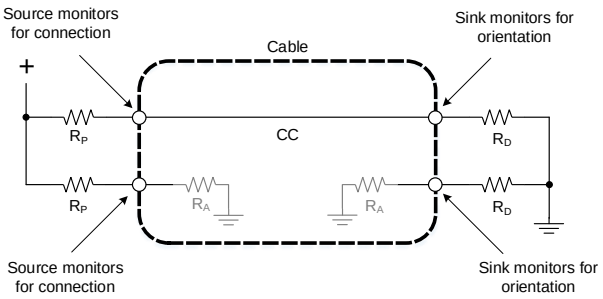

Figure 9: Current Source/Pull-Down CC Model

Initially, a source exposes independent R_P terminations on its CC1 and CC2 pins, and a sink exposes independent R_D terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this connection, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. Choose R_P based on the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Two special termination combinations on the CCx pins (as seen by a source) are defined for directly attached accessory modes: R_A/R_A for audio adapter accessory mode, and R_D/R_D for debug accessory mode. V_{BUS} is disabled in both of these scenarios (see Figure 10).

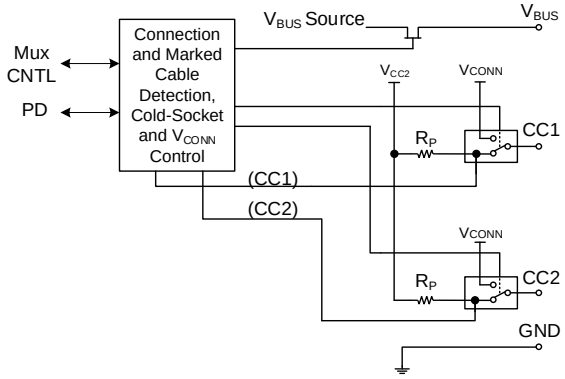

Figure 10: CC1 and CC2 Functional Block

The CC1 and CC2 functional block is described in greater detail below:

1. The source uses a FET to enable/disable power delivery across V_{BUS}. The source is disabled initially.
2. The source supplies pull-up resistors (R_P) on CC1 and CC2, then monitors both to detect a sink. The presence of a pull-down resistor (R_D) on either pin indicates that a sink is being attached. The value of R_P indicates the initial USB Type-C current level supported by the host. The MPQ4228's default R_P is 4.7kΩ, which represents a 3A current level.
3. The source uses the CCx's pull-down characteristic to detect and determine which CC pin is intended to supply power to VCONN (when R_A is detected).
4. Once a sink is detected, the source enables V_{BUS} and V_{CONN}.
5. The source can dynamically adjust the value of R_P to indicate a change in the available USB Type-C current to the sink (e.g at higher temperatures, the MPQ4228 changes R_P to 12.7kΩ to indicate a 1.5A current ability).
6. The source monitors the continued presence of R_D to detect if the sink detaches. When a detach event is detected, the source is removed. V_{BUS} and V_{CONN} return to step 2.

Disable Type-C Mode (Type-A Mode)

During initial start-up, the device sources a 10μA current on the CC1 pin for 50μs. To enter Type-A mode, a 97.6kΩ resistor should be connected to CC1 to create an internal 0.976V voltage. The USB is latched at Type-A mode until power is recycled. While the device operates in Type-A mode, Type-C mode is disabled. This means that the CC attach and detach logic is disabled, and V_{BUS} is always enabled. In Type-A mode, the current limit changes to the Type-A specifications.

To trigger Type-A mode, the external pull-down resistor should be 97.6kΩ. Do not connect an extra capacitor to the CC1 pin.

Negative Temperature Coefficient (NTC) Thermistor and Load Shedding

The MPQ4228 has a built-in NTC comparator that allows the external device's temperature to be sensed via the thermistor mounted near the device. This ensures a safe operating environment and prevents over-temperature conditions.

Connect a resistor from the NTC pin to GND, then connect the thermistor from the NTC pin to VCC2.

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If NTC is pulled between 50% and 70% of VCC2 before VIN start-up, the MPQ4228 enters Type-C 1.5A mode, and the ADJ function is disabled. If NTC is pulled above 70% of VCC2, the MPQ4228 disables the USB output after VIN start up, and the FLT pin stays low.

Once the NTC voltage rises to 50% of VCC2 during normal operation, the USB port's CC pin pull-up resistance (R_P) changes to 12.7kΩ, which indicates that its source capability has changed to 1.5A. Meanwhile, the internal R_D detection threshold changes to be between 0.4V and 1.6V, and the R_A detection threshold drops below 0.4V. The current limit is unchanged. The ADJ function is disabled, and V_{BUS} changes to the buck regulator's default output voltage.

If the NTC voltage falls to 24% of VCC2, the USB Type-C current capability changes to 3A (R_P = 4.7kΩ), and the MPQ4228 resumes normal operation (see Figure 11). Once the NTC voltage rises to 70% of VCC2, the MPQ4228 turns off the USB switch and pulls FLT low. The USB switch turns on when the NTC voltage falls to 60% of VCC2.

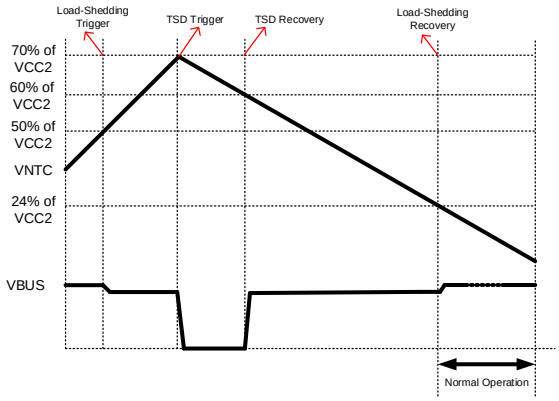

Figure 11: NTC Trigger and Recovery

Internal Load Shedding versus Temperature

The MPQ4228 has an internal temperature-sense function that works alongside the NTC pin. If the NTC voltage exceeds 50% of VCC2 (or the internal sensed temperature exceeds 145°C), the IC initiates load shedding. Disable the NTC function by floating the NTC pin or pulling the NTC pin low.

If the sensed temperature exceeds 145°C, the USB port's CC pin pull-up resistance (R_P) changes to 12.7kΩ to indicate that its source capability is 1.5A. The internal R_D detection threshold also changes to be between 0.4V and 1.6V, while the R_A detection threshold drops below 0.4V. The current limit is unchanged.

If the sensed temperature drops below 105°C and lasts for 16 seconds, the USB Type-C current capability changes back to 3A (R_P = 4.7kΩ). Line drop compensation is disabled when the IC initiates load shedding.

SYSTEM

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the USB switch's silicon die temperature exceeds 165°C, the device shuts down the USB current-limit switch. The CCx functional block and DP/DM functional blocks are active. When the temperature falls below its lower threshold, (typically 145°C), the USB current-limit switch is enabled.

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APPLICATION INFORMATION

Component Selection

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimal efficiency. The inductor value can be calculated with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% to 50% of the maximum load current. The maximum inductor peak current can be estimated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Buck Converter's Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimal performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications, a 100µF electrolytic capacitor and two 4.7µF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be calculated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, estimated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional, high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Buck Converter's Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Calculate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor affect the stability of the regulatory system. Four 22µF ceramic capacitors are recommended for a low output ripple and excellent control loop stability.

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MPQ4228 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.7V, while the falling threshold is about 3.25V. If the application requires a higher UVLO threshold, place an external resistor divider between EN/SYNC and IN to raise the UVLO threshold (see Figure 12).

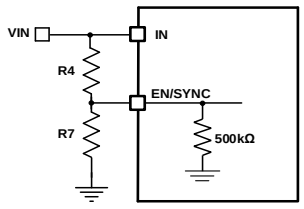

Figure 12: Adjustable UVLO using EN/SYNC Divider

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The UVLO rising and falling thresholds can be calculated with Equation (10) and Equation (11), respectively:

$$INUV_{RISING} = (1+\frac{R4}{500k\Omega//R7})\times V_{EN_RISING} \quad (10)$$

$$INUV_{FALLING} = (1+\frac{R4}{500k\Omega//R7})\times V_{EN_FALLING} \quad (11)$$

Where V_{EN_RISING} is 1.4V, and $V_{EN_FALLING}$ is 1.25V.

When selecting R4, ensure that it is large enough to limit the current flowing into EN/SYNC below 100μA.

ESD Protection for I/O Pins

High ESD levels should be considered for all USB I/O pins.

The CC1 and CC2 pins satisfy ±8kV IEC 61000-4-2 contact discharge ESD ratings and ±15kV IEC 61000-4-2 air discharge ESD ratings.

The DP and DM pins can pass ±8kV IEC 61000-4-2 contact discharge ESD ratings and ±15kV IEC 61000-4-2 air discharge ESD ratings with a small resistor and capacitor (see Figure 13).

Note that the resistor must have be at least 0603 in size to avoid being damaged during ESD tests.

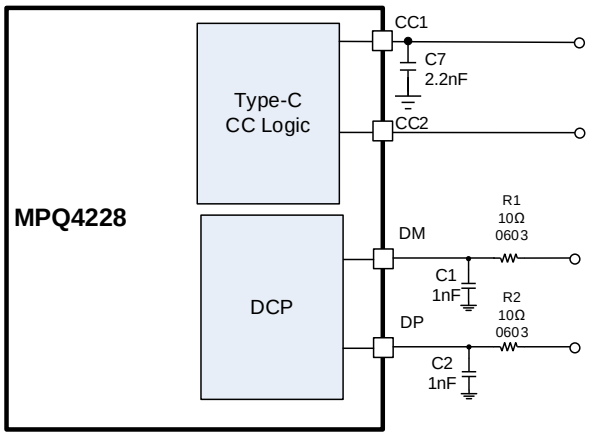

Figure 13: Recommended I/O Pins to Enhance ESD

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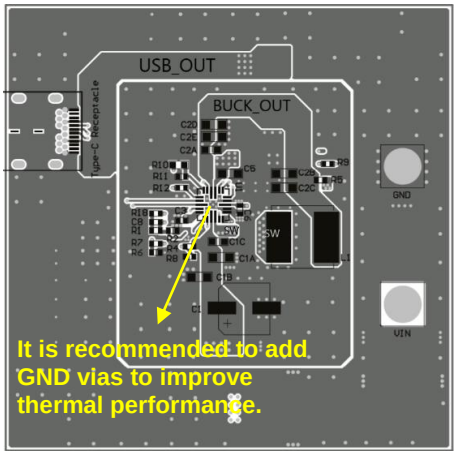
PCB Layout Guidelines [9]

Efficient PCB layout is critical for standard operation and thermal dissipation. Use a 4-layer PCB to improve thermal performance. For the best results, refer to Figure 14 and follow the guidelines below:

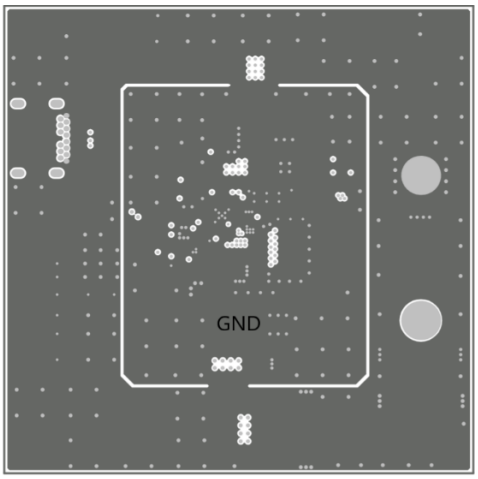
1. Place a ceramic input capacitor as close to IN and GND as possible (especially the small package size (0603) input bypass capacitor).
2. Keep the connection between the input capacitor and IN as short and wide as possible.
3. Place the VCC1/2 capacitor as close to the VCC1/2 and GND pins as possible.
4. Make the trace length between the VCC1/2 pins, VCC1/2 capacitors, and GND as short as possible.
5. Connect a large ground plane directly to GND.
6. Add vias near GND if the bottom layer is a ground plane.
7. Route SW and BST away from sensitive analog areas, such as FB.
8. Place the T-type feedback resistor close to the chip to ensure that the trace connected to FB is as short as possible.
9. Ensure that the SW area is small to reduce the EMC radiated noise.

Note:

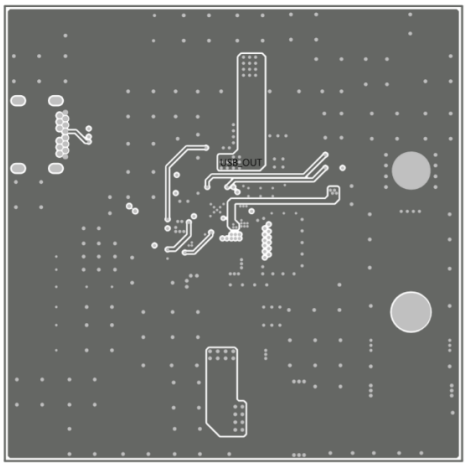
9) The recommended layout is based on Figure 15 on page 26).



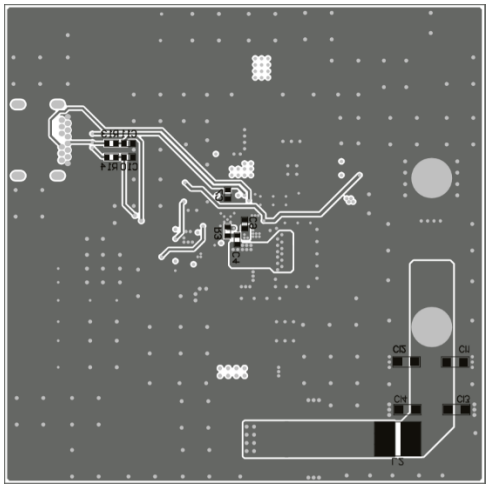
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 14: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

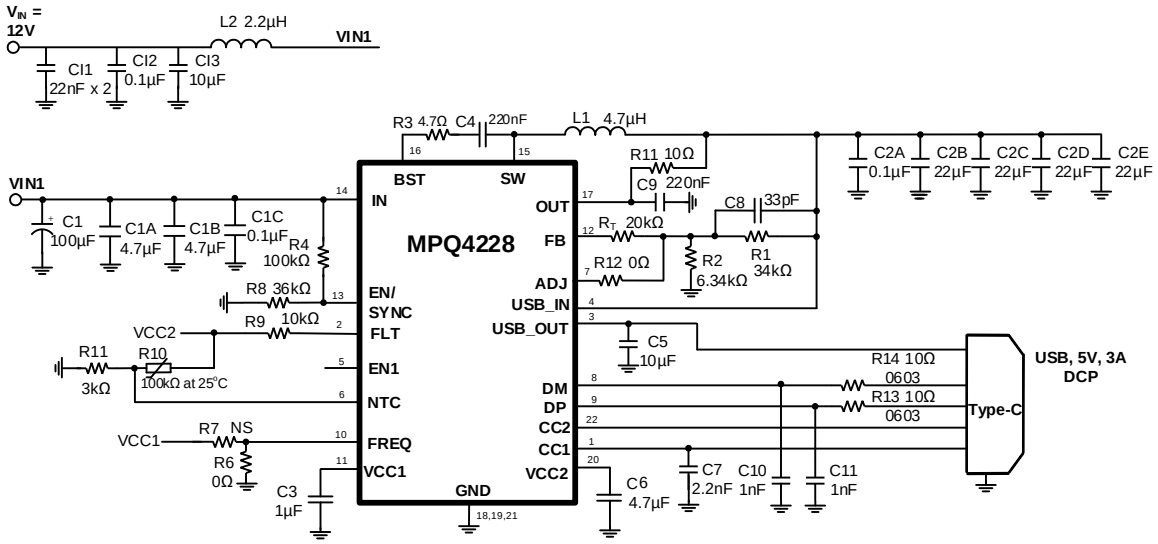

Figure 15: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 420kHz (Type-C DFP with BC1.2 DCP Mode)

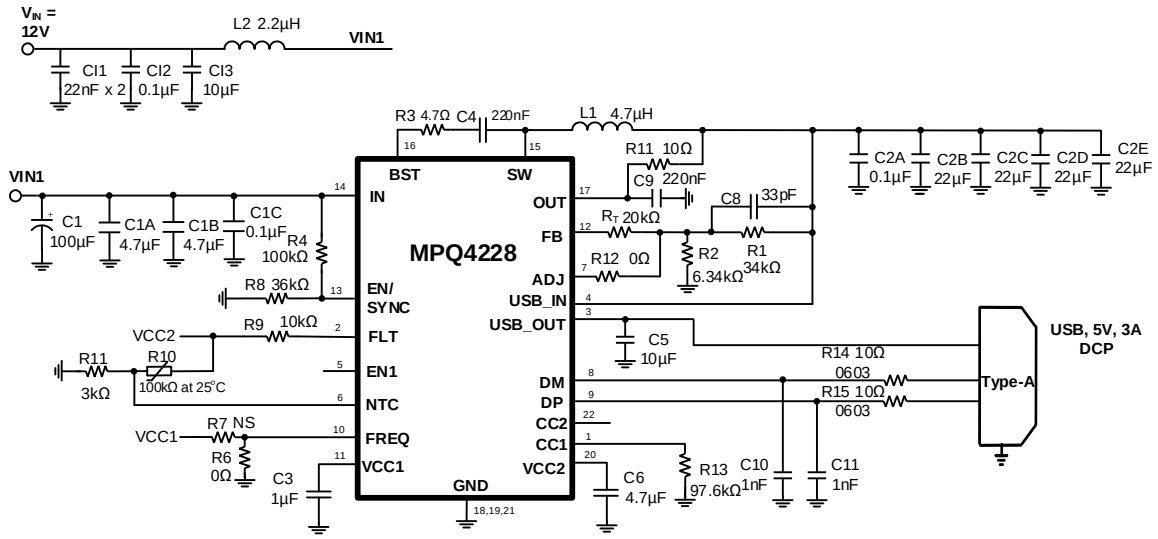

Figure 16: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 420kHz (Type-A Port with BC1.2 DCP Mode)

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TYPICAL APPLICATION CIRCUITS *(continued)*

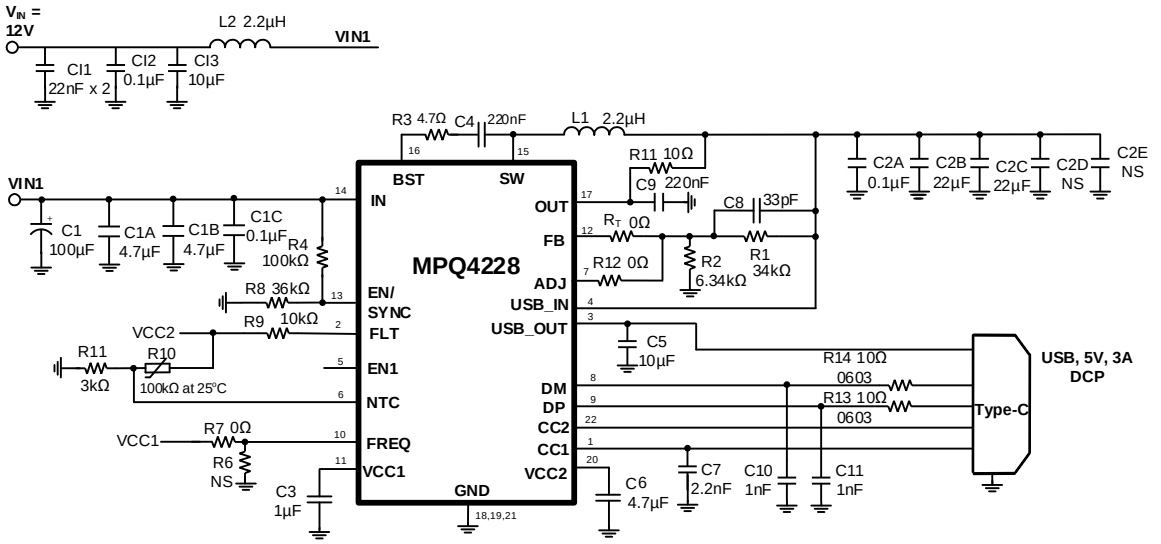

Figure 17: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 2.2MHz (Type-C DFP with BC1.2 DCP Mode)

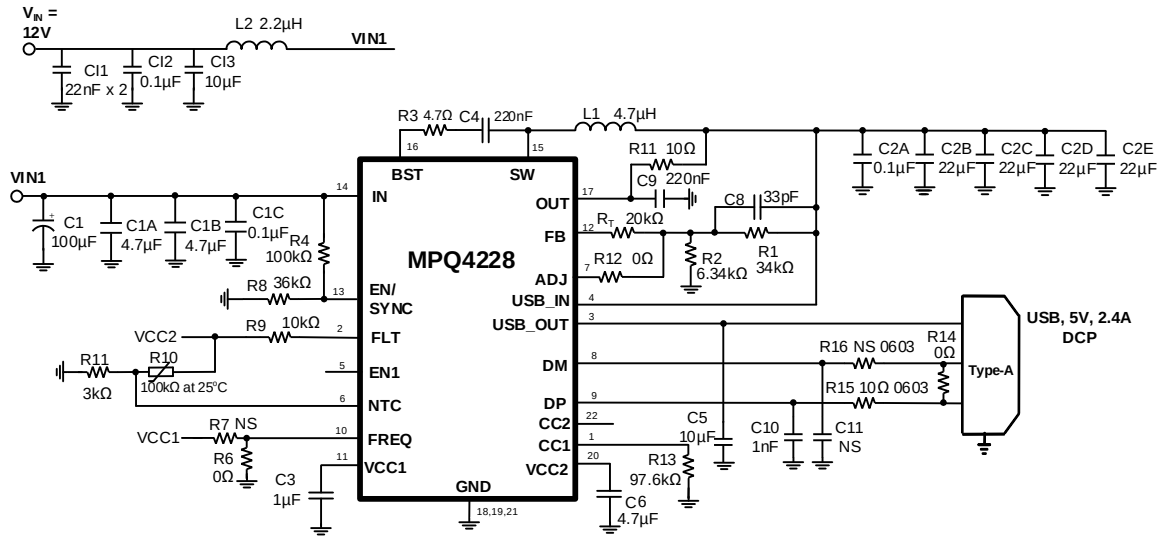

Figure 18: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.4A, f_{SW} = 420kHz (Type-A Port with BC1.2 DCP Mode, Divider 3 Mode)

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TYPICAL APPLICATION CIRCUITS *(continued)*

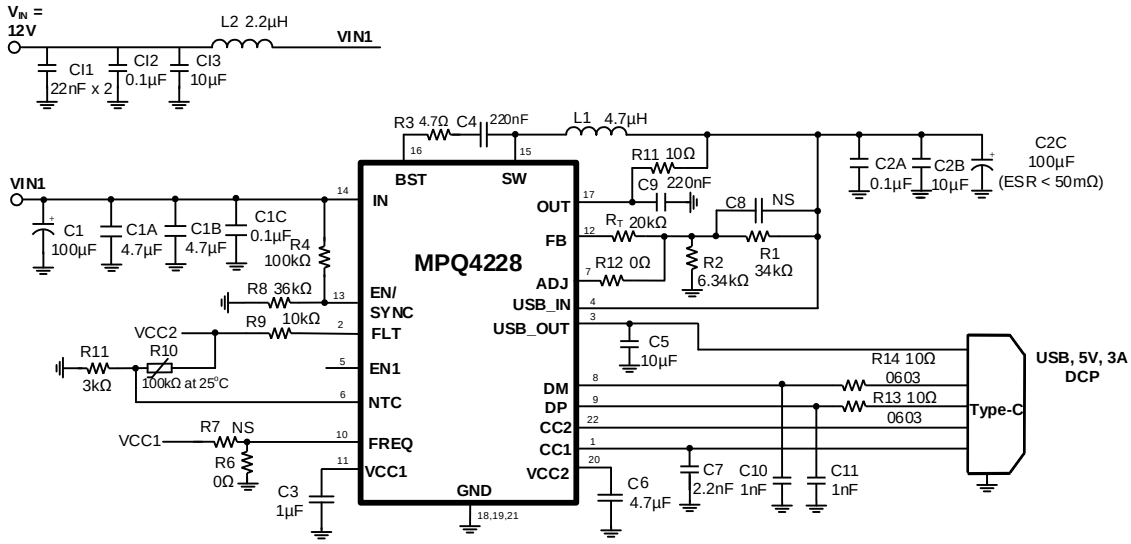

Figure 19: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 420kHz (Type-C DFP with BC1.2 DCP Mode, with Aluminum Buck Output Capacitor)

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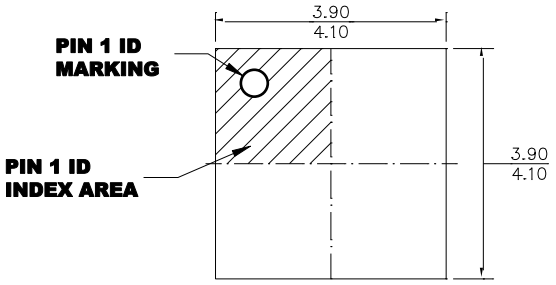
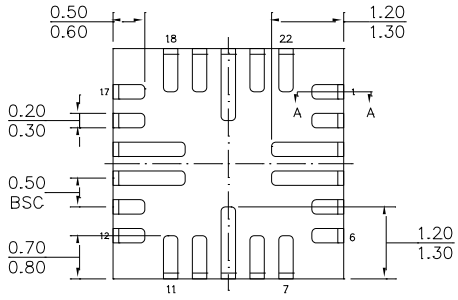
PACKAGE INFORMATION

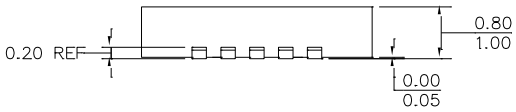
QFN-22 (4mmx4mm)



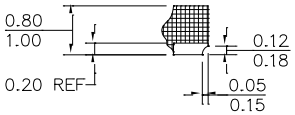
TOP VIEW



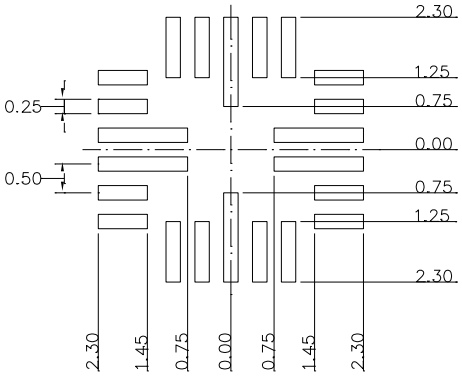
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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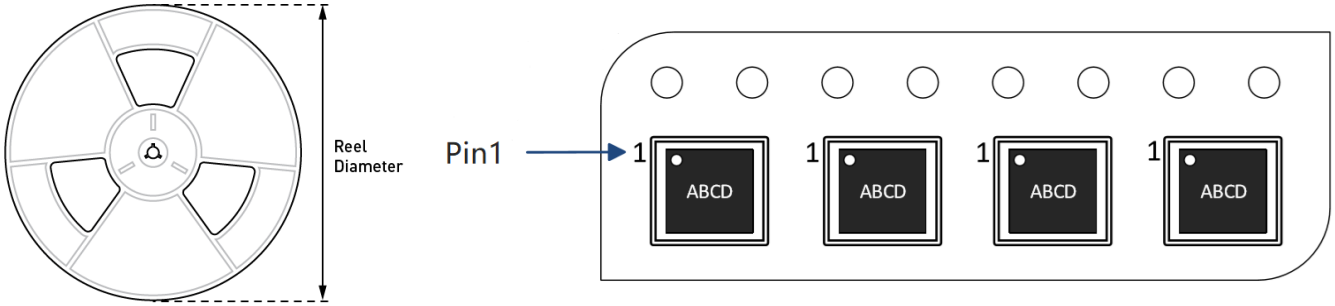
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4228GRE-AEC1-Z	QFN-22 (4mmx4mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/11/2021	Initial Release	-

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