MPQ3431A

21A, High-Efficiency, Fully Integrated, Synchronous Boost Converter with Configurable Input Current Limit, AEC-Q100 Qualified

DESCRIPTION

The MPQ3431A is a 450kHz, fixed-frequency, highly integrated boost converter with a wide input range. The MPQ3431A starts from an input voltage as low as 2.7V and supports up to 20W of load power from a single-cell battery with integrated low $R_{DS(ON)}$ power MOSFETs.

The MPQ3431A adopts constant-off-time (COT) control topology, which provides fast transient response. The MODE pin allows the user to select pulse-skip mode (PSM), forced continuous conduction mode (FCCM), or ultrasonic mode (USM) under light-load conditions. The configurable input current limit provides accurate overload protection. The low-side MOSFET limits the cycle-by-cycle inductor peak current, and the high-side MOSFET eliminates the requirement for an external Schottky diode.

Full protection features include programmable input under-voltage lockout (UVLO) and over-temperature protection (OTP).

The MPQ3431A is available in a QFN-13 (3mmx4mm) package.

FEATURES

- Guaranteed Industrial/Automotive Temp
- 2.7V to 13V Start-Up Voltage
- 0.8V to 13V Operation Voltage
- Up to 16V Output Voltage
- Supports 20W Average Power Load and 40W Peak Power Load from 3.3V
- Configurable Input Current Limit
- 21.5A Internal Switch Current Limit
- Integrated 6mΩ and 9.5mΩ Power MOSFETs
- 95% Efficiency for 3.6V VIN to 9V/3A
- Selectable PSM, >23kHz USM, and FCCM under Light-Load Conditions
- 450kHz Fixed Switching Frequency
- Adaptive COT for Fast Transient Response
- External Soft Start and Compensation Pins
- Programmable UVLO and Hysteresis
- 150°C Over-Temperature Protection (OTP)
- Available in a QFN-13 (3mmx4mm) Package
- AEC-Q100 Qualified

APPLICATIONS

- Automotive Boost
- Super Capacitors
- Backup Batteries

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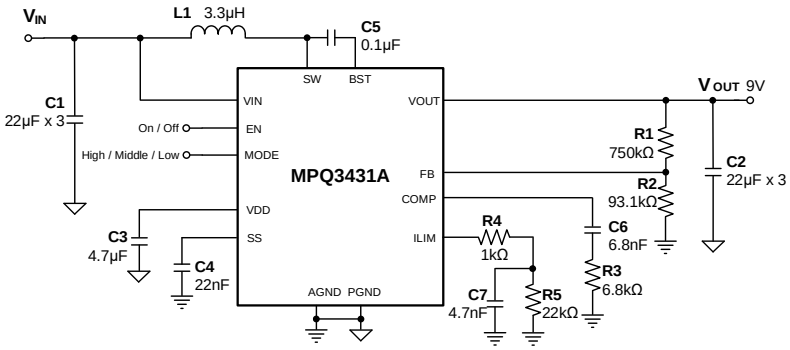
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3431AGL-AEC1	QFN-13 (3mmx4mm)	*See Below*	Level 1

* For Tape & Reel, add suffix –Z (e.g. MPQ3431AGL-AEC1–Z).

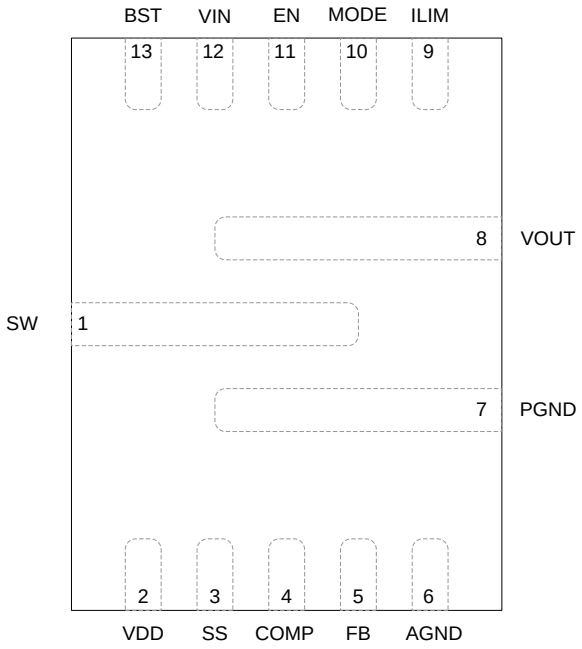
TOP MARKING

MPYW
3431
ALLL

MP: MPS prefix
Y: Year code
W: Week code
3431A: Part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-13 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Converter switch.** SW is connected to the drain of the internal low-side power MOSFET (LS-FET) and the source of the internal synchronous high-side power MOSFET (HS-FET). Connect the power inductor to SW.
2	VDD	**Internal bias supply.** Decouple VDD with a 4.7μF ceramic capacitor placed as close to VDD as possible. When VIN is greater than 3.4V, VDD is powered by VIN. Otherwise, VDD is powered by the higher voltage of either VIN or VOUT. If the bias voltage connected to VDD is above 3.4V, the regulator from VIN and VOUT is disabled. The VDD regulator starts working when VIN exceeds about 0.9V if EN is high. Supply VIN with a power source above 2.7V during VIN start-up to provide enough VDD power voltage.
3	SS	**Soft-start programming.** Place a capacitor from SS to AGND to set the VOUT rising slew rate.
4	COMP	**Internal error amplifier output.** Connect a capacitor and resistor in series from COMP to AGND for loop compensation.
5	FB	**Feedback input.** Connect a resistor divider from VOUT to FB.
6	AGND	**Analog ground.**
7	PGND	**Power ground.**
8	VOUT	**Output.** VOUT is connected to the drain of the HS-FET. VOUT powers VDD when VOUT is above VIN and VIN is below 3.4V.
9	ILIM	**Input current limit setting.** A resistor in parallel with a capacitor is used to set the input current limit. Place a 1kΩ resistor in series with ILIM to avoid noise injection. If the input current limit function is not used, connect ILIM to AGND.
10	MODE	**MODE selection.** If MODE is floating, the MPQ3431A works in ultrasonic mode (USM). If MODE is high, the MPQ3431A works in forced continuous conduction mode (FCCM). If MODE is low, the MPQ3431A works in pulse-skip mode (PSM).
11	EN	**Chip enable control.** When not in use, connect EN to VIN for automatic start-up. EN can program the VIN UVLO. Do not leave EN floating.
12	VIN	**Input supply.** VIN must be bypassed locally. Supply VIN with power source greater than 2.7V during VIN start-up to provide enough VDD power voltage.
13	BST	**Bootstrap.** A capacitor between BST and SW powers the synchronous HS-FET.

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ABSOLUTE MAXIMUM RATINGS (1)

SW .....-0.3V (-3.5V for <10ns) to +18V (22V for <10ns)
VIN, EN, MODE, VOUT ..... -0.3V to +18V
BST ..... -0.3V to V_{SW} + 4.5V
All other pins..... -0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (2) 4W (5)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Rating

Human-body model (HBM) .....±2kV
Charged-device model (CDM) .....±750V

Recommended Operating Conditions (3)

Start-up input voltage (V_{ST}) ..... 2.7V to 13V
Operation input voltage (V_{IN})..... 0.8V to 13V
Start-up input voltage with VDD bias (V_{ST2})..... ..... 0.9V to 13V
Maximum external VDD bias voltage 3.6V (4)
Boost output voltage (V_{OUT})..... V_{IN} to 16V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-13 (3mmx4mm)			
EVQ3431A-L-00A (5)	31	4	°C/W
JESD51-7 (6)	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) When the external VDD bias voltage drops below the normal VDD regulated voltage, the external power prevents the current from flowing out of VDD.
5) Measured on EV3431-L-00A, 4-layer 63mmx63mm PCB.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Start-up input voltage	V_{ST}	No VDD bias	2.7		13	V
		V_{DD} = 3V	0.9		13	V
Operating input voltage	V_{IN}		0.8		13	V
Operating VDD voltage [8]	V_{DD}	V_{IN} = 2.7V, 0mA to 10mA	2.3	2.55		V
		V_{IN} = 12V, 0mA to 15mA		3.4		V
VDD UVLO rising [8]	VDD_{UVLO-R}	VDD rising	2.2	2.4	2.6	V
VDD UVLO falling	VDD_{UVLO-F}	VDD falling	2	2.2	2.4	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on VIN			2	µA
Quiescent current	I_Q	V_{FB} = 1.1V, VIN = 3V, V_{OUT} = 9V, no switching, measured on VIN			25	µA
		V_{FB} = 1.1V, VIN = 3V, V_{OUT} = 9V, no switching, measured on VOUT		450	550	µA
Enable (EN) Control						
EN turn-on threshold voltage	V_{EN-ON}	V_{EN} rising (switching)		1.23		V
EN high threshold voltage	V_{EN-H}	V_{EN} rising (micro power)			1.0	V
EN low threshold voltage	V_{EN-L}	V_{EN} falling (micro power)	0.4			V
EN turn-on hysteresis current	I_{EN-HYS}	1.0V < EN < V_{EN-ON}	3.5	5	6.5	µA
EN input current	I_{EN}	V_{EN} = 0V, 1.5V		0		µA
EN turn-on delay		EN on to switching		65		µs
Frequency						
Switching frequency	f_{SW}		380	450	520	kHz
LS-FET minimum on time [9]	t_{MIN-ON}			80		ns
LS-FET maximum on time	t_{MAX-ON}			7.1		µs
Loop Control						
FB reference voltage	V_{REF}	T_J = 25°C	0.99	1	1.01	V
		T_J = -40°C to +125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.1V			50	nA
Error amp. voltage gain [10]	A_{V-EA}			300		V/V
Error amp. transconductance	G_{EA}			410		µA/V
Error amp. max output current		V_{FB} = 0.8V, V_{COMP} = 1V		60		µA
		V_{FB} = 1.2V, V_{COMP} = 1V		-60		µA
COMP to current gain	G_{CS}			32		A/V
COMP PSM threshold [9]	V_{PSM}	V_{MODE} = 0V		0.5		V
COMP high clamp		V_{FB} = 0.8V		2.6		V
Soft-start charge current	I_{SS}		6	7.5	9	µA
MODE Selection						
PSM MODE tri-state region	$V_{MODE-TRI}$				0.7	V
USM MODE tri-state region [11]			0.9		1.2	
FCCM MODE tri-state region			1.6		VDD	
Ultrasonic mode frequency	f_{USM}		23	33		kHz
HS-FET zero-current detection (ZCD) (PSM)		V_{FB} = 1V, L = 1.5µH, V_{OUT} = 9V, 25°C	-200	0	+300	mA
		V_{FB} = 1V, L = 1.5µH, V_{OUT} = 9V, -40°C to +125°C	-300	0	+400	mA
HS-FET ZCD (USM, FCCM) [9] [12]		V_{FB} = 1.1V			-2	A

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ELECTRICAL CHARACTERISTICS *(continued)*

VIN = V_{EN} = 3.3V, T_J = -40°C to +125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Switch						
Low-side switch on resistance	R_{ON-L}			6		mΩ
High-side synchronous switch on resistance	R_{ON-H}			9.5		mΩ
Low-side switch leakage current		V_{SW} = 16V, T_J = 25°C			0.15	μA
High-side switch leakage current		V_{OUT} = 16V, V_{SW} = 0V, T_J = 25°C			0.15	μA
BST Power						
BST voltage				3.3		V
Current Limit						
Switching current limit	$I_{PK-LIMT}$		15	21	26	A
ILIM current gain	I_{ILIM}	ILIM current vs. input current		4		μA/A
ILIM threshold voltage	V_{ILIM}			1.02		V
Protection						
Output OVP threshold				16.5		V
Output OVP hysteresis				0.2		V
Thermal Protection						
Thermal shutdown (9)	T_{SD}			175		°C
Thermal shutdown hysteresis (9)	T_{SD-HYS}			25		°C

Notes:

7) Guaranteed by over-temperature correlation. Not tested in production.
8) VDD regulation voltage from 2.7V. VIN is above the VDD UVLO rising threshold in each unit, which can guarantee that the IC starts up with 2.7V V_{IN}.
9) Guaranteed by sample characterization. Not tested in production.
10) Guaranteed by design. Not tested in production.
11) Add an external voltage within this range or float MODE for USM.
12) The HS-FET ZCD is below -2A in USM and FCCM.

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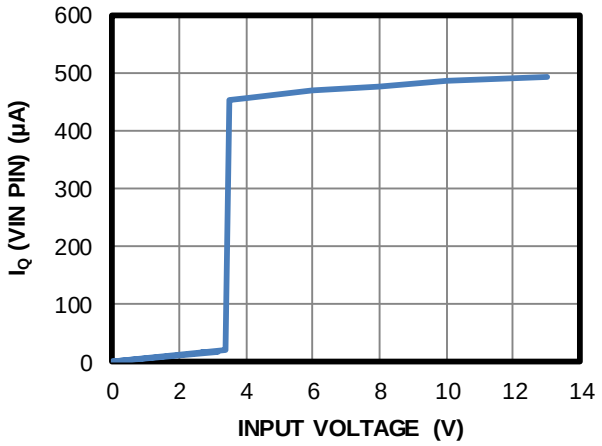
TYPICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

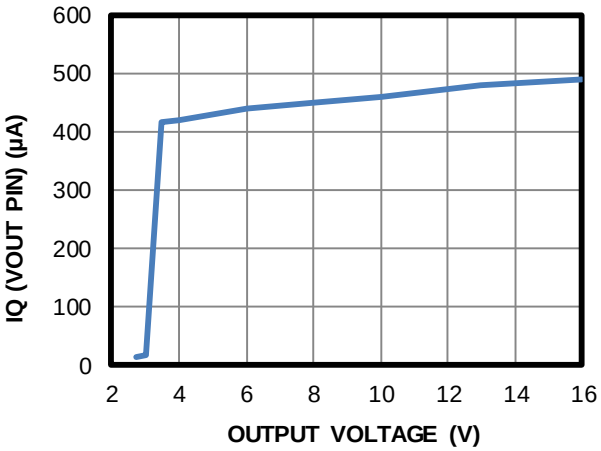
Quiescent Current (VIN Pin) vs. Input Voltage

V_{OUT} = 9V

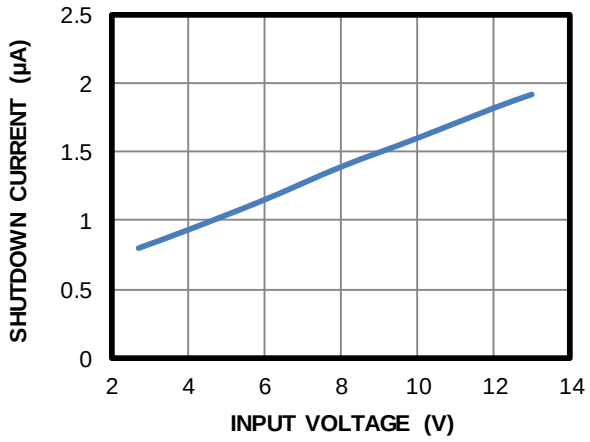


Quiescent Current (VOUT pin) vs. Output Voltage

V_{IN} = 3V

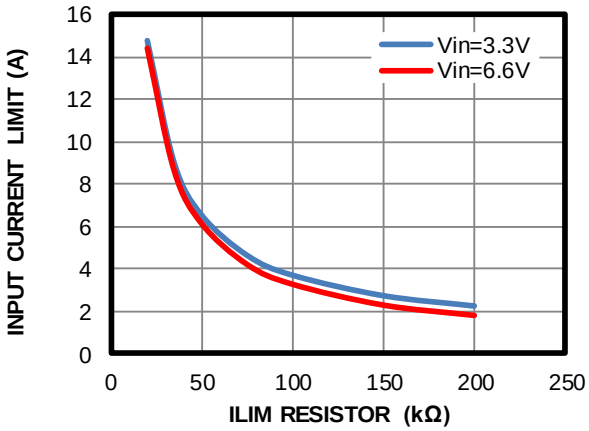


Shutdown Current vs. Input Voltage



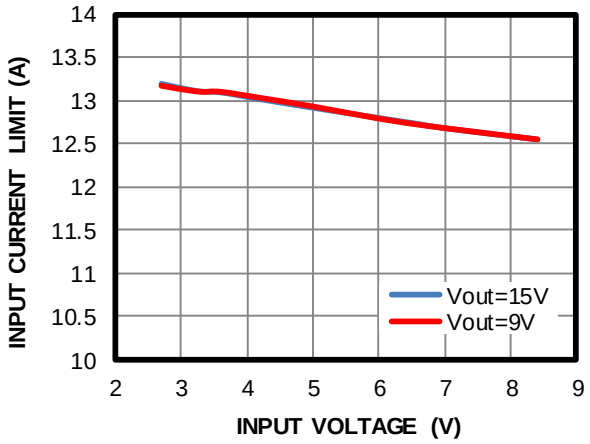
Input Current Limit vs. ILIM Resistor

V_{OUT} = 9V



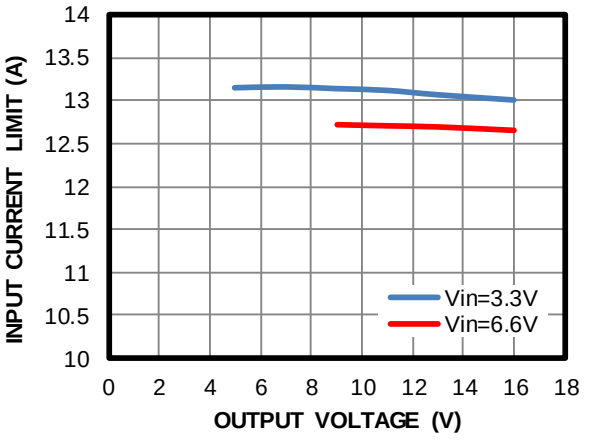
Input Current Limit vs. Input Voltage

R_{ILIM} = 22kΩ



Input Current Limit vs. Output Voltage

R_{ILIM} = 22kΩ



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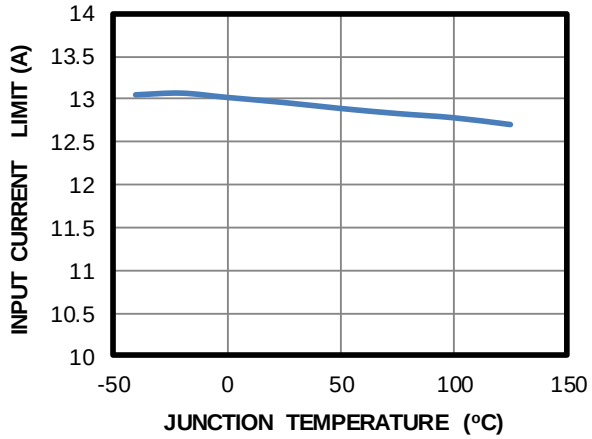
TYPICAL CHARACTERISTICS *(continued)*

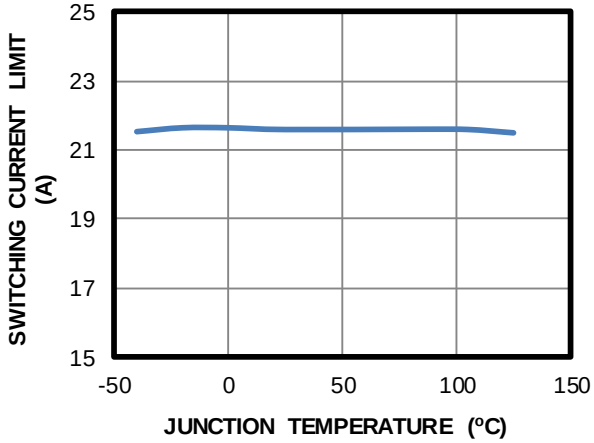
V_{IN} = V_{EN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

Input Current Limit vs. Junction Temperature

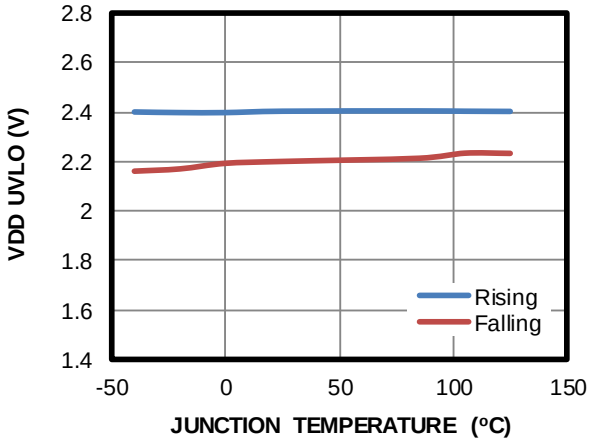
R_{ILIM} = 22kΩ



Switching Current Limit vs. Junction Temperature

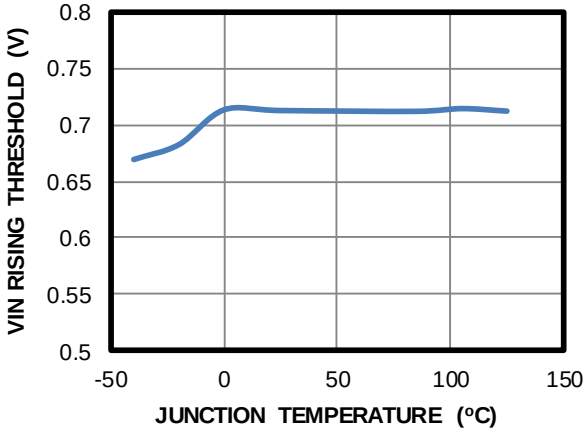


VDD Under-Voltage Lockout (UVLO) vs. Junction Temperature



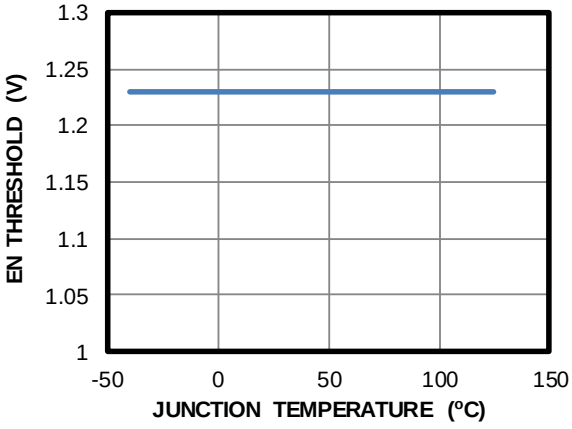
VIN Rising Threshold vs. Junction Temperature

V_{DD} bias = 3.3V

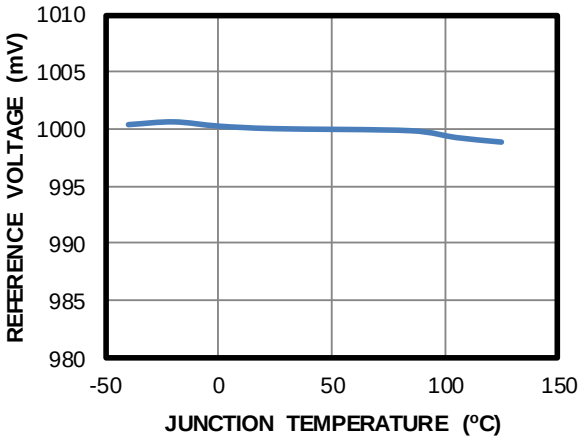


EN Threshold vs. Junction Temperature

IC start-up switching



Reference Voltage vs. Junction Temperature



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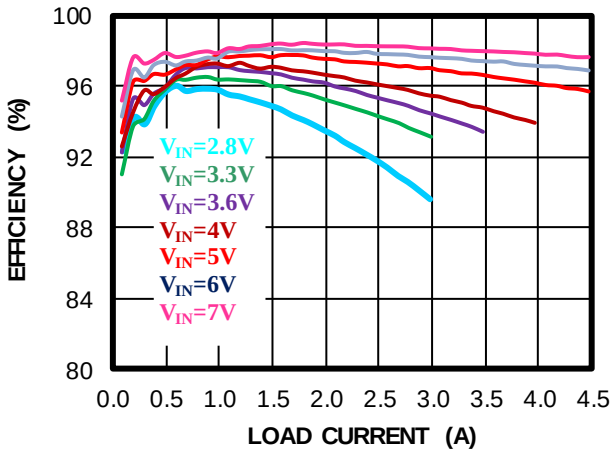
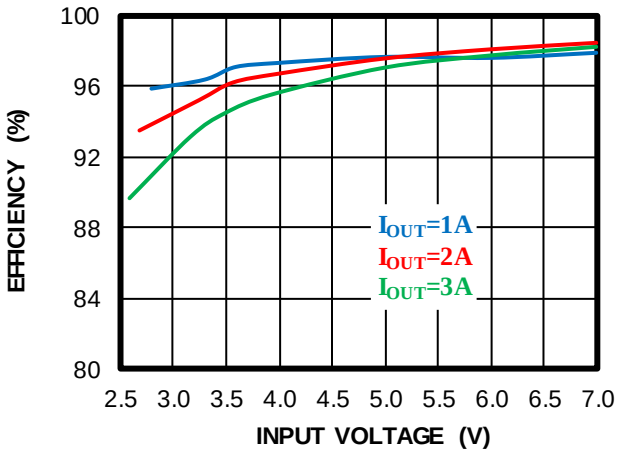
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

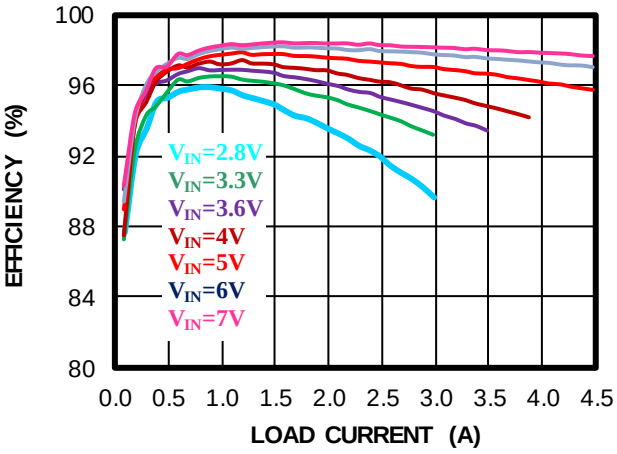
Load Efficiency
PSM



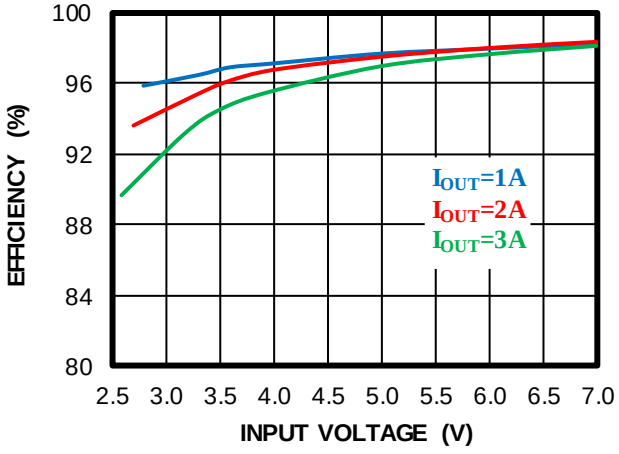
Line Efficiency
PSM



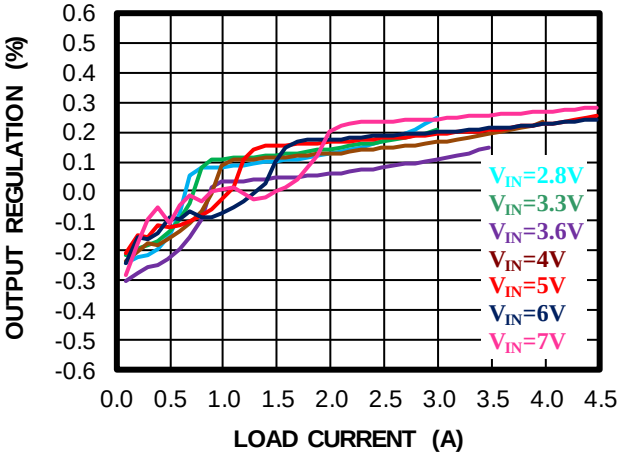
Load Efficiency
CCM



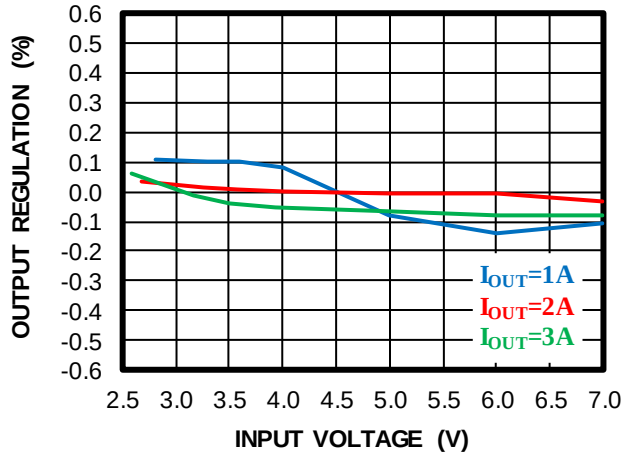
Line Efficiency
CCM



Load Regulation
PSM



Line Regulation
PSM



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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

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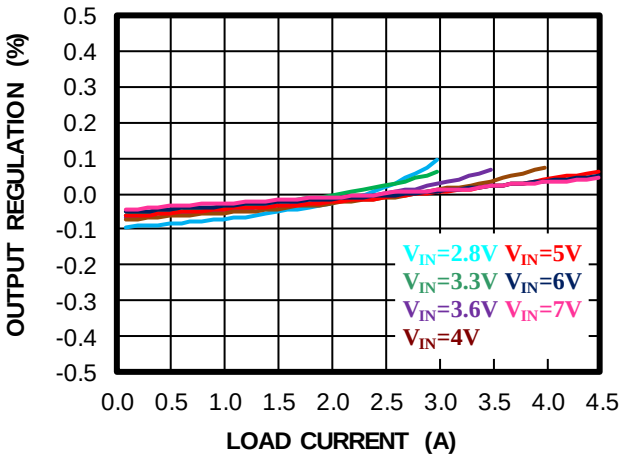
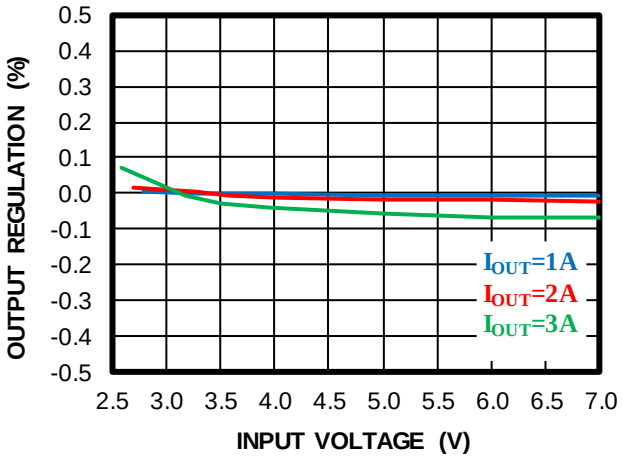
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

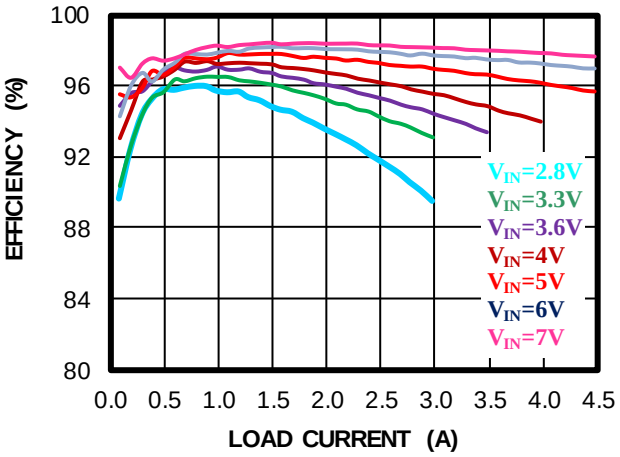
Load Regulation
CCM



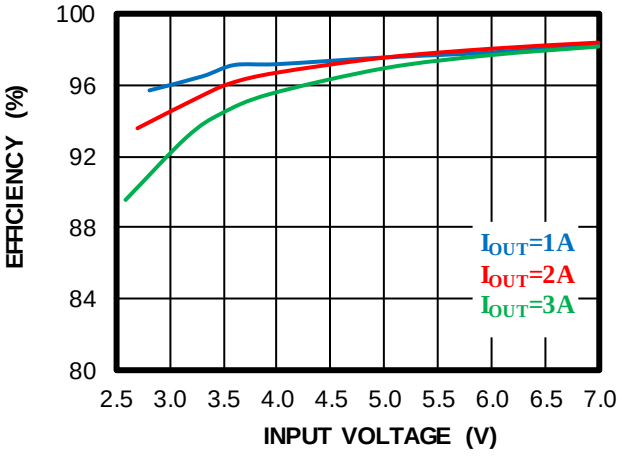
Line Regulation
CCM



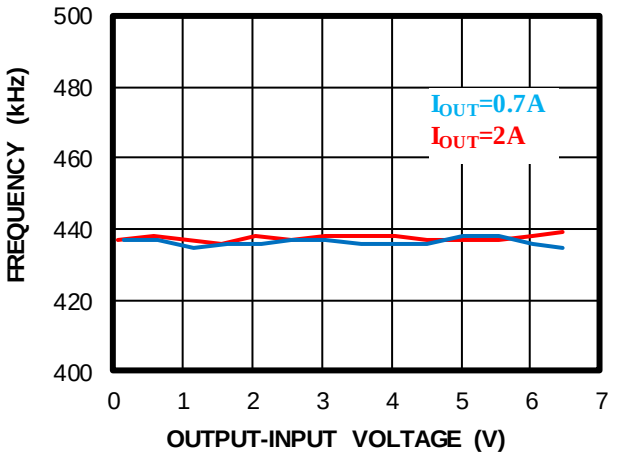
Load Efficiency
USM



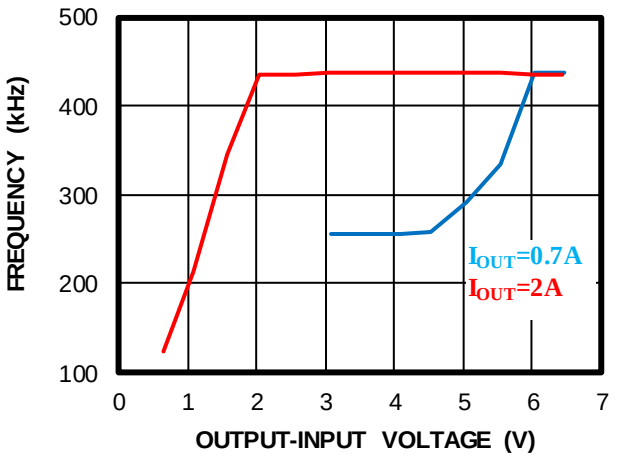
Line Efficiency
USM



Frequency vs. ΔV
CCM



Frequency vs. ΔV
PSM



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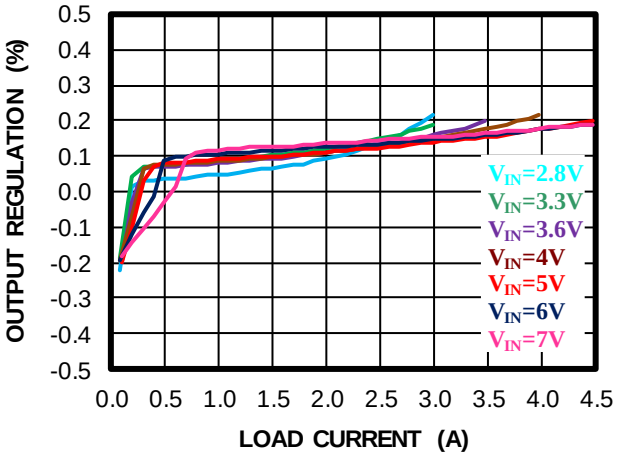
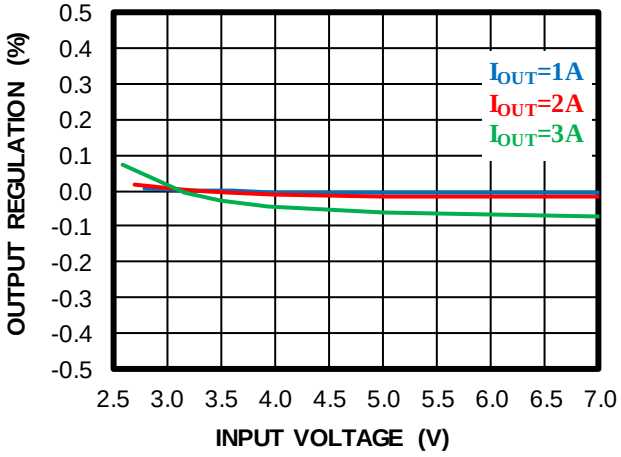
V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

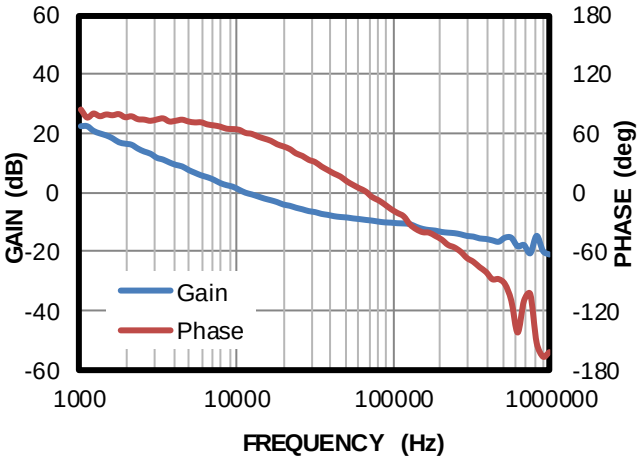
Load Regulation
USM



Line Regulation
USM



Bode Plot
I_{OUT} = 3.5A



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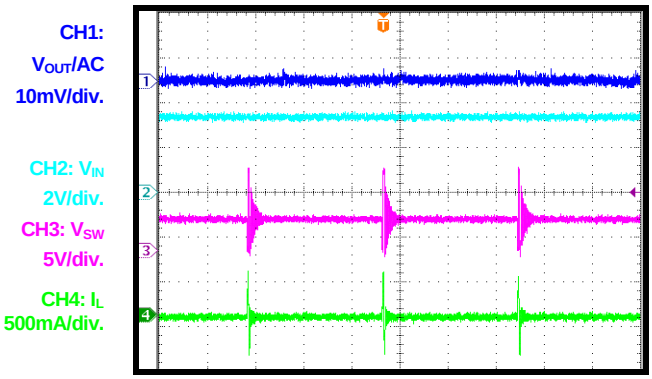
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

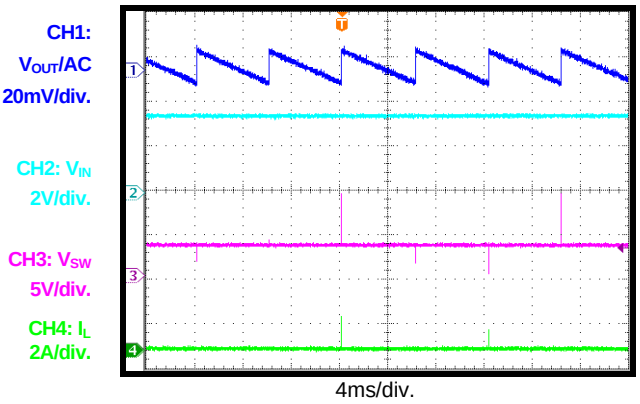
Steady State

I_{OUT} = 0A, USM



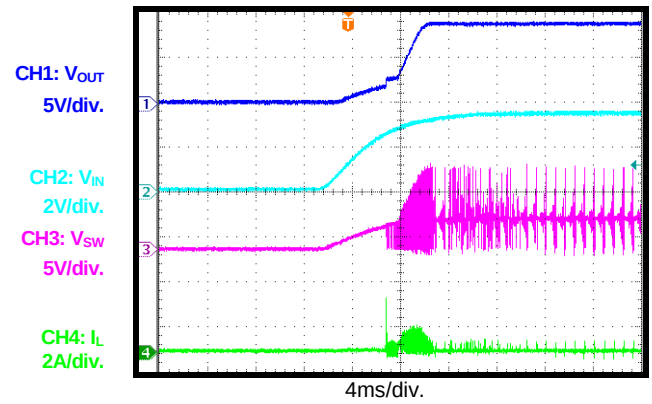
Steady State

I_{OUT} = 0A, PSM



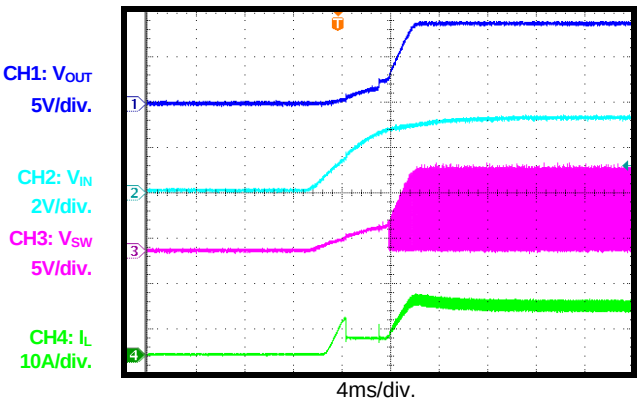
VIN Start-Up

I_{OUT} = 0A



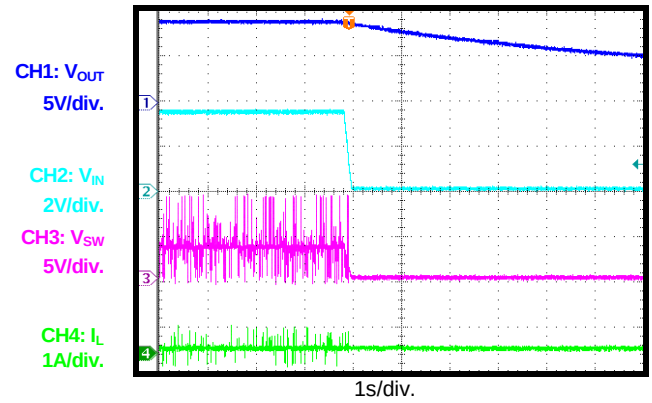
VIN Start-Up

I_{OUT} = 3.5A



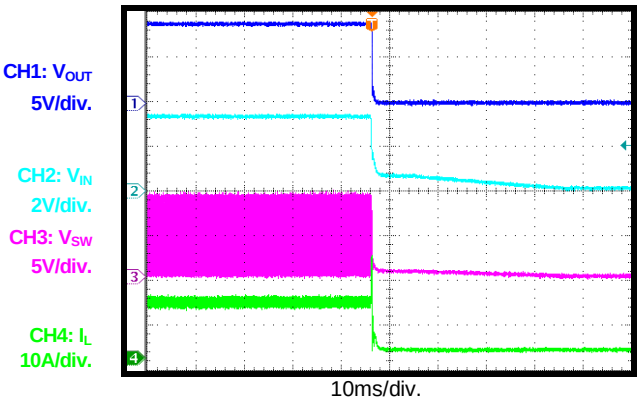
VIN Shutdown

I_{OUT} = 0A



VIN Shutdown

I_{OUT} = 3.5A



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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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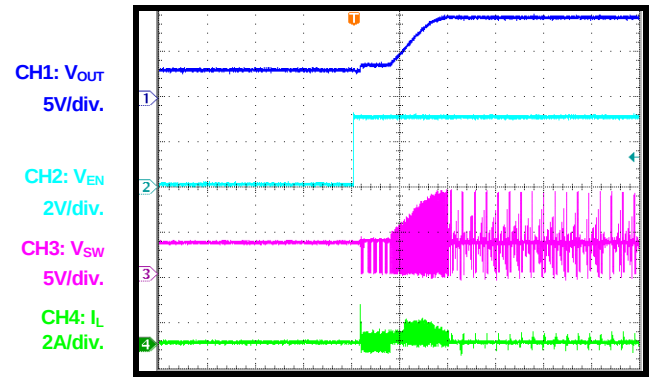
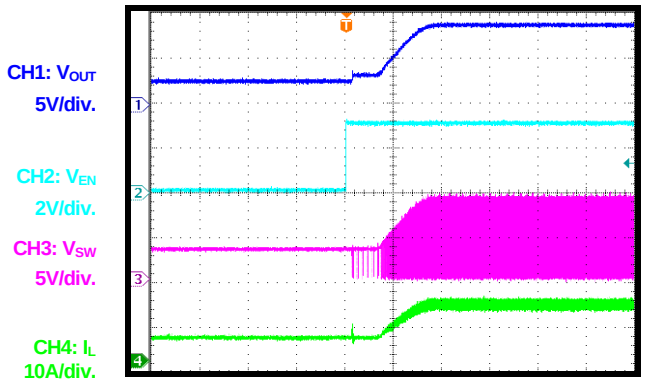
EN Start-Up

I_{OUT} = 0A



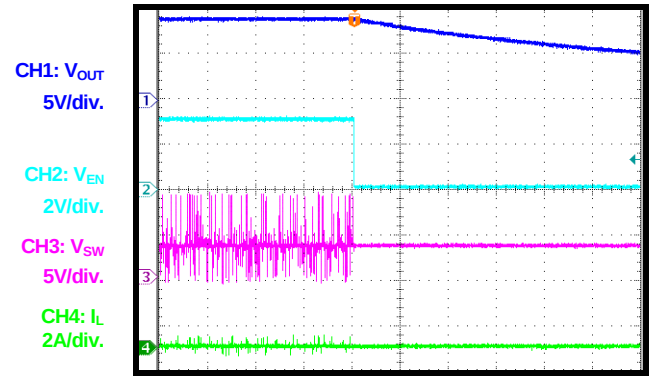
EN Start-Up

I_{OUT} = 3.5A



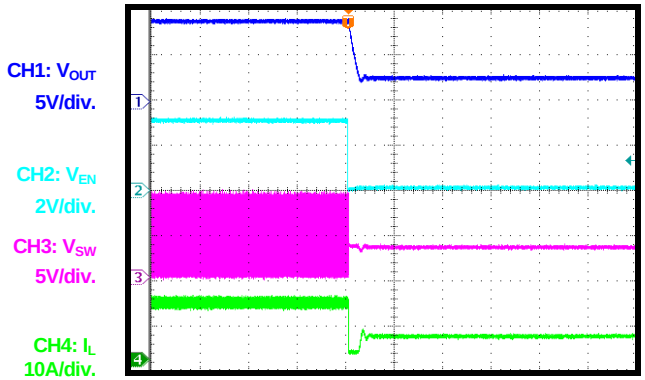
EN Shutdown

I_{OUT} = 0A



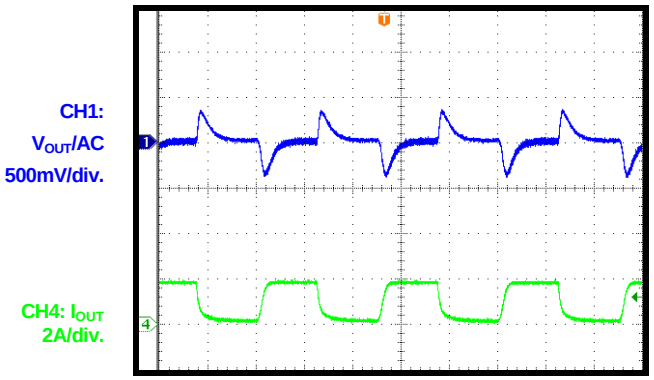
EN Shutdown

I_{OUT} = 3.5A



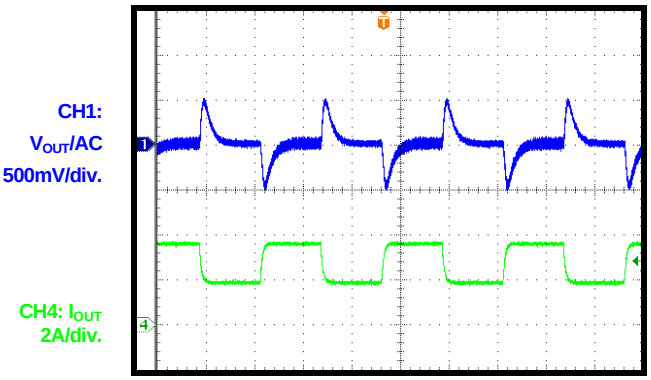
Load Transient

I_{OUT} = 0A to 1.75A, I_{RAMP} = 25mA/µs, USM



Load Transient

I_{OUT} = 3.5A to 1.75A, I_{RAMP} = 25mA/µs



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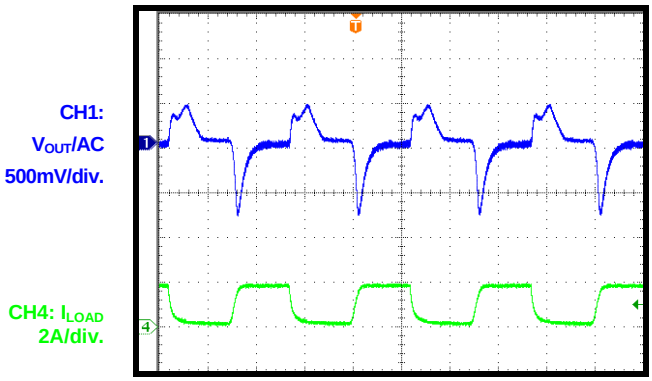
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

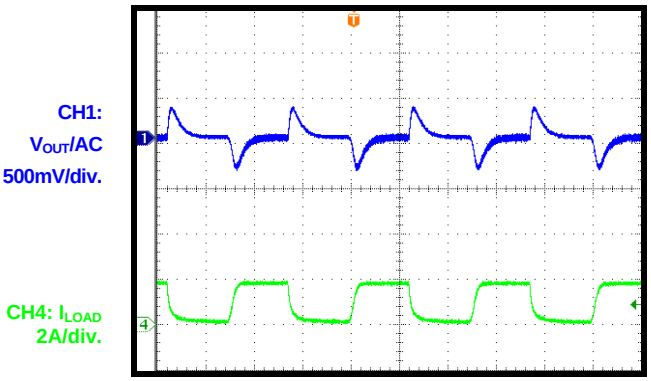
Load Transient

I_{OUT} = 0A to 1.75A, I_{RAMP} = 25mA/µs, PSM



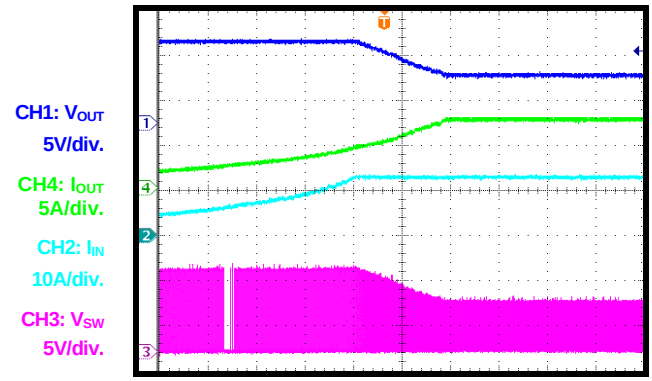
Load Transient

I_{OUT} = 0A to 1.75A, I_{RAMP} = 25mA/µs, FCCM



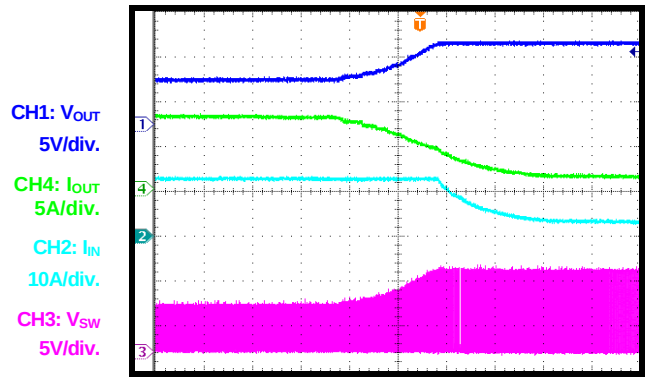
Over-Current Entry

Increase output current slowly



Over-Current Recovery

Decrease output current slowly



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FUNCTIONAL BLOCK DIAGRAM

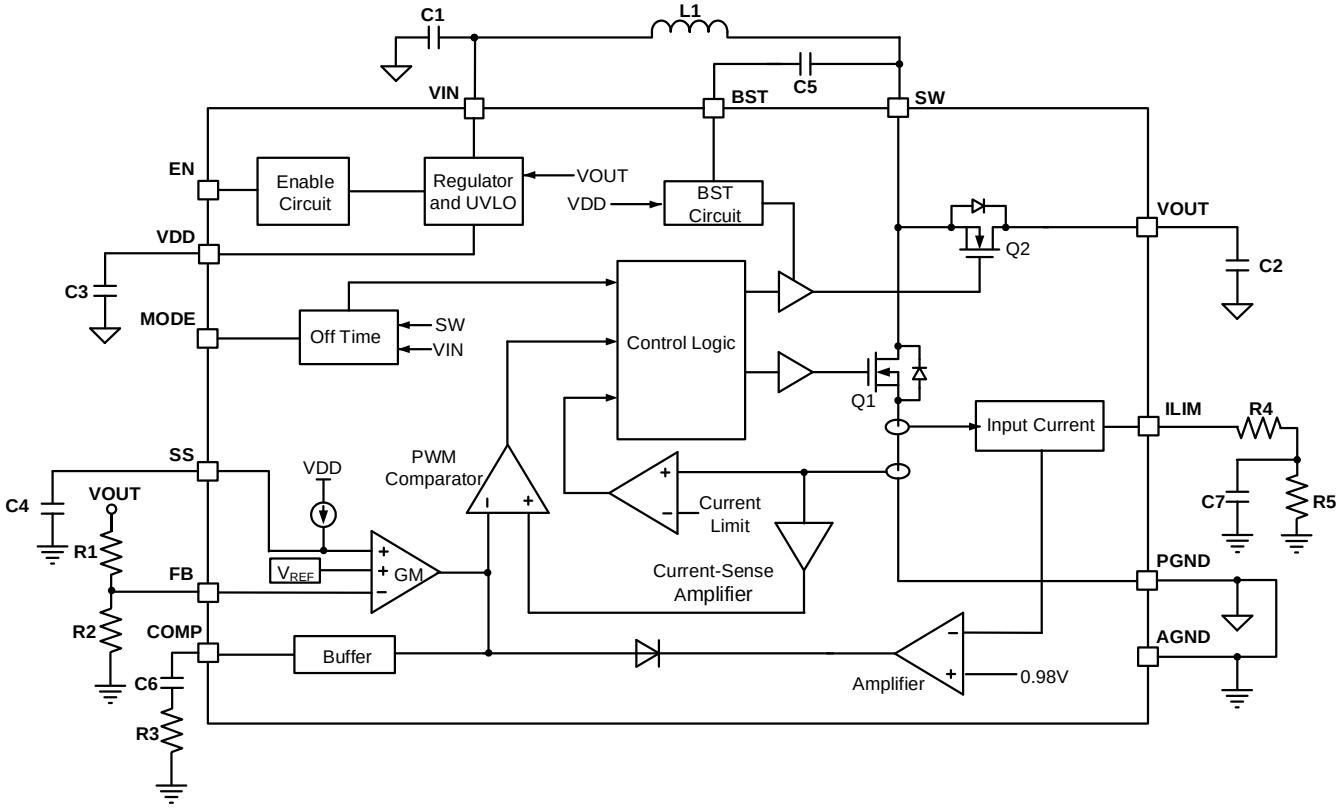

Figure 1: Functional Block Diagram

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OPERATION

The MPQ3431A is a 450kHz, fixed-frequency, high-efficiency boost converter with a wide input range. Its fully integrated low $R_{DS(ON)}$ MOSFETs provide small size and high efficiency for high-power step-up applications. Constant-off-time (COT) control provides fast transient response, while MODE provides flexible light-load performance design.

Boost Operation

The MPQ3431A uses COT control to regulate the output voltage. At the beginning of each cycle, the low-side N-channel MOSFET (LS-FET) (Q1) turns on and forces the inductor current to rise.

The device senses the current through the LS-FET. If the current signal rises above the COMP voltage (V_{COMP}), the pulse-width modulation (PWM) comparator flips and turns the LS-FET off. Then the inductor current flows to the output capacitor through the high-side switch MOSFET (HS-FET), and the inductor current decreases. V_{COMP} is an amplifier output that compares the feedback voltage (V_{FB}) against the internal reference voltage.

After a fixed off time, the LS-FET turns on again and the cycle repeats. In each cycle, the LS-FET off time is determined by the V_{IN} / V_{OUT} ratio, and the on time is controlled by V_{COMP}. The inductor peak current is controlled by COMP, and COMP is controlled by the output voltage. Therefore, the output voltage regulates the inductor current.

Operation Mode

The MPQ3431A works with a 450kHz quasi-constant frequency with PWM control in heavy-load conditions. When the load current decreases, the MPQ3431A works in forced continuous conduction mode (FCCM), pulse-skip mode (PSM), or ultrasonic mode (USM) based on the MODE setting. Select the mode before operating the device.

Forced Continuous Conduction Mode (FCCM)

If MODE is high (>1.6V), the MPQ3431A works in a fixed-frequency PWM mode for any load conditions. In this condition, the off time is determined by the internal circuit to achieve the 470kHz frequency based on the V_{IN} / V_{OUT} ratio.

When the load decreases, the average input current drops, and the inductor current from VOUT to VIN may become negative during the off time (while the LS-FET is off and HS-FET is on). This forces the inductor current to work in forced continuous conduction mode (FCCM) with a fixed frequency, and produces a lower V_{OUT} ripple than in PSM.

Pulse-Skip Mode (PSM)

The device works in PSM under light-load conditions if the MODE voltage (V_{MODE}) is below 0.7V. Once the inductor current drops to 0A, the HS-FET turns off to stop current flowing from VOUT to VIN, forcing the inductor current to work in discontinuous conduction mode (DCM). At the same time, the internal off time becomes longer when the MPQ3431A enters DCM. The off time is inversely proportional to the HS-FET on period in each cycle. In deep DCM conditions, the MPQ3431A slows down the switching frequency and saves power loss.

If V_{COMP} drops to the 0.5V PSM threshold, the MPQ3431A stops switching to further decrease the switching power loss. Switching resumes once V_{COMP} exceeds 0.5V. The switching pulse skips based on V_{COMP} under light-load conditions. PSM has much higher efficiency than FCCM under light-load conditions, but the V_{OUT} ripple may be higher, and the frequency may go down and produce audible noise.

Frequency is low in DCM, and if the LS-FET has a prolonged off time it does not turn on. If the load increases and COMP runs higher, the off time shortens and the MPQ3431A returns to the regular 600kHz fixed frequency, so the loop can respond to high-load currents.

Ultrasonic Mode (USM)

To prevent audible noise when there is a switching frequency below 20kHz in PSM, the MPQ3431A implements USM by floating MODE or setting MODE to the USM range, which is between 0.9V and 1.2V. In USM, the inductor current works in DCM, and the frequency stretches as if in PSM, when the load decreases to a moderate level. However, the

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switching does not stop when COMP drops to the 0.5V PSM threshold. The LS-FET on time is controlled by COMP, even if V_{COMP} is below the PSM threshold, unless it triggers the minimum on time.

If the load continues to decrease, the MPQ3431A continues decreasing the switching frequency. Once the LS-FET is off for 30µs, the device forces the LS-FET on. This limits the frequency to avoid audible frequency in light-load or no-load conditions.

USM may convert more energy to the output than the required load due to the minimum 23kHz frequency, which causes V_{OUT} to rise above the normal voltage setting. When V_{OUT} rises and V_{COMP} drops, the inductor peak current may also drop.

If V_{COMP} drops below one internally clamped level, the HS-FET zero-current detection (ZCD) threshold is gradually regulated to one negative level, so the energy in the inductor can flow back to VIN in each cycle. This keeps the output at the set voltage with a frequency greater than 23kHz. The MPQ3431A also works with a 450kHz frequency if V_{COMP} rises again.

If the frequency is above 33kHz, USM has the same efficiency as PSM. USM has more power loss than PSM if the frequency is clamped at the standard 33kHz, but USM does not introduce audible noise, which is caused by the group pulse in PSM.

Minimum On/Off Time

The MPQ3431A blanks the LS-FET on state with 80ns in each cycle to enhance noise immunity. This 80ns minimum on time restricts applications with a high V_{IN} / V_{OUT} ratio. The MPQ3431A also blanks the LS-FET off state with a minimum off time in each cycle. During the minimum off time, the LS-FET cannot turn on, and the minimum off time is short enough to convert the 0.8V input to a 16V output.

LS-FET and HS-FET Maximum On Time

If the inductor current cannot trigger V_{COMP} with an on time of 7.5µs, the MPQ3431A shuts down the LS-FET. After the LS-FET shuts down, the inductor current goes through the HS-FET and charges VOUT during the off time. This refreshes VOUT with a minimum frequency of about 133kHz in heavy-load transient conditions.

During CCM, the HS-FET on time is limited below 8µs. This limits the maximum LS-FET off time when V_{OUT} is close to V_{IN} in USM. If V_{IN} approaches V_{OUT} in USM or heavy-load PSM, the HS-FET may be turned off by the 8µs HS-FET maximum on time because the inductor current cannot ramp down within this 8µs limit. After the HS-FET turns off, the LS-FET turns on immediately with one pulse control by V_{COMP}, and the HS-FET turns on again. This makes the LS-FET work in a quasi-constant minimum duty cycle.

If V_{IN} is high enough, V_{OUT} is higher than the voltage set for this duty cycle ratio. The IC works with normal PSM logic under PSM and light-load conditions. The IC stops working when V_{OUT} exceeds the set voltage, and resumes switching when V_{OUT} drops below the set voltage.

VDD Power

The MPQ3431A internal circuit is powered by VDD. A ceramic capacitor no less than 4.7µF is required on VDD. When V_{IN} is below 3.4V, VDD is powered from the higher value of either VIN or VOUT. This allows the MPQ3431A to maintain a low $R_{DS(ON)}$ and high efficiency, even with a low input voltage. When V_{IN} exceeds 3.4V, VDD is always powered by VIN. This decreases the VOUT to VDD regulator loss because V_{OUT} is always above V_{IN}.

If VDD is powered by an external supply and the voltage exceeds 3.4V, the regulators from VIN and VOUT are disabled. In this condition, the MPQ3431A starts once the external VDD power supply exceeds VDD_{UVLO}, even if V_{IN} is as low as 0.9V. When VDD is powered by the external power supply, the MPQ3431A continues working if V_{IN} and V_{OUT} are dropping but remain above 0.8V. The external VDD power source should be limited within 3.6V.

There is a reverse-blocking circuit to limit the current flowing between VIN and VOUT. If the external VDD power exceeds the VDD regulation voltage, the current is supplied from the external power, and there is no path for the current from VDD to VIN or from VDD to VOUT.

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VDD is charged when V_{IN} exceeds 0.9V and EN is above the micro-power threshold. If EN is low, VDD is disconnected from VIN and VOUT.

Supply VIN with a power source exceeding 2.7V during VIN start-up to provide VDD with sufficient voltage power.

Start-Up

When the MPQ3431A input is powered, it starts charging VDD from VIN. Once EN is high and VDD rises above its UVLO threshold, the device starts switching with closed-loop control. If VDD is powered by an additional supply, the MPQ3431A starts switching once VDD exceeds its under-voltage lockout (UVLO) threshold.

After the IC is enabled, the MPQ3431A starts up with a soft start (SS). The SS signal is controlled by charging SS from 0V and comparing that value with the internal reference voltage. The lower of the two values is fed to the error amplifier to control the output voltage. After the SS signal rises above the reference voltage, soft start is completed and the internal reference takes charge of feedback loop regulation.

If there is a biased voltage on VOUT during PSM, the MPQ3431A stops switching until the SS signal rises above V_{FB}, which is proportional to the VOUT bias voltage. If the IC is in USM or FCCM, the device works with a frequency of about 33kHz to 450kHz. Both USM and FCCM have a negative inductor current, so the energy may transfer from VOUT to VIN if the V_{OUT} bias is high.

Synchronous Rectifier and BST Function

The MPQ3431A integrates both an LS-FET (Q1) and HS-FET (Q2) to reduce the number of external components. During switching, the rectifier switch (Q2) is powered from BST (typically 3.4V above the SW voltage). This 3.4V bootstrap voltage is charged from VDD when the LS-FET turns on.

Current Limit

The MPQ3431A provides both a fixed cycle-by-cycle switching peak current limit and programmable average input current limit function.

Switching Peak Current Limit

The MPQ3431A provides a fixed cycle-by-cycle switching peak current limit. In each cycle, the internal current-sensing circuit monitors the LS-FET current signal. Once the sensed current reaches the typical 21.5A current limit, the LS-FET (Q1) turns off. The LS-FET current signal is blanked for about 80ns internally to enhance noise immunity.

Input Current Limit

The MPQ3431A senses the LS-FET (Q1) average current when Q1 turns on and converts it to a µA current signal that is fed to ILIM. Simultaneously, a resistor on ILIM converts this current signal to a voltage signal that is fed to the negative input of the current-limit error amplifier. If the input current signal exceeds the current limit threshold, the current-limit amplifier output clamps V_{COMP}. As a result, the input current is limited by the internal COMP signal, and the output voltage decreases (see Figure 2).

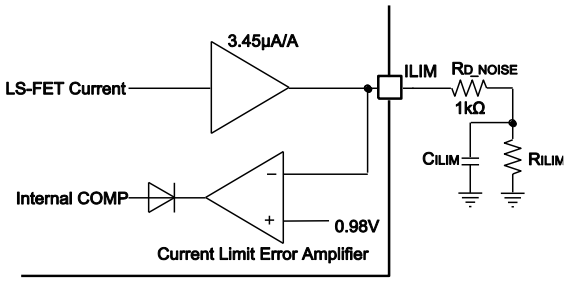

Figure 2: Input Overload Protection

R_{ILIM} is the input current-setting resistor, C_{ILIM} is used for current limit signal filtering, and R_{D_NOISE} is used to avoid noise affection. R_{D_NOISE}, R_{ILIM}, and C_{ILIM} are required to set the input current limit. Then the input current limit can be estimated with Equation (1):

$$I_{IN_LIM} = \frac{980}{3.45 \times (R_{ILIM} + 1)} + (1.2 - V_{IN} \times 0.12) \quad (1)$$

Where I_{IN_LIM} is the input current limit, R_{ILIM} is the input current limit setting resistor (in kΩ), and (1.2 - V_{IN} x 0.12) is the offset current and sense delay of the inner amplifier. It is typically recommended to use a 1kΩ for R_{D_NOISE}. If the input current limit function is not being used, connect ILIM to AGND.

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Enable (EN) and Configurable Under-Voltage Lockout (UVLO)

EN enables and disables the MPQ3431A. When applying a voltage above the EN high threshold (about 1V), the MPQ3431A starts up some of the internal circuits in micro-power mode. If the EN voltage exceeds the turn-on threshold (1.23V), the MPQ3431A enables all functions and starts boost operation. Boost switching is disabled when the EN voltage falls below its turn-on threshold (1.23V). To completely shut down the MPQ3431A, EN must have a low-level voltage below 0.4V. After shutdown, the MPQ3431A sinks a current from the input power (generally below 2μA). EN is compatible with voltages up to 13V. For automatic start-up, connect EN directly to VIN.

The MPQ3431A features a configurable UVLO hysteresis. When powering up in micro-power mode, EN sinks a 5μA current from an upper resistor (R_{TOP}) (see Figure 3).

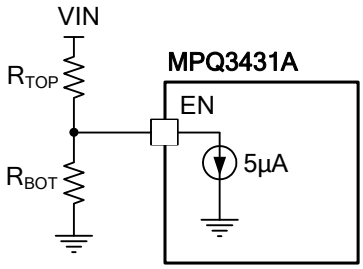

Figure 3: VIN VULO Program

VIN must increase to overcome the current sink. The VIN start-up threshold is calculated with Equation (2):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (2)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (typically 1.23V).

Once the EN voltage reaches V_{EN-ON}, the 5μA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold, which can be calculated with Equation (3):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (3)$$

Over-Voltage Protection (OVP)

If the device detects that VOUT is exceeding its 16.5V threshold, the MPQ3431A stops switching immediately until the voltage drops to 16.3V. This prevents an over-voltage condition on the output and internal power MOSFETs.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. When the die temperature exceeds 150°C, the IC shuts downs. Normal operation resumes when the die temperature drops to 25°C.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. Choose R1 to be between 300kΩ and 800kΩ. Calculate R2 with Equation (4):

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (4)$$

Where V_{REF} is 1V, R1 is the top feedback resistor, and R2 is the bottom feedback resistor.

Selecting the Input Capacitor

The input capacitor (C1) maintains the DC input voltage. Low-ESR ceramic capacitors are recommended. The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{V_{IN}}{8 f_{SW}^2 \times L \times C1} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (5)$$

Where f_{SW} is the switching frequency, and L is the inductor value.

Selecting the Output Capacitor

The boost converter has a discontinuous output current, and requires an output capacitor (C2) to supply AC current to the load. For the best performance, low-ESR ceramic capacitors are recommended. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times R_L \times C2} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (6)$$

Where R_L is the value of the load resistor.

Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of their low ESR and small temperature coefficients.

Selecting the Inductor

An inductor is required to transfer the energy between the input source and the output capacitors. An inductor with a larger value results in a lower ripple current and lower peak inductor current, reducing stress on the power MOSFET. However, a larger value inductor has a larger physical size, higher series resistance, and lower saturation current.

For most designs, the inductance value can be calculated with Equation (7):

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta I_L} \quad (7)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 20% to 50% of the maximum inductor peak current. Typically, a 1.5µH inductor is recommended. Ensure that the inductor does not saturate under the worst-case condition. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

Soft-Start (SS) Capacitor Selection

With the required output voltage rising time (t_{RISE}), C_{SS} can be calculated using Equation (8):

$$C_{SS} = \frac{t_{RISE} \times I_{SS}}{V_{REF}} \quad (8)$$

Where I_{SS} is the SS charging current (7.5µA). It is typically recommended to set C_{SS} to 22nF for about 3ms of the rising time.

Input Current Limit Setting

The ILIM resistor (R5) sets the input current limit. One 1kΩ resistor in series connected to ILIM prevents noise injection. Calculate R5 with Equation (9):

$$R5 = \frac{980}{3.45 \times \left[I_{IN_LIM} - (1.2 - V_{IN} \times 0.12) \right]} - 1 \quad (9)$$

For example, if the required current limit is 13A, and V_{IN} is 3.3V, then R5 is calculated to be 22.29kΩ, so choose a 22kΩ value for a 13A input current limit. Place a decoupling capacitor (4.7nF to 10nF) in parallel with R5.

If the input current limit function is not used, connect ILIM to AGND.

VDD Capacitor Selection

The MPQ3431A integrates the VDD power at about 3.4V, which powers the internal MOSFET gate driver and internal control circuit. One ceramic bypass capacitor (4.7µF or greater) is required for the internal regulator. Do not

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connect the external load to the VDD power.

BST Capacitor

The MPQ3431A uses one bootstrap circuit to power the output N-channel MOSFET. One external bootstrap capacitor is required for the charge pump power. A 0.1µF ceramic capacitor between BST and SW is recommended.

Configurable Under-Voltage Lockout (UVLO)

The MPQ3431A features a configurable under-voltage lockout (UVLO) hysteresis. When powering up, EN sinks a 5µA current from an upper resistor (R_{TOP}) (see Figure 3). V_{IN} must increase to overcome the current sink.

Estimate the V_{IN} start-up threshold with Equation (10):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (10)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (typically 1.23V).

Once the EN voltage reaches V_{EN-ON}, the 5µA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold, which can be calculated with Equation (11):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (11)$$

For automatic start-up, connect EN with a 30kΩ R_{TOP} resistor to operate with a 150mV hysteresis.

MODE Selection

The MPQ3431A can work in forced continuous conduction mode (FCCM), pulse-skip mode (PSM), or ultrasonic mode (USM) based on the MODE setting. Pull MODE directly to VDD for FCCM, float MODE for USM, and pull the MODE voltage to GND for PSM.

Compensation

The output of the transconductance error amplifier (COMP) compensates for the regulation control system. The system uses two poles and one zero to stabilize the control loop.

Pole f_{P1} is set by the output capacitor (C_{OUT}) and the load resistance. Pole f_{P2} starts from the origin. The zero f_{Z1} is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). These are calculated with Equation (12) and Equation (13), repectively:

$$f_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (12)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (13)$$

Where R_{LOAD} is the load resistance.

There is a right half-plane zero that exists in FCCM, where the inductor current does not drop to zero in each cycle. The frequency of the right half-plane zero (f_{RHPZ}) can be determined with Equation (14):

$$f_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz) \quad (14)$$

The right half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase margin and gain margin. The worst-case condition is when the device is at the minimum input voltage and maximum output power.

Design Example

Table 1 is a design example following the application guidelines for the specifications below.

Table 1: Design Example

V_{IN}	3V to 8.4V
I_{IN_LIM}	13A
V_{OUT}	9V
I_{OUT}	3.5A

See Figure 5 and Figure 6 for detailed application schematics. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 7. For more device applications, refer to the related evaluation board datasheet.

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PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. Use a 4-layer PCB for high-power applications. For best results, refer to Figure 4 and follow the guidelines below:

1. Place the output capacitor (C2A to C2C) as close to VOUT and PGND as possible.
2. Place a 0.1µF capacitor close to the IC (C2D) to reduce parasitic inductance.
3. Keep the connection of VOUT and PGND to the output capacitor short and wide with copper.
4. Place the copper, IC, and COUT on the same layer.
5. Place the FB dividers (R1 and R2) as close to FB as possible.
6. Route the FB trace away from noise sources, such as the SW node.
7. Place the current limit setting net (R4, R5, and C7) close to ILIM.
8. Connect the ILIM ground to AGND.
9. Connect the compensation components and SS capacitor to AGND with a short loop.
10. Connect the VDD capacitor to PGND with a short loop.
11. Keep the input loop (C1, L1, SW, and PGND) as small as possible.
12. Place enough GND vias close to the MPQ3431A for good thermal dissipation.
13. Use separated AGND and PGND layouts connected between the AGND and PGND pins under the package.

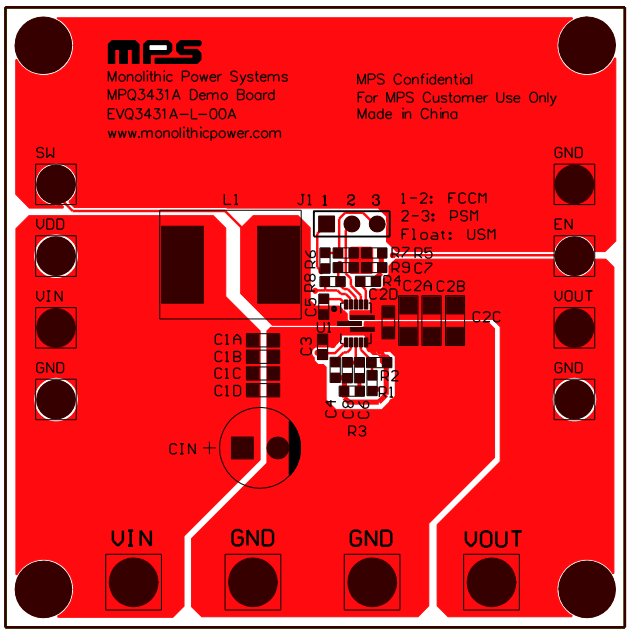

Figure 4: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

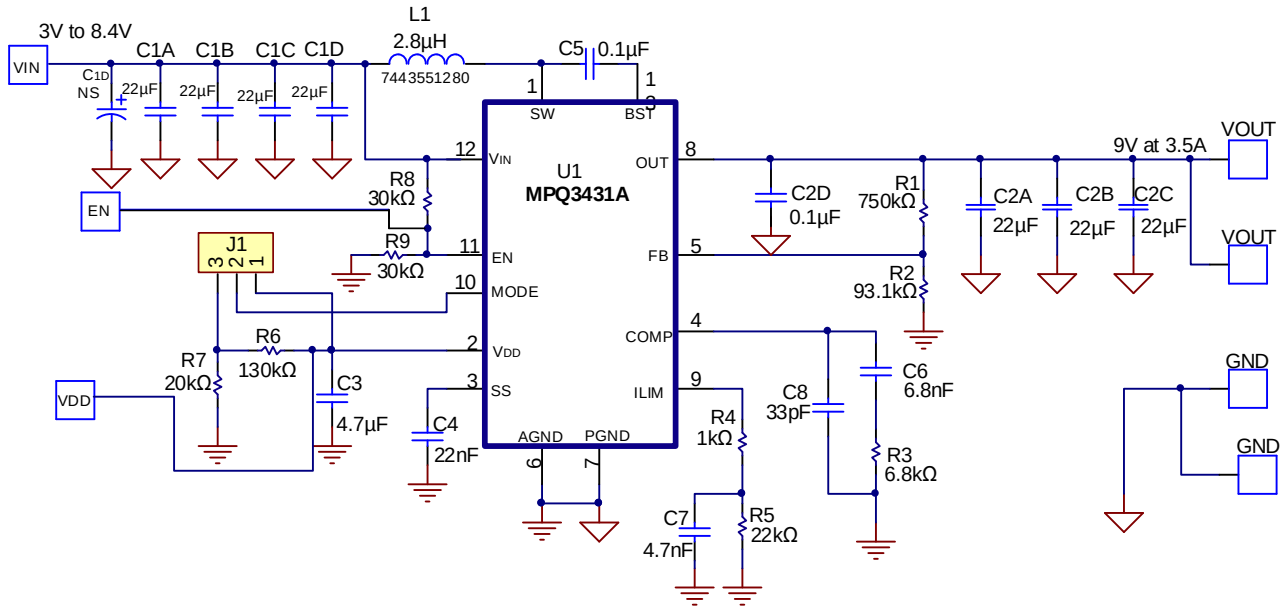

Figure 5: Typical Application Circuit

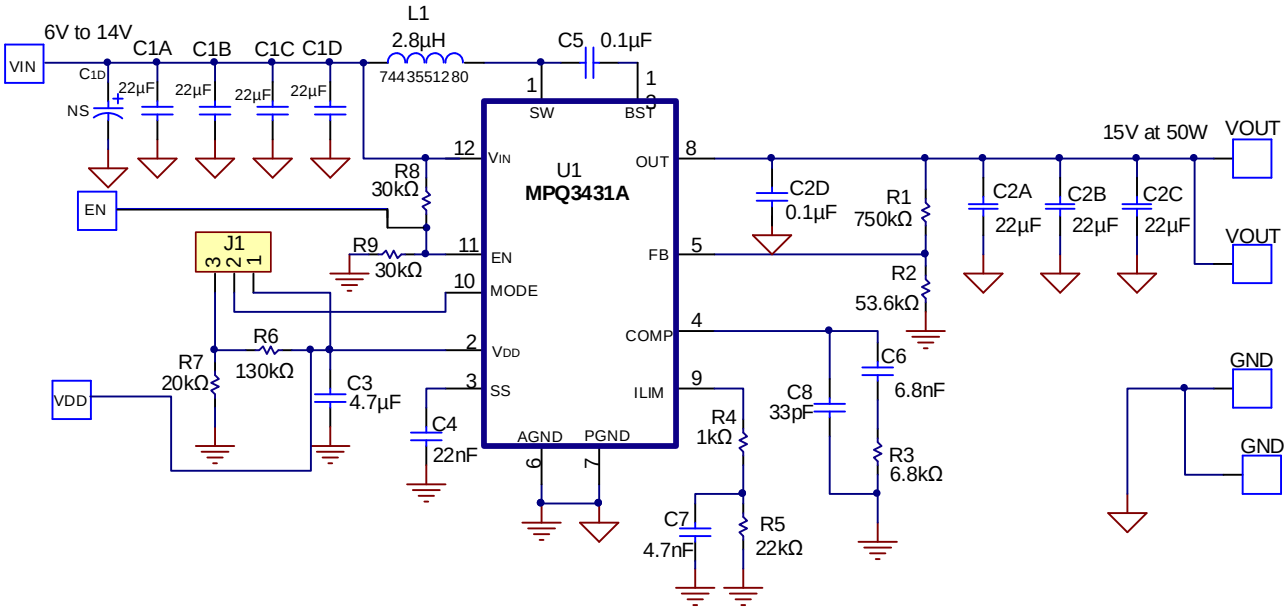

Figure 6: Typical Application Circuit with

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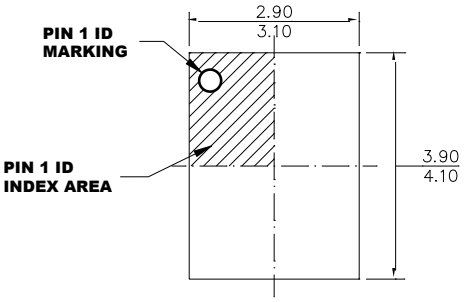
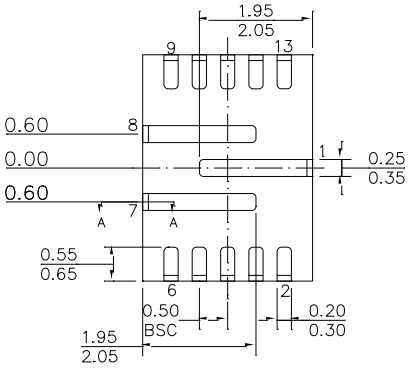
PACKAGE INFORMATION

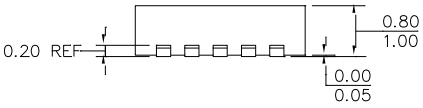
QFN-13 (3mmx4mm)



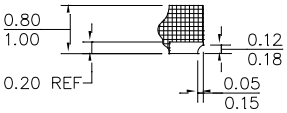
TOP VIEW



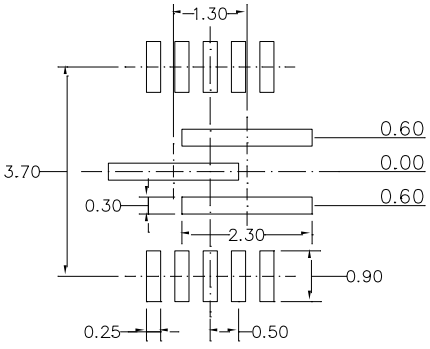
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,7 AND 8 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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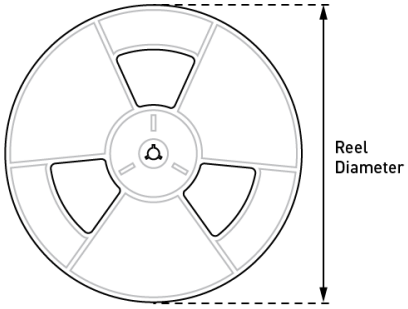
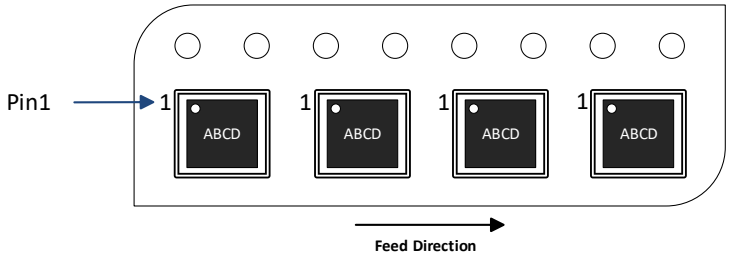
CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3431AGL-AEC1-Z	QFN-13 (3mmx4mm)	5000	N/A	13in	12mm	8mm

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