MPQ3425

3A, 55V Boost Converter with Programmable Switching Frequency, AEC-Q100 Qualified

DESCRIPTION

The MPQ3425 is a current control mode, step-up converter with a 3.5A, 90mΩ internal MOSFET that provides fast transient response. It operates with an input voltage as low as 3.1V, and can generate up to 55V.

The MPQ3425 features a configurable switching frequency of up to 1MHz for easy filtering and low noise. An external compensation pin allows the user to flexibly set loop dynamics and operates with small, low-ESR ceramic output capacitors. The soft start feature provides a small inrush current and can be programmed with an external capacitor.

Full protection features include under-voltage lockout (UVLO), current limiting, and thermal shutdown.

The MPQ3425 is available in a low-profile QFN-14 (3mmx4mm) package with an exposed pad.

FEATURES

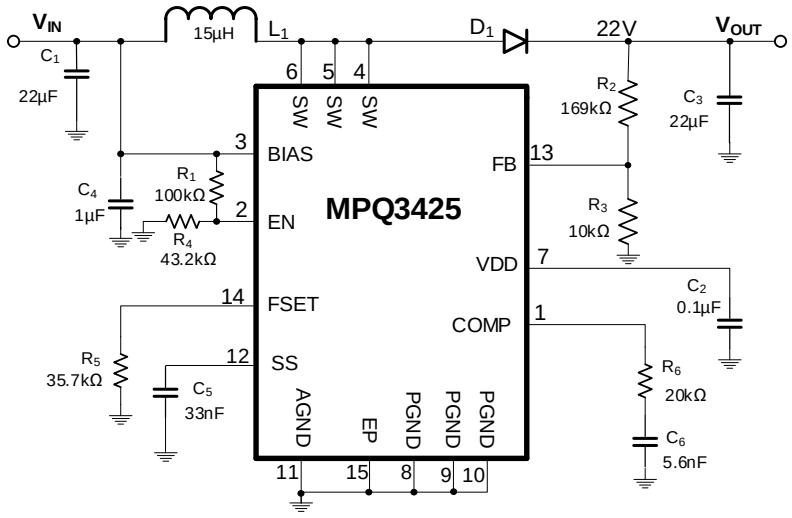
- Wide 3.1V to 22V BIAS Supply Voltage Range
- Wide 3V to 50V Input Voltage Range
- 3.5A, 90mΩ, Power MOSFET
- Output Voltage up to 55V
- Programmable 300kHz to 1MHz f_{SW}
- Programmable Under-Voltage Lockout (UVLO), Soft Start, UVLO Hysteresis
- Micropower Shutdown <1μA
- Thermal Shutdown OTP (160°C)
- Available in QFN-14 (3mmx4mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Systems
- Boost Converter and Single-Ended Primary-Inductance Converter (SEPIC) Topologies
- Pre-Boost Applications
- Microphones and Tuner Bias

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

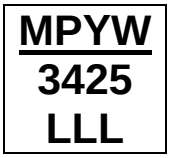
ORDERING INFORMATION

Part Number	Package **	Top Marking	MSL Rating
MPQ3425DL*	QFN-14 (3mmx4mm)	*See Below*	1
MPQ3425DL-AEC1**	QFN-14 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ3425DL-LF-Z).

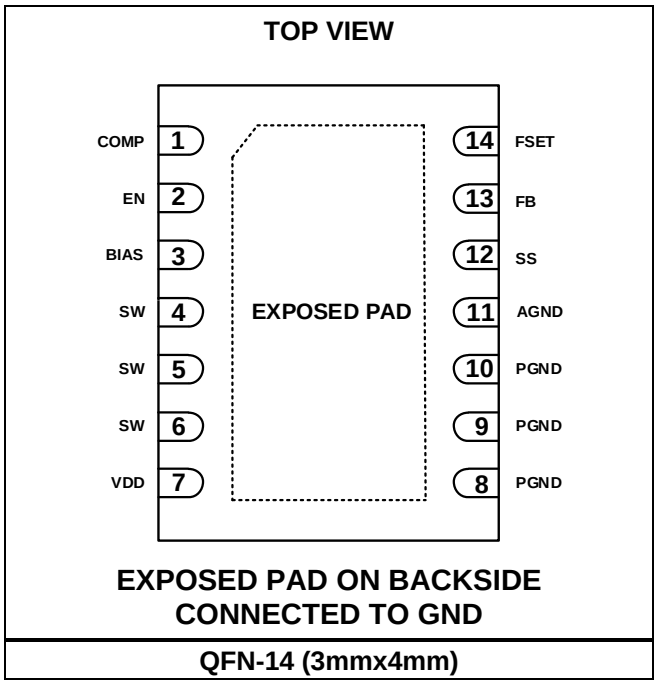
** For RoHS-compliant-packaging, add suffix -LF (e.g. MPQ3425DL-AEC1-LF-Z).

TOP MARKING (MPQ3425DL)



MP: MPS prefix
Y: Year code
W: Week code
3425: Part number
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (3mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	COMP	**Compensation.** Connect a capacitor and resistor in series from COMP to AGND for loop stability.
2	EN	**Regulator on/off control input.** Pull EN high to turn the converter on; pull EN low to turn it off. When not in use, connect EN to the (external or internal) input source through a 100kΩ pull-up resistor for automatic start-up if V_{IN} > 6V. EN can also be used to program V_{IN} UVLO. Do not leave EN floating.
3	BIAS	**Internal LDO supply.** BIAS must be bypassed locally.
4, 5, 6	SW	**Power switch output.** SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW.
7	VDD	**LDO output.**
8, 9, 10, exposed pad	PGND	**Power ground.** The bottom exposed pad is the power ground. For best thermal resistance, solder the exposed pad to the underlying PCB.
11	AGND	**Analog ground.** Connect AGND to the ground plane through the exposed pad.
12	SS	**Soft-start control.** Connect a soft-start capacitor (C_{SS}) to the SS pin. C_{SS} is charged with a constant current of 5μA. Leave SS disconnected if soft start functionality is not needed.
13	FB	**Feedback input.** The reference voltage is 1.25V. Connect a resistor divider to FB.
14	FSET	**Frequency programming.** Connect a resistor from FSET to AGND. The voltage on FSET is regulated internally to 0.5V. The current flowing out of FSET sets the operation frequency linearly.

ABSOLUTE MAXIMUM RATINGS (1)

SW .....-0.5V to +55V
BIAS.....-0.5V to +22V
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-14 ..... 2.5W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{BIAS}) .....3.1V to 22V
Output voltage (V_{OUT}).....3.1V to 55V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-14 (3x4) .....50 ..... 12 ... °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{BIAS} = V_{IN} = V_{EN} = 5V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Operating supply voltage	V_{BIAS}			3.1		22	V
Under-voltage lockout (UVLO) threshold		V_{BIAS} rising	T_J = 25°C	2.8		3.1	V
			T_J = -40°C to +125°C	2.75		3.15	
UVLO hysteresis					250		mV
VDD voltage gate driver voltage supply	V_{VDD}	C = 10nF				6	V
Shutdown supply current	I_{IN_SD}	V_{EN} = 0V				1	µA
Quiescent supply current	I_{IN}	V_{FB} = 1.35V	T_J = 25°C		650	900	µA
			T_J = -40°C to +125°C			950	
Switching frequency	f_{SW}	FSET = 84.5kΩ		0.44	0.55	0.66	MHz
Minimum off time	t_{OFF}	V_{FB} = 0V			40		ns
Minimum on time (4)	t_{ON}	V_{FB} = 1.35V			100		ns
EN high threshold		V_{EN} rising (switching)	T_J = 25°C	1.45	1.5	1.55	V
			T_J = -40°C to +125°C	1.4		1.6	
EN high threshold		V_{EN} rising (micropower)				1.0	V
EN low threshold			T_J = 25°C	0.5			V
			T_J = -40°C to +125°C	0.45			
EN input bias current		V_{EN} = 0V, 5V			0.1	1	µA
UVLO hysteresis current into EN		1V < EN < 1.4V			4		µA
Soft-start current	I_{SS}				6		µA
Feedback (FB) voltage	V_{FB}		T_J = 25°C	1.200	1.225	1.250	V
			T_J = -40°C to +125°C	1.19		1.26	
FB input bias current				-200	-100		nA
Error amplifier (EA) voltage gain (4)	A_{VEA}				300		V/V
EA transconductance (4)	G_{EA}				160		µA/V
EA output current (4)					20		µA
Current-sense gain (4)	G_{CS}	I_{SW} / V_{COMP}			9		A/V
SW on resistance	$R_{DS(ON)}$				90		mΩ
SW current limit	I_{LIMIT}	Duty cycle = 0%	T_J = 25°C	3.5	5		A
			T_J =-40°C to +125°C	3			
Thermal shutdown (4)	T_{SD}				160		°C

Note:

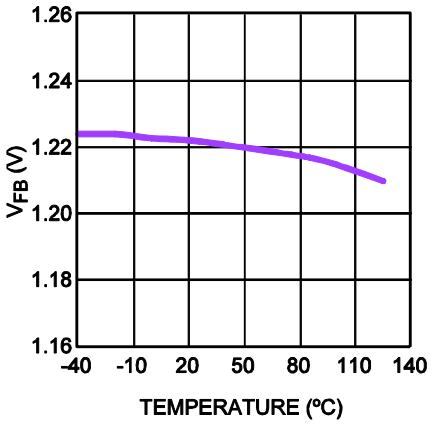
4) Guaranteed by design. Not tested in production.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

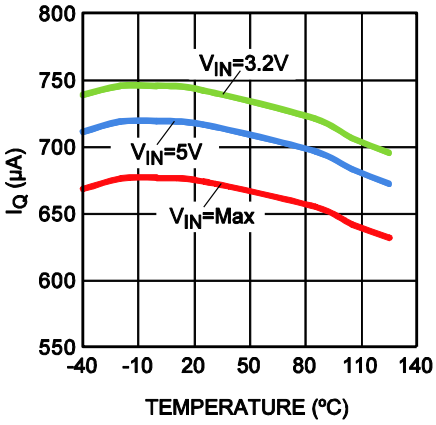
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 48V, C_{OUT} = 4.7µF, f_{SW} = 300kHz, T_A = 25°C, unless otherwise noted.

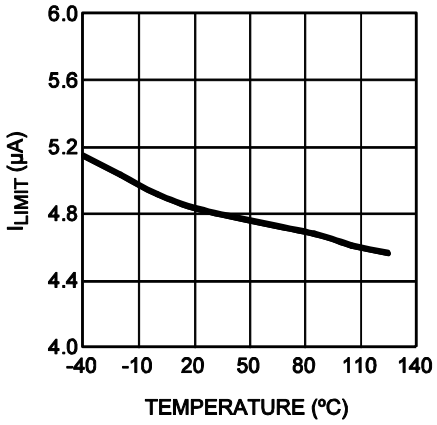
V_{FB} vs. Temperature



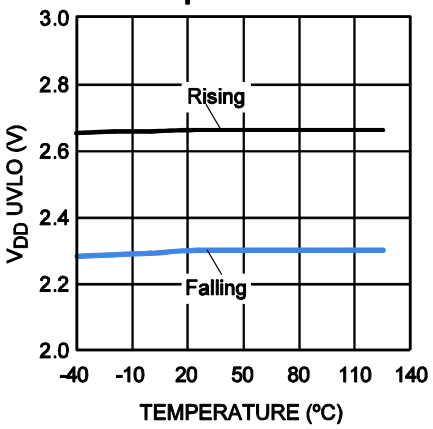
I_Q vs. Temperature



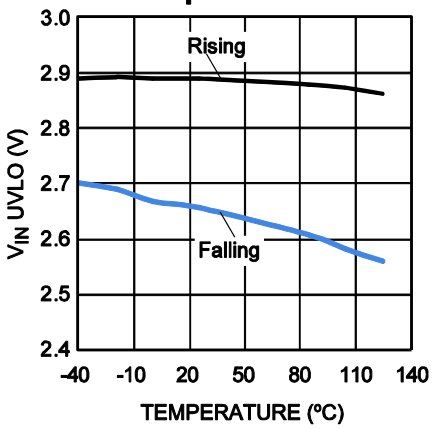
I_{LIMIT} vs. Temperature



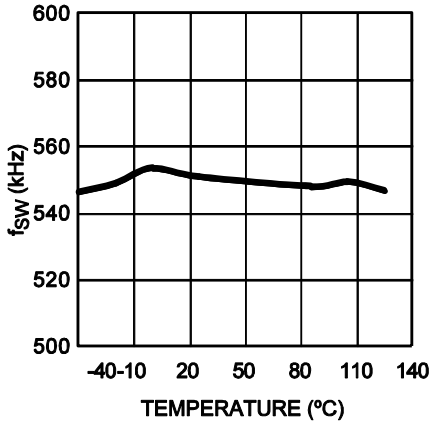
V_{DD} UVLO vs. Temperature



V_{IN} UVLO vs. Temperature



f_{SW} vs. Temperature

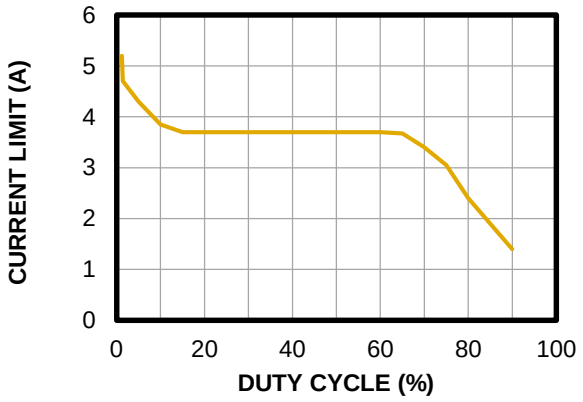


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

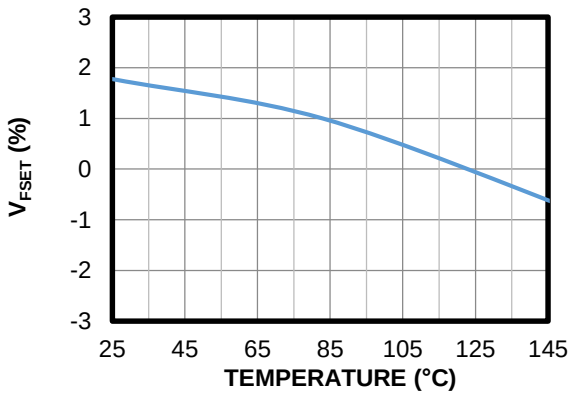
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} = 15V, L = 6.2µH, f_{SW} = 400kHz, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

Current vs. Duty Cycle

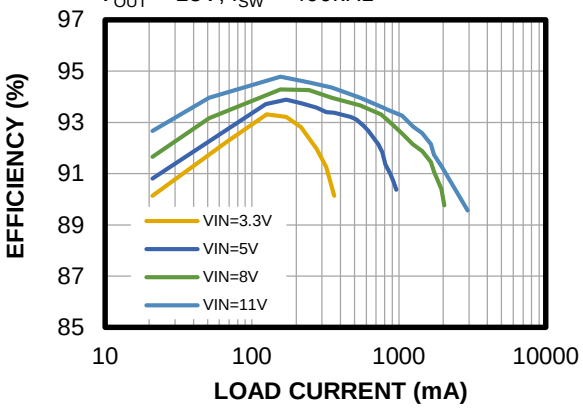


V_{FSET} vs Temperature



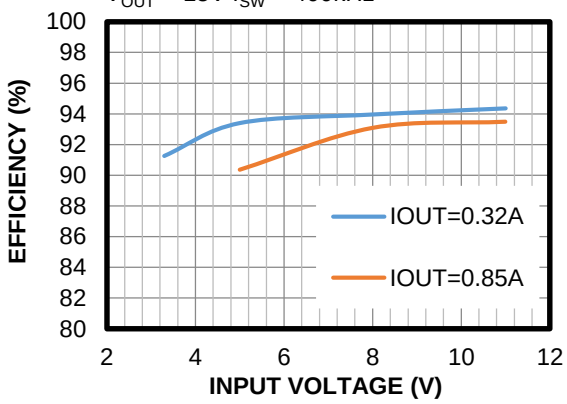
Efficiency vs. Load Current

V_{OUT} = 15V, f_{SW} = 400kHz



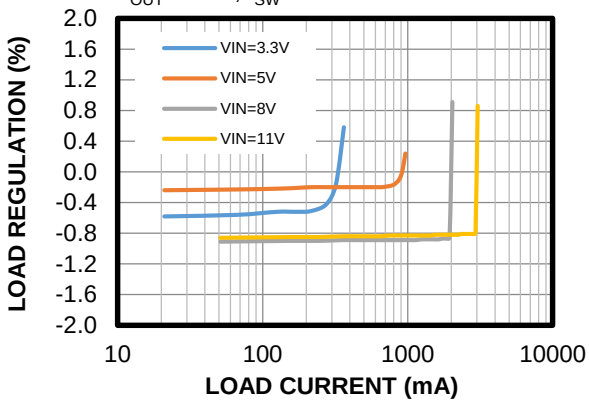
Efficiency vs. Input Voltage

V_{OUT} = 15V f_{SW} = 400kHz



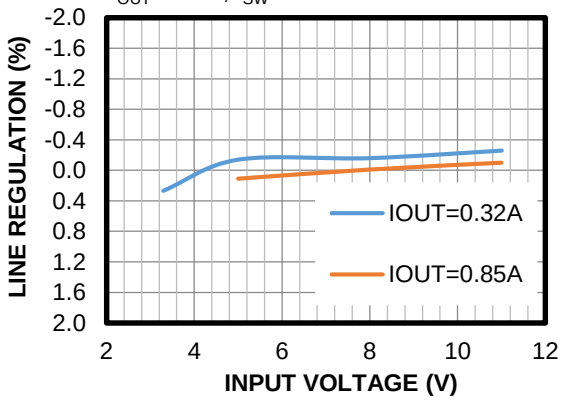
Load Regulation

V_{OUT} = 15V, f_{SW} = 400kHz



Line Regulation

V_{OUT} = 15V, f_{SW} = 400kHz



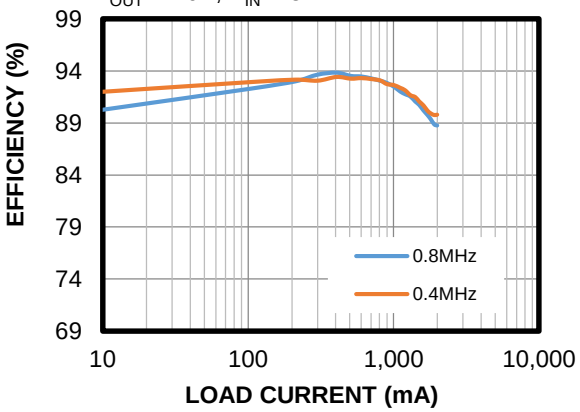
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{OUT} = 15V, L = 6.2µH, f_{SW} = 400kHz, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

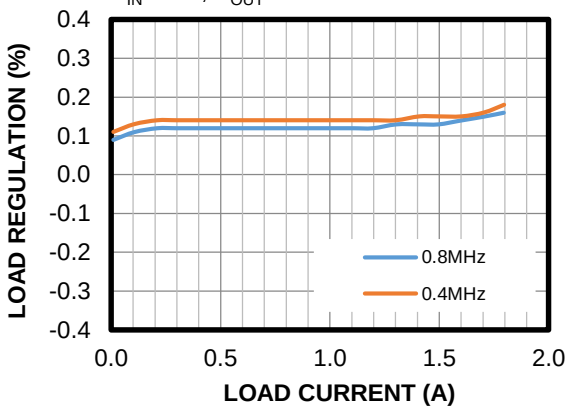
Efficiency vs. Load Current

V_{OUT} = 10V, V_{IN} = 5V



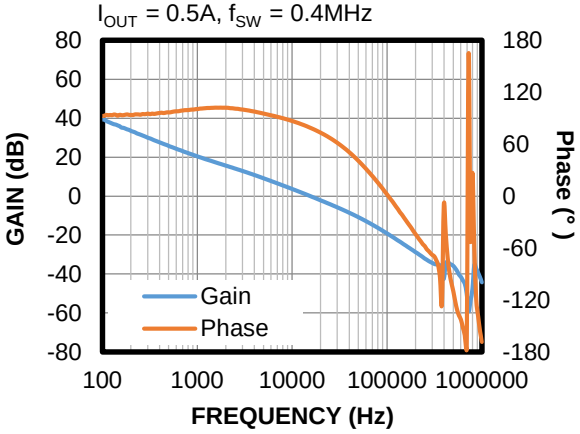
Load Regulation

V_{IN} = 5V, V_{OUT} = 10V



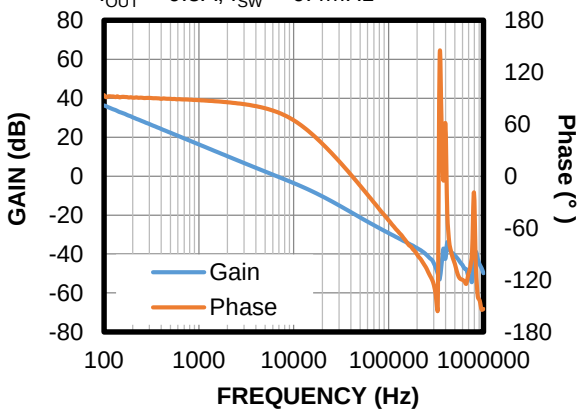
Bode Plot

V_{IN} = 10V, V_{OUT} = 15V,
I_{OUT} = 0.5A, f_{SW} = 0.4MHz



Bode Plot

V_{IN} = 5V, V_{OUT} = 15V,
I_{OUT} = 0.5A, f_{SW} = 0.4MHz

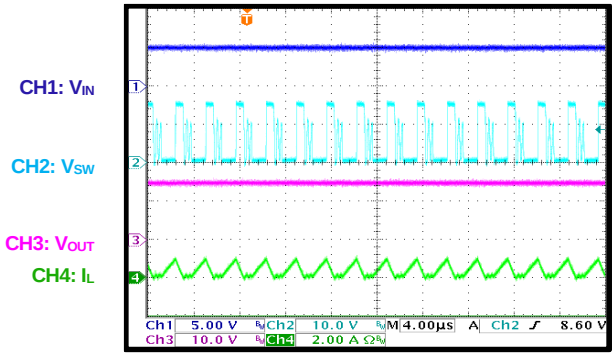


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

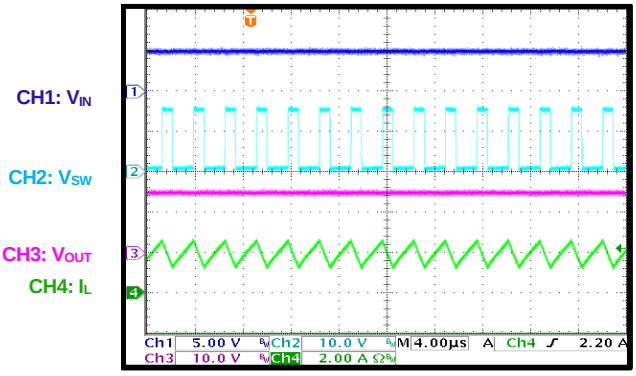
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{OUT} = 15V, L = 6.2µH, f_{SW} = 400kHz, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

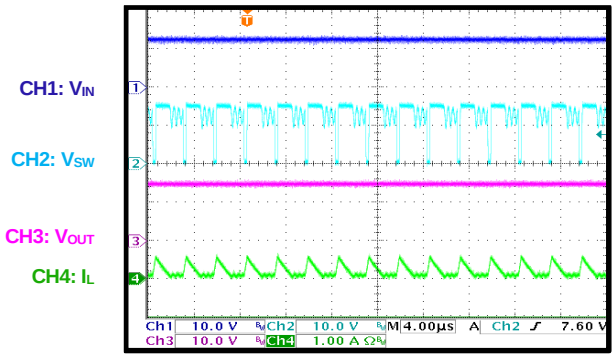
Steady State
V_{IN} = 5V, I_{OUT} = 0.1A



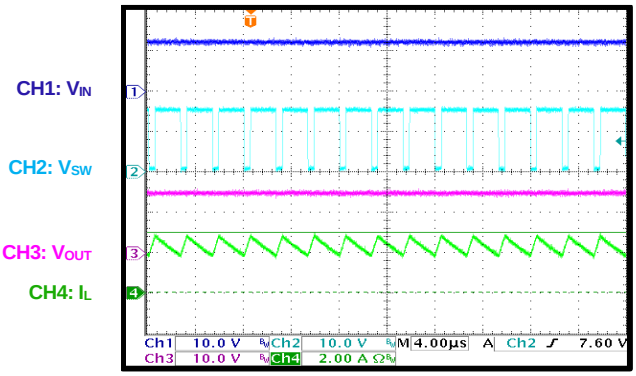
Steady State
V_{IN} = 5V, I_{OUT} = 0.6A



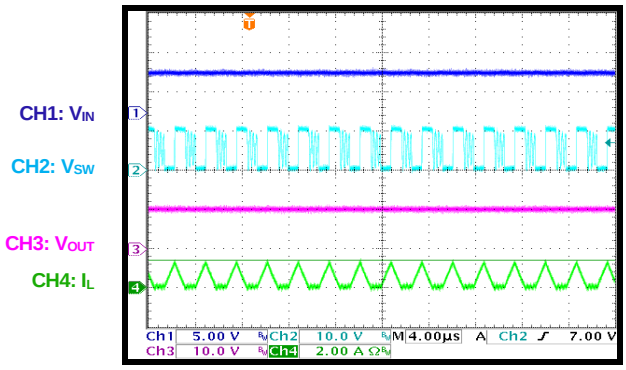
Steady State
V_{IN} = 12V, I_{OUT} = 0.1A



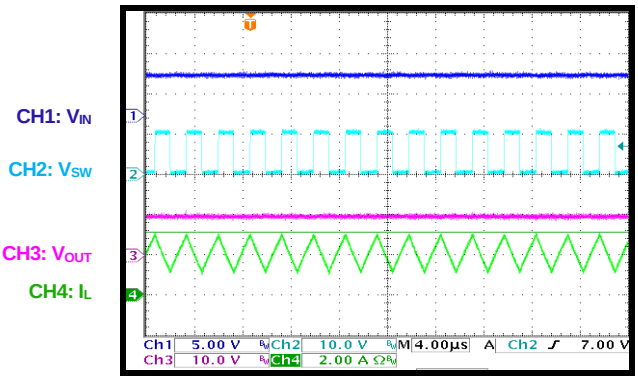
Steady State
V_{IN} = 12V, I_{OUT} = 1.8A



Steady State
V_{IN} = 5V, V_{OUT} = 10V, I_{OUT} = 0.2A



Steady State
V_{IN} = 5V, V_{OUT} = 10V, I_{OUT} = 1A



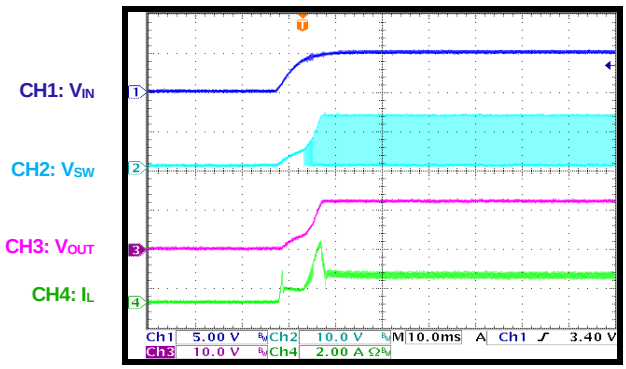
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{OUT} = 15V, L = 6.2µH, f_{SW} = 400kHz, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

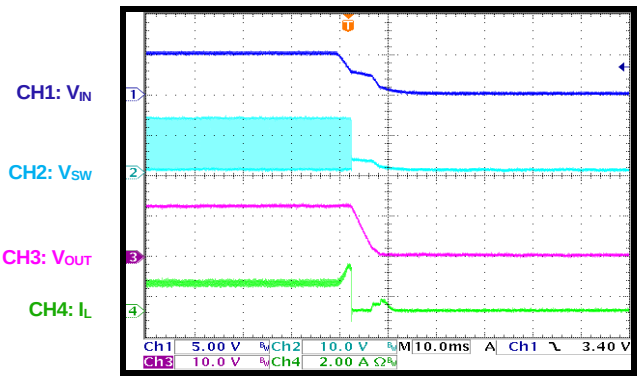
Start-Up through VIN

V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.5A



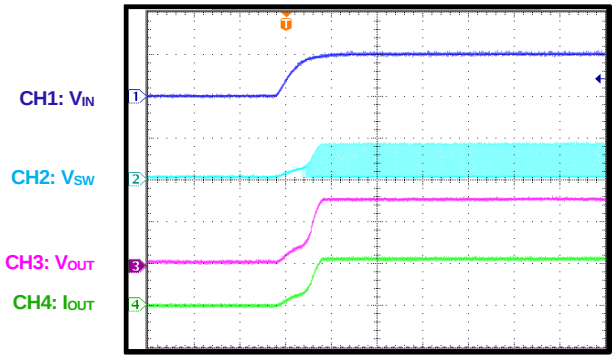
Shutdown through VIN

V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.5A



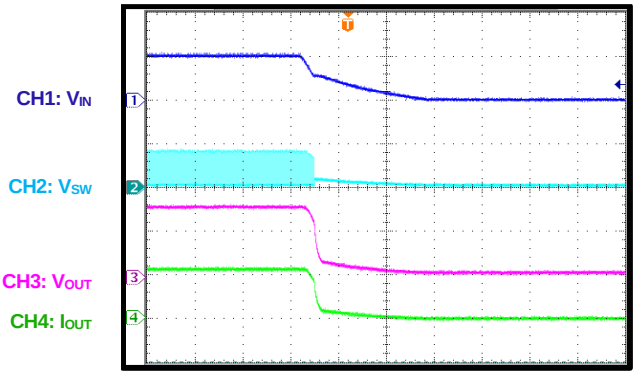
Start-Up through VIN

V_{IN} = 5V, I_{OUT} = 0.55A



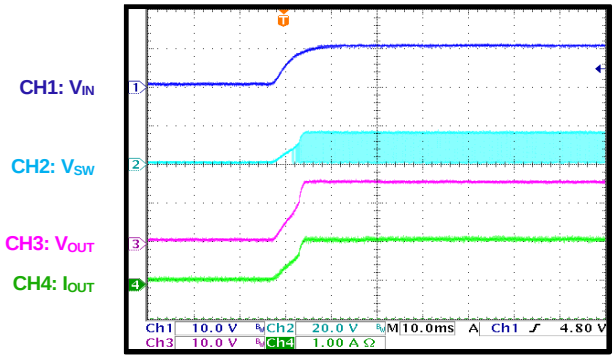
Shutdown through VIN

V_{IN} = 5V, I_{OUT} = 0.55A



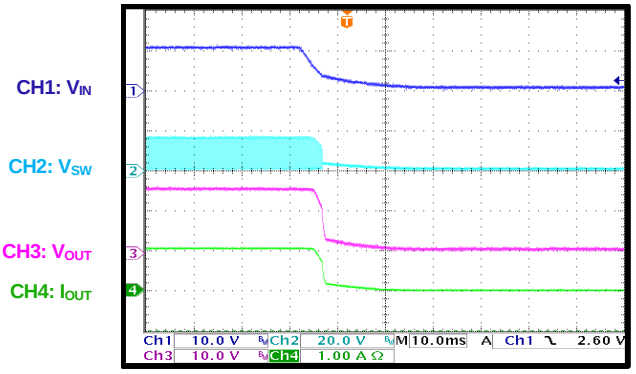
Start-Up through VIN

V_{IN} = 10V, I_{OUT} = 1A



Shutdown through VIN

V_{IN} = 10V, I_{OUT} = 1A



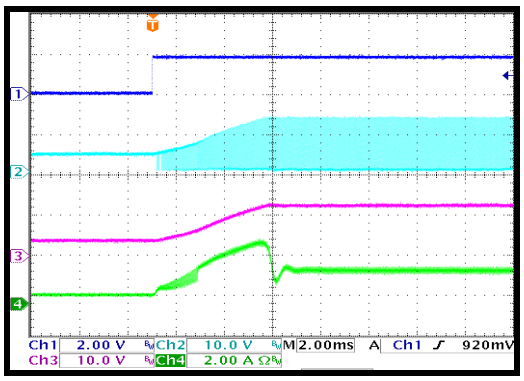
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{OUT} = 15V, L = 6.2µH, f_{SW} = 400kHz, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

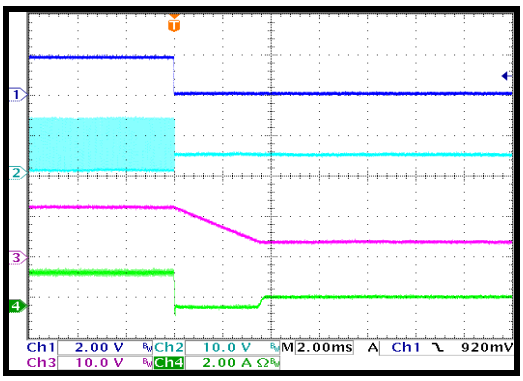
Start-Up through EN

V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1A



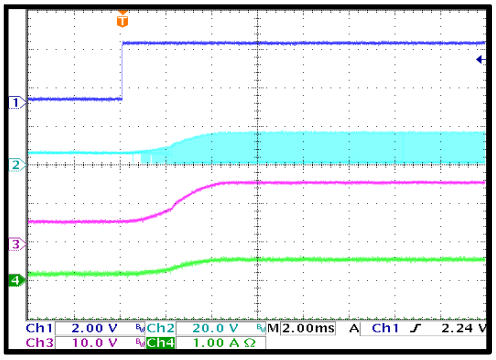
Shutdown through EN

V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1A



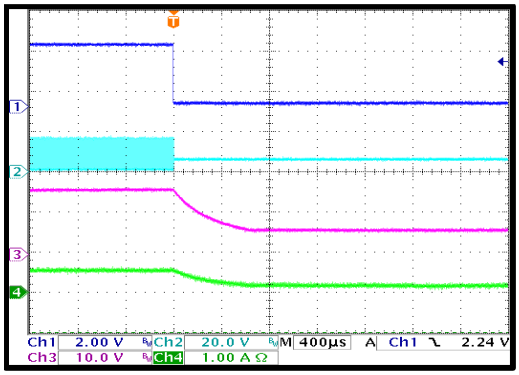
Start-Up through EN

V_{IN} = 5V, I_{OUT} = 0.5A



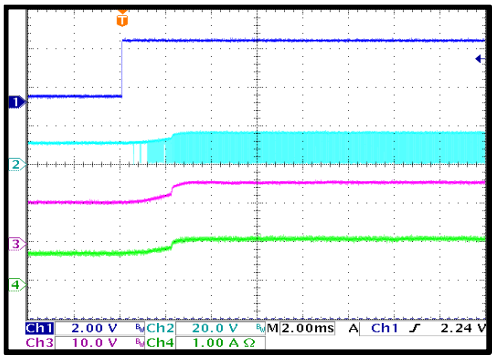
Shutdown through EN

V_{IN} = 5V, I_{OUT} = 0.5A



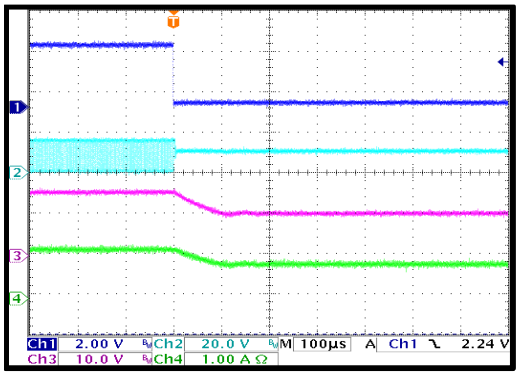
Start-Up through EN

V_{IN} = 10V, I_{OUT} = 1A



Shutdown through EN

V_{IN} = 10V, I_{OUT} = 1A



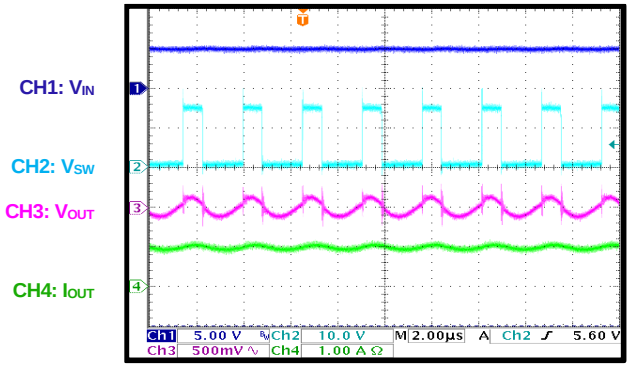
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{OUT} = 15V, L = 6.2µH, f_{SW} = 400kHz, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

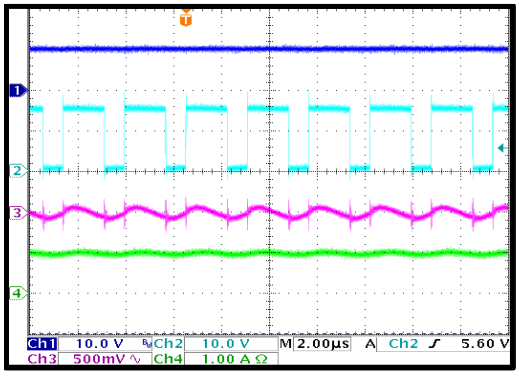
Ripple

V_{IN} = 5V, I_{OUT} = 1A



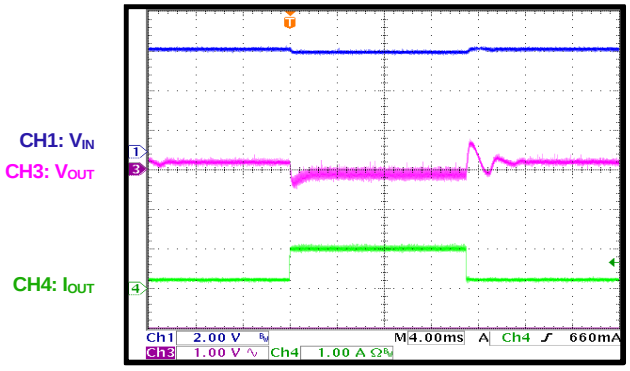
Ripple

V_{IN} = 10V, I_{OUT} = 1A



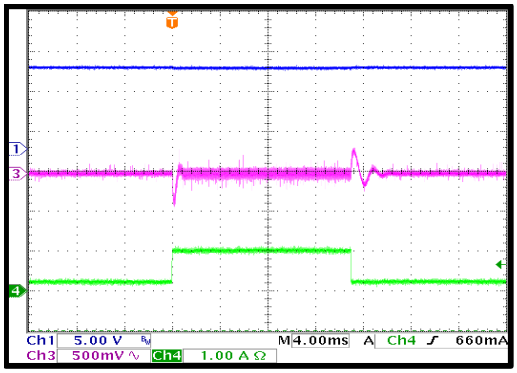
Load Transient

V_{IN} = 5V, I_{OUT} = 0.2A to 1A, I_{RAMP} = 2.5A/µs



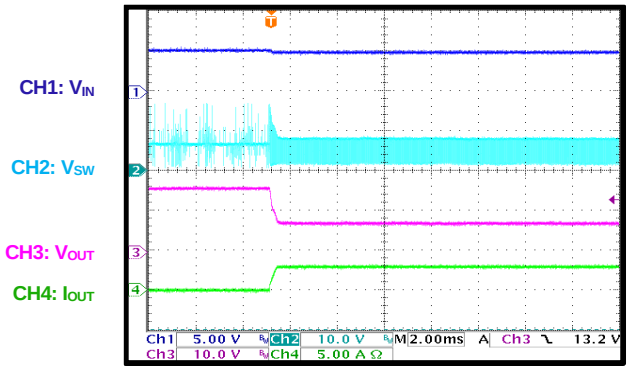
Load Transient

V_{IN} = 10V, I_{OUT} = 0.2A to 1A, I_{RAMP} = 2.5A/µs



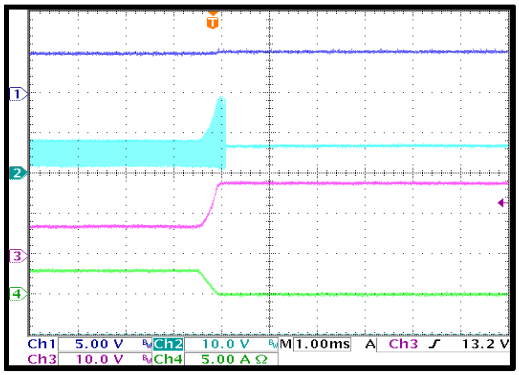
Over-Current Protection

V_{IN} = 5V, I_{OUT} = 0A to 3A



Over-Current Protection Recovery

V_{IN} = 5V, I_{OUT} = 3A to 0A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

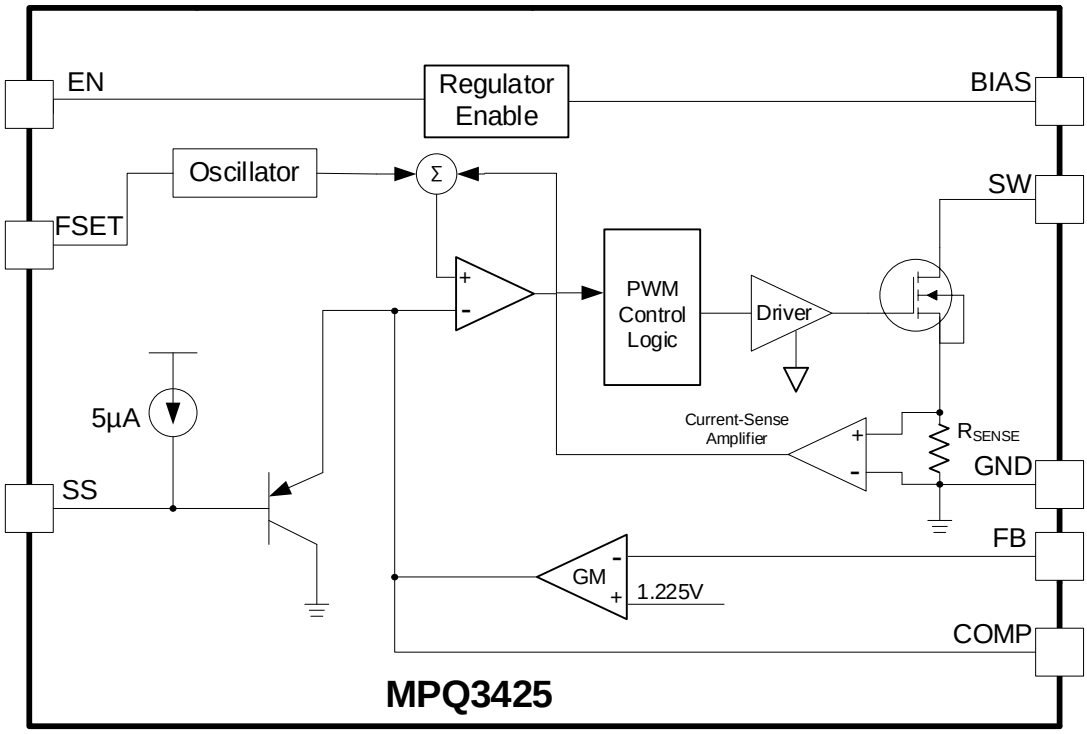


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

OPERATION

The MPQ3425 uses a constant-frequency, peak current control mode boost regulation architecture to regulate the feedback voltage (V_{FB}). Figure 1 on page 13 shows operation details for the MPQ3425.

At the beginning of each cycle, the N-channel MOSFET turns on, forcing the inductor current (I_L) to rise. The current at the source of the MOSFET is measured internally and converted to a voltage by the current-sense amplifier. The current-sense amplifier voltage is compared to the error voltage at COMP. The output voltage (V_{OUT}) of the error amplifier (EA) is an amplified version of the difference between the 1.225V reference voltage (V_{REF}) and V_{FB}.

When V_{REF} and V_{FB} are equal, the PWM comparator turns off the MOSFET. I_L flows to the output capacitor (C_{OUT}) through the external rectifier diode. This causes I_L to decrease. The peak inductor current is controlled by the COMP voltage (V_{COMP}), which is controlled by V_{OUT}. V_{OUT} is regulated by I_L to satisfy the load. Current mode regulation improves transient response and control loop stability.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the Switching Frequency

The switching frequency (f_{SW}) is set by R5, and can be calculated with Equation (1):

$$f_{SW} = 23 \times (R5^{-0.86}) \quad (1)$$

Where R5 is in kΩ.

Table 1 shows more frequency options.

Table 1: Frequency Selection

R5 (kΩ)	Frequency (MHz)
180	0.26
160	0.29
150	0.31
143	0.32
66.5	0.62
35.7	1.06

The switching frequency can go up to 1MHz. The LS-FET's off time must be longer than 500ns during normal boost operation.

UVLO Hysteresis

The MPQ3425 features a programmable UVLO hysteresis (see Figure 2). When VIN powers up, a 4µA current sink is applied to the resistor divider attached to EN. Therefore, VIN must increase by a set amount to overcome the current sink. This amount is the current sink times the resistor from VIN to EN. Once EN reaches 1.5V, the current sink turns off to create the reverse hysteresis for VIN falling.

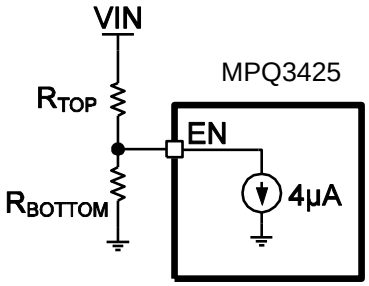


Figure 2: UVLO Hysteresis

The UVLO hysteresis can be calculated with Equation (2):

$$\text{UVLO Hysteresis} = 4\mu A \times R_{TOP} \quad (2)$$

Selecting the Soft-Start Capacitor

The MPQ3425 uses a soft-start (SS) timer that limits V_{COMP} during start-up to prevent excessive current at the input. This prevents premature termination of the source voltage at start-up due to an input current (I_{IN}) overshoot.

When power is applied to the MPQ3425 and the EN pin is asserted, a 5µA internal current source charges the external SS capacitor (C_{SS}). As C_{SS} is charged, the SS voltage (V_{SS}) rises. When V_{SS} reaches 250mV, the MPQ3425 begins switching at a quarter of the programmed frequency. This is known as frequency foldback mode.

At 800mV, f_{SW} becomes the programmed value. Soft start ends when V_{SS} reaches 2.5V. This limits I_L at start-up, forcing I_{IN} to rise slowly to the current required to regulate V_{OUT}.

The soft-start time (t_{SS}) is determined with Equation (3):

$$t_{SS} = \frac{C_{SS} \times 10^{-9} \times 2.5V}{6\mu A} \quad (3)$$

Where C_{SS} (nF) is the soft-start capacitor from SS to GND.

Setting the Output Voltage

V_{OUT} is sensed through two sensing resistors in series (R2 and R3). V_{FB} is typically 1.225V. V_{OUT} can be calculated with Equation (4):

$$V_{OUT} = V_{REF} \times (1 + \frac{R2}{R3}) \quad (4)$$

Where R2 is the top feedback resistor, R3 is the bottom feedback resistor, and V_{REF} is the reference voltage (typically 1.225V).

Select feedback resistors in the 10kΩ range or higher for optimum efficiency.

Selecting the Input Capacitor

An input capacitor is required to supply AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to keep noise minimal. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors are also sufficient.

Use an input capacitor with a value greater than 4.7µF. The capacitor can be electrolytic, tantalum, or ceramic. However, since the

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

capacitor absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with an RMS current rating greater than the inductor ripple current. See the Selecting the Inductor section to determine the inductor ripple current.

To ensure stable operation, place the input capacitor as close to the IC as possible. Alternately, a smaller, high-quality, 0.1µF ceramic capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, the larger capacitor should be tantalum or electrolytic. All ceramic capacitors should be placed close to the MPQ3425.

Selecting the Output Capacitor

The output capacitor must maintain the DC output voltage. Low-ESR capacitors are recommended to keep the output voltage ripple low. The characteristics of the output capacitor also affect the stability of the regulation control system. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. With ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is independent of the ESR. The output voltage ripple (V_{RIPPLE}) can be estimated with Equation (5):

$$V_{RIPPLE} \cong \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} \quad (5)$$

Where V_{IN} and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, f_{SW} is the switching frequency, and C_{OUT} is the capacitance of the output capacitor.

With tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. Estimate the output voltage ripple (V_{RIPPLE}) with Equation (6):

$$V_{RIPPLE} \cong \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}} \quad (6)$$

Where R_{ESR} is the equivalent series resistance of the output capacitor.

Choose an output capacitor that satisfies the output ripple and load transient requirements of the design. A 4.7µF to 22µF ceramic capacitor is suitable for most applications.

Selecting the Inductor

A larger-value inductor results in less ripple current and a lower peak inductor current, reducing stress on the internal N-channel switch. However, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current.

Allow the peak-to-peak ripple current to be approximately 30% to 50% of the maximum input current. Ensure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent regulation loss caused by the current limit. The inductor must not saturate under the worst-case load transient and start-up conditions. Calculate the required inductance with Equation (7):

$$L = \frac{V_{IN}\times(V_{OUT}-V_{IN})}{V_{OUT}\times f_{SW}\times \Delta I} \quad (7)$$

Where ΔI is the peak-to-peak inductor ripple current, ΔI = (30% to 50%) x I_{LOAD_MAX}.

Calculate the max input current (I_{IN_MAX}) with Equation (8):

$$I_{IN_MAX} = \frac{V_{OUT}\times I_{LOAD_MAX}}{V_{IN}\times \eta} \quad (8)$$

Where I_{LOAD_MAX} is the maximum load current, and η is the efficiency.

Selecting the Diode

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. Use a Schottky diode to reduce losses caused by the diode forward voltage and recovery time. The diode should be treated for a reverse voltage equal to or greater than V_{OUT}. The average current rating must be greater than the maximum load current, and the peak current rating must be greater than the peak inductor current.

Compensation

The output of the transconductance error amplifier (COMP) is used to compensate for the regulation control system. The system uses two poles (F_{P1} and F_{P2}) and one zero (F_{Z1}) to stabilize the control loop. F_{P1} is set by the

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

output capacitor (C_{OUT}) and the load resistance (R_{LOAD}). F_{P2} is set by the compensation capacitor (C_{COMP}). F_{Z1} is set by the compensation resistor (R_{COMP}) and C_{COMP}.

These poles are determined by Equation (9), Equation (10), and Equation (11), respectively:

$$F_{P1} = \frac{1}{2 \times \Pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (9)$$

$$F_{P2} = \frac{G_{EA}}{2 \times \Pi \times A_{VEA} \times C_{COMP}} (Hz) \quad (10)$$

$$F_{Z1} = \frac{1}{2 \times \Pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (11)$$

Where R_{LOAD} is the load resistance, G_{EA} is the error amplifier transconductance, and A_{VEA} is the error amplifier voltage gain.

The DC loop gain can be calculated with Equation (12):

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS}}{0.5 \times V_{OUT}^2} (V/V) \quad (12)$$

Where G_{CS} is the compensation voltage to the inductor current gain, and the V_{FB} is the feedback regulation threshold.

There is also a right half-plane zero (RHPZ) that exists in continuous conduction mode in step-up converters, where I_L does not drop to zero in each cycle.

The RHPZ frequency (f_{RHP}) can be calculated with Equation (13):

$$f_{RHP} = \frac{R_{LOAD}}{2 \times \Pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz) \quad (13)$$

Table 2 lists the recommended compensation components for different input voltages, output voltages, and capacitances of the most frequently used output ceramic capacitors. Ceramic capacitors have extremely low ESR values, so a second compensation capacitor from COMP to GND is not required.

For a faster control loop and better transient response, set capacitor C7 to the recommended value in Table 2. Then slowly increase the resistance of R6 and check the load step response on a bench to ensure that the ringing and overshoot on V_{OUT} at the edge of the load steps is minimal. Finally, check the compensation by calculating the DC loop gain and the crossover frequency.

The crossover frequency where the loop gain drops to 0dB (a gain of 1) can be obtained visually by placing a -20dB/decade slope at each pole, and a +20dB/decade slope at each zero. The crossover frequency should be at least one decade below f_{RHP} at the maximum output load current to obtain a high enough phase margin for stability.

Table 2: Component Selection

V_{IN} (V)	V_{OUT} (V)	C_{OUT} (µF)	R_{COMP} (kΩ)	C_{COMP} (nF)	Switching Frequency (kHz)	Inductor (µH)
3	12	4.7	10	6.8	600	8.2
3	12	10	15	6.8	600	8.2
5	12	10	12	4.7	600	6.8
5	12	22	25	4.7	600	6.8
5	18	4.7	12	4.7	600	10
5	18	10	25	4.7	600	10
12	22	4.7	10	6.8	600	10
12	22	10	20	6.8	600	10
12	24	22	40	6.8	600	10
12	48	4.7	30	4.7	600	33

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and low noise. For best results, refer to Figure 3 and follow the guidelines below:

1. Place all components as close to the IC as possible.
2. Keep the path between L1, D1, and C_{OUT} as short as possible to minimize noise and ringing.
3. Place C_{IN} close to IN for the best decoupling results.
4. Keep all feedback components close to FB to prevent noise injections on the FB trace.
5. Tie the ground return of C_{IN} and C_{OUT} close to GND.

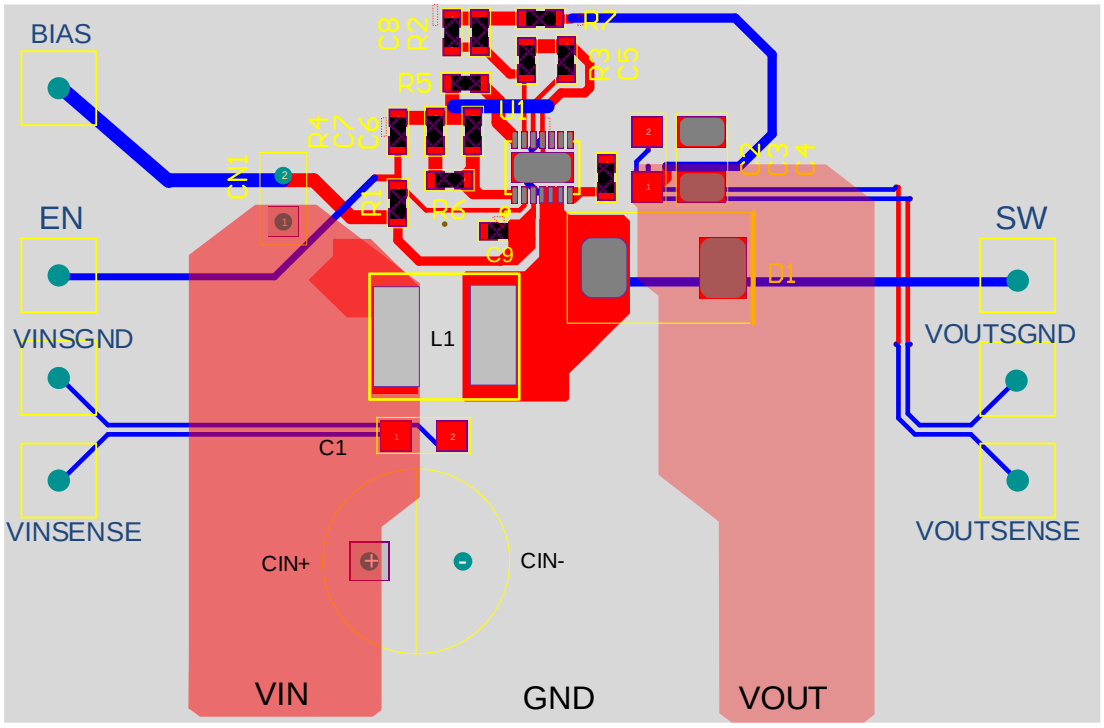


Figure 3: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

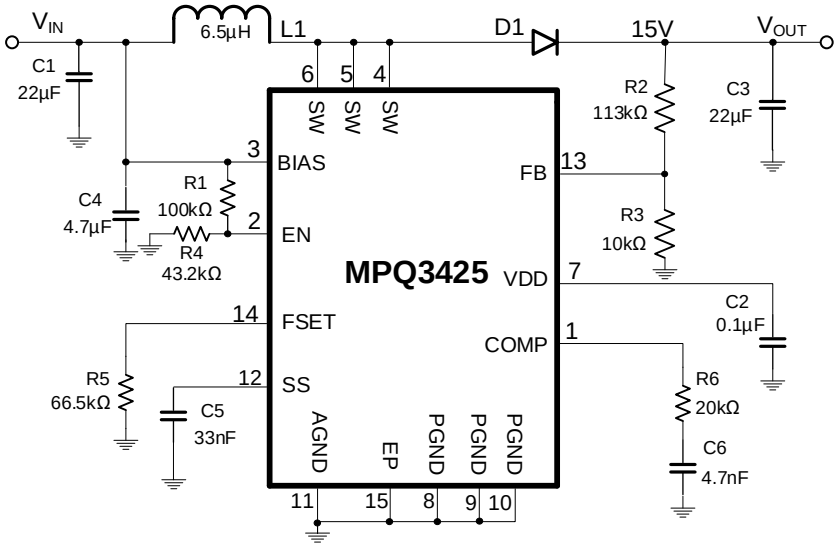


Figure 4: Typical Application Circuit for Boost Topology (15V Output)

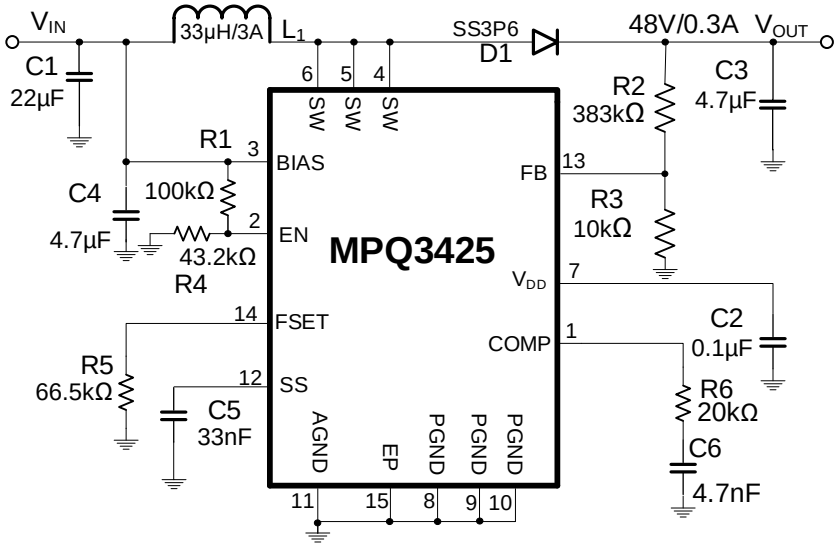


Figure 5: Typical Application for Boost Topology (48V Output)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

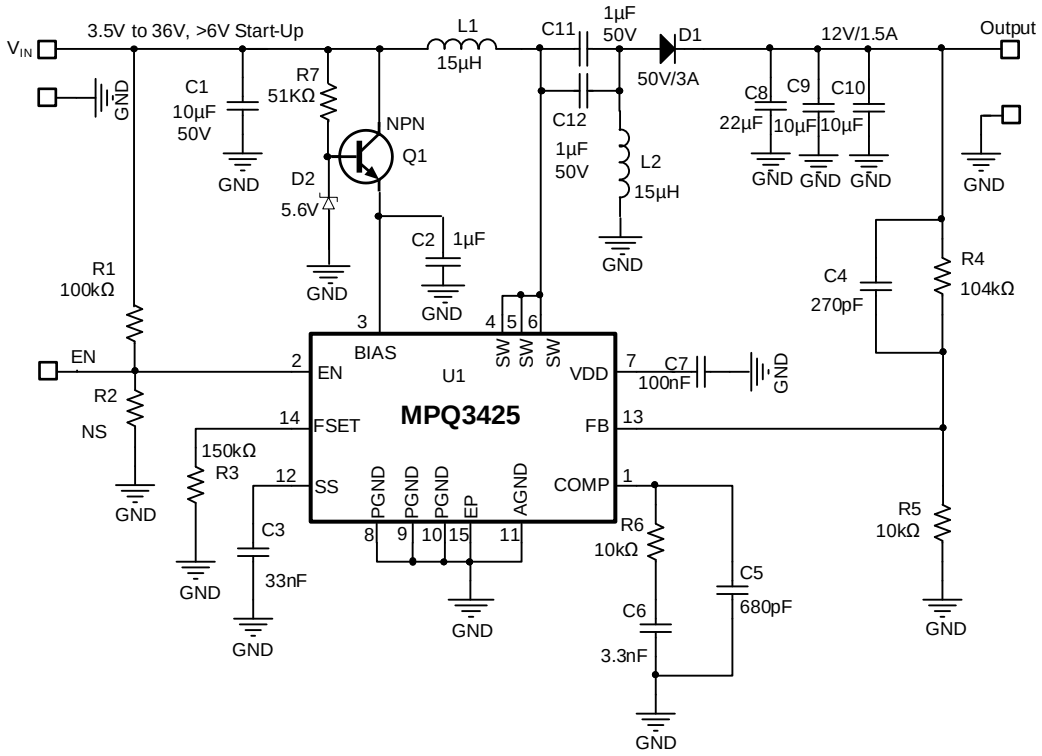


Figure 6: Typical Application for SEPIC Topology (BIAS with NPN Plus 5.6V Zener Diode)

Table 3: V_{IN} Supply Current for Different f_{SW}

f_{SW} (MHz)	V_{IN} Supply Current (mA)
0.5	3
1	4

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

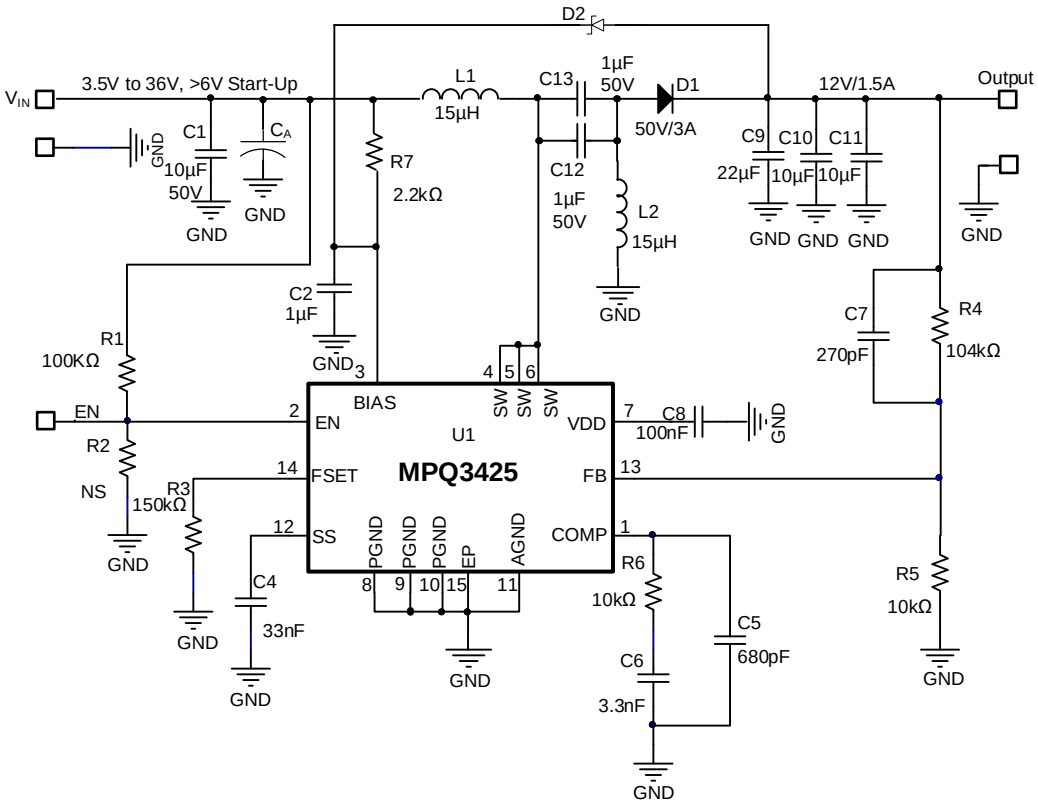


Figure 7: Typical Application for SEPIC Topology (Start-Up through BIAS and V_{OUT}) (5)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

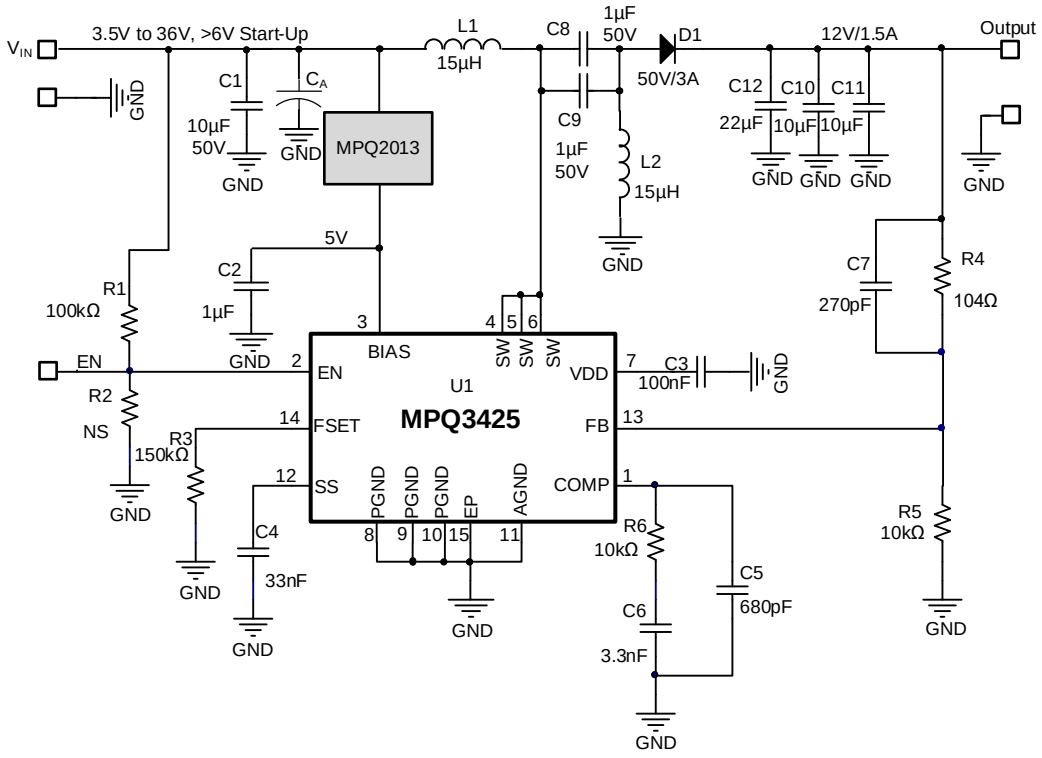


Figure 8: Typical Application for SEPIC Topology (Start-Up through LDO) (5)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

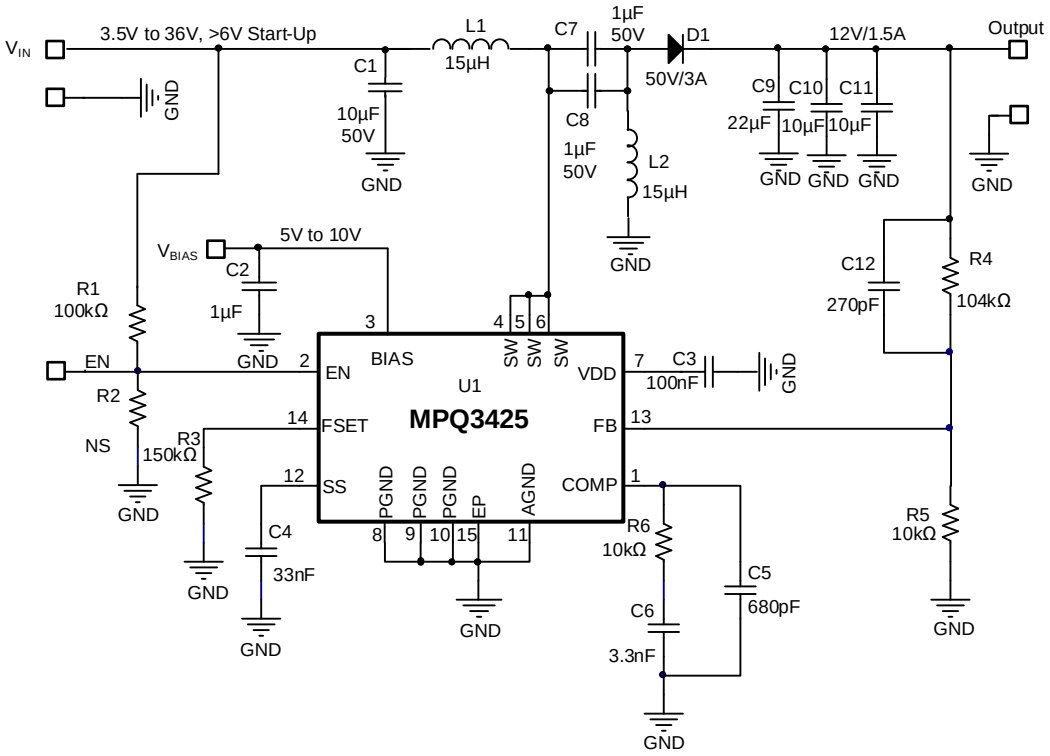


Figure 9: Typical Application for SEPIC Topology (Start-Up through BIAS) (5)

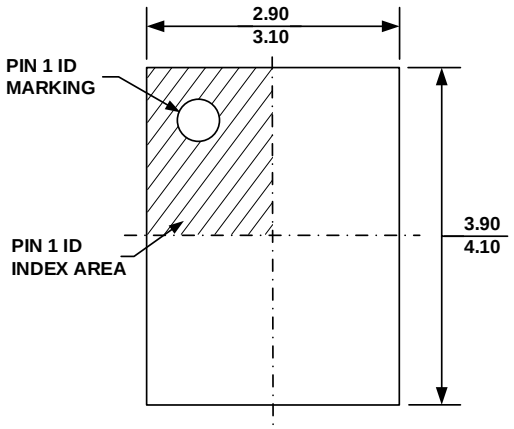
Note:

5) See Table 3 on page 20 for the V_{IN} Supply Current for Different f_{SW}.

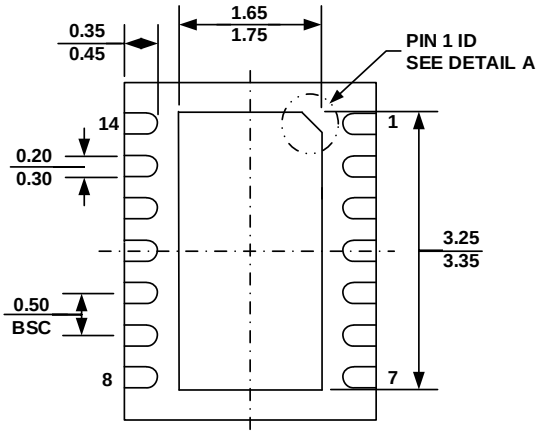
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PACKAGE INFORMATION

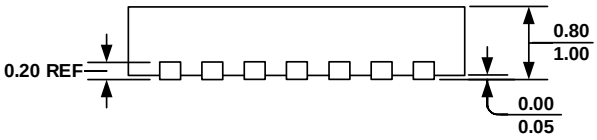
QFN-14 (3mmx4mm)



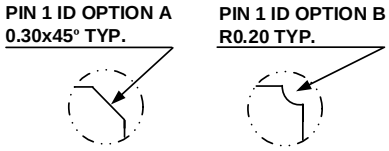
TOP VIEW



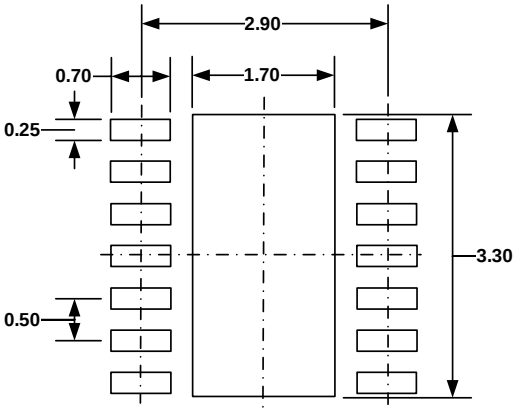
BOTTOM VIEW



SIDE VIEW



DETAIL A



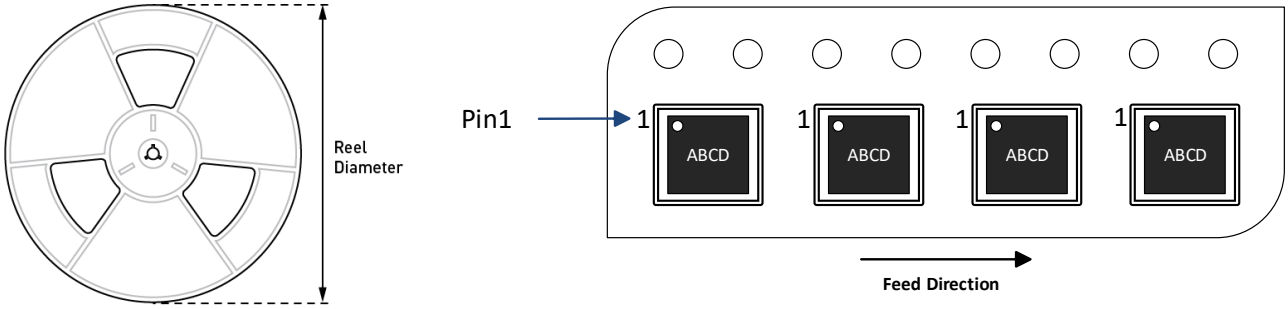
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3425DL-AEC1-Z	QFN-14 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	05/24/2016	Initial Release	-
1.01	6/6/2022	Updated the MSL Rating, and Top Marking, in the Ordering Information section	2
		Updated the ESD Ratings section	3
		Updated Package Information section	19
		Formatting updates	14–16, 20
		Updated footnote formatting	All
1.1	7/6/2023	• Added the QFN-14 (4mmx4mm) and wettable flank package information to the Description section • Updated the Features section: ○ Updated “Input Voltage Range” to “BIAS Supply Voltage Range” ○ Added the “Wide 3V to 50V Input Voltage Range” bullet point ○ Added thermal shutdown threshold (160°C) ○ Added the QFN-14 (4mmx4mm) and wettable flank package information • Updated the Applications section: ○ Added the “Boost Converter and Single-Ended Primary-Inductance Converter (SEPIC) Topologies” bullet point ○ Added the “Pre-Boost Applications” bullet point • Updated the name of pin 3 to “BIAS” in the Typical Application schematic	1
		Added the new part number (MPQ3425GRE-AEC1) information and QFN-14 (4mmx4mm) package information to the Ordering Information section; added the Top Marking section for the new part number (MPQ3425GRE)	2
		Updated the name of pin 3 to “BIAS” in the QFN-14 (3mmx4mm) package reference; added the QFN-14 (4mmx4mm) package reference	3
		• Updated the name of pin 3 to “BIAS” in the Pin Functions section • Updated the SW range from “-0.5V to +22V” to “-0.5V to +55V” in the Absolute Maximum Ratings section • Updated the V_{OUT} range from “3.1V to 22V” to “3.1V to 55V” in the Recommended Operating Conditions section • Updated the Thermal Resistance section: ○ Updated the first line to “QFN-14 (3mmx4mm)” ○ Added the QFN-14 (4mmx4mm) package information	4
		Updated the Electrical Characteristics conditions to “V_{BIAS} = V_{IN} = V_{EN} = 5V”; updated the “Operating input voltage” parameter to “Operating supply voltage”; updated the “V_{IN}” symbol to “V_{BIAS}”; updated “V_{IN}” to “V_{BIAS}” in the UVLO threshold parameter conditions	5
		Updated V_{OUT} condition to “48V” in the Typical Characteristics section	6
		Updated Figure 1	13
		Updated Figure 1 page reference	14

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REVISION HISTORY *(continued)*

Revision #	Revision Date	Description	Pages Updated
1.1	7/6/2023	Updated the reference to Table 3; updated Table 2	17
		Updated “MPQ3452” to “MPQ3425” in the headers	17–21
		Updated Figure 4 and Figure 5	19
		Added Table 3	20
		Added Figures 6–9	20–23
		Added the QFN-14 (4mmx4mm) package information to the Package Reference section	25–26
		Added the new part number (MPQ3425GRE-AEC1-Z) information to the Carrier Information section	27
		Updated “22V” to “55V” in the headers	All
1.2	1/10/2025	• Removed the QFN-14 (4mmx4mm) package and wettable-flank package information from the Description section • Removed "QFN-14 (4mmx4mm) package" and "QFN-14 (4mmx4mm) Package is Available in a Wettable Flank Package” from the Features section	1
		• Removed MPQ3425GRE-AEC1 from the Ordering Information section • Removed the top marking of MPQ3425GRE from the Top Marking section and made formatting edits • Removed the top view of MPQ3425GRE from the Package Reference section	2
		Removed the thermal resistance of the QFN-14 (4mmx4mm) package from the Absolute Maximum Ratings section	3
		Removed the QFN-14 (4mmx4mm) package from the Package Information section	23
		Removed MPQ3425GRE-AEC1-Z from the Carrier Information section	24
1.3	6/23/2025	• Updated max switching frequency from 2MHz to 1MHz in Description section • Updated max switching frequency from 2MHz to 1MHz in Features section	1
		• Updated the switching frequency options in Table 1 • Updated the Selecting the Switching Frequency section	14
		• Updated the V_{IN} supply current in Table 3	19

Notice: The information in this document is subject to change without notice. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.