MPQ3359C

1/2/3/4-Channel, Max 160mA/Ch, Boost WLED Controller with High Dimming Ratio, AEC-Q100 Qualified

DESCRIPTION

The MPQ3359C is a step-up controller with 4 channel current sources. The device is designed to drive white LED arrays as backlighting for medium-sized LCD panels.

The device uses peak current mode control as its pulse-width modulation (PWM) control architecture to regulate the boost converter. The device drives an external MOSFET to boost the output voltage (V_{OUT}) from a 3.5V to 40V input supply voltage (V_{IN}). The switching frequency (f_{SW}) can be configured via a resistor or an external clock.

Four channel current sources are applied to the LED cathode to adjust LED brightness. The MPQ3359C regulates the current in each LED string to the value set by an external current-setting resistor, with 2.5% current regulation accuracy between strings.

A low headroom voltage is provided to improve efficiency and IC thermal performance.

The MPQ3359C provides analog and PWM dimming with two separate input pins (EN/ADIM and PDIM). The device also has a fixed delay time between LED current channels to eliminate noise during PWM dimming.

Robust protections are included to guarantee safe device operation. Protection modes include input current (I_{IN}) over-current protection, cycle-by-cycle current limiting, over-voltage protection (OVP), over-temperature protection (OTP), LED short/open protection, LEDx short-to-GND protection and V_{OUT} short-to-GND protection.

The MPQ3359C is available in a QFN-20 (3mmx4mm) package, and is available in AEC-Q100 Grade 1.

FEATURES

- 3.5V to 40V Input Voltage (V_{IN}) Range
- 4 Channels with a Maximum of 160mA per Channel
- Configurable Switching Frequency (f_{SW}) Up to 2.2MHz
- External Sync SW Function
- Pulse-Width Modulation (PWM) Dimming
- Analog Dimming
- Deep Dimming Ratio
- Excellent EMI Performance and Frequency Spread Spectrum (FSS)
- Fixed 100µs Delay Time between LED Current Channels during PWM Dimming (Replaces Phase Shift)
- 2.5% Current Matching
- Cycle-by-Cycle Current Limiting
- Disconnect VOUT from VIN
- Input Over-Current Protection
- LED String Open/Short Protection
- Over-Temperature Protection (OTP)
- LEDx Pin Short-to-GND Protection
- V_{OUT} Short-to-GND Protection
- Ability to Disable LED4 if LED4 Is Unused
- Fault Indicator Signal Output
- Available in a QFN-20 (3mmx4mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Displays
- Tablets and Notebooks

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TYPICAL APPLICATION (1) (2) (3) (4)

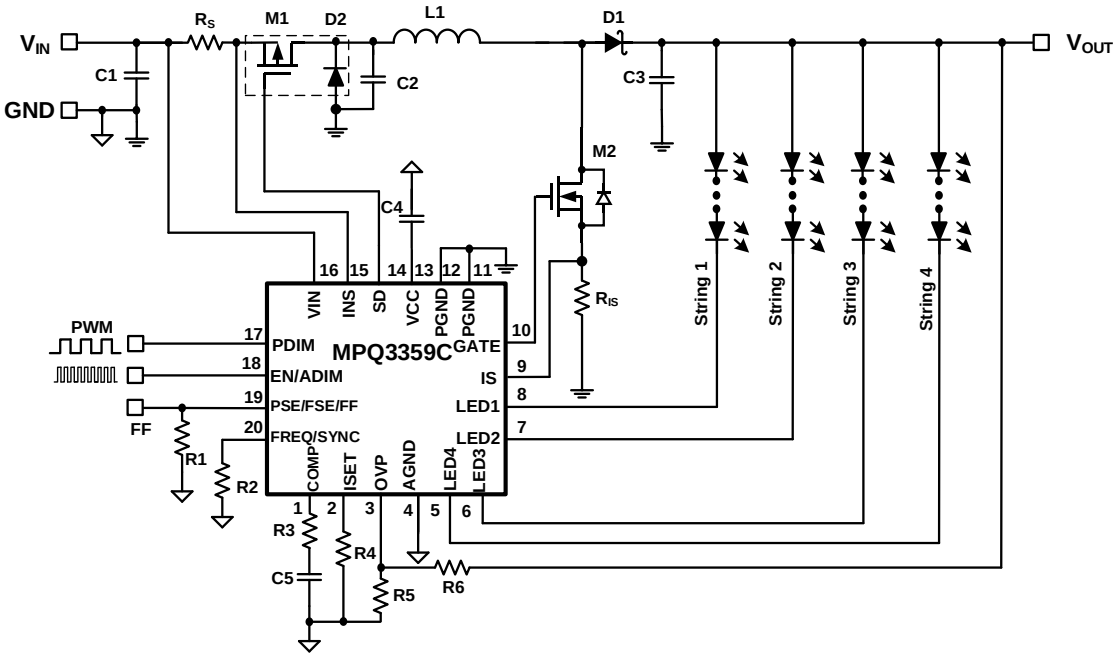

Figure 1: Typical Application with 4 Strings

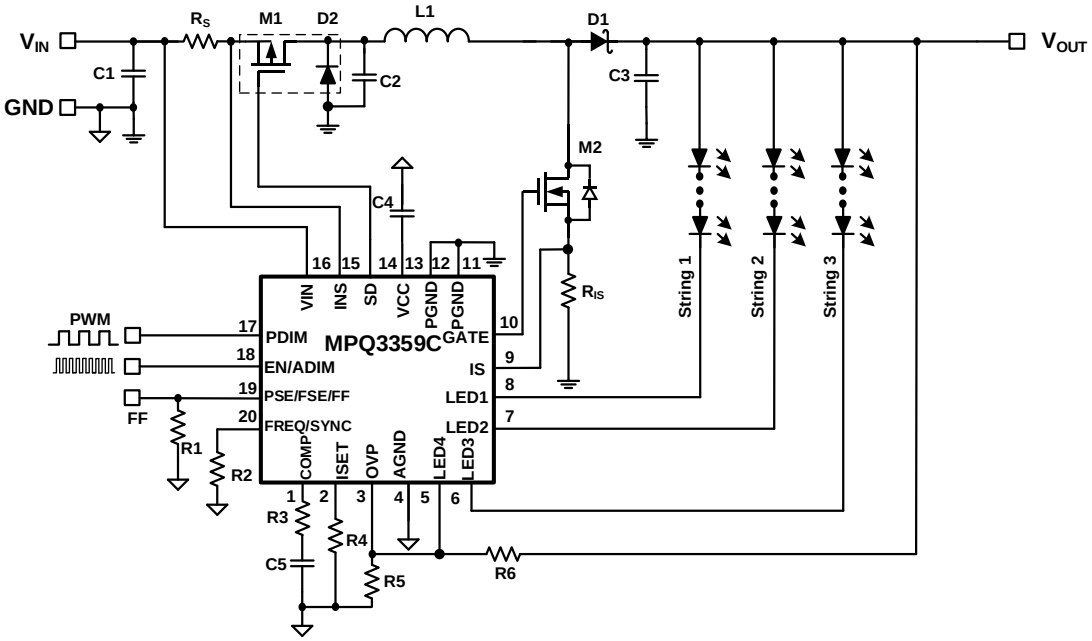

Figure 2: Typical Application with 3 Strings (Connect LED4 to the OVP Pin)

Notes:

1) For 1 channel, tie LED1~4 together.
2) For 2 channels, tie LED1~2 together, and tie LED3~4 together.
3) For 3 channels, connect the LED4 pin to the OVP pin.
4) M1 and D2 must be used together.

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3359CGLE-AEC1*	QFN-20 (3mmx4mm)	*See Below*	1

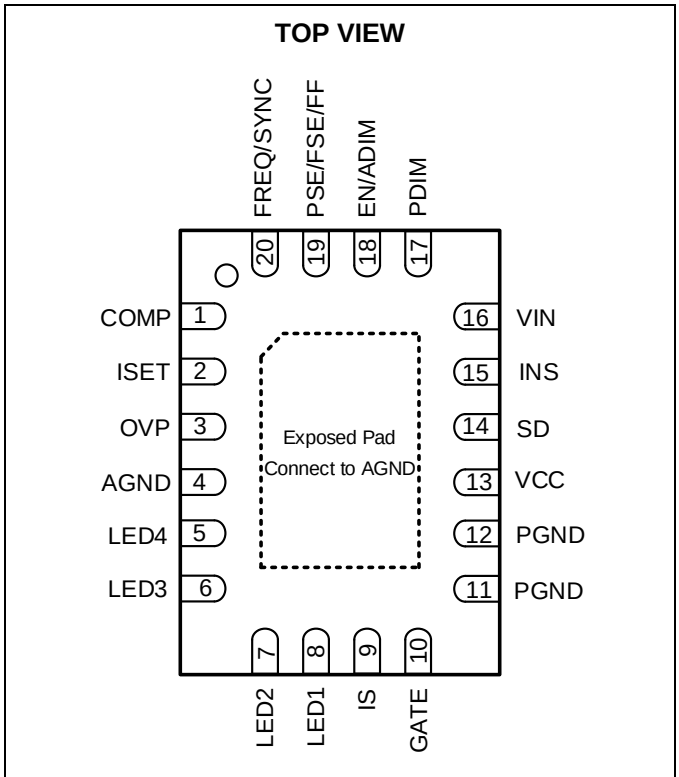
* For Tape & Reel, add suffix -Z (e.g. MPQ3359CGLE-AEC1-Z).

TOP MARKING (MPQ3359CGLE-AEC1)

MPYW
3359
CLLL
E

MP: MPS prefix
Y: Year code
W: Week code
3359C: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	COMP	**Compensation pin.**
2	ISET	**LED current setting.** Tie a current-setting resistor from ISET to GND to configure the current in each LED string.
3	OVP	**Over-voltage protection (OVP) pin.** Connect a resistor divider from the VOUT pin to the OVP pin and from the OVP pin to AGND to configure the OVP threshold.
4	AGND	**Analog ground.**
5	LED4	**LED string 4 current input.** Connect the LED string 4 cathode to this pin. If LED4 is not used, connect it directly to the OVP pin.
6	LED3	**LED string 3 current input.** Connect the LED string 3 cathode to this pin.
7	LED2	**LED string 2 current input.** Connect the LED string 2 cathode to this pin.
8	LED1	**LED string 1 current input.** Connect the LED string 1 cathode to this pin.
9	IS	**Low-side MOSFET (LS-FET) current-sense (CS) pin.** During normal operation, the IS pin senses the voltage across the external inductor current (I_L)-sensing resistor (R_{IS}) for peak current mode control. IS also limits I_L during every switching cycle.
10	GATE	**Power MOSFET driver output for the step-up converter.** The GATE pin drives the external N-channel power MOSFET.
11, 12	PGND	**Step-up converter power ground.**
13	VCC	**5V LDO output pin.** VCC provides power to the internal logic and gate driver. Place a ceramic capacitor as close to this pin as possible to reduce noise.
14	SD	**External disconnect P-channel MOSFET gate drive pin.** This pin turns off the external P-channel MOSFET if a fault occurs. Float this pin if it is not used.
15	INS	**Input CS pin.** When the voltage across a current-sense resister (R_S) exceeds the input current (I_{IN}) over-current protection (OCP) threshold, the MPQ3359C turns off the P-channel MOSFET. Connect this pin to VIN pin if it is not used.
16	VIN	**Power supply input.** The VIN pin supplies power to the IC.
17	PDIM	**Pulse-width modulation (PWM) dimming signal input pin.** Apply a 100Hz to 30kHz PWM signal to this pin for PWM dimming. PDIM is pulled low internally.
18	EN/ADIM	**IC enable and analog dimming signal input pin.** Apply a >5kHz PWM signal to this pin for analog dimming. EN/ADIM is pulled low internally. Pull this pin low for >60ms to shut down the IC.
19	PSE/FSE /FF	**Delay function enable, frequency spread spectrum (FSS) enable, and fault flag pin.** This pin is a current-source output (32μA). Connect a resistor from this pin to AGND to configure its voltage. After VIN and EN start up, the IC detects the PSE/FSE/FF pin's voltage to enable the corresponding functions: • >2.85V: Enable the delay function and FSS. • 2V to 2.55V: Enable the delay function only. • 1.27V to 1.8V: Enable FSS only. • <1.13V: Disable the delay function and FSS. If the delay function is enabled, there is a fixed 100μs delay between the LED current channels to reduce system stress and eliminate noise during PWM dimming. FSS improves EMI performance. The fault flag indicates the fault status if a fault occurs, and is always enabled.
20	FREQ/ SYNC	**Switching frequency (f_{SW}) setting and SYNC pin.** The FREQ/SYNC pin configures f_{SW}. Connect a resistor between FREQ/SYNC and AGND to set the converter's f_{SW}, or connect an external clock to this pin to synchronize the boost f_{SW}.
Exposed pad	AGND	**Chip ground.** Connect the exposed pad to AGND.

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ABSOLUTE MAXIMUM RATINGS (5)

Input voltage (V_{IN}) .....-0.3V to +42V
V_{LED1} to V_{LED4}.....-0.5V to +50V
V_{SD},V_{INS} .....V_{IN} - 6V to V_{IN}
V_{SD},V_{INS} ..... > -0.3V
V_{IS} .....-0.3V to +5V
All other pins .....-0.3V to +6V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (6)
QFN-20 (3mmx4mm)..... 3.59W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (7)

Supply voltage (V_{IN}) .....3.5V to 40V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (8) θ_{JA} θ_{JC}

QFN-20 (3mmx4mm)……..34.8…….1.7....°C/W

Notes:

5) Exceeding these ratings may damage the device.
6) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}		3.5		40	V
Quiescent supply current	I_Q	No switching		3		mA
Shutdown supply current	I_{ST}	V_{IN} = 12V, V_{EN} = 0V			1	μA
V_{IN} under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Rising edge		3.25	3.45	V
V_{IN} UVLO hysteresis				250		mV
Low-dropout (LDO) regulator output voltage	V_{CC}	V_{EN} = 2V, 6V < V_{IN} < 24V, 0mA < I_{VCC} < 10mA	4.8	5	5.4	V
EN voltage (V_{EN}) on threshold	V_{EN_ON}	V_{EN} rising	1.4			V
V_{EN} off threshold	V_{EN_OFF}	V_{EN} falling			0.5	V
EN/ADIM and PDIM pull-down resistance	$R_{EN/ADIM}$			1		MΩ
PSE/FSE/FF source current	I_{PSE}		29.7	32	34.3	μA
Step-Up Converter						
Gate driver source impedance	R_{GATE_SO}	V_{GATE} = 5V		4		Ω
Gate driver sink impedance	R_{GATE_SI}	V_{GATE} = 5V, I_{GATE} = 10mA		2.5		Ω
Switching frequency	f_{SW}	R_{FREQ} = 10kΩ	1.85	2.05	2.25	MHz
		R_{FREQ} = 50kΩ	400	440	480	kHz
FREQ voltage	V_{FREQ}		-5%	1.1	+5%	V
Maximum duty cycle	D_{MAX}	f_{SW} = 440kHz	92			%
Cycle-by-cycle current limiting	V_{LIM_CYC}		230	300		mV
SYNC low threshold	V_{SYNC_LO}	V_{SYNC} falling			0.5	V
SYNC high threshold	V_{SYNC_HI}	V_{SYNC} rising	1.4			V
COMP transconductance	G_{COMP}	ΔI_{COMP} ≤ 10μA		100		μA/V
COMP source current limit	I_{COMP_SO}			90		μA
COMP sink current limit	I_{COMP_SI}			90		μA
Current Dimming						
PDIM/ADIM input low threshold	V_{DIM_LO}	V_{DIM} falling			0.5	V
PDIM/ADIM input high threshold	V_{DIM_HI}	V_{DIM} rising	1.4			V
LED Current Regulator						
LEDx regulation voltage	V_{HD}	I_{LED} = 20mA		350		mV
		I_{LED} = 100mA		650		mV
Current matching [9]		I_{LED} = 20mA	-2.5		+2.5	%
		I_{LED} = 100mA	-2.5		+2.5	%
ISET voltage	V_{ISET}			1.2		V
LED current	I_{LED}	R_{ISET} = 12kΩ	97	100	103	mA
		R_{ISET} = 24kΩ, ADIM duty = 2%, I_{LED} = 1/50 x 50mA = 1mA	0.7	0.9	1.1	mA
Delay time	t_{DELAY}	Between I_{LED} channels		100		μs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protections						
Over-voltage protection (OVP) threshold	V_{OVP}		1.9	2	2.1	V
OVP hysteresis				200		mV
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails		100		mV
Input over-current protection (OCP) threshold	V_{IN_OCP}	Input current (I_{IN}) sense	80	100	120	mV
INS sink current	I_{INS}		16	20	24	µA
LEDx over-voltage (OV) threshold	V_{LEDx_OV}			5		V
LEDx OV fault timer	t_{LEDx_OV}			7.7		ms
LEDx UVLO threshold	V_{LEDx_UV}			100		mV
Thermal shutdown threshold (10)	T_{ST}	Rising edge		170		°C
		Hysteresis		20		°C
SD pull-down current	I_{SD}			60		µA
SD voltage (respective to V_{IN})	V_{SD-IN}	V_{IN} = 12V, V_{IN} - V_{SD}		5.3		V

Notes:

9) Matching is defined as the difference between the maximum current and minimum current, divided by 2 times the average current.
10) Guaranteed by design.

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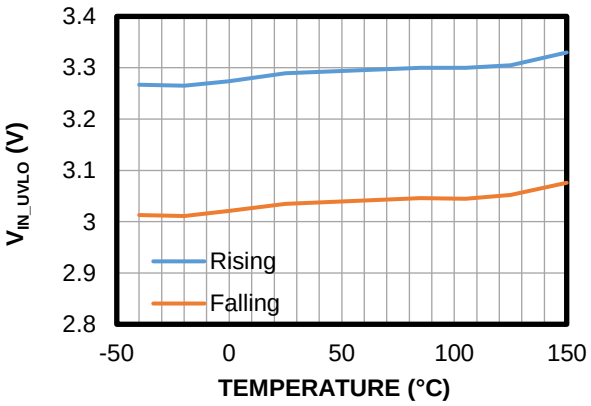
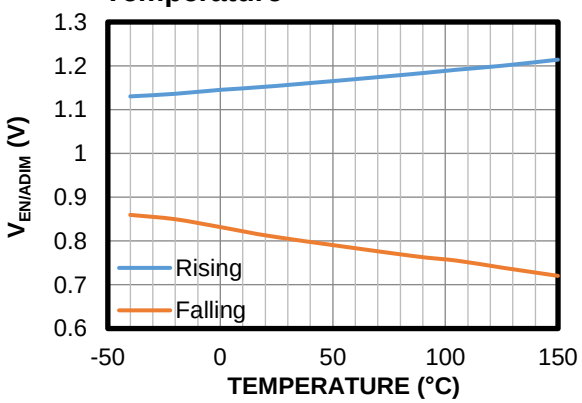
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, unless otherwise noted.

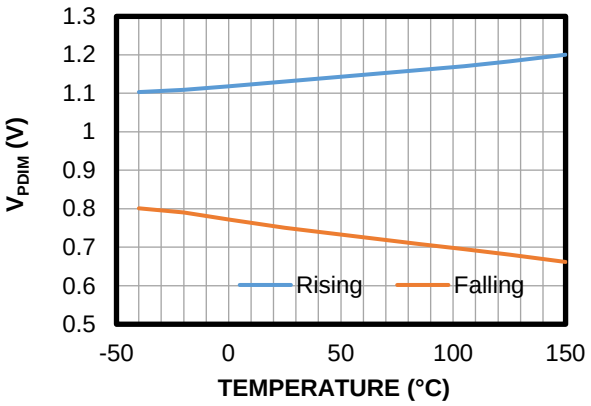
V_{IN} UVLO Threshold vs. Temperature



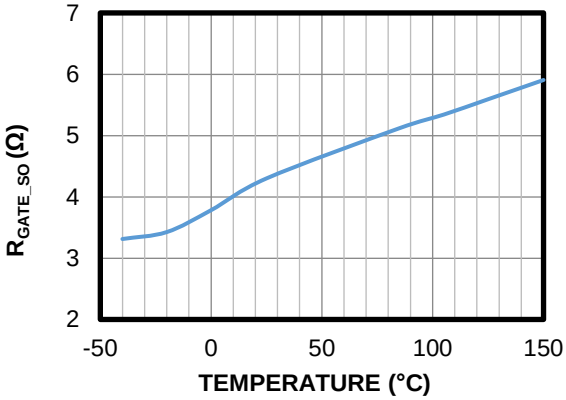
EN/ADIM Threshold vs. Temperature



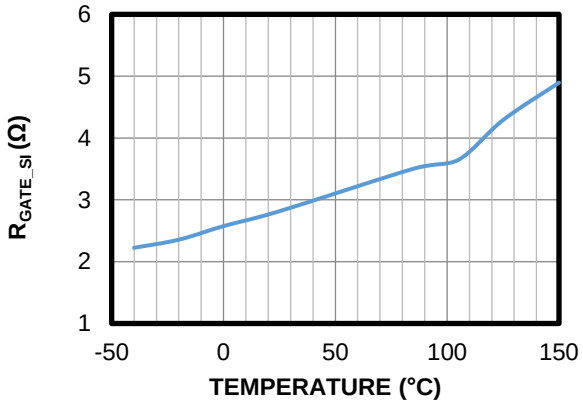
PDIM Threshold vs. Temperature



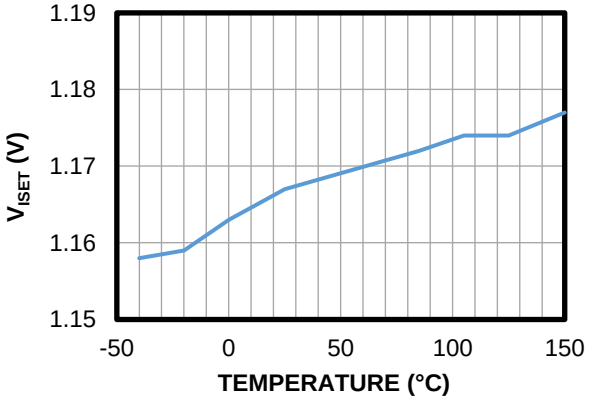
Gate Driver Source Impedance (R_{GATE_SO}) vs. Temperature



Gate Driver Sink Impedance (R_{GATE_SI}) vs. Temperature



ISET Voltage vs. Temperature



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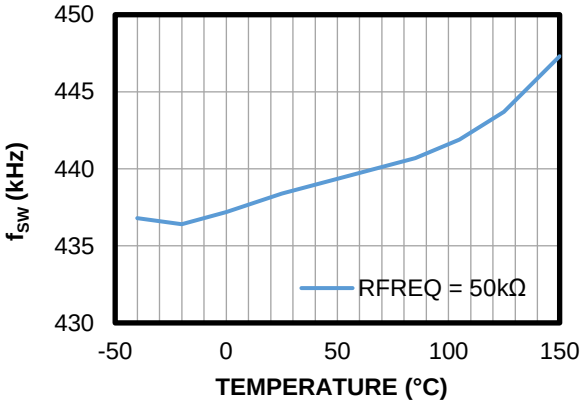
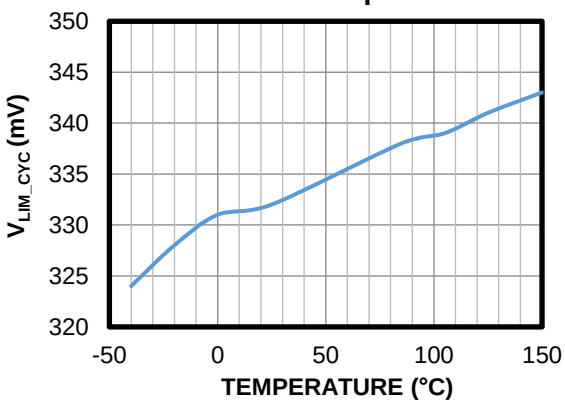
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, unless otherwise noted.

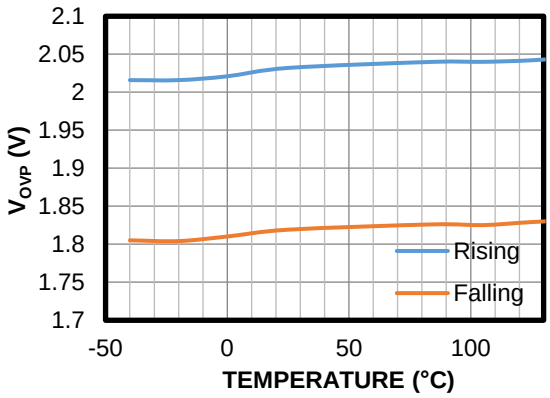
Switching Frequency vs. Temperature



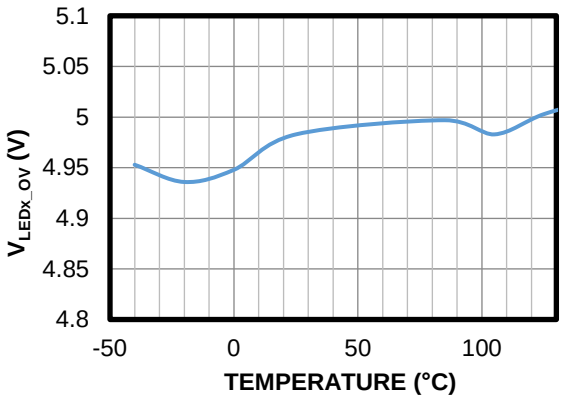
Cycle-by-Cycle Current Limit Threshold vs. Temperature



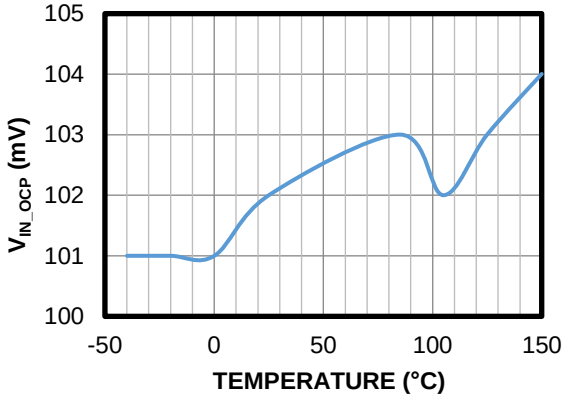
OVP Threshold vs. Temperature



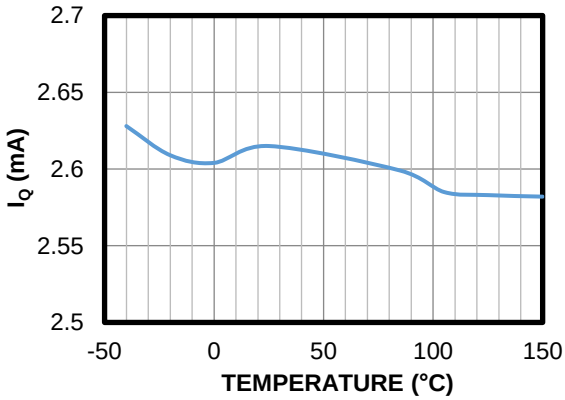
V_{LEDx} Over-Voltage Threshold vs. Temperature



I_{IN} OCP Threshold vs. Temperature



Quiescent Current vs. Temperature



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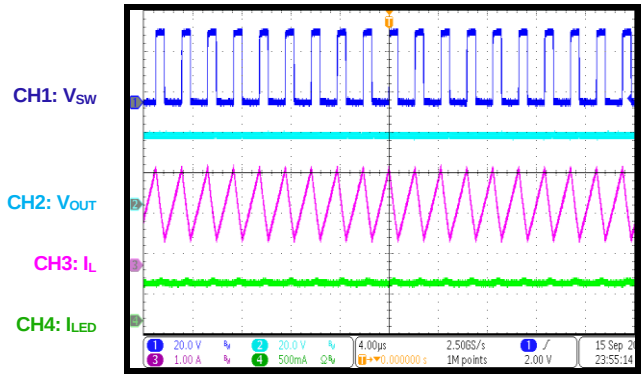
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, 4 strings, 12 LEDs in series, 120mA/string, L = 15µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted.

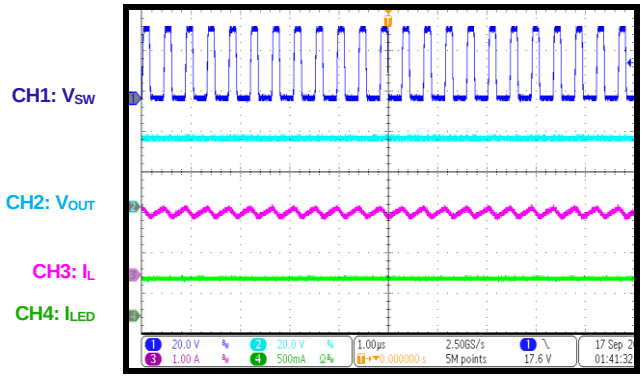
Steady State

f_{SW} = 440kHz

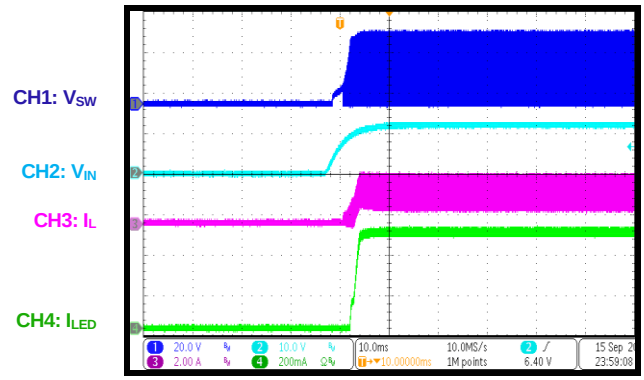


Steady State

f_{SW} = 2.2MHz

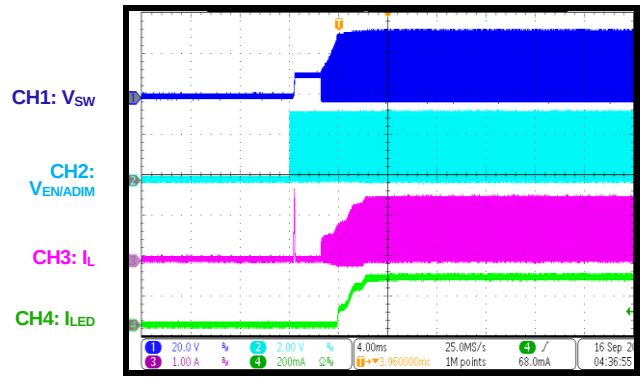


Start-Up through VIN



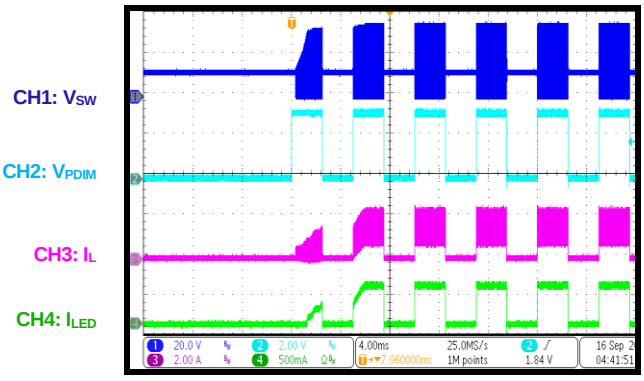
Start-Up through EN/ADIM

$f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 50%



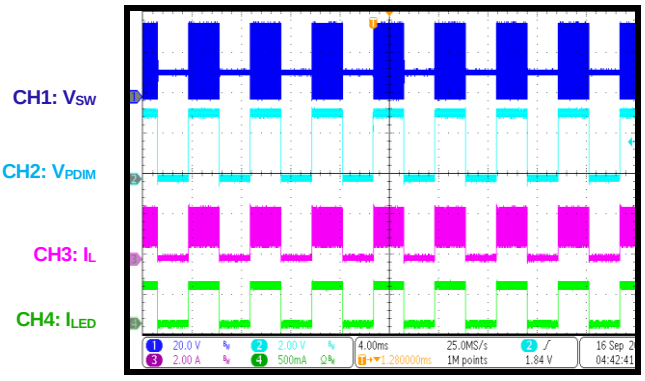
Start-Up through PDIM

f_{PDIM} = 200Hz, D_{PDIM} = 50%



PWM Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 50%



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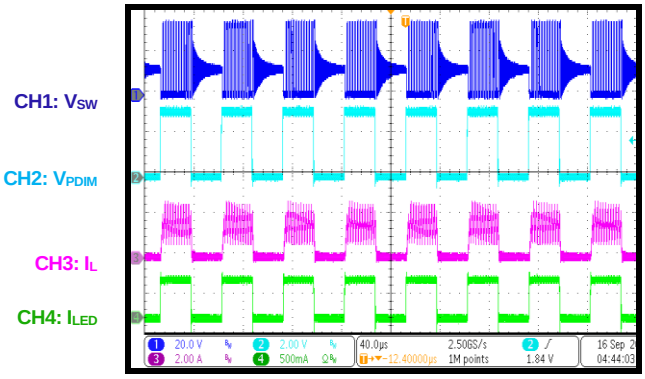
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 4 strings, 12 LEDs in series, 120mA/string, L = 15µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted.

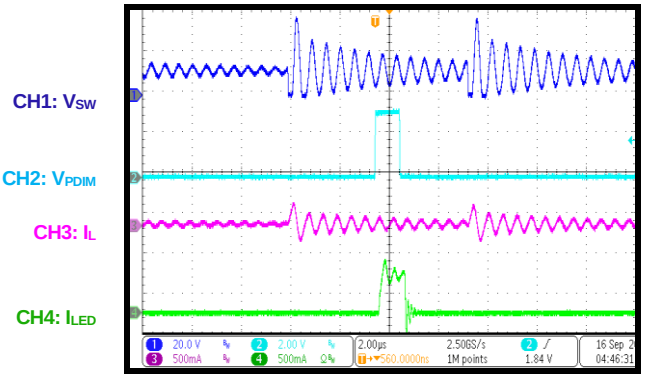
PWM Dimming

f_{PDIM} = 20kHz, D_{PDIM} = 50%



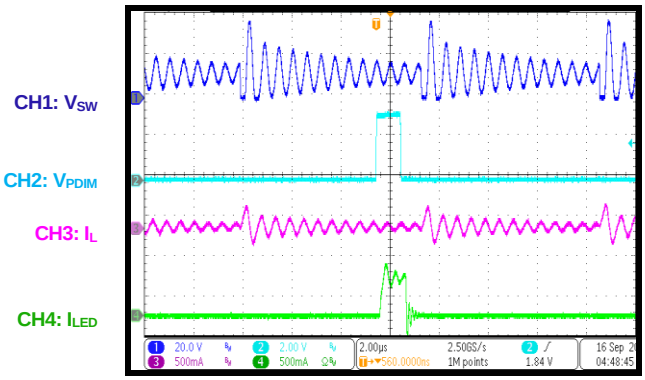
PWM Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 0.02%



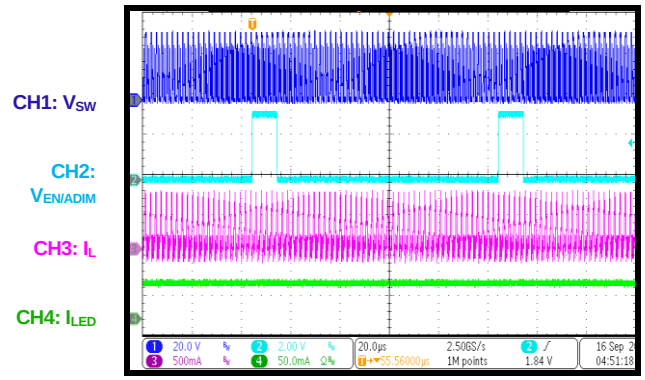
PWM Dimming

f_{PDIM} = 100Hz, D_{PDIM} = 0.01%



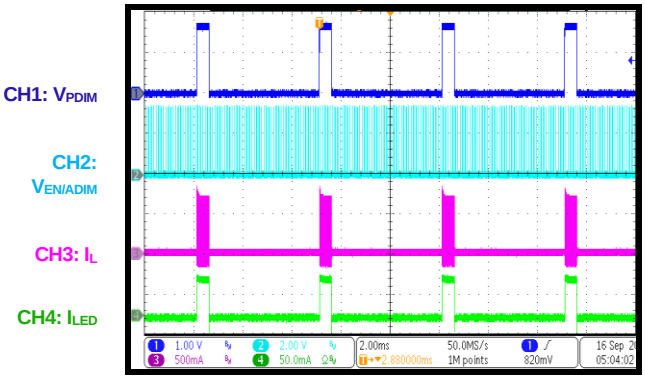
Analog Dimming

$f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 10%



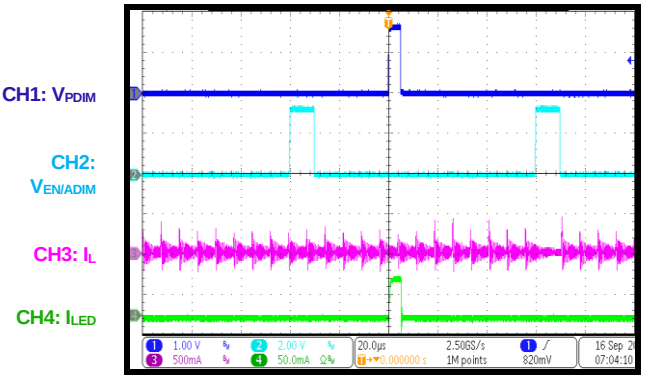
Both PWM Dimming and Analog Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 10%, $f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 10%



Both PWM Dimming and Analog Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 0.1%, $f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 10%



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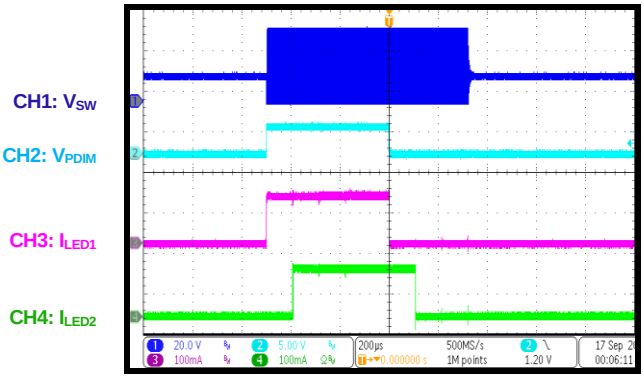
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

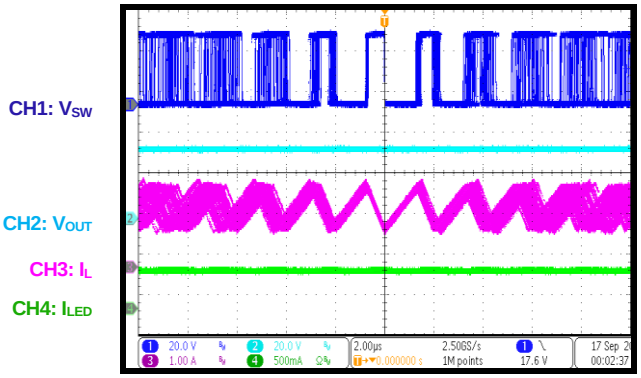
V_{IN} = 12V, 4 strings, 12 LEDs in series, 120mA/string, L = 15µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted.

PWM Dimming with 100µs Delay Time Function

f_{PDIM} = 200Hz, D_{PDIM} = 10%

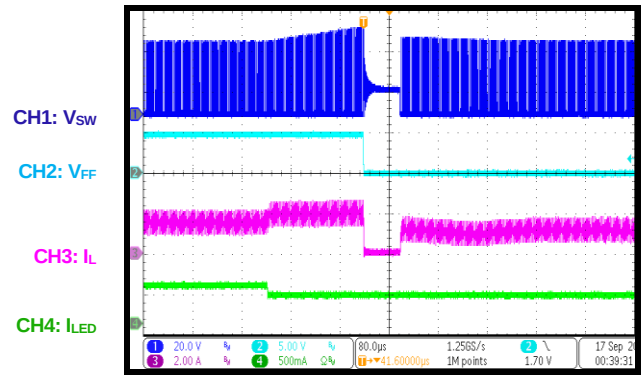


Frequency Spread Spectrum



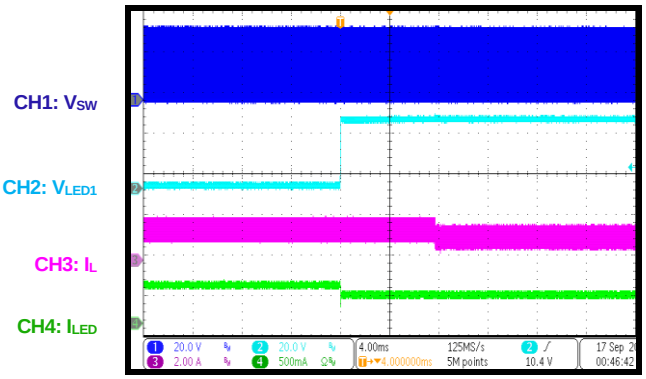
LED Open Protection

Open LED1 under normal operation



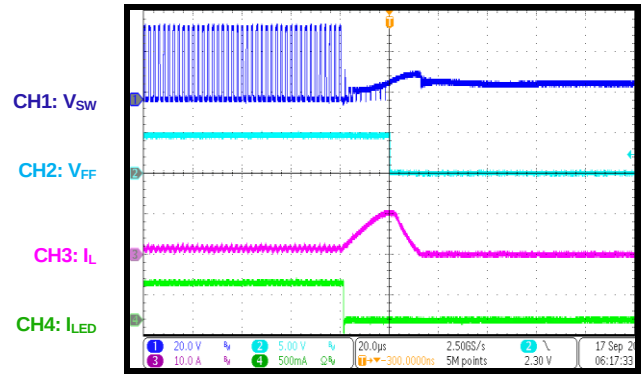
LED Short Protection

Short LED1 under normal operation

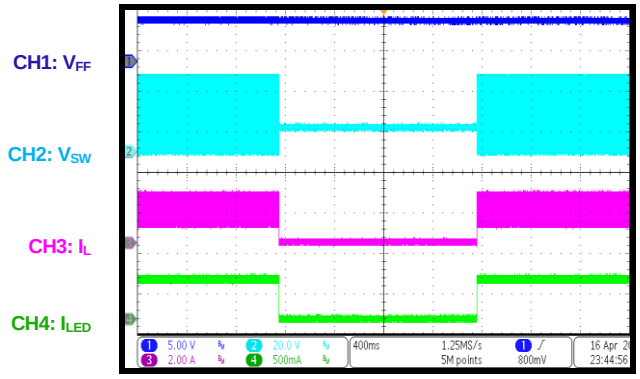


VOUT Short-to-GND Protection

Set the input OCP threshold = 10A



Over-Temperature Protection



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FUNCTIONAL BLOCK DIAGRAM

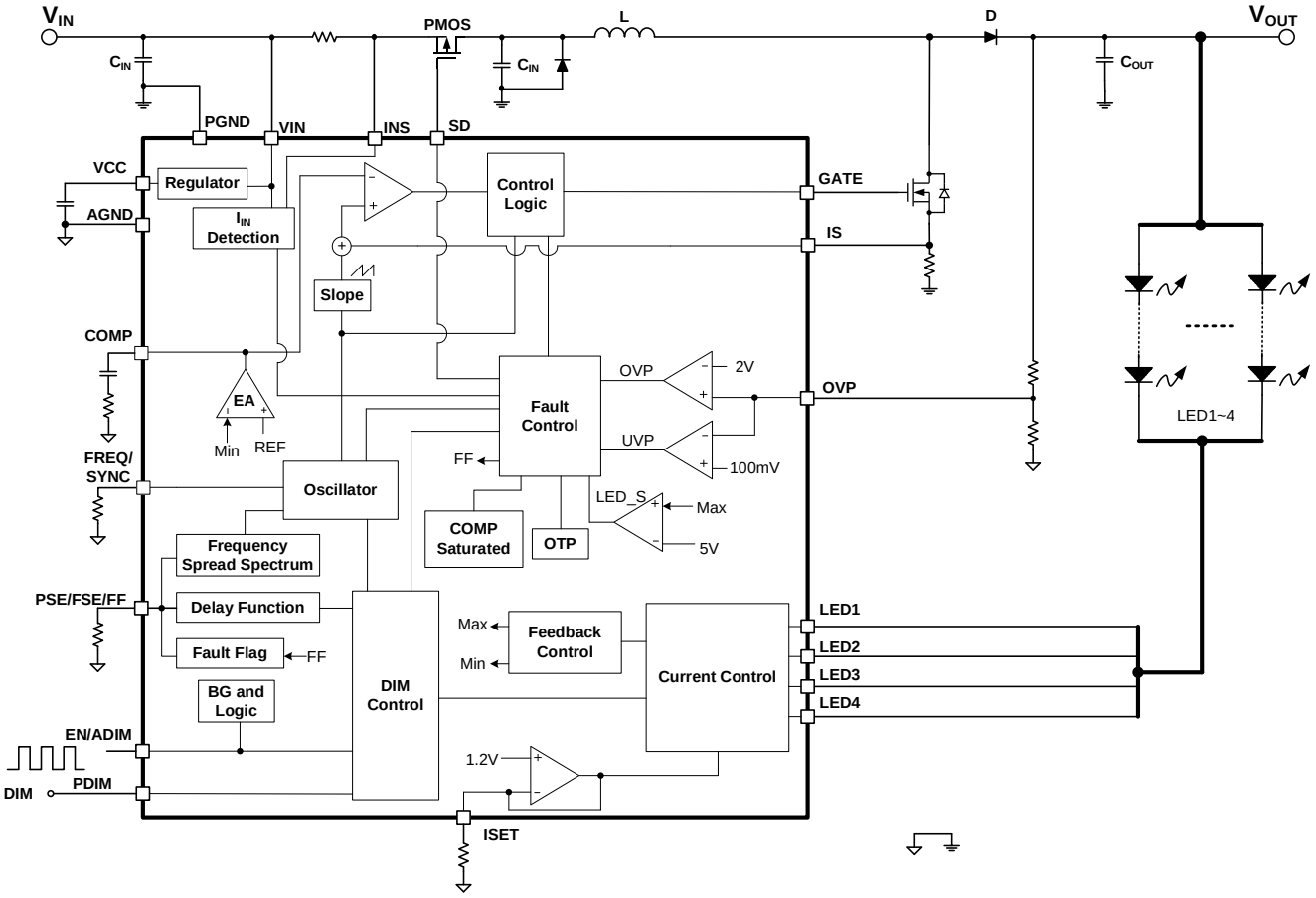

Figure 3: Functional Block Diagram

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OPERATION

The MPQ3359C is a configurable, fixed-frequency, peak current mode step-up controller with up to 4 channels of regulated current sources to drive an array of white LEDs (WLEDs).

Internal 5V Regulator

The MPQ3359C includes an internal linear regulator (VCC). When the input voltage (V_{IN}) exceeds 6V, this regulator provides a 5V power supply to the external MOSFET gate driver and the internal control circuitry. The VCC voltage (V_{CC}) drops to 0V when the device shuts down. The device remains disabled until V_{CC} exceeds under-voltage lockout (ULVO) threshold.

System Start-Up

When enabled, the MPQ3359C checks the topology connection. The IC draws current from the SD pin to turn on the P-channel MOSFET if it is used. The IC then monitors the OVP pin to see if the output is shorted to PGND. If the OVP pin's voltage (V_{OVP}) is below 100mV, the IC is disabled and latches off. The MPQ3359C continues to check other safety limits (e.g. over-voltage protection (OVP)). If all protection tests pass, the IC starts boosting the step-up converter.

The recommended start-up sequence is listed below:

1. V_{IN}
2. EN/ADIM
3. PWM dimming signal

Step-Up Converter

The MPQ3359C employs peak current mode control to regulate the output power (P_{OUT}). At the beginning of each switching cycle, the internal clock turns on the external N-channel MOSFET. During normal operation, the minimum turn-on time is about 100ns. A stabilizing ramp is added to the current-sense amplifier's output to prevent subharmonic oscillations for duty cycles exceeding 50%. This result is fed into the PWM comparator. When the summed voltage reaches the output voltage (V_{OUT}) of the error amplifier (EA), the external N-MOSFET turns off.

The EA's V_{OUT} is an amplified signal of the difference between the reference voltage (V_{REF}) and the feedback voltage (V_{FB}). The converter automatically chooses the lowest active LEDx pin voltage (V_{LEDx}) as V_{FB} to provide a sufficient voltage to power all the LED arrays.

If V_{FB} drops below V_{REF}, the EA's output increases. Then more current flows through the N-channel MOSFET, which increases the power delivered to the output. This forms a closed loop that regulates V_{OUT}.

During light-load operation (e.g. when V_{OUT} is almost equal to V_{IN}), the converter operates in pulse-skip mode (PSM) with a fixed switching frequency (f_{SW}). In this mode, the MOSFET turns on for a minimum on time, then the converter discharges the power to the output for the remaining period. The external MOSFET remains off until V_{OUT} requires another boost.

Ability to Disable LED4 if LED4 Is Unused

If LED4 is unused, connect it directly to the OVP pin. Then IC can disable the internal functional block of LED4 and remove LED4 from the boost control loop. Then the PSE/FSE/FF pin can provide optimal performance for a 3-string application.

Dimming Control

The MPQ3359C provides analog and PWM dimming with two separate EN/ADIM and PDIM input pins.

Pulse-Width Modulation (PWM) Dimming Mode

When a PWM signal is applied to PDIM pin, the LED current (I_{LED}) amplitude remains at the full-scale I_{LED}, and the I_{LED} duty cycle is the same as the input PWM signal duty cycle. The I_{LED} duty cycle follows the PWM input duty cycle, and the I_{LED} frequency is the same as the PWM input.

Analog Dimming Mode

The PWM input signal is connected to EN/ADIM pin. The I_{LED} amplitude is equal to I_{SET} x D_{DIM}, where I_{SET} is the full-scale I_{LED}, and D_{DIM} is the duty cycle of the input PWM signal.

To improve analog dimming performance, a PWM signal >5kHz is recommended.

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To ensure good performance with a small dimming ratio, the minimum V_{LEDx} rises to 1.2V when the dimming duty cycle is below 10%. Analog dimming supports a 200:1 dimming ratio.

Deep Dimming Ratio for PWM Dimming

When the PWM pin on time is shorter than 5µs, V_{OUT} is regulated to be 93% of V_{OVP} (see Figure 4).

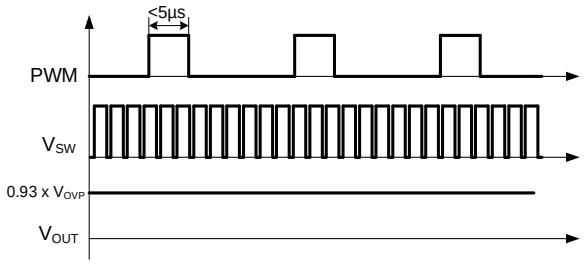

Figure 4: Deep Dimming Ratio for PWM Dimming

PSE/FSE/FF Pin

When V_{CC} exceeds its UVLO threshold, the PSE/FSE/FF pin sources a current (typically 32µA) to charge the resistor between the PSE/FSE/FF pin and AGND. The IC detects the voltage of this pin to enable certain functions (see Table 1).

Table 1: PSE/FSE/FF Pin Function

PSE/FSE/FF Pin Voltage	Frequency Spread Spectrum	Delay Function
<1.13V	Disabled	Disabled
1.27V to 1.8V	Enabled	Disabled
2V to 2.55V	Disabled	Enabled
>2.85V	Enabled	Enabled

The PSE/FSE/FF pin must have a suitable voltage to match the logic level of the microcontroller (MCU). After V_{CC} exceeds its UVLO threshold for a delay (typically 310µs), the IC raises the voltage on the PSE/FSE/FF pin to be between 4.35V and 5.22V when V_{IN} exceeds 6V (see Figure 5).

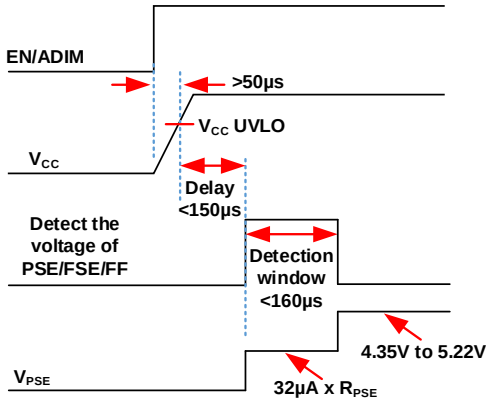

Figure 5: PSE/FSE/FF Pin Timing

Delay Time Function

To reduce inrush current and audible noise during PWM dimming, the MPQ3359C employs a delay time function. There is a 100µs delay time between the LED channels (See Figure 6).

When the delay time function is enabled, the recommended I_{LED} pulse on time is ≥10µs.

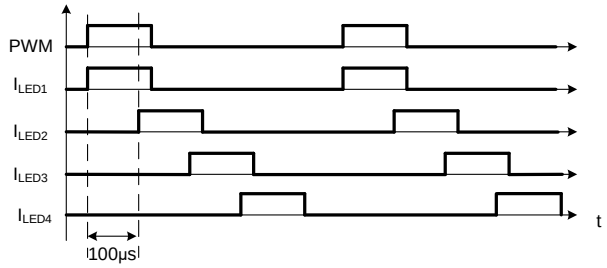

Figure 6: 100µs Delay Time with 4 Channels

Frequency Spread Spectrum (FSS)

The MPQ3359C uses f_{SW} jitter to spread the f_{SW} spectrum. This reduces the spectrum spike around f_{SW} and its harmonic frequencies.

The jitter frequency is ±10% of f_{SW}.

The modulation frequency is fixed at 6kHz.

Protections

The MPQ3359C provides LED open protection, LED short protection, input current (I_{IN}) over-current protection (OCP), VOUT short-to-GND protection, LEDx short-to-GND protection, and thermal protection. If any of the above protections are triggered (excluding thermal protection), PSE/FSE/FF is pulled to AGND. Once the IC recovers from the protection condition, PSE/FSE/FF is pulled high again.

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LED Open Protection

LED open protection is achieved by detecting V_{OVP} and V_{LEDx}. If one string is open during normal operation, the respective V_{LEDx} drops low to ground, and the IC keeps charging V_{OUT} until it reaches the OVP threshold.

If OVP is triggered, the IC stops switching and marks off the fault string that has a V_{LEDx} below 100mV. The remaining LED strings force V_{OUT} back into normal regulation. The string with the largest voltage drop determines the output regulation value.

Every 500µs, the LEDx pin that was marked off turns on for 4µs to check whether the open fault has been removed.

If all used strings are open, the IC latches off and cannot recover until V_{IN} is reset or EN/ADIM is pulled low for >60ms and the device is turned on again.

LED Short Protection

The MPQ3359C monitors V_{LEDx} to check whether a short string fault occurs. If one or more strings are shorted, the shorted LEDx pins tolerate the high voltage stress. If any V_{LEDx} exceeds the short protection threshold, an internal counter starts counting.

If the fault condition lasts for 7.7ms (D_{PWM} = 100%), the fault string is marked off. Once a string is marked off, it disconnects from the V_{OUT} loop until the short fault is removed.

Every 500µs, the LEDx pin that was marked off turns on for 4µs to check whether the short fault has been removed.

If all the active LEDx pins' voltage exceed the threshold for 480ms (D_{PWM} = 100%), all strings are marked off and IC latches off.

LED short protection is disabled when an open LED condition occurs, which helps avoid mis-triggering LED short protection.

LEDx Short-to-GND Protection

If an LEDx pin is shorted to PGND or AGND, the COMP voltage (V_{COMP}) increases and saturates. If V_{COMP} is saturated for 40ms, LEDx short-to-GND protection is triggered. PSE/FSE/FF is pulled low, and SD is pulled high to turn off the external P-channel MOSFET. Then the IC latches off.

VOUT Short-to-GND Protection

If VOUT is shorted to GND, V_{OUT} decreases. If V_{OVP} reaches its UVLO threshold and lasts for 10µs, VOUT short-to-GND protection is triggered. SD is pulled high to turn off the external P-channel MOSFET, then VOUT disconnects from VIN and the IC latches off.

Cycle-by-Cycle Current Limiting

To prevent internal or external components from exceeding the current stress rating, the IC has cycle-by-cycle current limit protection. If the current exceeds the current limit value, the IC stops switching until the next clock cycle.

Input Over-Current Protection (OCP)

To prevent I_{IN} from exceeding the current stress rating, the INS pin detects the voltage across the input sense resistor (R_S) (see Figure 7). If the voltage between the VIN and INS pins (V_{IN} - V_{INS}) reaches the protection threshold for 3µs, then the P-channel MOSFET turns off and the MPQ3359C latches off.

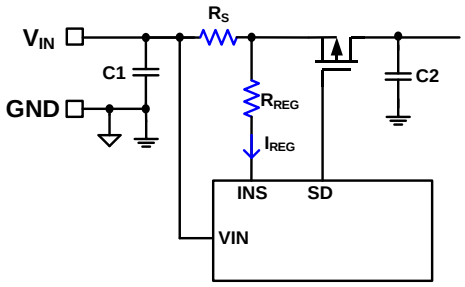

Figure 7: Typical I_{IN} Current Detection Circuit

For flexibility when selecting R_S, the INS pin has a 20µA sink current capability. It is possible to add a resistor (R_{REG}); then V_{IN} - V_{INS} is equal to the sum voltage of (R_S + R_{REG}).

Thermal Shutdown

If the die's junction temperature (T_J) exceeds the upper threshold (T_{ST}), the IC shuts down. Once the temperature drops below the lower threshold, the IC recovers. The hysteresis value is about 20°C.

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APPLICATION INFORMATION

LED Current Setting

The LED current (I_{LED}) amplitude is set by an external resistor connected from ISET to AGND. I_{LED} can be calculated with Equation (1):

$$I_{LED}\left(mA\right)=\frac{1200}{R_{ISET}\left(k\Omega\right)} \quad (1)$$

If R_{ISET} = 10kΩ, then I_{LED} is 120mA.

Setting the Switching Frequency

The switching frequency (f_{SW}) can be programmed with a resistor or external clock.

When using an external resistor on FREQ/SYNC to configure f_{SW}, f_{SW} can be estimated with Equation (2):

$$f_{SW}\left(kHz\right)=\frac{22000}{R_{FREQ}\left(k\Omega\right)} \quad (2)$$

If R_{FREQ} = 44.2kΩ, then f_{SW} is set to 500kHz.

There may be some deviation between the actual f_{SW} and the calculated value from Equation (2). R_{FREQ} = 50kΩ is recommended for a typical f_{SW} of 440kHz, and R_{FREQ} = 9.1kΩ is recommended for a typical f_{SW} of 2.2MHz.

Synchronize f_{SW} with an external clock to improve EMI, efficiency, and thermal performance.

A ≥250kHz external clock frequency is recommended for the external SYNC SW function.

If using the external clock on the FREQ/SYNC pin, do not stop the clock during operation, or the MPQ3359C may operate abnormally.

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at f_{SW} should be less than the input source impedance to prevent the high-frequency switching current from passing through to the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, a 10μF ceramic capacitor is sufficient.

Selecting the Inductor and Current-Sensing Resistor (R_{IS})

The MPQ3359C requires an inductor to supply a higher V_{OUT} while being driven by V_{IN}. A larger-value inductor results in less ripple current, lower peak inductor current, and less stress on the external N-channel MOSFET. However, it also has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under worst-case load conditions. Select the minimum inductance to ensure that the boost converter works in continuous conduction mode with high efficiency and good EMI performance. Calculate the required inductance with Equation (3):

$$L\geq\frac{\eta\times V_{OUT}\times D\times\left(1-D\right)^{2}}{2\times f_{SW}\times I_{LOAD}} \quad (3)$$

Where V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{LOAD} is the LED load current, and η is the efficiency, and D is the switching duty cycle.

D can be estimated with Equation (4):

$$D=1-\frac{V_{IN}}{V_{OUT}} \quad (4)$$

Where V_{IN} is the input voltage.

The switching current is used for peak current mode control. To avoid reaching the current limit, the voltage across the current-sense (CS) resistor (R_{IS}) must be less than 70% of the current limit voltage (V_{LIM_CYC}) in the worst-case scenario. Calculate R_{IS} and $I_{L(PEAK)}$ with Equation (5) and Equation (6), respectively:

$$R_{IS}=\frac{0.7\times V_{LIM_CYC}}{I_{L(PEAK)}} \quad (5)$$

$$I_{L(PEAK)}=\frac{V_{OUT}\times I_{LOAD}}{\eta\times V_{IN}}+\frac{V_{IN}\times\left(V_{OUT}-V_{IN}\right)}{2\times L\times f_{SW}\times V_{OUT}} \quad (6)$$

Selecting the Power MOSFET

The MPQ3359C is capable of driving a wide variety of N-channel power MOSFETS. The critical parameters of selection for a MOSFET

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are the maximum drain-to-source voltage ($V_{DS(MAX)}$), maximum current ($I_{D(MAX)}$), on resistance ($R_{DS(ON)}$), gate source charge (Q_{GS}) and gate drain charge (Q_{GD}), and total gate charge (Q_G).

Ideally, the off-state voltage across the MOSFET is equal to V_{OUT}. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times V_{OUT}.

The maximum current through the power MOSFET occurs at the minimum V_{IN} and the maximum output power. The maximum RMS current ($I_{RMS(MAX)}$) through the MOSFET can be calculated using Equation (7) and Equation (8):

$$I_{RMS(MAX)} = I_{IN(MAX)} \times \sqrt{D_{MAX}} \quad (7)$$

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}} \quad (8)$$

The MOSFET's current rating should be greater than 2 x $I_{RMS(MAX)}$.

The MOSFET's on resistance determines the conduction loss, which can be calculated using Equation (9):

$$P_{COND} = I_{RMS}{}^2 \times R_{DS(ON)} \times k \quad (9)$$

Where *k* is the MOSFET's temperature coefficient.

The switching loss is related to Q_{GD} and Q_{GS}, which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the V_{GS} vs. Q_G chart in the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage. These two parameters are required to estimate the turn-on and turn-off losses, and can be calculated with Equation (10):

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW} \quad (10)$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, V_{DS} is the drain-to-source voltage, and R_G is the gate resistance.

Calculating the switching loss is the most difficult part of loss estimation. The formula above provides a simplified equation. For more accurate estimates, the equation becomes much more complex.

The total gate charge (Q_G) is used to calculate the gate drive loss, and can be calculated with Equation (11):

$$P_{DR} = Q_G \times V_{DR} \times f_{SW} \quad (11)$$

Where V_{DR} is the drive voltage.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) keeps the V_{OUT} ripple (ΔV_{OUT}) small and ensures feedback loop stability. The C_{OUT} impedance must be low at f_{SW}. Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. For most applications, a 10μF ceramic capacitor is sufficient.

Setting the Over-Voltage Protection (OVP)

Open-string protection is achieved through the detecting V_{OVP}. In some cases, an LED string failure results in V_{FB} always being 0V. The MPQ3359C continues boosting V_{OUT} higher and higher. If V_{OUT} reaches the set OVP threshold, OVP is triggered.

To ensure that the chip functions properly, an appropriate OVP threshold is required. The recommended threshold is about 1.2 times maximum V_{OUT} for normal operation. The OVP threshold is set by a resistor divider from the VOUT to the OVP pin and the OVP pin to AGND. The OVP threshold can be calculated with Equation (12):

$$V_{OVP} = 2(V) \times (1 + \frac{R_{HIGH}}{R_{LOW}}) \quad (12)$$

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PCB Layout Guidelines

Efficient PCB layout is critical to reduce EMI noise and achieve stable operation. For the best results, refer to Figure 8 and follow the guidelines below:

1. The high-frequency switching current flows through the loop between the N-channel MOSFET (M2), output diode (D1), output capacitors (C4 and C5), PGND, and current-sense resistor (R_{IS}). Keep this loop as short as possible to reduce noise and EMI.
2. Internally connect the IC's exposed pad to the AGND pin, and refer all logic signals to AGND.
3. Externally connect PGND to AGND, routing PGND away from the logic signals.
4. Place the ceramic capacitors for the VIN pin and VCC pins as close to the IC as possible.

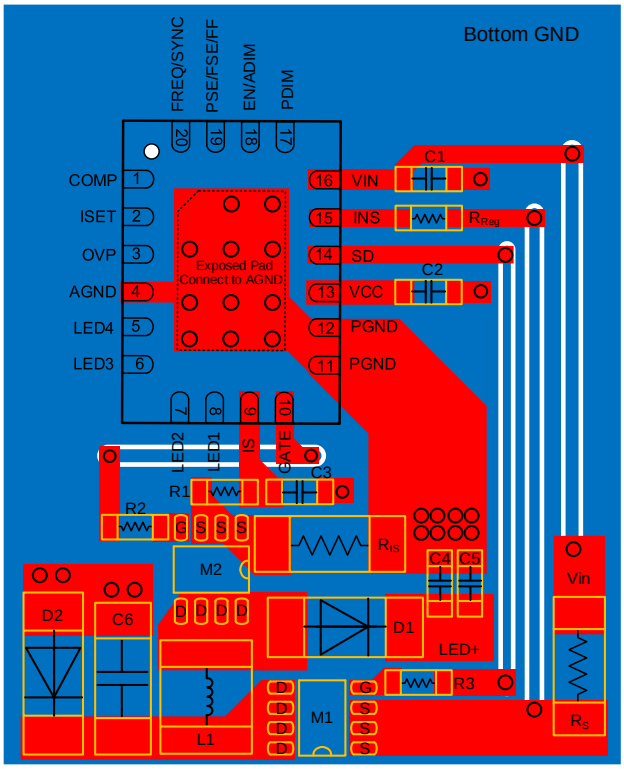

Figure 8: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

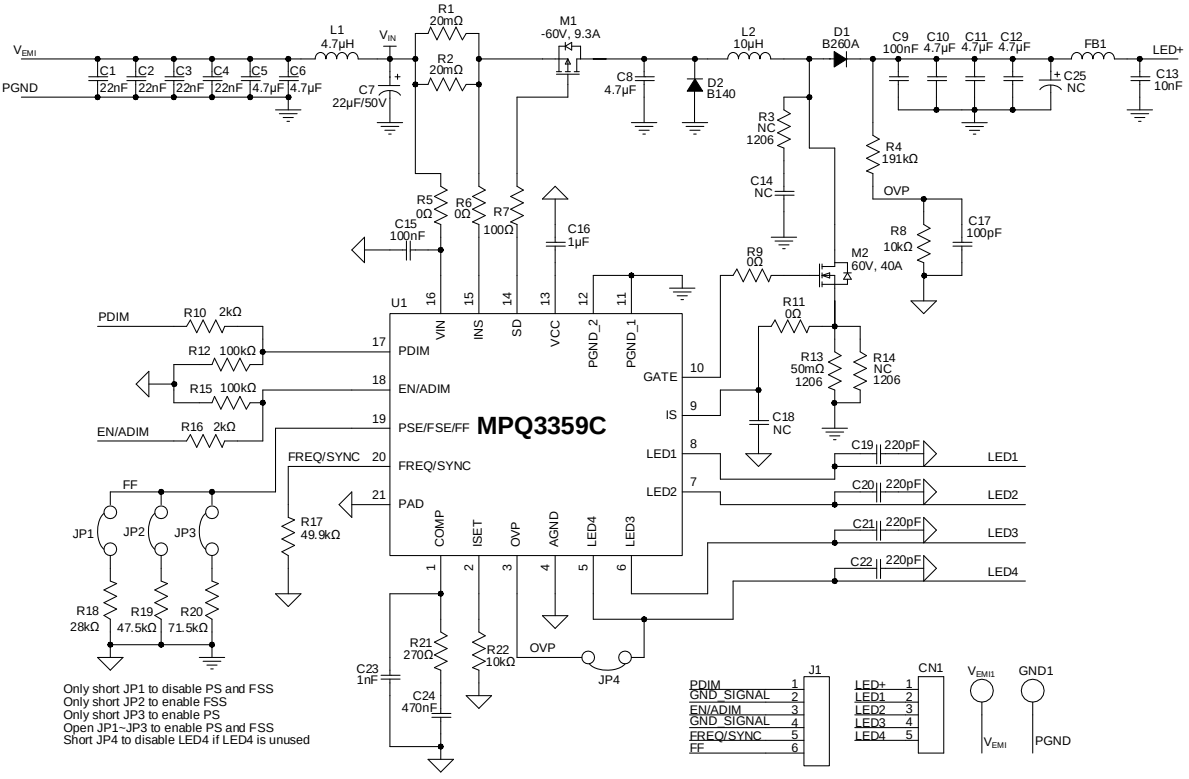

Figure 9: Typical Application Circuit (Boost)

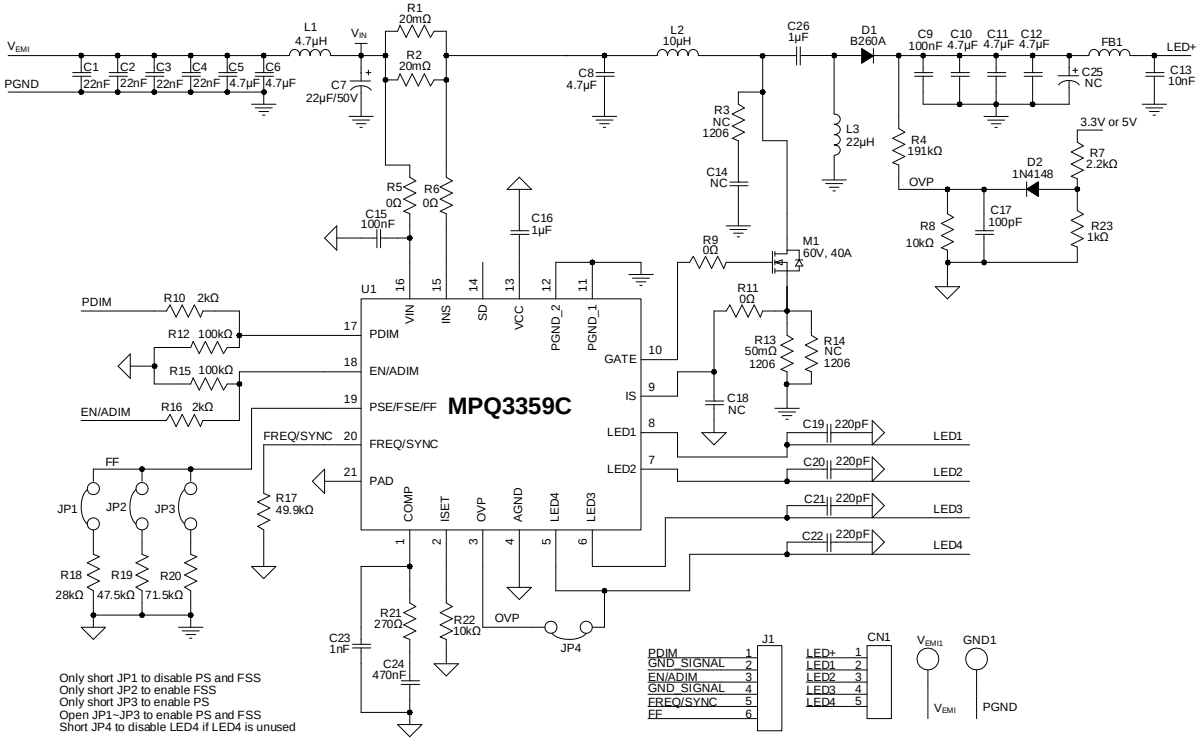

Figure 10: Typical Application Circuit (SEPIC)

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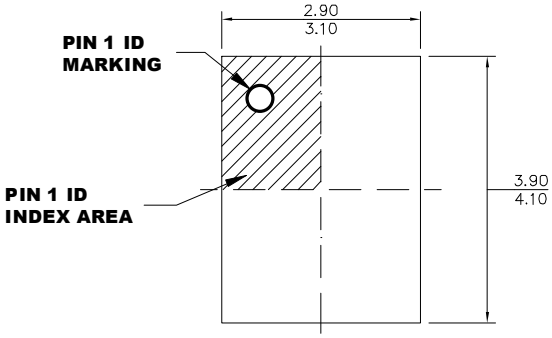
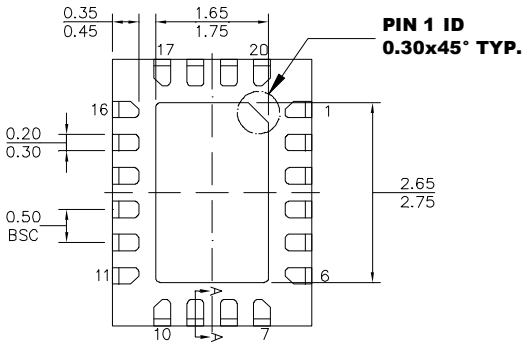
PACKAGE INFORMATION

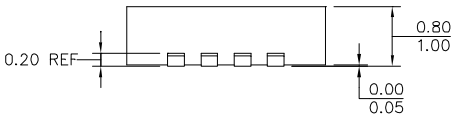
QFN-20 (3mmx4mm)
Wettable Flank



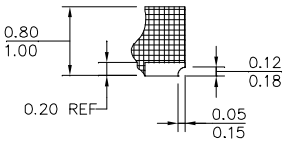
TOP VIEW



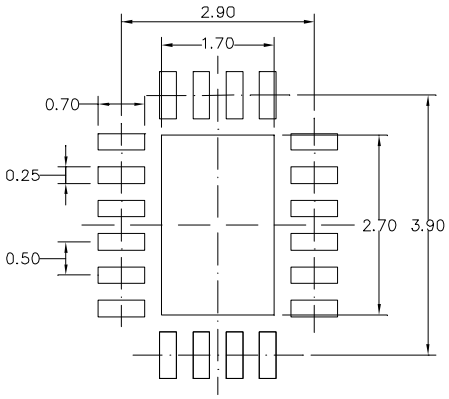
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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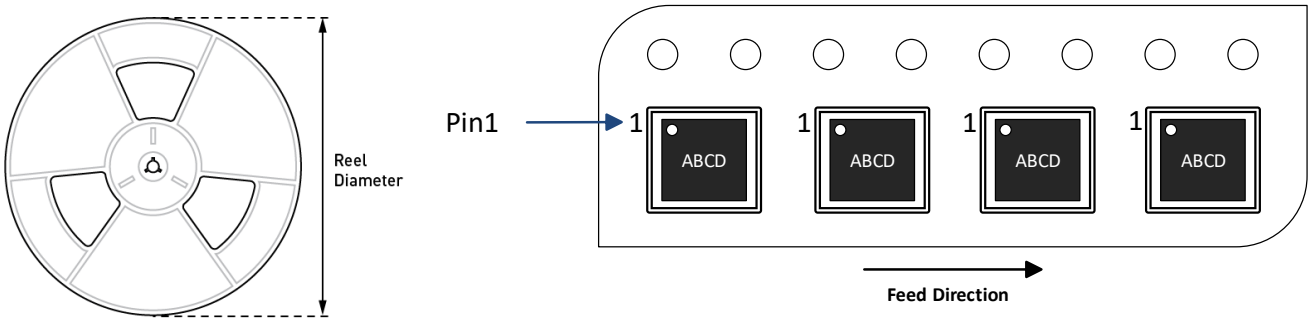
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3359CGLE-AEC1-Z	QFN-20 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/19/2025	Initial Release	-

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