MPQ3322

24-Channel, Max 100mA/Ch, Current Source LED Driver with Independent PWM and Analog Dimming, AEC-Q100 Qualified

DESCRIPTION

The MPQ3322 is a 24-channel LED driver with a 24V voltage rating and maximum 100mA current sources. It is designed to drive the LED arrays for backlighting, RGB lighting, and interior ambient lighting in automotive LCD panels and lamps.

The MPQ3322 employs low headroom to regulate the LED current (I_{LEDx}, where x = 1 to 24). The adaptive voltage feedback for the previous power stage optimizes the output voltage for the LED strings, which achieves higher system efficiency.

The MPQ3322 supports independent 12-bit pulse-width modulation (PWM) and 6-bit analog dimming for each channel via the CAN-based differential interface. The resistor on the ISET pin (R_{ISET}) configures the maximum I_{LEDx} amplitude.

Robust protections are included to guarantee safe operation of the device. Protection modes include LED open protection, LED short protection (with a configurable threshold via the STH bits (04h, bits[1:0]) and over-temperature protection. All fault statuses can be read through the CAN interface. In addition, the failsafe function ensures that the MPQ3322 remains operating in a pre-set state if communication information is lost.

The FF pin and single lamp mode (SLM) support single-IC and multi-IC applications for two fault statuses. If one channel fails, then the IC either only turns off the failed LED string or shuts down all channels.

The MPQ3322 is available in a QFN-40 (6mmx6mm) package with wettable flanks, and is available in AEC-Q100 Grade 0.

FEATURES

- 3.5V to 22V Input Voltage (V_{IN}) Range
- 24 Channels with Max 100mA per Channel
- <2.5% Current Matching
- Low-Dropout Voltage (500mV at 100mA)
- Independent 12-Bit Pulse-Width Modulation (PWM) Dimming
- Independent 6-Bit Analog Dimming
- Adaptive Voltage Feedback Function
- 2MHz CAN-Based Differential Interface
- Cascades Up to 16 ICs (Pin-Configurable Device Address)
- Improves EMI with LED Current (I_{LEDx}, where x = 1 to 24) with Slew Rate and Phase Shift
- LED Open/Short Protection
- Fault Indicator Signal Output
- Configurable FF Mode: Fault Flag Mode (FFM) and Single Lamp Mode (SLM)
- Failsafe for Loss of Communication
- Failsafe Mode Set Function
- One-Time Programmable (OTP) Memory
- Available in a QFN-40 (6mmx6mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 0

APPLICATIONS

- Automotive Interior Light
- Automotive RGB Light
- Automotive Ambient Light
- Automotive Reading Light
- Automotive Displays
- General Light

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TYPICAL APPLICATIONS

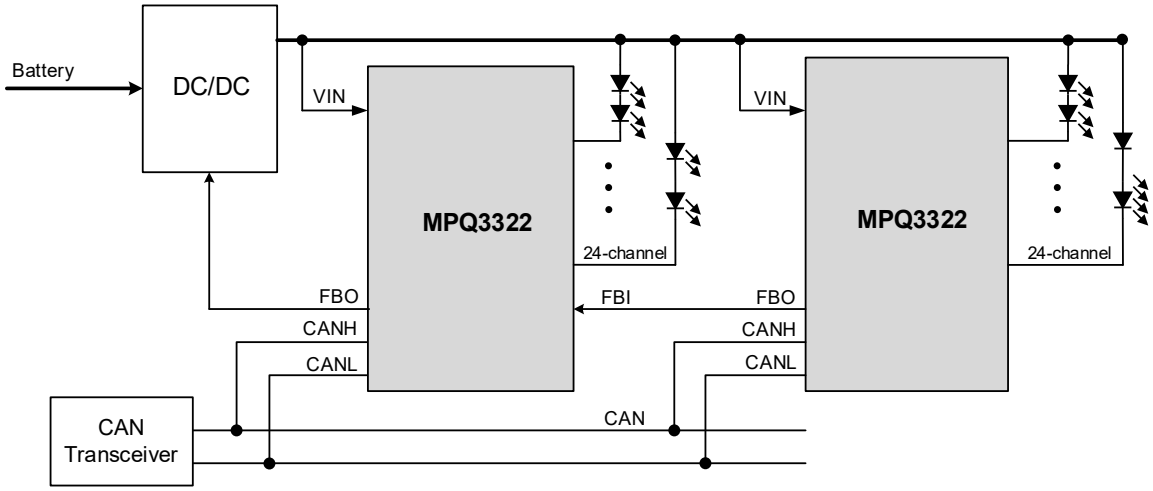

Figure 1: Typical Application (Multiple IC Application with CAN)

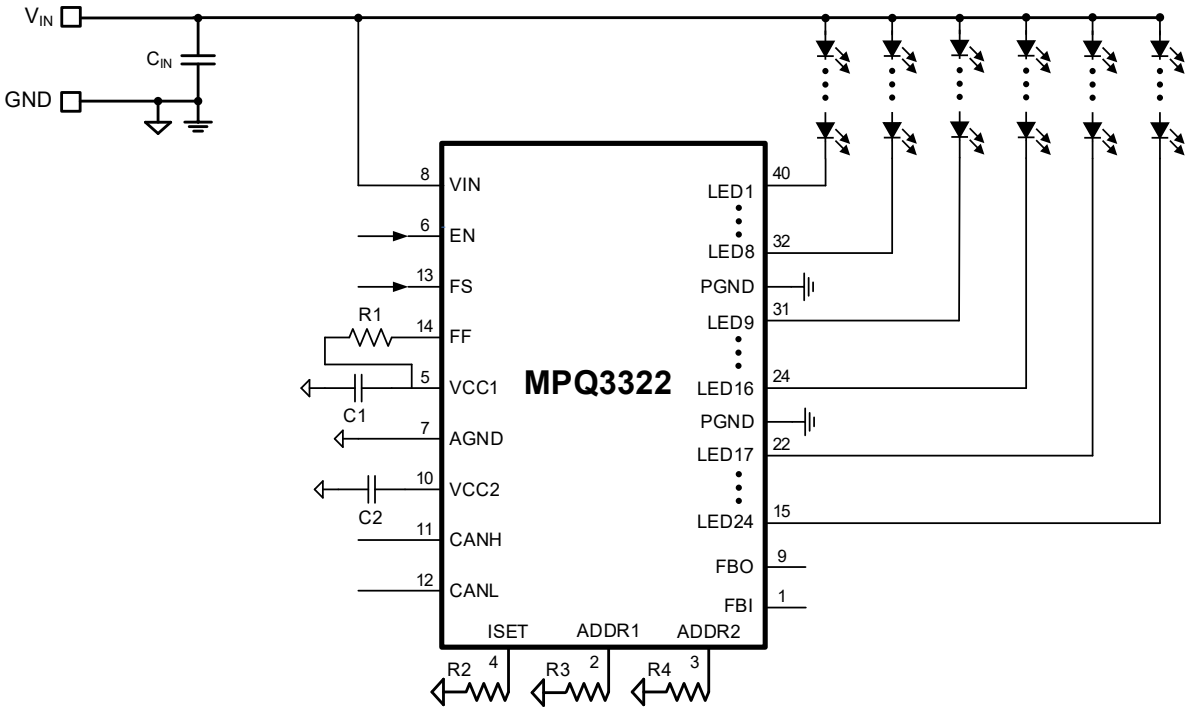

Figure 2: Typical Application Circuit with CAN

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3322GQKE-xxxx-AEC1**	QFN-40 (6mmx6mm) WF***	*See Below*	2
MPQ3322GQKE-0000-AEC1			

* For Tape & Reel, add suffix -Z (e.g. MPQ3322GQKE-xxxx-AEC1-Z).

** “xxxx” is the register setting option. The default code is “0000”. For custom options, contact an MPS FAE to obtain an “xxxx” value.

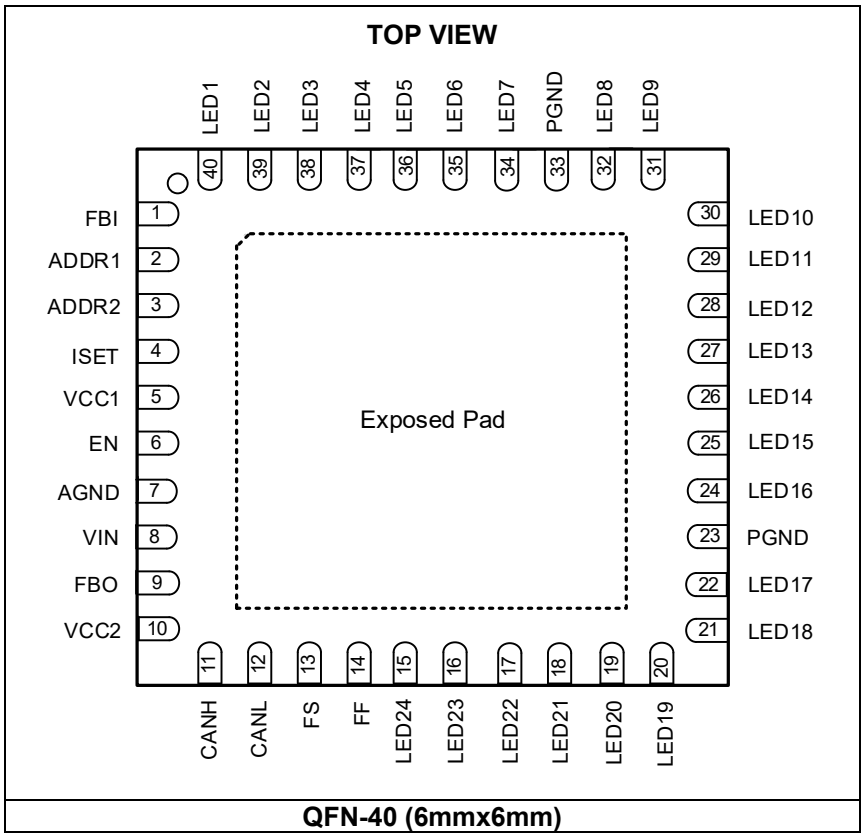
*** Wettable Flanks

TOP MARKING

MPSYYWW
MP3322
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP3322: Part number
LLLLLLLLL: Lot number
E: Wettable Flanks

PACKAGE REFERENCE



QFN-40 (6mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	FBI	**Feedback input.** FBI is the input pin for the LEDx pin's (where x = 1 to 24) voltage regulation information when multiple MPQ3322 devices are cascaded. Connect the FBI pin to VCC1 or disable the pin via the EN_FBI bit (0Ah, bit[5]) if it is not used.
2	ADDR1	**IC address setting 1.** The ADDR1 pin provides a current source output (30μA). Connect a resistor between ADDR1 and AGND to configure the ADDR1 pin voltage (V_{ADDR1}).
3	ADDR2	**IC address setting 2.** The ADDR2 pin provides a current source output (30μA). Connect a resistor between ADDR2 and AGND to configure the ADDR2 pin voltage (V_{ADDR1}).
4	ISET	**LED current setting.** Connect an LED current setting resistor between the ISET pin and AGND to configure the LED current (I_{LEDx}, where x = 1 to 24).
5	VCC1	**LDO1 output.** The VCC1 pin provides power for the internal logic and gate driver. Place a ceramic capacitor as close to this pin as possible.
6	EN	**IC enable.** Pull the EN pin high to enable the IC; pull EN low to disable the IC.
7	AGND	**Analog ground.**
8	VIN	**Input voltage.** Connect an input capacitor (C_{IN}) to the VIN pin.
9	FBO	**Feedback output.** The FBO pin has two functions, depending on whether the IC is set as the primary or secondary device: • If the IC is set as the primary device, then the FBO pin regulates the DC/DC converter via a resistor divider network. • If the IC is set as the secondary device, then the FBO pin outputs the LEDx pin's voltage regulation information when multiple MPQ3322 devices are used.
10	VCC2	**LDO2 output.** The VCC2 pin provides power for the internal CAN differential interface.
11	CANH	**Positive differential interface.**
12	CANL	**Negative differential interface.**
13	FS	**Failsafe input.** An external failsafe signal is provided to the FS pin to enter the pre-set mode.
14	FF	**Fault flag.** The FF pin is an active low, open-drain output. FF pulls low if any faults occur.
15–22	LED24–17	**LED strings 24–17 current input.** Connect the cathodes of LED channels 17–24 to these pins. Connect the LEDx pin to AGND if it is not used, or disable LEDx via the EN3 (00h) command.
23, 33	PGND	**Power ground.**
24–32	LED16~8	**LED strings 16–8 current input.** Connect the cathodes of LED channels 8–16 to these pins. Connect the LEDx pin to AGND if it is not used, or disable LEDx via the EN2 (01h) command and the EN8 bit (02h, bit[7]).
34–40	LED7~1	**LED strings 7–1 current input.** Connect the cathodes of LED channels 1–7 to these pins. Connect the LEDx pin to AGND if it is not used, or disable LEDx via bits[6:0] of the EN1 (02h) command.
-	Exposed pad	**Exposed thermal pad.** The exposed pad has no internal electrical connection to AGND. Connect the exposed pad to the external AGND plane on the board for optimal thermal performance.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{FBO}, V_{FF},$V_{LED1–24}$ .....-0.3V to +24V
V_{CANH}, V_{CANL} .....-0.3V to +24V
V_{CC1}.....-0.3V to +4.8V
All other pins .....-0.3V to +5V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-40 (6mmx6mm)..... 4.14W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±1.5kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3.5V to 22V
V_{CANH}, V_{CANL} .....-0.3V to +4.5V
All other logic input pins.....-0.3V to +5V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-40 (6mmx6mm) ……30.2…...2.7..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage range	V_{IN}		3.5		22	V
Quiescent supply current	I_Q	V_{IN} = 12V, V_{EN} = 2V, no I_{LEDx} (where x = 1 to 24)			8	mA
Shutdown supply current	I_{ST}	V_{EN} = 0V, V_{IN} = 12V			2	µA
LDO output voltage	V_{CC1}	4.5V < V_{IN} < 22V, 0 < I_{VCC1} < 20mA	3.1	3.3	3.5	V
	V_{CC2}	6V < V_{IN} < 22V, 0 < I_{VCC2} < 50mA	4.3	4.5	4.7	V
V_{IN} under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Rising edge	3	3.2	3.4	V
		Falling edge	2.7	2.9	3.1	V
Enable (EN)						
EN rising threshold	V_{EN_ON}	EN rising	1.5			V
EN falling threshold	V_{EN_OFF}	EN falling			0.4	V
EN pull-down resistor	R_{EN}			0.5		MΩ
LED Regulator						
ISET pin voltage	V_{ISET}		0.95	1	1.05	V
LED current (where x = 1 to 24)	I_{LEDx}	R_{ISET} = 20kΩ, V_{LEDx} = 300mV, ILEDx (where x = 1 to 24) (0Eh to 25h, bits[5:0]) = 0x10	-5%	25	+5%	mA
		R_{ISET} = 20kΩ, V_{LEDx} = 500mV, T_J = 25°C	-2%	100	+2%	mA
		R_{ISET} = 20kΩ, V_{LED} = 500mV, T_J = -40°C to +150°C	-4%	100	+4%	mA
LED current matching		I_{LEDx} = 100mA	-2.5		+2.5	%
LEDx pin voltage (V_{LEDx}) rising threshold	V_{LEDx_RISING}			500		mV
V_{LEDx} falling threshold	$V_{LEDx_FALLING}$			700		mV
Dimming						
Pulse-width modulation (PWM) frequency	f_{PWM}	FPWM (03h, bits[7:4]) = 0000b	170	200	230	Hz
PWM duty step	t_{PWM}	12-bit resolution, FPWM = 0001b (250Hz)		0.97		µs
Phase shift	t_{DELAY}	PSEN (03h, bit[1]) = 1, 24 channels, FPWM = 0000b		208		µs
LED current step		I_{LEDx} = 25mA, analog dimming step, 6 bits		0.4		mA
LED current slew rate during PWM dimming		SLEW (03h, bits[3:2]) = 01, rising edge		4		µs
		SLEW = 11, rising edge		16		µs
FBO Output						
FBO minimum voltage	V_{L_FBO}	FBOS (09h, bits[7:0]) = 00h		0.5		V
FBO typical voltage	V_{T_FBO}	FBOS = B2h		1.198		V
FBO maximum voltage	V_{H_FBO}	FBOS = FFh		1.5		V
Protection						
Short LED string protection threshold	V_{SLP}	STH (04h, bits[1:0]) = 01	3.2	4	4.8	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Short LED string protection time	t_{SLP}	V_{LEDx} > STH		2		ms
Open LED string protection threshold	T_{LED_UV}			100	130	mV
Open LED string protection time	t_{LEDO}	V_{LEDx} < 100mV, manual mode		2		ms
Thermal warning threshold (6)	T_{WARN}	TH_OTW (06h, bit[7]) = 0		140		°C
Thermal shutdown threshold (6)	T_{ST}			170		°C
Thermal shutdown hysteresis (6)	T_{ST_HYS}			20		°C
CANH and CANL Receiver						
Absolute rating	V_{CANH}, V_{CANL}		-0.3		+24	V
Baud rate	f_{BR}		0.01		2	MHz
Receiver recessive voltage	V_{RRV}				0.5	V
Receiver dominant voltage	V_{RDV}		1.35			V
Input resistance	R_{IN}		6		65	kΩ
Differential input resistance	R_{DIN}		12		100	kΩ
Input capacitance on the CANH and CANL pins (6)	C_{IN_P}			20		pF
Low-to-high level propagation delay time (6)	$t_{P_L2H_R}$	L_R = 60Ω, L_C = 50pF, VCC2 = 4.5V, see Figure 5 on page 8	3	13	30	ns
High-to-low level propagation delay time (6)	$t_{P_H2L_R}$	L_R = 60Ω, L_C = 50pF, VCC2 = 4.5V, see Figure 5	5	18	35	ns
CANH and CANL Driver						
CANH and CANL recessive output	V_{OR}	L_R = 60Ω	1.75	2.25	2.75	V
CANH dominant output	V_{OD+}	L_R = 60Ω	2.4	3.25	4.1	V
CANL dominant output	V_{OD-}	L_R = 60Ω	0.35	1.2	2.05	V
Differential output voltage (dominant)	V_{OUT_DIF}	L_R = 60Ω	1.5	2	3	V
Output symmetry (dominant or recessive)	V_{SYM}	VCC2 = 4.5V, V_{CANH} + V_{CANL}	4.05	4.5	4.95	V
Output current			50			mA
Differential output rising time (6)	t_R	L_R = 60Ω, L_C = 50pF, VCC2 = 4.5V, see Figure 6 on page 8	2	5	15	ns
Differential output falling time (6)	t_F	L_R = 60Ω, L_C = 50pF, VCC2 = 4.5V, see Figure 6	20	25	35	ns
Low-to-high level propagation delay time (6)	$t_{P_L2H_D}$	L_R = 60Ω, L_C = 50pF, VCC2 = 4.5V, see Figure 6	2	7	15	ns
High-to-low level propagation delay time (6)	$t_{P_L2H_D}$	L_R = 60Ω, L_C = 50pF, VCC2 = 4.5V, see Figure 6	10	22	40	ns

Notes:

5) Matching is defined as the difference between the maximum current and the minimum current, divided by 2 times the average current.
6) Not tested in production. Guaranteed by characterization.

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TIMING DIAGRAMS

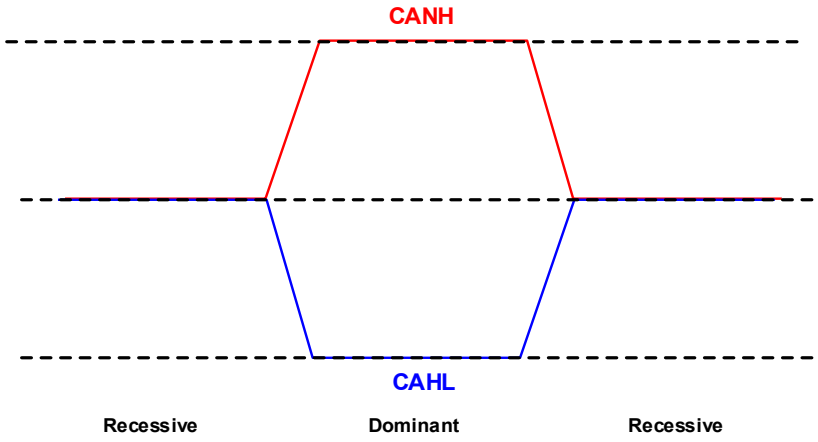

Figure 4: Differential Interface Timing Diagram

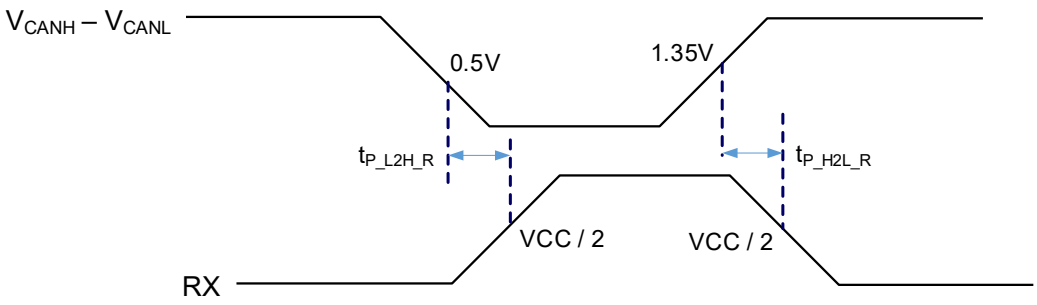

Figure 5: Receiver Interface Timing Diagram

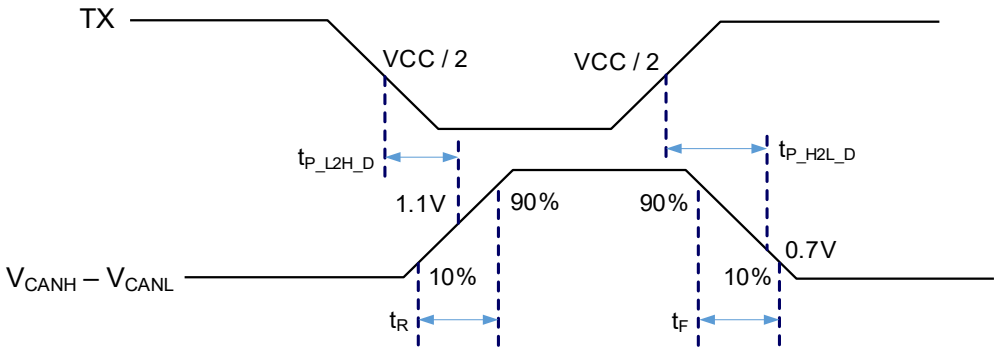

Figure 6: Driver Interface Timing Diagram

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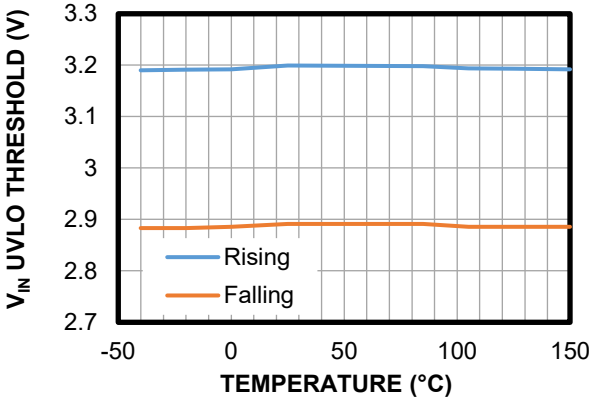
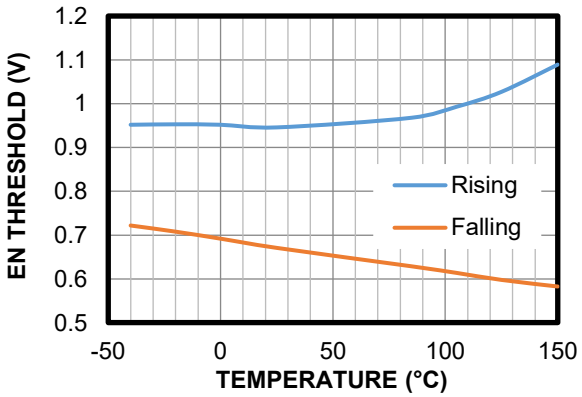
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, unless otherwise noted.

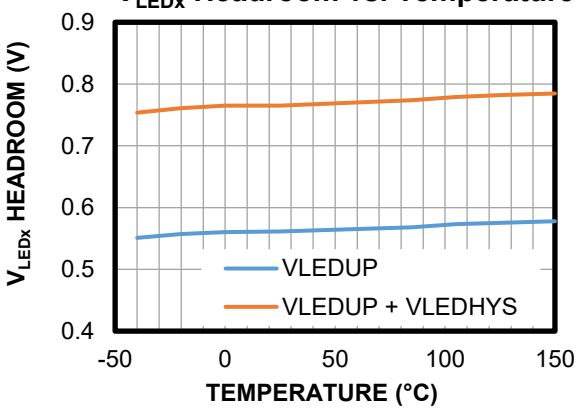
V_{IN} UVLO Threshold vs. Temperature



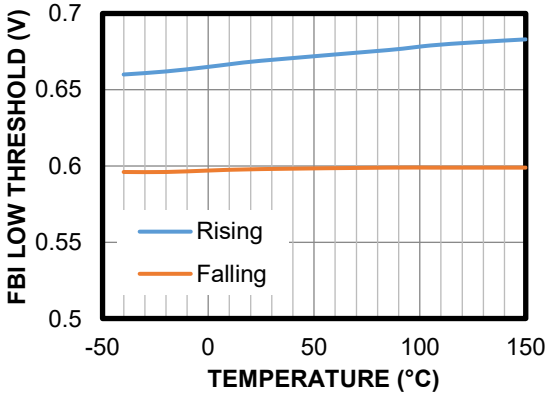
EN Threshold vs. Temperature



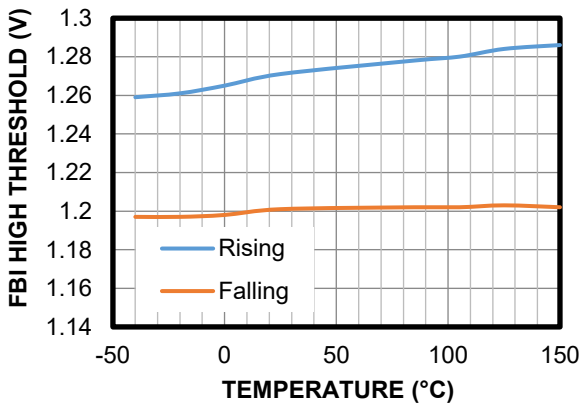
V_{LEDx} Headroom vs. Temperature



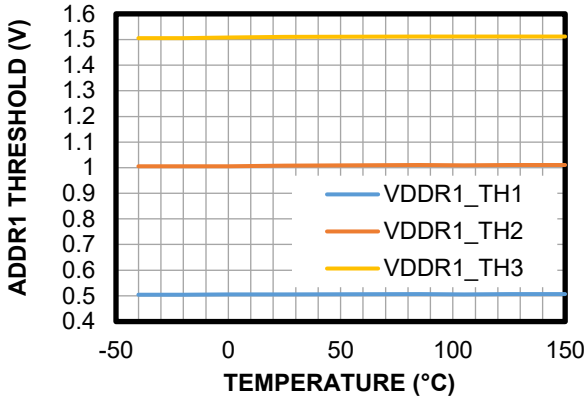
FBI Low Threshold vs. Temperature



FBI High Threshold vs. Temperature



ADDR1 Threshold vs. Temperature



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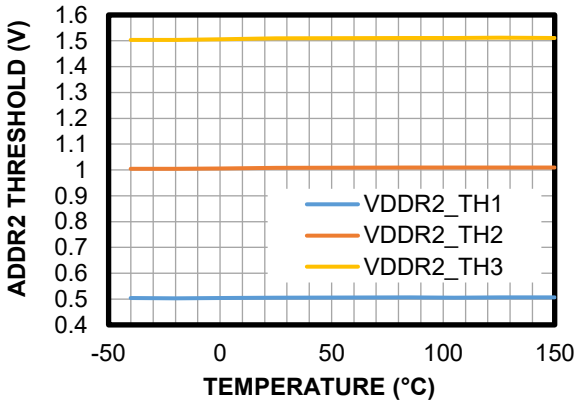
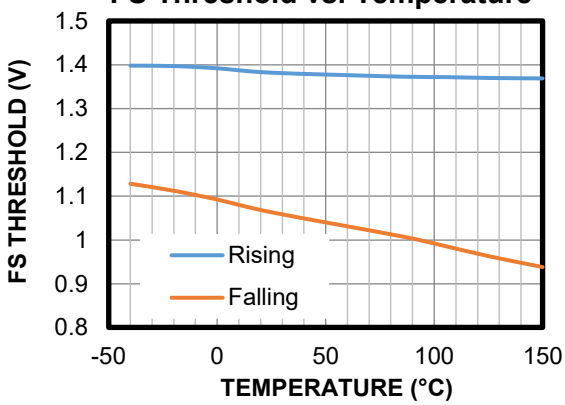
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, unless otherwise noted.

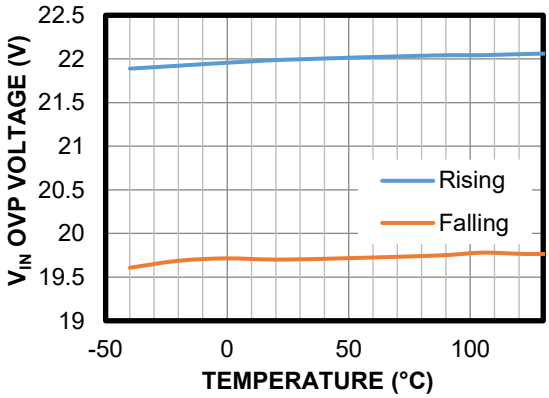
ADDR2 Threshold vs. Temperature



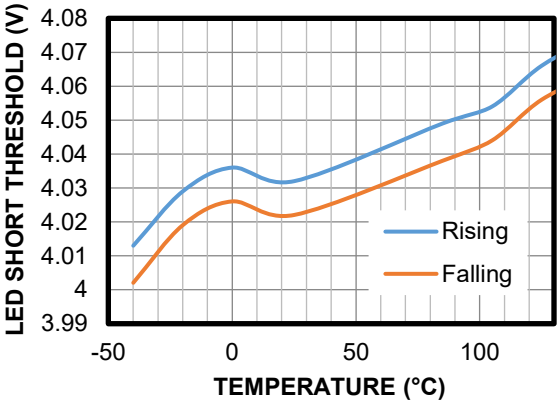
FS Threshold vs. Temperature



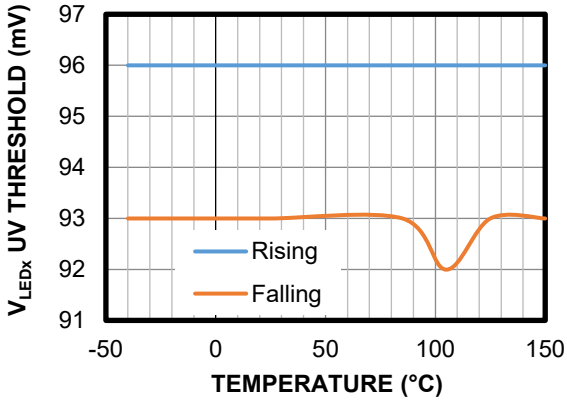
V_{IN} OVP Voltage vs. Temperature



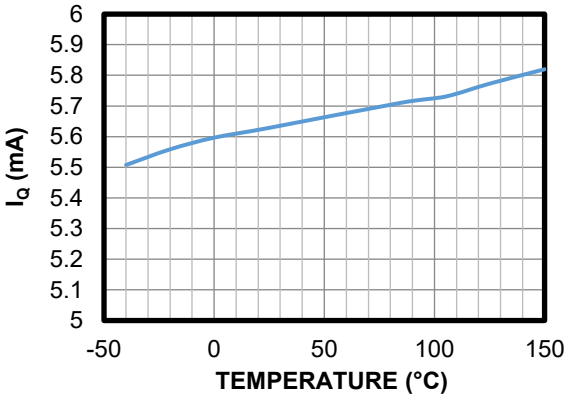
LED Short Threshold vs. Temperature



V_{LEDx} UV Threshold vs. Temperature



Quiescent Supply Current vs. Temperature



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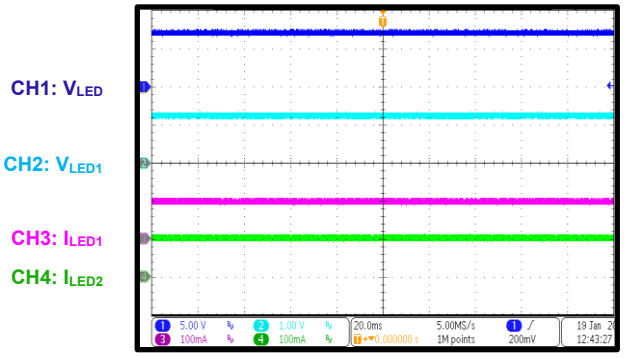
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN_IC} = 12V, 2 LEDs in series (V_{LED} = 6.7V), 100mA/string, f_{PWM} = 200Hz, adaptive mode, T_A = 25°C, unless otherwise noted.

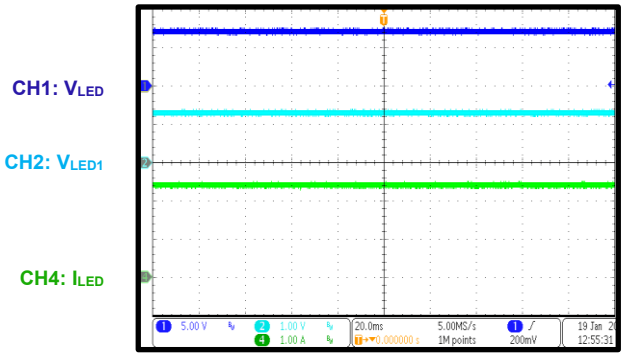
Steady State

CH1 duty = 100%, CH2 duty = 100%



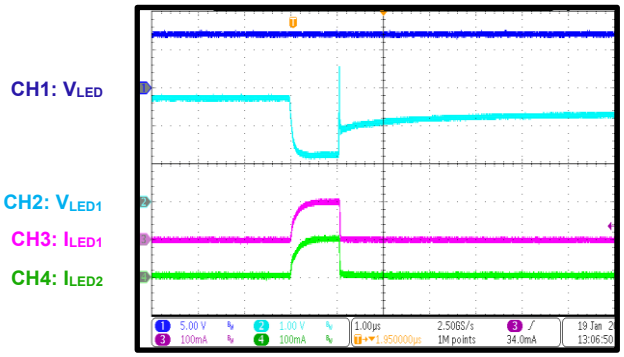
Steady State

All channels' duty = 100%



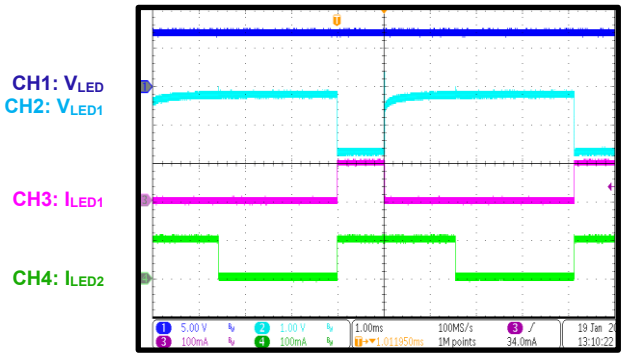
PWM Dimming

CH1 duty = 0.024%, CH2 duty = 0.024%



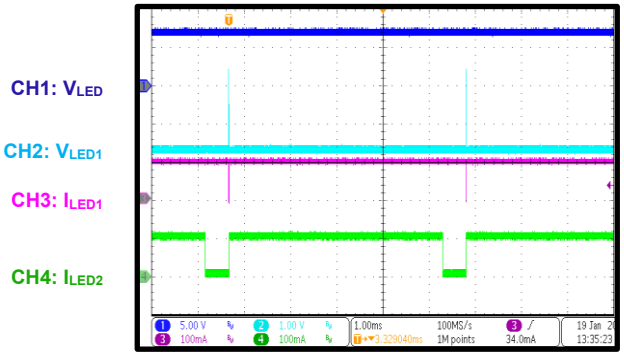
PWM Dimming

CH1 duty = 20%, CH2 duty = 50%



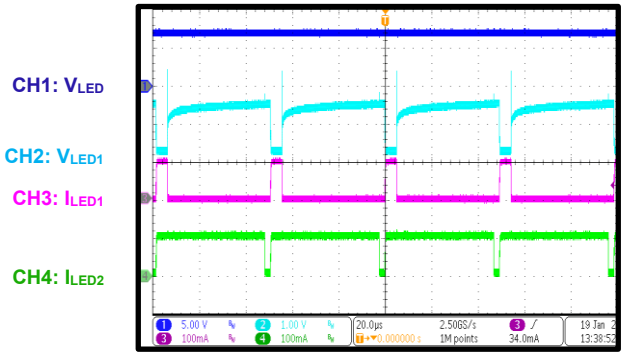
PWM Dimming

CH1 duty = 99.878%, CH2 duty = 89.988%



PWM Dimming

f_{PWM} = 20.8kHz, CH1 duty = 10%, CH2 duty = 95%



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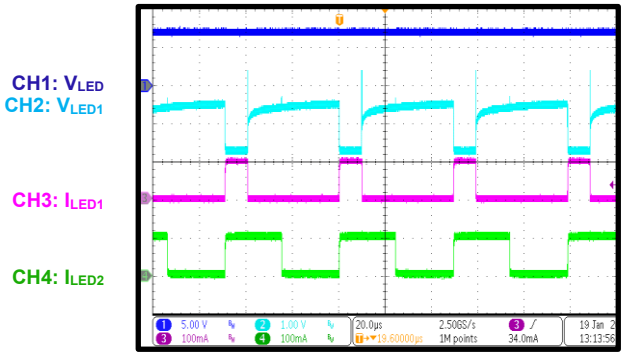
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_IC} = 12V, 2 LEDs in series (V_{LED} = 6.7V), 100mA/string, f_{PWM} = 200Hz, adaptive mode, T_A = 25°C, unless otherwise noted.

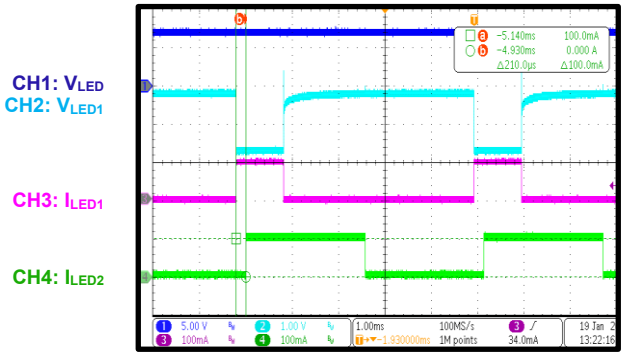
PWM Dimming

f_{PWM} = 20.8kHz, CH1 duty = 20%,
CH2 duty = 50%



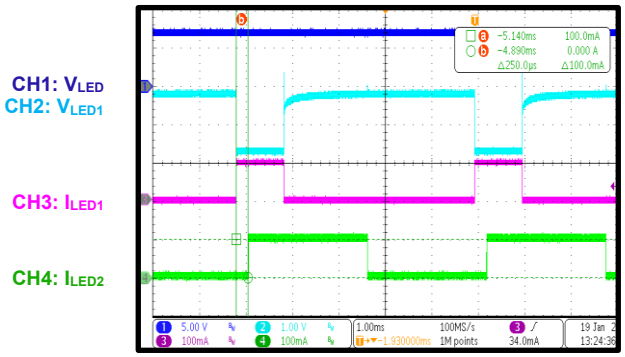
PWM Dimming

Phase shift enabled, CH1 duty = 20%,
CH2 duty = 50%



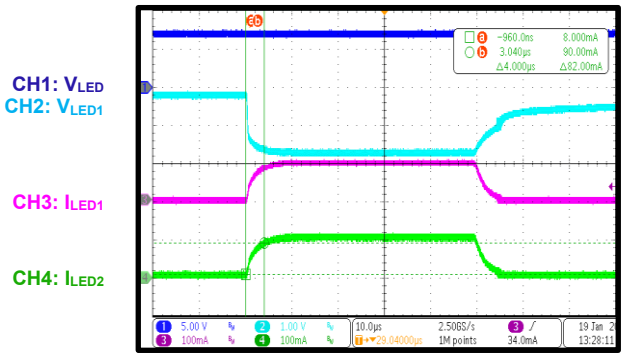
PWM Dimming

Phase shift enabled, CH21–24 disabled,
CH1 duty = 20%, CH2 duty = 50%



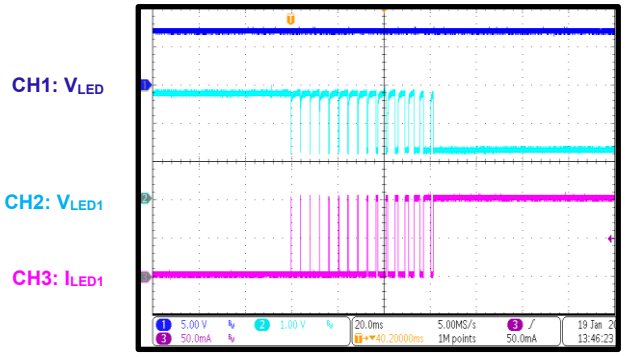
PWM Dimming

Slew rate enabled = 4µs,
CH1 duty = 0.977%, CH2 duty = 0.977%



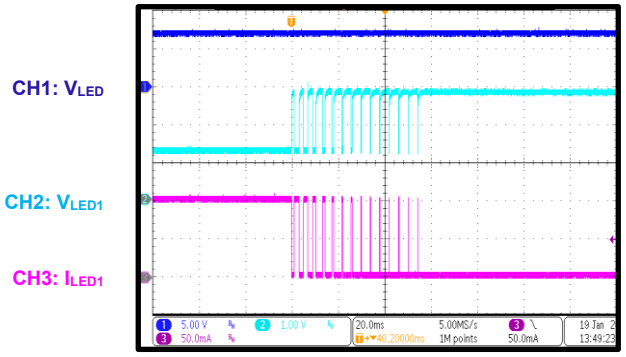
Automatic PWM Dimming

f_{PWM} = 250Hz, 4 points/cycle,
CH1 duty = 0% to 100%



Automatic PWM Dimming

f_{PWM} = 250Hz, 4 points/cycle,
CH1 duty = 100% to 0%



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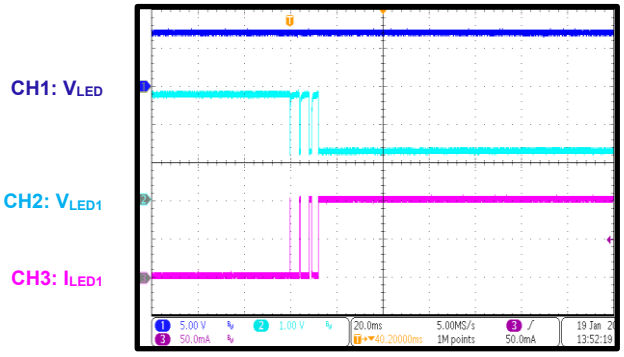
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_IC} = 12V, 2 LEDs in series (V_{LED} = 6.7V), 100mA/String, F_{PWM}=200Hz, Adaptive Mode, T_A = 25°C, unless otherwise noted.

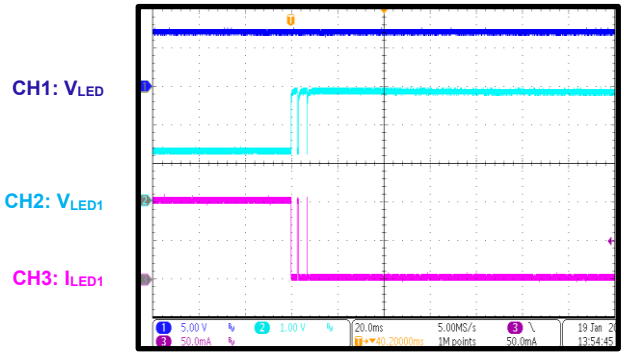
Automatic PWM Dimming

f_{PWM} = 250Hz, 16 points/cycle,
CH1 duty = 0% to 100%



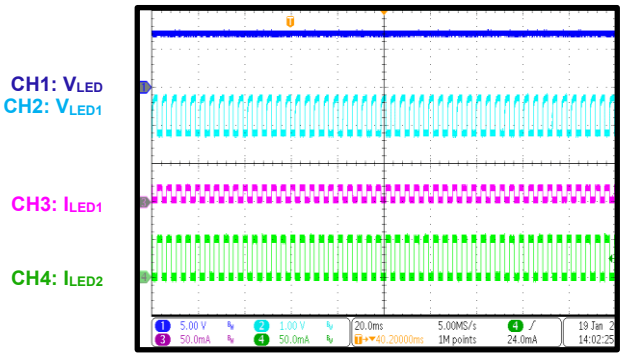
Automatic PWM Dimming

f_{PWM} = 250Hz, 16 points/cycle,
CH1 duty = 100% to 0%



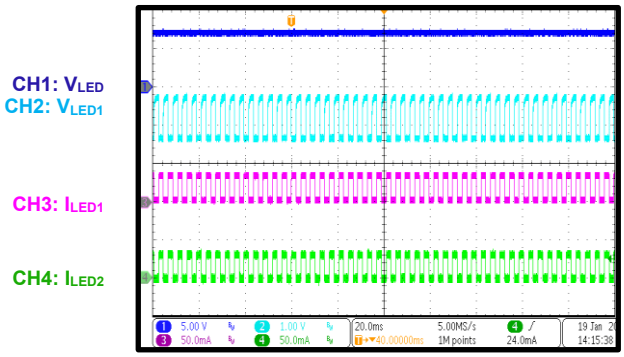
Analog Dimming

CH1 duty = 50%, CH2 duty = 50%,
I_{SET1} = 15.8mA, I_{SET2} = 50mA

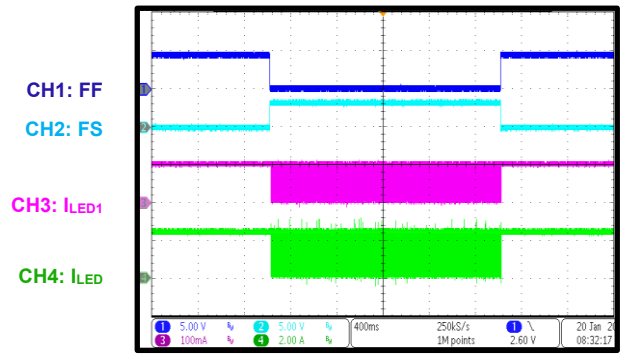


Analog Dimming

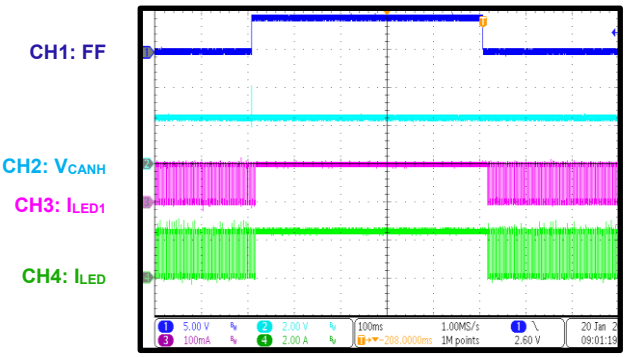
CH1 duty = 50%, CH2 duty = 50%,
I_{SET1} = 31.74mA, I_{SET2} = 31.74mA



FS Mode Entry/Recovery with FS Input



Failsafe Entry/Recovery with CAN Difference



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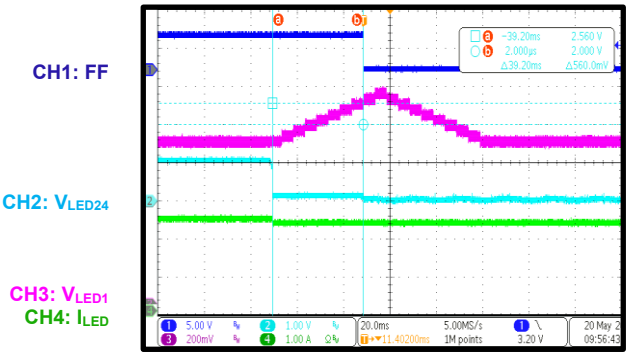
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_IC} = 12V, 2 LEDs in series (V_{LED} = 6.7V), 100mA/string, f_{PWM} = 200Hz, adaptive mode, T_A = 25°C, unless otherwise noted.

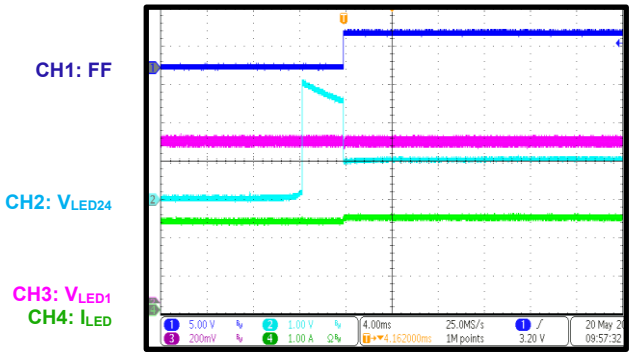
Open Protection

Open channel 24 in normal operation, hiccup mode, T_OPS (05h, bits[5:3]) = 3'b011



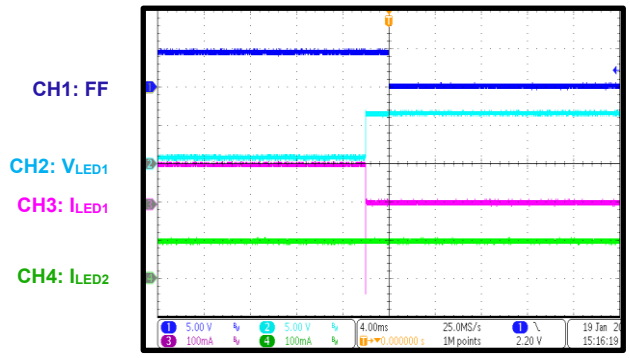
Open Protection

Recover channel 24, hiccup mode



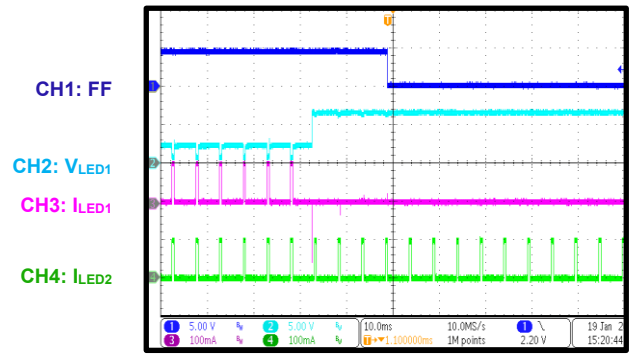
Short Protection

Short channel 1 in normal operation, latch mode

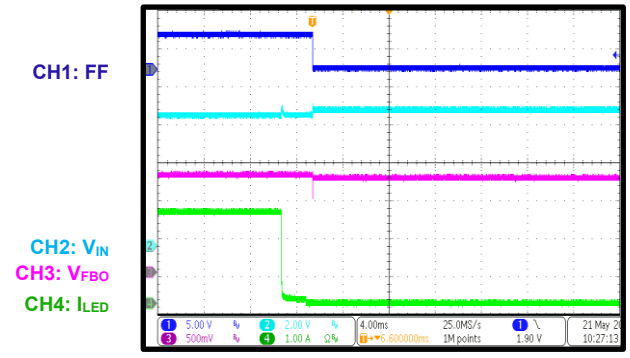


Short Protection

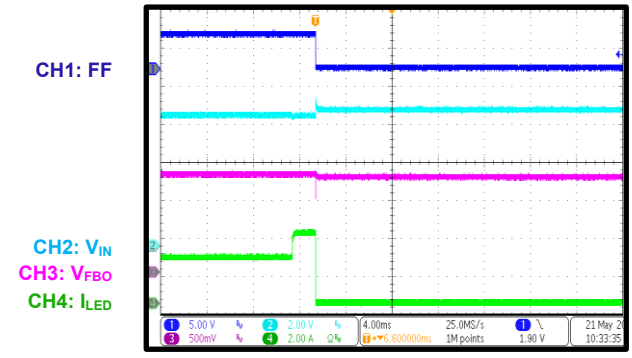
Short channel 1 in normal operation, latch mode



ISET Pin Open Protection



ISET Pin Short Protection



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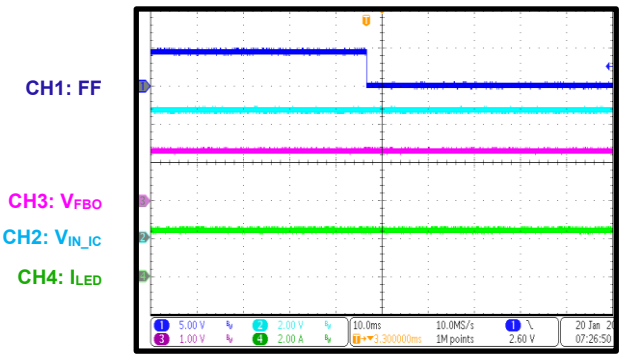
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN_IC} = 12V, 2 LEDs in series (V_{LED} = 6.7V), 100mA/string, f_{PWM} = 200Hz, adaptive mode, T_A = 25°C, unless otherwise noted.

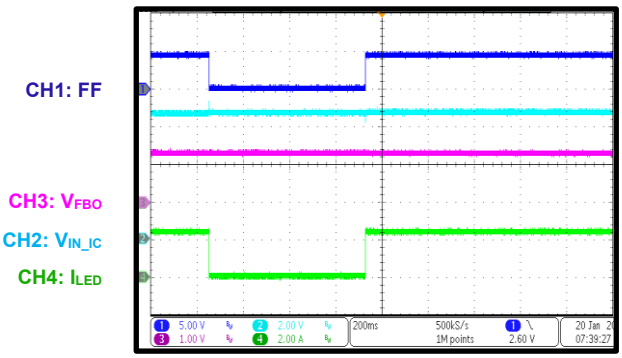
VIN Low Voltage Detection

Adjust V_{IN_IC} from 9.5V to 9V with 0.1V step



Over-Temperature Protection

Heat the IC then recover



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FUNCTIONAL BLOCK DIAGRAM

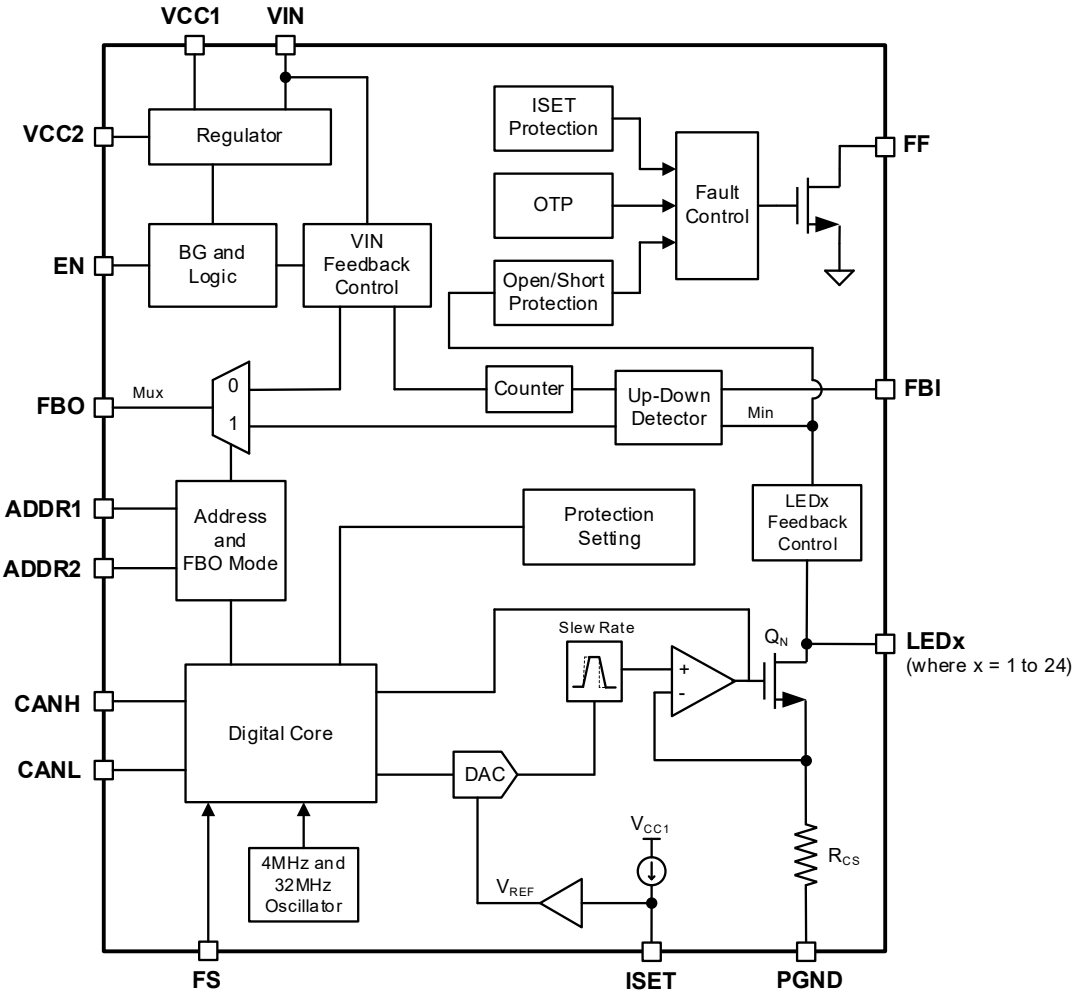

Figure 7: Functional Block Diagram

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OPERATION

The MPQ3322 is a 24-channel LED driver with a 24V voltage rating and maximum 100mA internal current source. It is designed to drive the LED arrays for backlighting, RGB lighting, and interior ambient lighting in automotive LCD panels and lamps.

Internal VCC1 and VCC2 Regulators

The MPQ3322 includes two internal linear regulators: VCC1 (typically 3.3V) and VCC2 (typically 4.5V). If the input voltage (V_{IN}) exceeds 4.5V, then the VCC1 regulator outputs a 3.3V power supply to the internal MOSFET and internal control circuity. The VCC1 voltage (V_{CC1}) drops to 0V when the chip shuts down. The chip remains disabled until V_{CC1} exceeds its under-voltage lockout (UVLO) threshold. If V_{IN} exceeds 6V, then the VCC2 regulator outputs a 4.5V power supply to the CAN differential circuit and external CAN transceiver.

Start-Up

Once the EN pin voltage (V_{EN}) exceeds its rising threshold (V_{EN_ON}) and V_{CC1} exceeds its UVLO threshold, the system initiates and enables the CAN differential interface.

Figure 8 shows the recommended start-up sequence if a buck converter is used as the MPQ3322's pre-power stage, and the FBO pin regulates the buck converter.

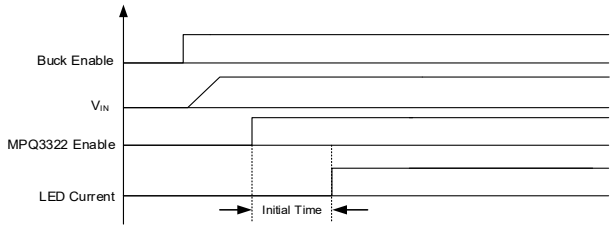

Figure 8: Start-Up Sequence

The initial time is set via the T_INI bits (05h, bits[2:0]).

Channel Selection

The LED channel can be disabled by setting the corresponding ENx command (where x = 1 to 3) (00h to 03h) to 0.

Adaptive Feedback Control (AFC) for the Pre-Power Stage

The MPQ3322 features adaptive feedback control (AFC) for the pre-power stage (see Figure 9).

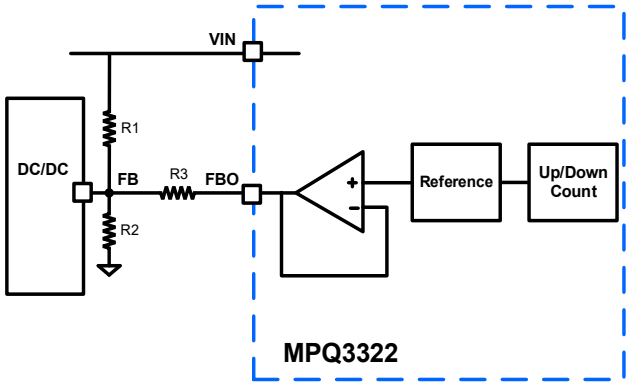

Figure 9: DC/DC Regulation Block

When the DC/DC converter's power supply starts operation, the initial V_{IN} can be set via the resistor dividers (R1 and R2), and can be calculated with Equation (1):

$$V_{IN} = V_{FB} \times (1 + \frac{R1}{R2}) \quad (1)$$

After the MPQ3322 is enabled, the FBO voltage (V_{FBO}) is regulated to a value set via the FBOS bits (09h, bits[7:0]). V_{IN} can be estimated with Equation (2):

$$V_{IN} = V_{FB} \times (1 + \frac{R1}{R2}) + \frac{R1}{R3} \times (V_{FB} - V_{FBO}) \quad (2)$$

Where V_{FBO} ranges between 0.5V and 1.5V with an 8-bit resolution (about 3.922mV/step).

After the current source begins operation, V_{IN} is regulated to a secondary voltage according to the minimum active LEDx pin voltage (V_{LEDx_MIN}) (where x = 1 to 24) via the FBO pin. This optimizes system efficiency and improves the IC's thermal performance.

V_{LEDx_MIN} is monitored periodically. If V_{LEDx_MIN} is below 0.5V, set via the VLEDUP bits (07h, bits[3:2]), then V_{IN} increases. If V_{LEDx_MIN} exceeds the sum of the VLEDUP bits and the VLEDHYS bits (07h, bits[1:0]), then V_{IN} decreases. The VLEDHYS bits set the hysteresis voltage.

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Adaptive Feedback Control (AFC) for Multiple ICs

The AFC function also supports applications with multiple ICs. The minimum active LEDx pin voltage (V_{LEDx}) between the multiple ICs controls the pre-power stage. The FBI and FBO pins deliver the V_{IN} regulation information to the ICs.

When the device address is within the range of 0000~0010, it is considered a primary IC; when the device address is within 0011~1111, it is considered a secondary IC. Figure 10 shows the FBO and FBI control methods for a multiple IC circuit.

FBI Input Detector

Connect the FBO pin of the second MPQ3322 device to the FBI pin of the first MPQ3322 device in the multiple IC circuit (see Figure 10). The FBI voltage (V_{FBI}) determines whether V_{IN} is sufficient for the latest IC, described below:

- If V_{FBI} is below 0.6V, then V_{IN} is not sufficient for the latest IC.
- If 0.6V < V_{FBI} < 1.2V, then V_{IN} does not need to change for the latest IC.
- If V_{FBI} exceeds 1.2V, then V_{IN} is too high for the latest IC.

Connect the final secondary IC's FBI pin to VCC1 or disable it via the EN_FBI bit (0Ah, bit[5]).

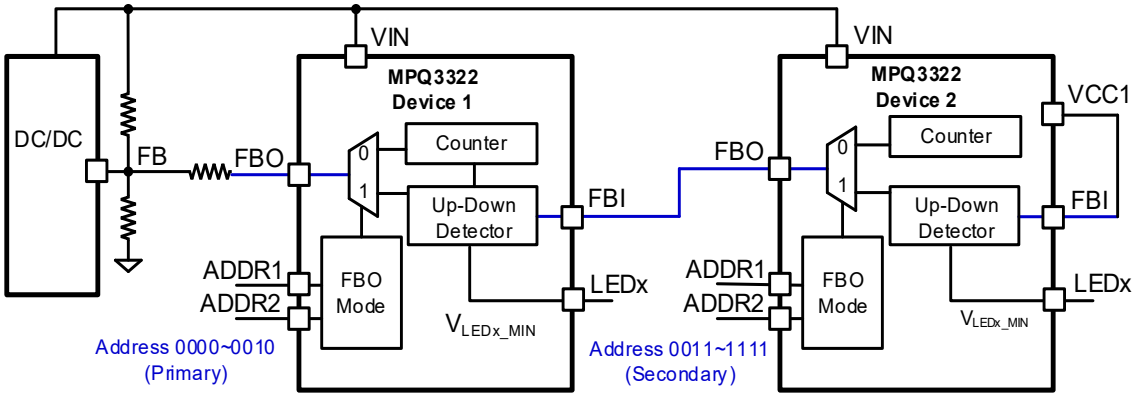

Figure 10: Multiple IC Circuit

Secondary FBO Output Detector

V_{LEDx_MIN} determines the FBO output and whether V_{IN} increases or decreases, described below:

- If V_{LEDx_MIN} is below 0.5V (default) or V_{FBI} is below 0.6V, then the FBO pin outputs 0.3V, meaning V_{IN} must increase.
- If V_{LEDx_MIN} exceeds 0.7V (default) and V_{FBI} exceeds 1.2V, then the FBO pin output 1.5V, meaning V_{IN} must decrease.

For other scenarios, the FBO pin outputs 0.9V, and V_{IN} remains at the same level. Table 1 shows the relationship between the secondary IC's V_{FBI} and V_{FBO}.

Table 1: Secondary V_{FBI} vs. V_{FBO}

Conditions	Secondary V_{FBO} (V)
V_{FBI} below 0.6V, or any V_{LEDx} below 0.5V	0.3
Other conditions	0.9
V_{FBI} exceeds 1.2V, and all V_{LEDx} exceeds 0.7V	1.5

Primary FBO Output Detector

The primary IC's FBO pin is connected to the DC/DC converter's FB resistor divider to regulate V_{IN}. V_{FBO} ranges between 0.5V and 1.5V, with an 8-bit resolution (see Figure 10 for the detailed circuit). If the primary IC's FBO pin is connected from one PCB to another PCB, then ensure that noise is not coupled directly on the signal. Since FBO is connected to a high-impedance feedback network, it can be more sensitive to noise if a

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board-to-board cable/connection without shielding or a poor ground return path is used.

LED Current Setting

The LED current (I_{LEDx}) (where x = 1 to 24) amplitude is set via an external resistor connected between the ISET pin and AGND. The LED current amplitude for all channels can be calculated with Equation (3):

$$I_{LED}\,(mA) = \frac{2000}{R_{ISET}\,(k\Omega)} \quad (3)$$

Unused LED Channel Setting

If connecting the LEDx pin of unused channel to AGND, then the MPQ3322 can automatically detect the unused LED string and remove it from the control loop during start-up. To prevent accidentally triggering this function, the capacitors between the LED1–24 pins and AGND should be below 1nF.

The MPQ3322 can also disable the unused string via the EN1 (02h), EN2 (01h), and EN3 (00h) commands.

LED Current Slew Rate Control

Changing the I_{LEDx} rising/falling slew rate during pulse-width modulation (PWM) dimming can sufficiently optimize EMI performance. The I_{LEDx} rising/falling slew rate is controlled via the SLEW bits (03h, bits[3:2]):

- If SLEW = 00, then there is no slew rate.
- If SLEW = 01, then the slew rate is 4μs.
- If SLEW = 10, then the slew rate is 8μs.
- If SLEW = 11, then the slew rate is 16μs.

Phase-Shift Function

To reduce inrush current and eliminate audible noise during PWM dimming, an optional channel-by-channel phase-shift function can be enabled by setting the PSEN bit (03h, bit[1]) high.

If the phase-shift function is enabled, then the I_{LEDx} rising edge of channel x (where x = 1 to 23) + 1 is delayed by a fixed time relative to channel x's I_{LEDx} rising edge.

The shifted phase depends on the used LED channels, and can be calculated with Equation (4):

$$\text{Phase}\,(^\circ) = \frac{360}{n}\,(^\circ) \quad (4)$$

Where *n* is number of used LED channels.

For example, if all 24 channels are used, then the phase shifts by 15° between LED channel x + 1 current (I_{LEDx+1}) (where x = 1 to 23) and the LEDx current (I_{LEDx}) (where x = 1 to 23) (see Figure 11).

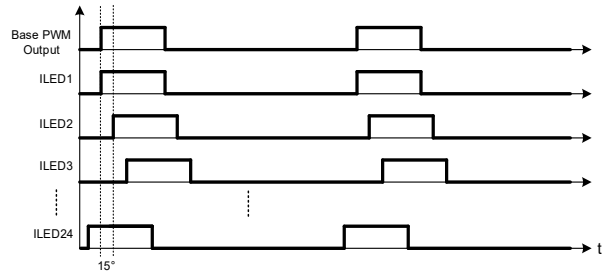

Figure 11: Phase Shift with 24 Channels

Figure 12 shows the phase-shift function with 18 channels enabled, where the shifted phase is 20°.

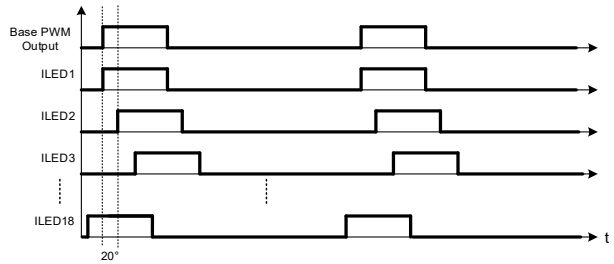

Figure 12: Phase Shift with 18 Channels

If the phase-shift function is enabled, then it is strongly recommended to avoid connecting multiple channels to a single LED string.

Oscillator Jitter

To improve electromagnetic interference (EMI) performance, the MPQ3322 utilizes a frequency spread spectrum (FSS) technique. This feature reduces EMI noise at the internal 4M clock frequency and its harmonic frequencies. The FSS function operates by modulating the internal clock frequency within ±10% of the central frequency, using a 15.6kHz modulation frequency. Additionally, the FSS function can be disabled via the EN_OSCJ bit (04h, bit[2]).

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Dimming

The MPQ3322 supports 6-bit analog dimming, voltage jumping, independent 12-bit PWM dimming, and automatic logarithmic dimming for each channel through the CAN-based differential interface.

Analog Dimming

During analog dimming, the value can be modified via the ILEDx commands (where x = 1 to 24) (0Eh to 25h) to adjust the corresponding I_{LEDx} amplitude. The I_{LEDx} amplitude can be estimated with Equation (5):

$$I_{LEDx} = \frac{ILEDx[5:0]}{63} \times I_{LED} \quad (5)$$

Where ILEDx[5:0] is the analog dimming code for the corresponding channel.

Voltage Jumping Function

In certain applications, if the customer requires a fast response to changes in analog dimming variations, the voltage jumping function can be enabled via the JUMPEN bit (06h, bit[6]). When the dimming duty increases and exceeds a predetermined threshold set via the JUMPTH bits (07h, bits[7:6]), V_{IN} rapidly increases by a specified amount determined via the JUMPST bits (07h, bits[5:4]).

Pulse-Width Modulation (PWM) Dimming

During PWM dimming, I_{LEDx} is chopped, meaning the I_{LEDx} amplitude stays the same while the I_{LEDx} duty cycle varies with the PWM dimming command.

The PWM dimming duty cycle is set via the PWM dimming commands PWM1_L (26h) to PWM24_H (55h). The duty cycle (D_x) can be calculated with Equation (6):

$$D_x = \frac{PWMx[11:0]}{4095} \quad (6)$$

Where PWMx[11:0] is the PWM dimming command for channel x (where x = 1 to 24).

If any of the PWMx bits (where x = 1 to 24) for commands PWM1_L (26h) to PWM24_H (55h) are set to 0x0000, then the corresponding I_{LEDx} is 0A. Duty cycle changes are triggered by writing values to the 4 most significant bits (MSB) of the PWM duty command. The PWM dimming frequency can be selected via the FPWM bits (03h, bits[7:4]).

The PWM dimming frequency and PWM dimming duty cycle can be changed on the fly.

Automatic Logarithmic Dimming

To reduce the burden on the communication bus, the MPQ3322 provides imbedded, automatic logarithmic dimming based on a fixed, 64-point look-up table. Assuming there are a total of 64 steps between 0% duty cycle (0) and 100% duty cycle (4095), the logarithmic curve can be fixed. This means that the duty cycle for 64 steps can be calculated using software, then confirmed in digital circuity. Figure 13 shows the logarithmic dimming curve.

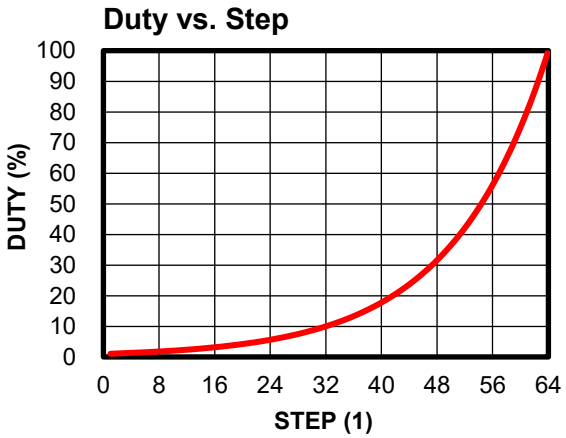

Figure 13: Logarithmic Dimming Curve

If the configured duty cycle is not equal to the duty cycle in the logarithmic dimming curve, then one more step is required to change the configured duty cycle.

IC Temperature Reading

The MPQ3322's die temperature can be read via the ICTR_FULL bits (75h, bits[3:0]) from 80°C to 170°C, with a 10°C resolution per step.

Protections

The MPQ3322 supports a variety of diagnostic features, including V_{IN} UVLO, LED short protection, LED open protection, ISET pin open/short protection, thermal warning and shutdown, and failsafe mode.

The FF pin is an active-low open drain that is pulled high to an external voltage source. If a

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protection is triggered, then the fault bit in the corresponding command is set.

For LED open and short protection, there are three possible scenarios, described below:

1. The EN_LOP bit (08h, bit[2]) and the EN_SLP bit (08h, bit[1]) enable LED open protection and LED short protection, respectively.
2. If the CHxDIA bit (where x = 1 to 24) (0Bh to 0Dh, bits[7:0]) is set to 0, then the LED open/short protection mechanism remains active, but the IC does not pull down the FF pin and generate a fault flag.
3. If an LED short/open protection is triggered, then the LATCH bit (08h, bit[0]) enables selecting between hiccup mode and latch-off mode.

If the LATCH bit is set to 0, then hiccup mode is selected, and the fault channel attempts to conduct 20µs every 20ms to detect whether the fault is cleared. The FF pin is released once the fault condition is removed. The fault bit set via the FO3 (6Eh), FO2 (6Fh), FO1 (70h), FS3 (71h), FS2 (72h), or FS1 (73h) command remains until it is cleared via the MCU.

If the LATCH bit is set to 1, then latch-off mode is selected, and the fault is triggered. The fault channel remains off until power-on reset (POR) or until the EN pin turns off to reset the channel. Meanwhile, the other channels operate normally.

V_{IN} Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. If V_{IN} UVLO is triggered, then the IC stops working, and all registers are reset.

VIN Low Voltage Detection

If the EN_VIN_LV bit (77h, bit[4]) is set to 1 and V_{IN} is below 7 x FBOS (3.5V to 10.5V), then the IC pulls down the FF pin and sets the FT_VINLV bit (74h, bit[7]) to 1. VIN low voltage detection hysteresis is about 350mV.

LED Open Protection

The MPQ3325 provides integrated LED open diagnostics by detecting the LEDx voltage (V_{LEDx}) (where x = 1 to 24). During operation, if an LED open fault occurs in a channel, then the respective V_{LEDx} is low. If the AFC function is used and V_{LEDx} drops below the protection threshold (about 100mV), then V_{LEDx} lasts for 8 FBO regulation steps, set via the T_OPS bits (05h, bits[5:3]). If AFC is not used and V_{LEDx} drops below the protection threshold for 2ms (with 100% duty cycle), then LED open protection is triggered, the fault channel is turned off, the corresponding CHxO bit (where x = 1 to 24) (6Eh to 70h) is set, and the FF pin is pulled low.

LED Short Protection

The MPQ3322 monitors V_{LEDx} to determine whether a short string fault has occurred. If one or more strings are shorted, then the respective LEDx pin (where x = 1 to 24) tolerates high-voltage stress. If V_{LEDx} exceeds the LED short protection threshold, then an internal counter starts. If this fault condition lasts for 2ms (D_{PWM} = 100%), then the fault channel is turned off, the corresponding CHxS fault bit is set, and the FF pin is pulled low.

The LED short protection threshold is configured via the STH bits (04h, bits[1:0]), and can be set to the following values:

- If STH = 00, then the threshold is 2V.
- If STH = 01, then the threshold is 4V.
- If STH = 10, then the threshold is 8V.
- If STH = 11, then the threshold is 10V.

ISET Pin Open/Short Protection

The MPQ3322 implements a current monitor for the ISET resistor to provide open and short diagnostics and protection. The device monitors the current flowing out of the ISET pin (I_{SET}). If I_{SET} exceeds 100µA, then an ISET pin short condition asserts. If I_{SET} drops below 5µA, then an ISET pin open condition asserts.

ISET pin open or short protection is a latch-off protection. If an open or short fault is detected, then the FT_ISET bit (74h, bit[2]) is set. The MPQ3322 latches off and asserts the FF pin.

Over-Temperature Warning (OTW)

If the IC temperature exceeds 140°C (as set via the TH_OTW bit (06h, bit[7])), then over-temperature warning (OTW) is triggered. In this case, the IC continues to operate normally, but the FF pin is pulled low and the FT_OTW bit (74h,

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bit[1]) is set. Once the OTW condition is removed, the FF pin returns to its normal high state.

The OTW function can be enabled via the EN_OTW bit (08h, bit[3]). Additionally, the EN_FFOT bit (08h, bit[4]) controls whether the FF pin is pulled low if an OTW condition occurs.

Over-Temperature Protection

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the IC temperature exceeds 170°C, then over-temperature protection is triggered, causing all channels to shut down. The FF pin is pulled low, and the FT_OTP bit (74h, bit[0]) is set to indicate that an over-temperature (OT) condition has been detected. If the temperature drops 20°C below the thermal shutdown threshold, then the MPQ3322 recovers, and the channels turn on using the previous settings without re-initializing.

Failsafe Mode

The MPQ3322 supports two failsafe modes: failsafe mode and FS mode. Both modes allow for customizable PWM duty and LED amplitude settings. Failsafe mode is configured between the 0x56 to 0x61 address range, and provides a specific set of configuration options for ensuring reliable operation in critical applications. FS mode is configured between the 0x62 to 0x6D address range, and offers more flexibility and customization options compared to failsafe mode; this allows users to finetune their PWM duty and LED amplitude settings according to specific requirements.

In failsafe mode, the MPQ3322 uses a grouping method to regulate its PWM and analog outputs. Each duty and amplitude register regulates the PWM duty cycle and analog amplitude level for four LED channels.

Figure 14 shows MPQ3322 in failsafe mode. The IC transitions to failsafe mode when the FS pin drops below the FS falling threshold and a configurable watchdog detects a communication failure. Otherwise, the IC remains in FS mode as long as the FS pin remains high.

To configure the registers of failsafe mode or FS mode, one-time programmable (OTP) the non-volatile memory (NVM) must be configured before use. If the customer must modify these register values during operation, then the correct password is required to be written to the PCF (80h) command. The password sequence is as follows: 0x5B, 0x82, 0xEA, and 0x8E.

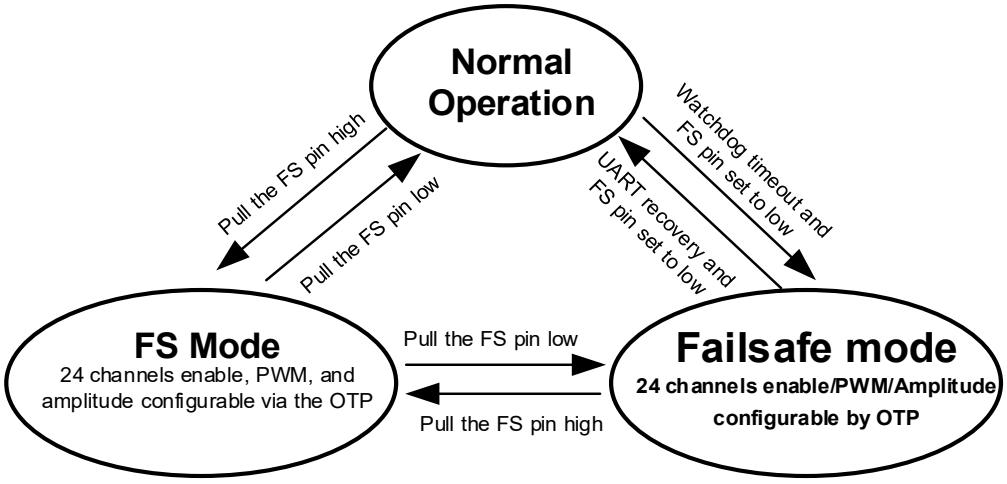

Figure 14: Failsafe Mode State Diagram

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CAN INTERFACE

CAN-Based Differential Protocol

The MPQ3322 employs a CAN-based differential interface protocol, where each transmission frame begins with a SYNC byte, followed by multiple data bytes.

Each byte consists of a 10-bit structure: 1 start bit, 8 data bits, and 1 stop bit. Figure 15 shows a single byte structure, where the least significant bit (LSB) data starts after the start bit.

Figure 15: Single Byte Data Format

The differential interface supports both write and readback commands. When a command is received, the MPQ3322 responds to the MCU by clearing the watchdog timer, set via the TWD bits (0Ah, bits[3:0]), after the CRC byte is verified. In addition, if communication is interrupted in the middle of the transmission, then the MPQ3322 waits longer than the CAN timeout timer set via the TCAN bits (04h, bits[7:5]), resets communication, and waits for a new communication. The idle period between bytes are also required to be within the timeout timer.

Table 2 shows the write command with status feedback. Figure 16 shows the frame structure of a typical write action. When the MCU writes data to the MPQ3322, it must transmit the following byte sequence: SYNC, DEV_ADDR, REG_ADDR, DATA, and CRC. The MPQ3322 verifies the cyclic redundancy check (CRC) value after receiving all bytes. If verification is successful, then the MPQ3322 responds with a status byte, followed by a new CRC value. This confirms that the write operation was completed successfully.

Table 2: Write Command with Status Feedback (7)

ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP
Sync byte	Device address byte	Register address byte	DATA[0]	DATA[n]	CRC byte	Status byte	CRC byte

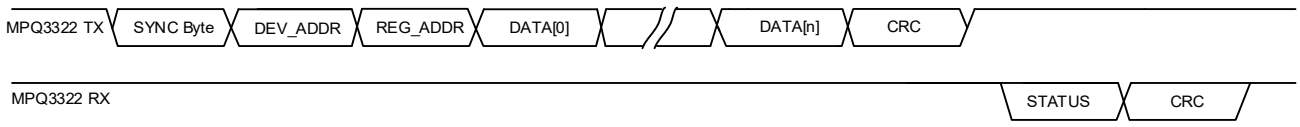

Figure 16: Frame Structure of Typical Write Action

Table 3 shows the read command with data feedback. Figure 17 on page 24 shows the frame structure of a typical readback action. When the primary starts a readback action, it transmits the following bytes in sequence: SYNC, DEV_ADDR, REG_ADDR, and CRC. Once the complete frame is received, the MPQ3322 verifies the CRC value. If the verification is successful, then the MPQ3322 immediately responds with the DATA and CRC bytes.

Table 3: Read Command with Data Feedback (7)

ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP	ST + 8 bits + SP
Sync byte	Device address byte	Register address byte	CRC byte	DATA[0]	DATA[n]	CRC byte

Note:

7) ST refers to the start bit, and SP refers to the stop bit.

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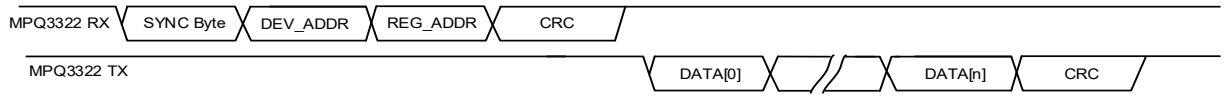

Figure 17: Frame Structure of Typical Readback Action

Synchronization Byte

The first byte transmitted from the MCU to the MPQ3322 is the SYNC byte: 01010101. This synchronization byte functions as a clock signal, allowing the secondary (MPQ3322) to synchronize its internal high-frequency clock with the MCU clock. To ensure reliable communication and prevent clock drift over time, the SYNC byte must be transmitted for each new frame. With this approach, communication reliability is improved, and the cost for the external crystal oscillator is reduced.

Table 4 shows the SYNC byte settings, and Table 5 shows the device address byte settings that follow the SYNC byte. Figure 18 shows the SYNC byte's timing diagram.

Table 4: SYNC Byte Settings

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1

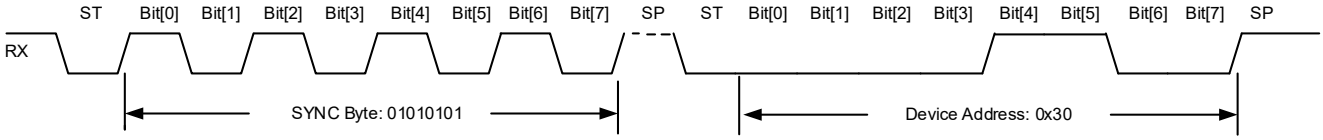

Figure 18: SYNC Byte Timing Diagram

Table 5: Device Address Byte Settings

Bit	Name	Description
7	READ/WRITE	1: Write mode 0: Read mode
6	BROADCAST	1b: Broadcast, only accepts write commands (requires setting the device address to 0000) 0b: Single device only
5:4	DATA_LENGTH	00b: 1 byte 01b: 2 bytes 10b: 4 bytes 11b: 8 bytes
3:0	DEV_ADDR	The device address.

Chip Address

Up to 16 unique device addresses can be configured via the ADDR1 and ADDR2 pins. During the initial boot-up, the IC checks address. Once the address is checked, it does not change unless IC power-on reset (POR) occurs.

Table 6 on page 25 shows the recommended ADDR1 and ADDR2 resistances (R_{ADDR1} and R_{ADDR2}, respectively), based on the device address.

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Table 6: Recommended ADDR1 and ADDR2 Resistances for Different Device Addresses

R_{ADDR1} (kΩ)	R_{ADDR2} (kΩ)	Address
0	0	0000
	24.9	0001
	41.2	0010
	60.4	0011
24.9	0	0100
	24.9	0101
	41.2	0110
	60.4	0111
41.2	0	1000
	24.9	1001
	41.2	1010
	60.4	1011
60.4	0	1100
	24.9	1101
	41.2	1110
	60.4	1111

Register Address Byte

The register address byte consists of an 8-bit binary code that uniquely identifies the desired register (see Table 7). The possible values for this byte range between the EN3 (00h) to DEV_ID (76h) commands and the PCF (80h) command, providing a total of 77 unique addresses.

Table 7: Register Address Bye

Bits	Bit Name	Description
7:0	REG_ADDR	Register address

DATA Byte

Following the register address frame, the data frame contains 1 or more data bytes that can be transmitted simultaneously. The MPQ3322 supports two modes of data transmission: single-byte writing and multi-byte writing. The number of data bytes to be written is specified in the device address byte (see Table 6 on page 24). There are four possible options for the number of data bytes: 1, 2, 4 or 8.

STATUS Byte

The status register contains error information and is used to monitor the system status. Table 8 shows the status byte settings.

Table 8: STATUS Byte Settings

D7	D6	D5	D4	D3	D2	D1	D0
ICTR1	ICTR0	CH_S	CH_O	FT_FS	FT_ISET	FT_OTW	FT_OTP

The die temperature is read via ICTR1 and ICTR0 from Table 8:

- If ICTR1 and ICTR0 are set to 00, then the die temperature is below 80°C.
- If ICTR1 and ICTR0 are set to 01, then the die temperature is between 80°C and 110°C.
- If ICTR1 and ICTR0 are set to 10, then the die temperature is between 110°C and 140°C.
- If ICTR1 and ICTR0 are set to 11, then the die temperature exceeds 140°C.

CRC Byte

The CRC algorithm for multiple bytes of binary data employs the following polynomial: $X^8 + X^5 + X^4 + 1$. The CRC code consists of an 8-bit binary, and the initial value is 0xFF. It is important to keep in mind that the CRC calculation does not include the SYNC byte.

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SUPPORTED CAN INTERFACE COMMANDS

00h~0Ah, 0Eh~6Dh, and 77h include one-time programmable (OTP) memory.

Command Name	R/W	Add	Default (8)	D7	D6	D5	D4	D3	D2	D1	D0
EN3	R/W	00h	FFh	EN24	EN23	EN22	EN21	EN20	EN19	EN18	EN17
EN2	R/W	01h	FFh	EN16	EN15	EN14	EN13	EN12	EN11	EN10	EN9
EN1	R/W	02h	FFh	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1
DIM1	R/W	03h	01h	FPWM				SLEW		PSEN	EN
DIM2	R/W	04h	00h	TCAN			EN_GDA	EN_GDP	EN_ OSCJ	STH1:0	
CON1	R/W	05h	28h	OVP		T_OPS			T_INI		
CON2	R/W	06h	20h	TH_ OTW	JUMPEN	EN_ MODU	EN_LAD	HOLDCB	AUDS		
CON3	R/W	07h	08h	JUMPTH		JUMPST		VLEDUP1:0		VLEDHYS	
CON4	R/W	08h	D6h	EN_OPF	EN_SFP	EN_SLM	EN_ FFOT	EN_ OTW	EN_LOP	EN_SLP	LATCH
FBO	R/W	09h	B3h	FBOS							
CON5	R/W	0Ah	70h	RSTF	EN_FBO	EN_FBI	EN_FF_ FS	TWD			
DIA3	R/W	0Bh	FFh	CH24 DIA	CH23 DIA	CH22 DIA	CH21DIA	CH20 DIA	CH19 DIA	CH18 DIA	CH17DI A
DIA2	R/W	0Ch	FFh	CH16 DIA	CH15 DIA	CH14 DIA	CH13DIA	CH12 DIA	CH11 DIA	CH10 DIA	CH9DIA
DIA1	R/W	0Dh	FFh	CH8DIA	CH7DIA	CH6DIA	CH5DIA	CH4DIA	CH3DIA	CH2DIA	CH1DIA
ILED1	R/W	0Eh	3Fh	RESERVED		ILED1					
ILED2	R/W	0Fh	3Fh	RESERVED		ILED2					
ILED3	R/W	10h	3Fh	RESERVED		ILED3					
ILED4	R/W	11h	3Fh	RESERVED		ILED4					
ILED5	R/W	12h	3Fh	RESERVED		ILED5					
ILED6	R/W	13h	3Fh	RESERVED		ILED6					
ILED7	R/W	14h	3Fh	RESERVED		ILED7					
ILED8	R/W	15h	3Fh	RESERVED		ILED8					
ILED9	R/W	16h	3Fh	RESERVED		ILED9					
ILED10	R/W	17h	3Fh	RESERVED		ILED10					
ILED11	R/W	18h	3Fh	RESERVED		ILED11					
ILED12	R/W	19h	3Fh	RESERVED		ILED12					
ILED13	R/W	1Ah	3Fh	RESERVED		ILED13					
ILED14	R/W	1Bh	3Fh	RESERVED		ILED14					
ILED15	R/W	1Ch	3Fh	RESERVED		ILED15					
ILED16	R/W	1Dh	3Fh	RESERVED		ILED16					
ILED17	R/W	1Eh	3Fh	RESERVED		ILED17					
ILED18	R/W	1Fh	3Fh	RESERVED		ILED18					
ILED19	R/W	20h	3Fh	RESERVED		ILED19					
ILED20	R/W	21h	3Fh	RESERVED		ILED20					
ILED21	R/W	22h	3Fh	RESERVED		ILED21					
ILED22	R/W	23h	3Fh	RESERVED		ILED22					

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SUPPORTED CAN INTERFACE COMMANDS *(continued)*

00h~0Ah, 0Eh~6Dh, and 77h include one-time programmable (OTP) memory.

Command Name	R/W	Add	Default (8)	D7	D6	D5	D4	D3	D2	D1	D0
ILED23	R/W	24h	3Fh	RESERVED		ILED23					
ILED24	R/W	25h	3Fh	RESERVED		ILED24					
PWM1_L	R/W	26h	FFh	PWM1							
PWM1_H	R/W	27h	0Fh	RESERVED				PWM1			
PWM2_L	R/W	28h	FFh	PWM2							
PWM2_H	R/W	29h	0Fh	RESERVED				PWM2			
PWM3_L	R/W	2Ah	FFh	PWM3							
PWM3_H	R/W	2Bh	0Fh	RESERVED				PWM3			
PWM4_L	R/W	2Ch	FFh	PWM4							
PWM4_H	R/W	2Dh	0Fh	RESERVED				PWM4			
PWM5_L	R/W	2Eh	FFh	PWM5							
PWM5_H	R/W	2Fh	0Fh	RESERVED				PWM5			
PWM6_L	R/W	30h	FFh	PWM6							
PWM6_H	R/W	31h	0Fh	RESERVED				PWM6			
PWM7_L	R/W	32h	FFh	PWM7							
PWM7_H	R/W	33h	0Fh	RESERVED				PWM7			
PWM8_L	R/W	34h	FFh	PWM8							
PWM8_H	R/W	35h	0Fh	RESERVED				PWM8[11:8]			
PWM9_L	R/W	36h	FFh	PWM9							
PWM9_H	R/W	37h	0Fh	RESERVED				PWM9			
PWM10_L	R/W	38h	FFh	PWM10							
PWM10_H	R/W	39h	0Fh	RESERVED				PWM10			
PWM11_L	R/W	3Ah	FFh	PWM11							
PWM11_H	R/W	3Bh	0Fh	RESERVED				PWM11			
PWM12_L	R/W	3Ch	FFh	PWM12							
PWM12_H	R/W	3Dh	0Fh	RESERVED				PWM12			
PWM13_L	R/W	3Eh	FFh	PWM13							
PWM13_H	R/W	3Fh	0Fh	RESERVED				PWM13			
PWM14_L	R/W	40h	FFh	PWM14							
PWM14_H	R/W	41h	0Fh	RESERVED				PWM14			
PWM15_L	R/W	42h	FFh	PWM15							
PWM15_H	R/W	43h	0Fh	RESERVED				PWM15			
PWM16_L	R/W	44h	FFh	PWM16							
PWM16_H	R/W	45h	0Fh	RESERVED				PWM16			
PWM17_L	R/W	46h	FFh	PWM17							
PWM17_H	R/W	47h	0Fh	RESERVED				PWM17			

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SUPPORTED CAN INTERFACE COMMANDS *(continued)*

00h~0Ah, 0Eh~6Dh, and 77h include one-time programmable (OTP) memory.

Command Name	R/W	Add	Default (8)	D7	D6	D5	D4	D3	D2	D1	D0
PWM18_L	R/W	48h	FFh	PWM18							
PWM18_H	R/W	49h	0Fh	RESERVED				PWM18			
PWM19_L	R/W	4Ah	FFh	PWM19							
PWM19_H	R/W	4Bh	0Fh	RESERVED				PWM19			
PWM20_L	R/W	4Ch	FFh	PWM20							
PWM20_H	R/W	4Dh	0Fh	RESERVED				PWM20			
PWM21_L	R/W	4Eh	FFh	PWM21							
PWM21_H	R/W	4Fh	0Fh	RESERVED				PWM21			
PWM22_L	R/W	50h	FFh	PWM22							
PWM22_H	R/W	51h	0Fh	RESERVED				PWM22			
PWM23_L	R/W	52h	FFh	PWM23							
PWM23_H	R/W	53h	0Fh	RESERVED				PWM23			
PWM24_L	R/W	54h	FFh	PWM24							
PWM24_H	R/W	55h	0Fh	RESERVED				PWM24			
FS1ILED1	R/W	56h	3Fh	RESERVED		FS1ILED1					
FS1ILED2	R/W	57h	3Fh	RESERVED		FS1ILED2					
FS1ILED3	R/W	58h	3Fh	RESERVED		FS1ILED3					
FS1ILED4	R/W	59h	3Fh	RESERVED		FS1ILED4					
FS1ILED5	R/W	5Ah	3Fh	RESERVED		FS1ILED5					
FS1ILED6	R/W	5Bh	3Fh	RESERVED		FS1ILED6					
FS1PWM1	R/W	5Ch	FFh	FS1PWM1							
FS1PWM2	R/W	5Dh	FFh	FS1PWM2							
FS1PWM3	R/W	5Eh	FFh	FS1PWM3							
FS1PWM4	R/W	5Fh	FFh	FS1PWM4							
FS1PWM5	R/W	60h	FFh	FS1PWM5							
FS1PWM6	R/W	61h	FFh	FS1PWM6							
FS2ILED1	R/W	62h	3Fh	RESERVED		FS2ILED1					
FS2ILED2	R/W	63h	3Fh	RESERVED		FS2ILED2					
FS2ILED3	R/W	64h	3Fh	RESERVED		FS2ILED3					
FS2ILED4	R/W	65h	3Fh	RESERVED		FS2ILED4					
FS2ILED5	R/W	66h	3Fh	RESERVED		FS2ILED5					
FS2ILED6	R/W	67h	3Fh	RESERVED		FS2ILED6					
FS2PWM1	R/W	68h	FFh	FS2PWM1							
FS2PWM2	R/W	69h	FFh	FS2PWM2							
FS2PWM3	R/W	6Ah	FFh	FS2PWM3							

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SUPPORTED CAN INTERFACE COMMANDS *(continued)*

00h~0Ah, 0Eh~6Dh, and 77h include one-time programmable (OTP) memory.

Command Name	R/W	Add	Default (8)	D7	D6	D5	D4	D3	D2	D1	D0
FS2PWM4	R/W	6Bh	FFh	FS2PWM4							
FS2PWM5	R/W	6Ch	FFh	FS2PWM5							
FS2PWM6	R/W	6Dh	FFh	FS2PWM5							
FO3	R/W	6Eh	00h	CH24O	CH23O	CH22O	CH21O	CH20O	CH19O	CH18O	CH17O
FO2	R/W	6Fh	00h	CH16O	CH15O	CH14O	CH13O	CH12O	CH11O	CH10O	CH9O
FO1	R/W	70h	00h	CH8O	CH7O	CH6O	CH5O	CH4O	CH3O	CH2O	CH1O
FS3	R/W	71h	00h	CH24S	CH23S	CH22S	CH21S	CH20S	CH19S	CH18S	CH17S
FS2	R/W	72h	00h	CH16S	CH15S	CH14S	CH13S	CH12S	CH11S	CH10S	CH9S
FS1	R/W	73h	00h	CH8S	CH7S	CH6S	CH5S	CH4S	CH3S	CH2S	CH1S
FSS	R/W	74h	00h	FT_ VINLV	FT_OV	CH_S	CH_O	FT_FS	FT_ISET	FT_OTW	FT_OTP
T_IC	R	75h	00h	RESERVED		FB_UP	FB_ DOWN	ICTR_FULL			
ID	R	76h	22h	ID							
EN4	W/R	77h	27h	RESERVED			EN_VIN_ LV	EN_FB_ INIT	EN_ DIMOL	EN_ ISETS	EN_ ISETO
PCF	W/R	80h	00h	PWFS							

Note:

8) The default values are for the MPQ3322GQKE-0000-AEC1-Z registers. If the user wants to change the default value of OTP available registers, contact an MPS FAE to obtain a custom suffix “xxxx” value for the MPQ3322GQKE-xxxx-AEC1-Z.

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REGISTER MAP

EN3 (00h)

Format: Unsigned binary

The EN3 command sets the enable of channel 24 to channel 17.

Bits	Access	Bit Name	Default	Description
7	R/W	EN24	1’b1	Enables channel 24. 1’b0: Disabled 1’b1: Enabled
6	R/W	EN23	1’b1	Enables channel 23. 1’b0: Disabled 1’b1: Enabled
5	R/W	EN22	1’b1	Enables channel 22. 1’b0: Disabled 1’b1: Enabled
4	R/W	EN21	1’b1	Enables channel 21. 1’b0: Disabled 1’b1: Enabled
3	R/W	EN20	1’b1	Enables channel 20. 1’b0: Disabled 1’b1: Enabled
2	R/W	EN19	1’b1	Enables channel 19. 1’b0: Disabled 1’b1: Enabled
1	R/W	EN18	1’b1	Enables channel 18. 1’b0: Disabled 1’b1: Enabled
0	R/W	EN17	1’b1	Enables channel 17. 1’b0: Disabled 1’b1: Enabled

EN2 (01h)

Format: Unsigned binary

The EN2 command sets the enable of channel 16 to channel 9.

Bits	Access	Bit Name	Default	Description
7	R/W	EN16	1’b1	Enables channel 16. 1’b0: Disabled 1’b1: Enabled
6	R/W	EN15	1’b1	Enables channel 15. 1’b0: Disabled 1’b1: Enabled
5	R/W	EN14	1’b1	Enables channel 14. 1’b0: Disabled 1’b1: Enabled

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4	R/W	EN13	1’b1	Enables channel 13. 1’b0: Disabled 1’b1: Enabled
3	R/W	EN12	1’b1	Enables channel 12. 1’b0: Disabled 1’b1: Enabled
2	R/W	EN11	1’b1	Enables channel 11. 1’b0: Disabled 1’b1: Enabled
1	R/W	EN10	1’b1	Enables channel 10. 1’b0: Disabled 1’b1: Enabled
0	R/W	EN9	1’b1	Enables channel 9. 1’b0: Disabled 1’b1: Enabled

EN1 (02h)

Format: Unsigned binary

The EN1 command sets the enable of channel 8 to channel 1.

Bits	Access	Bit Name	Default	Description
7	R/W	EN8	1’b1	Enables channel 8. 1’b0: Disabled 1’b1: Enabled
6	R/W	EN7	1’b1	Enables channel 7. 1’b0: Disabled 1’b1: Enabled
5	R/W	EN6	1’b1	Enables channel 6. 1’b0: Disabled 1’b1: Enabled
4	R/W	EN5	1’b1	Enables channel 5. 1’b0: Disabled 1’b1: Enabled
3	R/W	EN4	1’b1	Enables channel 4. 1’b0: Disabled 1’b1: Enabled
2	R/W	EN3	1’b1	Enables channel 3. 1’b0: Disabled 1’b1: Enabled
1	R/W	EN2	1’b1	Enables channel 2. 1’b0: Disabled 1’b1: Enabled
0	R/W	EN1	1’b1	Enables channel 1. 1’b0: Disabled 1’b1: Enabled

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DIM1 (03h)

Format: Unsigned binary

The DIM1 command sets the pulse-width modulation (PWM) dimming frequency, LED current slew rate, phase shift enable, and IC enable.

Bits	Access	Bit Name	Default	Description
7:4	R/W	FPWM3:0	4’b 0000	Sets the PWM dimming frequency. 4’b 0000~4’b0100: 200Hz (default) to 400Hz, 50Hz/step 4’b 0101: 500Hz 4’b 0110: 600Hz 4’b 0111: 800Hz 4’b 1000: 1kHz 4’b 1001: 1.2kHz 4’b 1010: 2kHz 4’b 1011: 4kHz 4’b 1100: 5.9kHz 4’b 1101: 7.8kHz 4’b 1110: 9.6kHz 4’b 1111: 20.8kHz
3:2	R/W	SLEW	2’b 00	Sets the LED current slew rate. 2’b 00: No slew rate 2’b 01: 4μs 2’b 10: 8μs 2’b 11: 16μs
1	R/W	PSEN	1’b0	Enables the phase shift. 1’b 0: Disabled 1’b 1: Enabled
0	R/W	EN	1’b1	Enables the MPQ3322. 1’b 0: Disabled 1’b 1: Enabled

DIM2 (04h)

Format: Unsigned binary

The DIM2 command sets the CAN timeout timer, analog global dimming enable, pulse-width modulation (PWM) global dimming enable, oscillator jitter enable, and the LED short protection threshold.

Bits	Access	Bit Name	Default	Description
7:5	R/W	TCAN	3’b 000	Sets the CAN timeout timer. 3’b 000: 125μs 3’b 001: 15.625μs 3’b 010: 31.25μs 3’b 011: 62.5μs 3’b 100: 156.25μs 3’b 101: 312.5μs 3’b 110: 625μs 111: 1.25ms
4	R/W	EN_GDA	1’b0	Enables analog global dimming. 1’b0: Disabled 1’b1: Enabled, where all channels’ analog duty follows channel 1

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3	R/W	EN_GDP	1’b0	Enables PWM global dimming. 1’b0: Disabled 1’b1: Enabled, where all channels’ PWM duty follows channel 1
2	R/W	EN_OSCJ	1’b0	Enables the oscillator jitter. 1’b0: Disabled 1’b1: Enabled
1:0	R/W	STH	2’b 00	Sets the LED short protection threshold. 2’b 00: 2V 2’b 01: 4V 2’b 10: 8V 2’b 11: 10V

CON1 (05h)

Format: Unsigned binary

The CON1 command sets over-voltage protection (OVP), the open protection time, and the current source delay time.

Bits	Access	Bit Name	Default	Description
7:6	R/W	OVP	2’b 00	If adaptive feedback control (AFC) is used, then the OVP function is enabled. The IC reports V_{IN} OVP once the input voltage (V_{IN}) exceeds the OVP threshold. 2’b 00: 22V 2’b 01: 16.5V 2’b 10: 11V 2’b 11: 5.5V
5:3	R/W	T_OPS	3’b 101	If an LED string is open and the fault lasts for the steps of FBO regulation set via these bits, then the LED string under an open fault is turned off. 3’b 000~3’b 010: 4 steps 3’b 011: 8 steps … 3’b 110: 64 steps 3’b 111: 128 steps
2:0	R/W	T_INI	3’b 000	Sets the delay time to enable the current source after the EN pin goes high. 3’b 000: 0μs 3’b 001: 500μs 3’b 010: 1ms 3’b 011: 2ms 3’b 100: 5ms 3’b 101: 10ms 3’b 110: 25ms 3’b 111: 50

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CON2 (06h)

Format: Unsigned binary

The CON2 command sets the over-temperature warning (OTW) threshold, jumping function, modulation, and logarithmic dimming.

Bits	Access	Bit Name	Default	Description
7	R/W	TH_OTW	1’b0	Sets the OTW threshold. 1’b0: 140°C 1’b1: 110°C
6	R/W	JUMPEN	1’b0	Enables the voltage jumping function. 1’b0: Disabled 1’b1: Enabled
5	R/W	EN_MODU	1’b1	Enables the modulation function. 1’b0: Disables the up-down counter, and maintains modulation at the same level 1’b1: Enables the up-down counter
4	R/W	EN_LAD	1’b0	Sets logarithmic automatic dimming. 1’b0: Manual mode. The PWM dimming duty is changed during the next PWM dimming cycle 1’b1: Automatic dimming mode (logarithmic dimming). Changes the duty value according to the fixed exponential curve with a speed set via bits[2:0] of this command
3	R/W	HOLDCB	1’b0	Holds the current brightness. 1’b0: Normal operation dimming duty value changes 1’b1: Stops all ongoing automatic dimming ramping, and holds the current dimming value, regardless of whether the final duty has been reached
2:0	R/W	AUDS	3’b 000	Sets the automatic dimming speed for a 64-point logarithmic curve. 3’b 000: Jumps 4 points in one PWM cycle (0% to 100%, with 16ms for 1kHz) 3’b 001: Jumps 8 points in one PWM cycle (0% to 100%, with 8ms for 1kHz) 3’b 010: Jumps 16 points in one PWM cycle (0% to 100%, with 4ms for 1kHz) 3’b 011: Jumps 2 points in one PWM cycle (0% to 100%, with 32ms for 1kHz) 3’b100: Jumps 1 point in one PWM cycle (0% to 100%, with 64ms for 1kHz) Others: Same as 3’b 000

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CON3 (07h)

Format: Unsigned binary

The CON3 command sets the duty cycle and jumping steps for the voltage jumping function, as well as the LEDx voltage (V_{LEDx}) (where x = 1 to 24) threshold and V_{LEDx} comparison hysteresis for adaptive feedback control (AFC) threshold.

Bits	Access	Bit Name	Default	Description
7:6	R/W	JUMPTH	2'b 00	The duty cycle variation threshold triggers the voltage jumping function. This threshold is the maximum variation of the analog dimming register between all channels. 2'b 00: 8% 2'b 01: 16% 2'b 10: 32% 2'b 11: 64%
5:4	R/W	JUMPST	2'b 00	Sets the jumping steps, where the FBO output voltage changes 3.92mV/step. 2'b 00: 4steps 2'b 01: 8 steps 2'b 10: 16 steps 2'b 11: 32 steps The actual V_{IN} change can be calculated with the following equation (for more details, see the Adaptive Feedback Control (AFC) for Multiple ICs section on page 18): $V_{IN} = V_{FB} \times (1 + \frac{R1}{R2}) + \frac{R3}{R2} \times (V_{FB} - V_{FBO})$
3:2	R/W	VLEDUP	2'b 10	Sets the V_{LEDx} threshold for increasing V_{IN} for AFC control. 2'b 00: 0.3V 2'b 01: 0.4V 2'b 10: 0.5V 2'b 11: 0.6V
1:0	R/W	VLEDHYS	2'b 00	Sets the V_{LEDx} comparison hysteresis for AFC control. V_{IN} decreases if the minimum V_{LEDx} exceeds the sum of the headroom voltage (V_{LEDx_UP}) and the hysteresis voltage (V_{LEDx_HYS}), which are set via bits[3:2] of this command and these bits, respectively. 2'b 00: 0.3V 2'b 01: 0.4V 2'b 10: 0.5V 2'b 11: 0.6V

CON4 (08h)

Format: Unsigned binary

The CON4 command sets the enable of various protections, including open protection, short protection, single lamp mode (SLM), over-temperature protection, over-temperature warning (OTW), LED string open/short protection, and latch-up mode.

Bits	Access	Bit Name	Default	Description
7	R/W	EN_OPF	1'b1	Determines if an LED open fault pulls the FF pin low. 1'b0: Disabled 1'b1: Enabled

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6	R/W	EN_SFP	1’b1	Determines if an LED short fault pulls the FF pin low. 1’b0: Disabled 1’b1: Enabled
5	R/W	EN_SLM	1’b0	Enables SLM. If any fault condition that pulls the FF pin low occurs, then all the MPQ3322 devices shut down, and the SLM function requires all the FF pins to be connected together. 1’b0: Disabled 1’b1: Enabled
4	R/W	EN_FFOT	1’b1	Determines if an OTW or over-temperature protection pulls the FF pin low. 1’b0: Disabled 1’b1: Enabled
3	R/W	EN_OTW	1’b0	Enables OTW. 1’b0: Disabled 1’b1: Enabled
2	R/W	EN_LOP	1’b1	Enables LED string open protection. 1’b0: Disabled 1’b1: Enabled
1	R/W	EN_SLP	1’b1	Enables LED string short protection. 1’b0: Disabled 1’b1: Enabled
0	R/W	LATCH	1’b0	Enables the latch-up mode. 0: Disabled. The device enters hiccup mode if a fault occurs 1: Enabled. The fault is latched up

FBO (09h)

Format: Unsigned hexadecimal

The FBO command sets the initial FBO pin voltage (V_{FBO_INIT}).

Bits	Access	Bit Name	Default	Description
7:0	R/W	FBOS	8’h b3	V_{FBO_INIT} ranges between 0.5V and 1.5V, with 3.922mV/step. 8’h 00: 0.5V 8’h 01: (0.5V + 3.922mV) … 8’h b2: 1.198V 8’h b3: 1.202V … 8’h ff: 1.5V

CON5 (0Ah)

Format: Unsigned binary

The CON5 command sets the FBI and FBO pin enable, as well as the watchdog time.

Bits	Access	Bit Name	Default	Description
7	R/W	RSTF	1’b0	IC restart flag. When the IC starts up, this bit is always set to 0. (This bit cannot be configured via the OTP memory.)
6	R/W	EN_FBO	1’b1	The FBO pin controls adaptive feedback control (AFC). 1’b0: Disabled 1’b1: Enabled

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5	R/W	EN_FBI	1’b1	The FBI pin controls AFC. 1’b0: Disabled 1’b1: Enabled
4	R/W	EN_FF_FS	1’b1	Pulls the FF pin low if entering failsafe mode. 1’b0: Disabled 1’b1: Enabled
3:0	R/W	TWD	4’b 0000	Sets the watchdog time. 4’b 0000: Disabled. Does not enter failsafe mode automatically 4’b 0001: 200μs 4’b 0010: 500μs 4’b 0011: 1ms 4’b 0100: 2ms 4’b 0101: 5ms 4’b 0110:10ms 4’b 0111: 20ms 4’b 1000: 50ms 4’b 1001: 100ms 4’b 1010: 200ms 4’b 1011: 500ms 4’b 1100~4’b 1111: Directly enters failsafe mode

DIA3 (0Bh)

Format: Unsigned binary

The DIA3 command enables the diagnostics for channel 24 to channel 17.

Bits	Access	Bit Name	Default	Description
7	R/W	CH24DIA	1’b1	Enables channel 24’s diagnostics. 1’b0: Disabled 1’b1: Enabled
6	R/W	CH23DIA	1’b1	Enables channel 23’s diagnostics. 1’b0: Disabled 1’b1: Enabled
5	R/W	CH22DIA	1’b1	Enables channel 22’s diagnostics. 1’b0: Disabled 1’b1: Enabled
4	R/W	CH21DIA	1’b1	Enables channel 21’s diagnostics. 1’b0: Disabled 1’b1: Enabled
3	R/W	CH20DIA	1’b1	Enables channel 20’s diagnostics. 1’b0: Disabled 1’b1: Enabled
2	R/W	CH19DIA	1’b1	Enables channel 19’s diagnostics. 1’b0: Disabled 1’b1: Enabled
1	R/W	CH18DIA	1’b1	Enables channel 18’s diagnostics. 1’b0: Disabled 1’b1: Enabled

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0	R/W	CH17DIA	1’b1	Enables channel 17’s diagnostics. 1’b0: Disabled 1’b1: Enabled

DIA2 (0Ch)

Format: Unsigned binary

The DIA2 command enables the diagnostics for channel 16 to channel 9.

Bits	Access	Bit Name	Default	Description
7	R/W	CH16DIA	1’b1	Enables channel 16’s diagnostics. 1’b0: Disabled 1’b1: Enabled
6	R/W	CH15DIA	1’b1	Enables channel 15’s diagnostics. 1’b0: Disabled 1’b1: Enabled
5	R/W	CH14DIA	1’b1	Enables channel 14’s diagnostics. 1’b0: Disabled 1’b1: Enabled
4	R/W	CH13DIA	1’b1	Enables channel 13’s diagnostics. 1’b0: Disabled 1’b1: Enabled
3	R/W	CH12DIA	1’b1	Enables channel 12’s diagnostics. 1’b0: Disabled 1’b1: Enabled
2	R/W	CH11DIA	1’b1	Enables channel 11’s diagnostics. 1’b0: Disabled 1’b1: Enabled
1	R/W	CH10DIA	1’b1	Enables channel 10’s diagnostics. 1’b0: Disabled 1’b1: Enabled
0	R/W	CH9DIA	1’b1	Enables channel 9’s diagnostics. 1’b0: Disabled 1’b1: Enabled

DIA1 (0Dh)

Format: Unsigned binary

The DIA1 command enables the diagnostics for channel 8 to channel 1.

Bits	Access	Bit Name	Default	Description
7	R/W	CH8DIA	1’b1	Enables channel 8’s diagnostics. 1’b0: Disabled 1’b1: Enabled
6	R/W	CH7DIA	1’b1	Enables channel 7’s diagnostics. 1’b0: Disabled 1’b1: Enabled

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5	R/W	CH6DIA	1’b1	Enables channel 6’s diagnostics. 1’b0: Disabled 1’b1: Enabled
4	R/W	CH5DIA	1’b1	Enables channel 5’s diagnostics. 1’b0: Disabled 1’b1: Enabled
3	R/W	CH4DIA	1’b1	Enables channel 4’s diagnostics. 1’b0: Disabled 1’b1: Enabled
2	R/W	CH3DIA	1’b1	Enables channel 3’s diagnostics. 1’b0: Disabled 1’b1: Enabled
1	R/W	CH2DIA	1’b1	Enables channel 2’s diagnostics. 1’b0: Disabled 1’b1: Enabled
0	R/W	CH1DIA	1’b1	Enables channel 1’s diagnostics. 1’b0: Disabled 1’b1: Enabled

ILED1 (0Eh)

Format: Unsigned hexadecimal

The ILED1 command includes channel 1’s analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED1	8’h 3f	Channel 1’s analog dimming register.

LED2 (0Fh)

Format: Unsigned hexadecimal

The ILED2 command includes channel 2’s analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED2	8’h 3f	Channel 2’s analog dimming register.

ILED3 (10h)

Format: Unsigned hexadecimal

The ILED3 command includes channel 3’s analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED3	8’h 3f	Channel 3’s analog dimming register.

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ILED4 (11h)

Format: Unsigned hexadecimal

The ILED4 command includes channel 4's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED4	8'h 3f	Channel 4's analog dimming register.

ILED5 (12h)

Format: Unsigned hexadecimal

The ILED5 command includes channel 5's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED5	8'h 3f	Channel 5's analog dimming register.

ILED6 (13h)

Format: Unsigned hexadecimal

The ILED6 command includes channel 6's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED6	8'h 3f	Channel 6's analog dimming register.

ILED7 (14h)

Format: Unsigned hexadecimal

The ILED7 command includes channel 7's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED7	8'h 3f	Channel 7's analog dimming register.

ILED8 (15h)

Format: Unsigned hexadecimal

The ILED8 command includes channel 8's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED8	8'h 3f	Channel 8's analog dimming register.

ILED9 (16h)

Format: Unsigned hexadecimal

The ILED9 command includes channel 9's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED9	8'h 3f	Channel 9's analog dimming register.

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ILED10 (17h)

Format: Unsigned hexadecimal

The ILED10 command includes channel 10's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED10	8'h 3f	Channel 10's analog dimming register.

ILED11 (18h)

Format: Unsigned hexadecimal

The ILED11 command includes channel 11's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED11	8'h 3f	Channel 11's analog dimming register.

ILED12 (19h)

Format: Unsigned hexadecimal

The ILED12 command is channel 12's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED12	8'h 3f	Channel 12's analog dimming register.

ILED13 (1Ah)

Format: Unsigned hexadecimal

The ILED13 command includes channel 13's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED13	8'h 3f	Channel 13's analog dimming register.

ILED14 (1Bh)

Format: Unsigned hexadecimal

The ILED14 command includes channel 14's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED14	8'h 3f	Channel 14's analog dimming register.

ILED15 (1Ch)

Format: Unsigned hexadecimal

The ILED15 command includes channel 15's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED15	8'h 3f	Channel 15's analog dimming register.

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ILED16 (1Dh)

Format: Unsigned hexadecimal

The ILED16 command includes channel 16's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED16	8'h 3f	Channel 16's analog dimming register.

ILED17 (1Eh)

Format: Unsigned hexadecimal

The ILED17 command includes channel 17's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED17	8'h 3f	Channel 17's analog dimming register.

ILED18 (1Fh)

Format: Unsigned hexadecimal

The ILED18 command includes channel 18's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED18	8'h 3f	Channel 18's analog dimming register.

ILED19 (20h)

Format: Unsigned hexadecimal

The ILED19 command includes channel 19's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED19	8'h 3f	Channel 19's analog dimming register.

ILED20 (21h)

Format: Unsigned hexadecimal

The ILED20 command includes channel 20's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED20	8'h 3f	Channel 20's analog dimming register.

ILED21 (22h)

Format: Unsigned hexadecimal

The ILED21 command includes channel 21's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED21	8'h 3f	The analog dimming register of channel21

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ILED22 (23h)

Format: Unsigned hexadecimal

The ILED22 command includes channel 22's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED22	8'h 3f	Channel 22's analog dimming register.

ILED23 (24h)

Format: Unsigned hexadecimal

The ILED23 command includes channel 23's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED23	8'h 3f	Channel 23's analog dimming register.

ILED24 (25h)

Format: Unsigned hexadecimal

The ILED24 command includes channel 24's analog dimming register.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	ILED24	8'h 3f	Channel 24's analog dimming register.

PWM1_L (26h)

Format: Unsigned hexadecimal

The PWM1_L command includes the 8 least significant bits (LSB) of the pulse-width modulation (PWM) dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM1	8'h ff	Channel 1's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4 most significant bits (MSB) are written.

PWM1_H (27h)

Format: Unsigned hexadecimal

The PWM1_H command includes the 4 most significant bits (MSB) of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM1	4'h f	Channel 1's PWM dimming duty register, 4MSB.

PWM2_L (28h)

Format: Unsigned hexadecimal

The PWM2_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM2	8'h ff	Channel 2's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM2_H (29h)

Format: Unsigned hexadecimal

The PWM2_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM2	4’h f	Channel 2’s PWM dimming duty register, 4MSB.

PWM3_L (2Ah)

Format: Unsigned hexadecimal

The PWM3_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM3	8’h ff	Channel 3’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM3_H (2Bh)

Format: Unsigned hexadecimal

The PWM3_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM3	4’h f	Channel 3’s PWM dimming duty register, 4MSB.

PWM4_L (2Ch)

Format: Unsigned hexadecimal

The PWM4_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM4	8’h ff	Channel 4’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM4_H (2Dh)

Format: Unsigned hexadecimal

The PWM4_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM4	4’h f	Channel 4’s PWM dimming duty register, 4MSB.

PWM5_L (2Eh)

Format: Unsigned hexadecimal

The PWM5_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM5	8’h ff	Channel 5’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM5_H (2Fh)

Format: Unsigned hexadecimal

The PWM5_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM5	4’h f	Channel 5’s PWM dimming duty register, 4MSB.

PWM6_L (30h)

Format: Unsigned hexadecimal

The PWM6_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM6	8’h ff	Channel 6’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM6_H (31h)

Format: Unsigned hexadecimal

The PWM6_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM6	4’h f	Channel 6’s PWM dimming duty register, 4MSB.

PWM7_L (32h)

Format: Unsigned hexadecimal

The PWM7_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM7	8’h ff	Channel 7’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM7_H (33h)

Format: Unsigned hexadecimal

The PWM7_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM7	4’h f	Channel 7’s PWM dimming duty register, 4MSB.

PWM8_L (34h)

Format: Unsigned hexadecimal

The PWM8_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM8	8’h ff	Channel 8’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM8_H (35h)

Format: Unsigned hexadecimal

The PWM8_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM8	4'h f	Channel 8's PWM dimming duty register, 4MSB.

PWM9_L (36h)

Format: Unsigned hexadecimal

The PWM9_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM9	8'h ff	Channel 9's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM9_H (37h)

Format: Unsigned hexadecimal

The PWM9_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM9	4'h f	Channel 9's PWM dimming duty register, 4MSB.

PWM10_L (38h)

Format: Unsigned hexadecimal

The PWM10_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM10	8'h ff	Channel 10's PWM dimming duty register, 8LSB. The dimming duty only changes when 4MSB is written.

PWM10_H (39h)

Format: Unsigned hexadecimal

The PWM10_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM10	4'h f	Channel 10's PWM dimming duty register, 4MSB.

PWM11_L (3Ah)

Format: Unsigned hexadecimal

The PWM11_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM11	8'h ff	Channel 11's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM11_H (3Bh)

Format: Unsigned hexadecimal

The PWM11_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM11	4’h f	Channel 11’s PWM dimming duty register, 4MSB.

PWM12_L (3Ch)

Format: Unsigned hexadecimal

The PWM12_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM12	8’h ff	Channel 12’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM12_H (3Dh)

Format: Unsigned hexadecimal

The PWM12_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM12	4’h f	Channel 12’s PWM dimming duty register, 4MSB.

PWM13_L (3Eh)

Format: Unsigned hexadecimal

The PWM13_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM13	8’h ff	Channel 13’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM13_H (3Fh)

Format: Unsigned hexadecimal

The PWM13_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM13	4’h f	Channel 13’S PWM dimming duty register, 4MSB.

PWM14_L (40h)

Format: Unsigned hexadecimal

The PWM14_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM14	8’h ff	Channel 14’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM14_H (41h)

Format: Unsigned hexadecimal

The PWM14_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM14	4'h f	Channel 14's PWM dimming duty register, 4MSB.

PWM15_L (42h)

Format: Unsigned hexadecimal

The PWM15_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM15	8'h ff	Channel 15's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM15_H (43h)

Format: Unsigned hexadecimal

The PWM15_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM15	4'h f	Channel 15's PWM dimming duty register, 4MSB.

PWM16_L (44h)

Format: Unsigned hexadecimal

The PWM16_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM16	8'h ff	Channel 16's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM16_H (45h)

Format: Unsigned hexadecimal

The PWM16_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM16	4'h f	Channel 16's PWM dimming duty register, 4MSB.

PWM17_L (46h)

Format: Unsigned hexadecimal

The PWM17_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM17	8'h ff	Channel 17's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM17_H (47h)

Format: Unsigned hexadecimal

The PWM17_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM17	4’h f	Channel 17’s PWM dimming duty register, 4MSB.

PWM18_L (48h)

Format: Unsigned hexadecimal

The PWM18_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM18	8’h ff	Channel 18’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM18_H (49h)

Format: Unsigned hexadecimal

The PWM18_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM18	4’h f	Channel 18’s PWM dimming duty register, 4MSB.

PWM19_L (4Ah)

Format: Unsigned hexadecimal

The PWM19_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM19	8’h ff	Channel 19’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM19_H (4Bh)

Format: Unsigned hexadecimal

The PWM19_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM19	4’h f	Channel 19’s PWM dimming duty register, 4MSB.

PWM20_L (4Ch)

Format: Unsigned hexadecimal

The PWM20_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM20	8’h ff	Channel 20’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM20_H (4Dh)

Format: Unsigned hexadecimal

The PWM20_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM20	4’h f	Channel 20’s PWM dimming duty register, 4MSB.

PWM21_L (4Eh)

Format: Unsigned hexadecimal

The PWM21_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM21	8’h ff	Channel 21’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM21_H (4Fh)

Format: Unsigned hexadecimal

The PWM21_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM21	4’h f	Channel 21’s PWM dimming duty register, 4MSB.

PWM22_L (50h)

Format: Unsigned hexadecimal

The PWM22_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM22	8’h ff	Channel 22’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM22_H (51h)

Format: Unsigned hexadecimal

The PWM22_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM22	4’h f	Channel 22’s PWM dimming duty register, 4MSB.

PWM23_L (52h)

Format: Unsigned hexadecimal

The PWM23_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM23	8’h ff	Channel 23’s PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

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PWM23_H (53h)

Format: Unsigned hexadecimal

The PWM23_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM23	4'h f	Channel 23's PWM dimming duty register, 4MSB.

PWM24_L (54h)

Format: Unsigned hexadecimal

The PWM24_L command includes the 8LSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:0	R/W	PWM24	8'h ff	Channel 24's PWM dimming duty register, 8LSB. The dimming duty only changes when the 4MSB are written.

PWM24_H (55h)

Format: Unsigned hexadecimal

The PWM24_H command includes the 4MSB of the PWM dimming duty.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	N/A	Reserved.
3:0	R/W	PWM24	4'h f	Channel 24's PWM dimming duty register, 4MSB.

FS1ILED1 (56h)

Format: Unsigned hexadecimal

The FS1ILED1 command includes the analog dimming register in failsafe mode for LED1 to LED4.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS1ILED1	6'h 3f	The LED current analog dimming register in failsafe mode. These bits control four LED channels: LED1 to LED4.

FS1ILED2 (57h)

Format: Unsigned hexadecimal

The FS1ILED2 command includes the analog dimming register in failsafe mode for LED5 to LED8.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS1ILED2	6'h 3f	The LED current analog dimming register in failsafe mode. These bits control four LED channels: LED5 to LED8.

FS1ILED3 (58h)

Format: Unsigned hexadecimal

The FS1ILED3 command includes the analog dimming register in failsafe mode for LED9 to LED12.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS1ILED3	6'h 3f	The LED current analog dimming register in failsafe mode. These bits control four LED channels: LED9 to LED12.

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FS1ILED4 (59h)

Format: Unsigned hexadecimal

The FS1ILED4 command includes the analog dimming register in failsafe mode for LED13 to LED16.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS1ILED4	6'h 3f	The LED current analog dimming register in failsafe mode. These bits control four LED channels: LED13 to LED16.

FS1ILED5 (5Ah)

Format: Unsigned hexadecimal

The FS1ILED5 command includes the analog dimming register in failsafe mode for LED17 to LED20.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS1ILED5	6'h 3f	The LED current analog dimming register in failsafe mode. These bits control four LED channels: LED17 to LED20.

FS1ILED6 (5Bh)

Format: Unsigned hexadecimal

The FS1ILED6 command includes the analog dimming register in failsafe mode for LED21 to LED14.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS1ILED6	6'h 3f	The LED current analog dimming register in failsafe mode. These bits control four LED channels: LED21 to LED14.

FS1PWM1 (5Ch)

Format: Unsigned hexadecimal

The FS1PWM1 command includes the PWM dimming register in failsafe mode for LED1 to LED4.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS1PWM1	8'h ff	The LED current PWM dimming register in failsafe mode, only for the 8MSB. These bits control four LED channels: LED1 to LED4.

FS1PWM2 (5Dh)

Format: Unsigned hexadecimal

The FS1PWM2 command includes the PWM dimming register in failsafe mode for LED5 to LED8.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS1PWM2	8'h ff	The LED current PWM dimming register in failsafe mode, only for the 8MSB. These bits control four LED channels: LED5 to LED8.

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FS1PWM3 (5Eh)

Format: Unsigned hexadecimal

The FS1PWM3 command includes the PWM dimming register in failsafe mode for LED9 to LED12.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS1PWM3	8'h ff	The LED current PWM dimming register in failsafe mode, only for the 8MSB. These bits control four LED channels: LED9 to LED12.

FS1PWM4 (5Fh)

Format: Unsigned hexadecimal

The FS1PWM4 command includes the PWM dimming register in failsafe mode for LED13 to LED16.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS1PWM4	8'h ff	The LED current PWM dimming register in failsafe mode, only for the 8MSB. These bits control four LED channels: LED13 to LED16.

FS1PWM5 (60h)

Format: Unsigned hexadecimal

The FS1PWM5 command includes the PWM dimming register in failsafe mode for LED17 to LED20.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS1PWM5	8'h ff	The LED current PWM dimming register in failsafe mode, only for the 8MSB. These bits control four LED channels: LED17 to LED20.

FS1PWM6 (61h)

Format: Unsigned hexadecimal

The FS1PWM6 command includes the PWM dimming register in failsafe mode for LED21 to LED24.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS1PWM6	8'h ff	The LED current PWM dimming register in failsafe mode, only for the 8MSB. These bits control four LED channels: LED21 to LED24.

FS2ILED1 (62h)

Format: Unsigned hexadecimal

The FS2ILED1 command includes the analog dimming register in FS mode for LED1 to LED4.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS2ILED1	6'h 3f	The LED current analog dimming register in FS mode. These bits control four LED channels: LED1 to LED4.

FS2ILED2 (63h)

Format: Unsigned hexadecimal

The FS2ILED2 command includes the analog dimming register in FS mode for LED5 to LED8.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS2ILED2	6'h 3f	The LED current analog dimming register in FS mode. These bits control four LED channels: LED5 to LED8.

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FS2ILED3 (64h)

Format: Unsigned hexadecimal

The FS2ILED3 command includes the analog dimming register in FS mode for LED9 to LED12.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS2ILED3	6'h 3f	The LED current analog dimming register in FS mode. These bits control four LED channels: LED9 to LED12.

FS2ILED4 (65h)

Format: Unsigned hexadecimal

The FS2ILED4 command includes the analog dimming register in FS mode for LED13 to LED16.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS2ILED4	6'h 3f	The LED current analog dimming register in FS mode. These bits control four LED channels: LED13 to LED16.

FS2ILED5 (66h)

Format: Unsigned hexadecimal

The FS2ILED5 command includes the analog dimming register in FS mode for LED17 to LED20.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS2ILED5	6'h 3f	The LED current analog dimming register in FS mode. These bits control four LED channels: LED17 to LED20.

FS2ILED6 (67h)

Format: Unsigned hexadecimal

The FS2ILED6 command includes the analog dimming register in FS mode for LED21 to LED24.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5:0	R/W	FS2ILED6	6'h 3f	The LED current analog dimming register in FS mode. These bits control four LED channels: LED21 to LED24.

FS2PWM1 (68h)

Format: Unsigned hexadecimal

The FS2PWM1 command includes the PWM dimming register in FS mode for LED1 to LED4.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS2PWM1	8'h ff	The LED current PWM dimming register in FS mode, only for the 8MSB. These bits control four LED channels: LED1 to LED4.

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FS2PWM2 (69h)

Format: Unsigned hexadecimal

The FS2PWM2 command includes the PWM dimming register in FS mode for LED5 to LED8.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS2PWM2	8'h ff	The LED current PWM dimming register in FS mode, only for the 8MSB. These bits control four LED channels: LED5 to LED8.

FS2PWM3 (6Ah)

Format: Unsigned hexadecimal

The FS2PWM3 command includes the PWM dimming register in FS mode for LED9 to LED12.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS2PWM3	8'h ff	The LED current PWM dimming register in FS mode, only for the 8MSB. These bits control four LED channels: LED9 to LED12.

FS2PWM4 (6Bh)

Format: Unsigned hexadecimal

The FS2PWM4 command includes the PWM dimming register in FS mode for LED13 to LED16.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS2PWM4	8'h ff	The LED current PWM dimming register in FS mode, only for the 8MSB. These bits control four LED channels: LED13 to LED16.

FS2PWM5 (6Ch)

Format: Unsigned hexadecimal

The FS2PWM5 command includes the PWM dimming register in FS mode for LED17 to LED20.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS2PWM5	8'h ff	The LED current PWM dimming register in FS mode, only for the 8MSB. These bits control four LED channels: LED17 to LED20.

FS2PWM6 (6Dh)

Format: Unsigned hexadecimal

The FS2PWM6 command includes the PWM dimming register in FS mode for LED21 to LED24.

Bits	Access	Bit Name	Default	Description
7:0	R/W	FS2PWM6	8'h ff	The LED current PWM dimming register in FS mode, only for the 8MSB. These bits control four LED channels: LED21 to LED24.

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FO3 (6Eh)

Format: Unsigned binary

The FO3 command includes the open protection fault flag for channel 24 to channel 17. If the fault is removed in hiccup mode, then write 1 to reset the fault bit to 0.

Bits	Access	Bit Name	Default	Description
7	R/W	CH24O	1'b0	Channel 24's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
6	R/W	CH23O	1'b0	Channel 23's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
5	R/W	CH22O	1'b0	Channel 22's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
4	R/W	CH21O	1'b0	Channel 21's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
3	R/W	CH20O	1'b0	Channel 20's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
2	R/W	CH19O	1'b0	Channel 19's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
1	R/W	CH18O	1'b0	Channel 18's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
0	R/W	CH17O	1'b0	Channel 17's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs

FO2 (6Fh)

Format: Unsigned binary

The FO2 command includes the open protection fault flag for channel 16 to channel 9. If the fault is removed in hiccup mode, then write 1 to reset the fault bit to 0.

Bits	Access	Bit Name	Default	Description
7	R/W	CH16O	1'b0	Channel 16's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
6	R/W	CH15O	1'b0	Channel 15's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
5	R/W	CH14O	1'b0	Channel 14's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs

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4	R/W	CH13O	1'b0	Channel 13's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
3	R/W	CH12O	1'b0	Channel 12's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
2	R/W	CH11O	1'b0	Channel 11's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
1	R/W	CH10O	1'b0	Channel 10's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
0	R/W	CH9O	1'b0	Channel 9's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs

FO1 (70h)

Format: Unsigned binary

The FO1 command includes the open protection fault flag for channel 8 to channel 1. If the fault is removed in hiccup mode, then write 1 to reset the fault bit to 0.

Bits	Access	Bit Name	Default	Description
7	R/W	CH8O	1'b0	Channel 8's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
6	R/W	CH7O	1'b0	Channel 7's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
5	R/W	CH6O	1'b0	Channel 6's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
4	R/W	CH5O	1'b0	Channel 5's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
3	R/W	CH4O	1'b0	Channel 4's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
2	R/W	CH3O	1'b0	Channel 3's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
1	R/W	CH2O	1'b0	Channel 2's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
0	R/W	CH1O	1'b0	Channel 1's open protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs

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FS3 (71h)

Format: Unsigned binary

The FO3 command includes the short protection fault flag for channel 24 to channel 17. If the fault is removed in hiccup mode, then write 1 to reset the fault bit to 0.

Bits	Access	Bit Name	Default	Description
7	R/W	CH24S	1'b0	Channel 24's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
6	R/W	CH23S	1'b0	Channel 23's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
5	R/W	CH22S	1'b0	Channel 22's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
4	R/W	CH21S	1'b0	Channel 21's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
3	R/W	CH20S	1'b0	Channel 20's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
2	R/W	CH19S	1'b0	Channel 19's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
1	R/W	CH18S	1'b0	Channel 18's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
0	R/W	CH17S	1'b0	Channel 17's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs

FS2 (72h)

Format: Unsigned binary

The FS2 command includes the short protection fault flag for channel 16 to channel 9. If the fault is removed in hiccup mode, then write 1 to reset the fault bit to 0.

Bits	Access	Bit Name	Default	Description
7	R/W	CH16S	1'b0	Channel 16's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs
6	R/W	CH15S	1'b0	Channel 15's short protection fault flag. 1'b0: No fault 1'b1: A fault occurs
5	R/W	CH14S	1'b0	Channel 14's short protection fault flag. 1'b0: There is no fault 1'b1: A fault occurs

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4	R/W	CH13S	1’b0	Channel 13’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
3	R/W	CH12S	1’b0	Channel 12’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
2	R/W	CH11S	1’b0	Channel 11’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
1	R/W	CH10S	1’b0	Channel 10’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
0	R/W	CH9S	1’b0	Channel 9’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs

FS1 (73h)

Format: Unsigned binary

The FS1 command includes the short protection fault flag for channel 8 to channel 1. If the fault is removed in hiccup mode, then write 1 to reset the fault bit to 0.

Bits	Access	Bit Name	Default	Description
7	R/W	CH8S	1’b0	Channel 8’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
6	R/W	CH7S	1’b0	Channel 7’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
5	R/W	CH6S	1’b0	Channel 6’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
4	R/W	CH5S	1’b0	Channel 5’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
3	R/W	CH4S	1’b0	Channel 4’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
2	R/W	CH3S	1’b0	Channel 3’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
1	R/W	CH2S	1’b0	Channel 2’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs
0	R/W	CH1S	1’b0	Channel 1’s short protection fault flag. 1’b0: There is no fault 1’b1: A fault occurs

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FSS (74h)

Format: Unsigned binary

The FSS command includes several fault flags.

Bits	Access	Bit Name	Default	Description
7	R/W	FT_VINLV	1'b0	This bit is set if V_{IN} is below 7 x FBOS (09h, bits[7:0]), and the EN_VIN_LV bit (77h, bit[4]) is set to 1. 1'b0: There is no fault 1'b1: A fault occurs If V_{IN} exceeds 7 x FBOS again, then write 1 to reset this bit to 0.
6	R/W	FT_OV	1'b0	This bit is set if V_{IN} reaches the over-voltage protection (OVP) threshold. If a fault occurs, then this bit remains set to 1. 1'b0: There is no fault 1'b1: A fault occurs If V_{IN} is below the OVP threshold, then write 1 to reset this bit to 0.
5	R/W	CH_S	1'b0	This bit is set if any channel triggers short LED protection. If a fault occurs, then this bit remains set to 1. 1'b0: There is no fault 1'b1: A fault occurs If the fault is removed in hiccup mode, then write 1 to reset this bit to 0.
4	R/W	CH_O	1'b0	This bit is set if any channel triggers open LED protection. If a fault occurs, then this bit remains set to 1. 1'b0: There is no fault 1'b1: A fault occurs If the fault is removed in hiccup mode, then write 1 to reset this bit to 0.
3	R/W	FT_FS	1'b0	This bit is set when entering failsafe mode. If a fault occurs, then this bit remains set to 1. 1'b0: There is no fault 1'b1: A fault occurs When exiting failsafe mode, write 1 to reset this bit to 0.
2	R/W	FT_ISET	1'b0	Indicates ISET pin open/short fault. If a fault occurs, then this bit remains set to 1. 1'b0: There is no fault 1'b1: A fault occurs This bit is reset if the power resets.
1	R/W	FT_OTW	1'b0	Indicates over-temperature warning (OTW). If a fault occurs, then this bit remains set to 1. 1'b0: There is no fault 1'b1: A fault occurs If the fault is removed, then write 1 to reset this bit to 0.

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0	R/W	FT_OTP	1’b0	Indicates an over-temperature protection fault. If a fault occurs, then this bit remains set to 1. 1’b0: There is no fault 1’b1: A fault occurs If the fault is removed, then write 1 to reset this bit to 0.

T_IC (75h)

Format: Unsigned binary

The T_IC command reads the status of the internal status bits (FB_UP and FB_DOWN), as well as the IC temperature.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	N/A	Reserved.
5	R	FB_UP	1’b0	If V_{IN} must decrease, then this bit is set to 1 by the MPQ3322. If this bit and bit[4] of this command are set to 0, then V_{IN} maintains the same value.
4	R	FB_DOWN	1’b0	If V_{IN} must increase, then this bit is set to 1 by the MPQ3322.
3:0	R	ICTR_FULL3:0	4’b0000	These bits read the IC temperature and refresh every 10ms. 4’b 0000: Below 80°C 4’b 0001: Between 80°C and 90°C 4’b 0010: Between 90°C and 100°C 4’b 0011: Between 100°C and 110°C 4’b 0100: Between 110°C and 120°C 4’b 0101: Between 120°C and 130°C 4’b 0110: Between 130°C and 140°C 4’b 0111: Between 140°C and 150°C 4’b 1000: Between 150°C and 160°C 4’b 1001: Between 160°C and 170°C 4’b 1010: Exceeds 170°C

DEV_ID (76h)

Format: Unsigned hexadecimal

The ID command reads the device’s ID.

Bits	Access	Bit Name	Default	Description
7:0	R	ID	8’h 22	Reads the device’s ID.

EN4 (77h)

Format: Unsigned binary

The FSS command includes several fault flags.

Bits	Access	Bit Name	Default	Description
7:5	R	RESERVED	N/A	Reserved.
4	R/W	EN_VIN_LV	1’b0	Enables VIN low voltage detection (where V_{IN} is below 6 x FBOS (09h, bits[7:0]). 1’b0: Disabled 1’b1: Enabled
3	R/W	EN_FB_INIT	1’b0	If an open/short protection is triggered, then reset the FBO voltage to the FBOS value. 1’b0: Disabled 1’b1: Enabled

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2	R/W	EN_DIMOL	1'b1	If the dimming off time is ≤1μs, then the output duty is 100%. 1'b0: Disabled 1'b1: Enabled
1	R/W	EN_ISETS	1'b1	Enables the ISET pin short protection. 1'b0: Disabled 1'b1: Enabled
0	R/W	EN_ISETO	1'b1	Enables the ISET pin open protection. 1'b0: Disabled 1'b1: Enabled

PCF (80h)

Format: Unsigned hexadecimal

The PCF command includes the passcode that is required before writing to the failsafe registers.

Bits	Access	Bit Name	Default	Description
7:0	W	PWFS	8'h 00	Provides the passcode to change the registers of 0x56~0x6D. The write sequence is as follows: 0x5B→0x82→0xEA→0x8E, then write 0x56~0x6D.

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APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is important to achieve reliable operation, good EMI performance, and excellent thermal performance. For the best result, refer to Figure 19 and follow the guidelines below:

1. Place the feedback resistors close to the DC/DC converter. This ensures that the trace connected to the DC/DC converter's FB pin is as short as possible if the AFC is used.
2. Place the capacitors as close to the input as possible.
3. For the CAN-based differential interface, maintain the differential pair (CANH and CANL) as a tightly coupled pair. Ensure that the two traces run parallel to each other, with consistent spacing along their entire length.
4. A larger ground copper area typically improves performance and thermal dissipation.

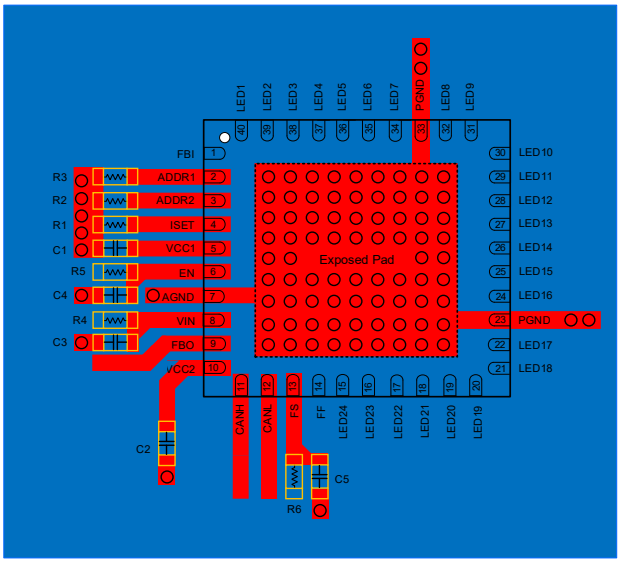

Figure 19: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

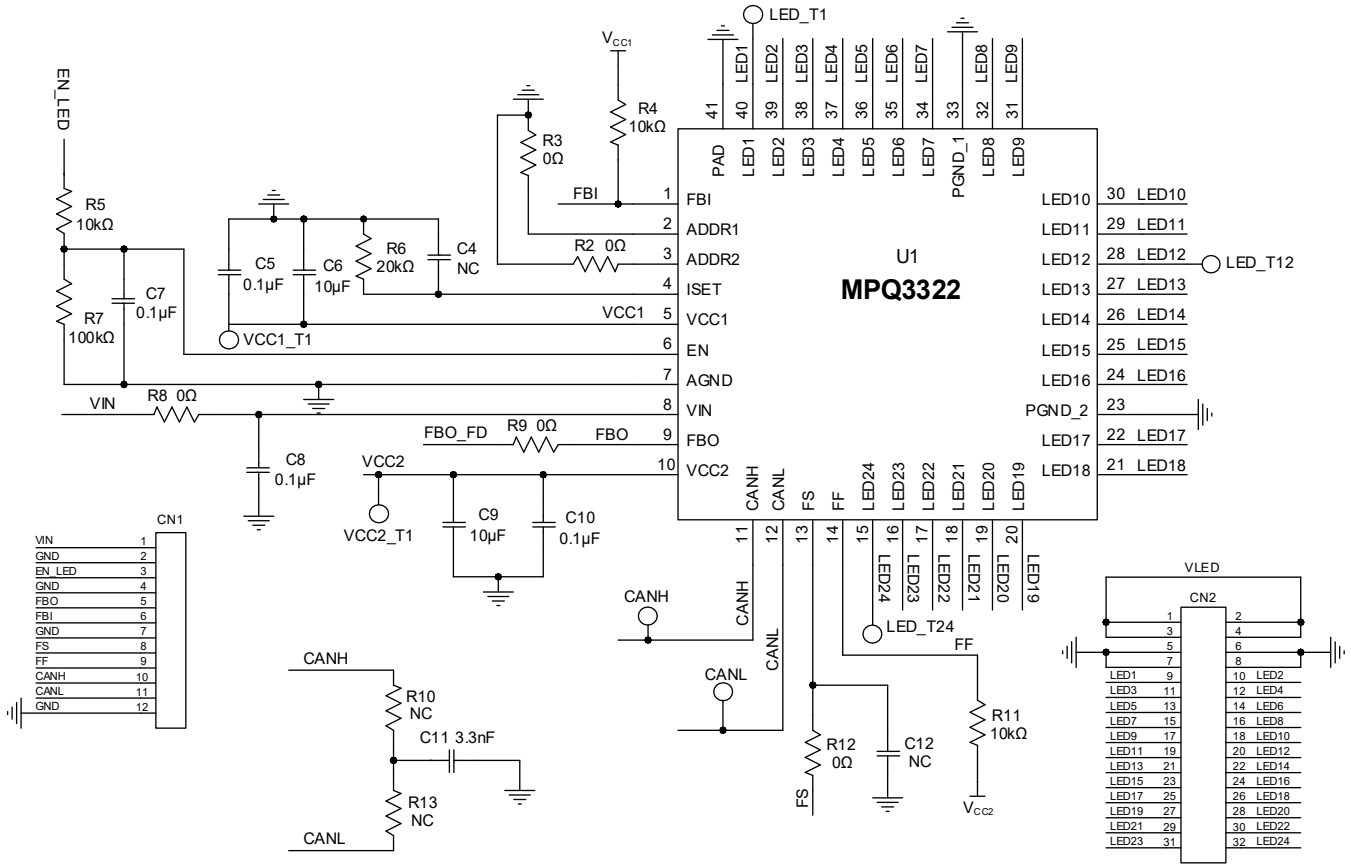

Figure 20: Typical Application Circuit

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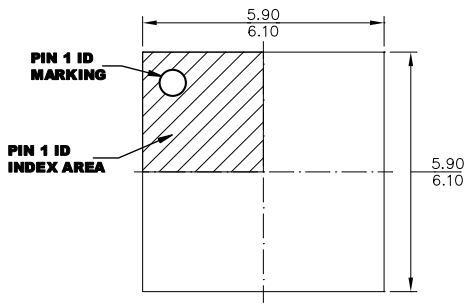
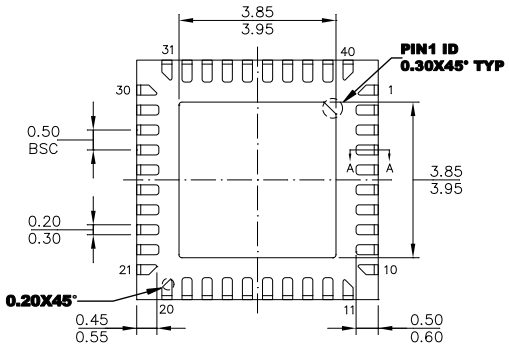
PACKAGE INFORMATION

QFN-40 (6mmx6mm) WF

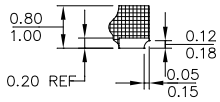


TOP VIEW

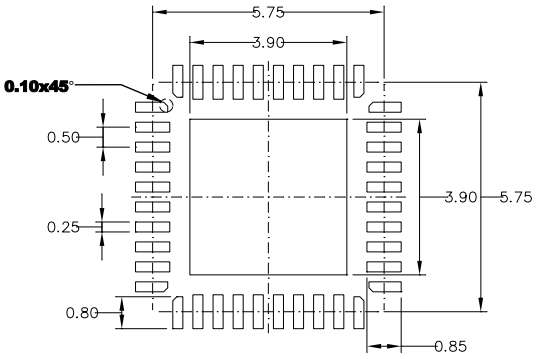


BOTTOM VIEW

SIDE VIEW



SECTION A-A



RECOMMENDED LAN PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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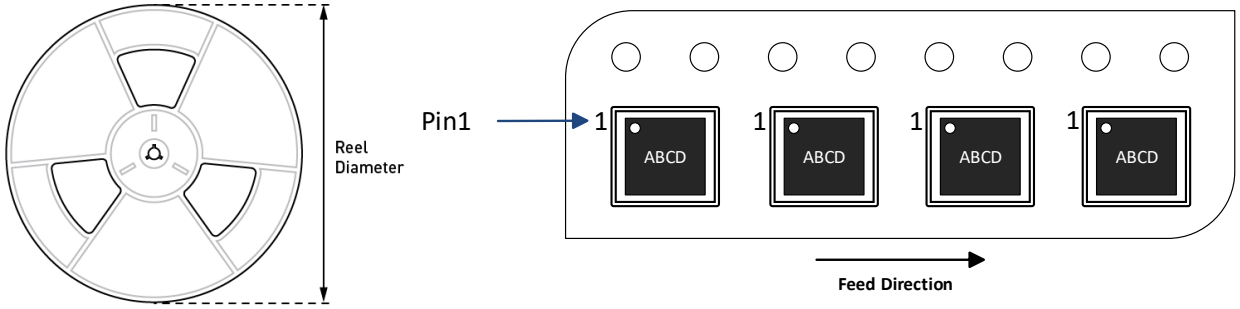
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3322GQKE-xxxx-AEC1-Z	QFN-40 (6mmx 6mm) WF	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/23/2025	Initial Release	-

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