MPQ3321

48-Channel, Max 80mA/Ch, Current Source LED Driver with Independent Analog and PWM Dimming, AEC-Q100 Qualified

DESCRIPTION

The MPQ3321 is a 48-channel LED driver with a 22V voltage rating and maximum 80mA current sources. It is designed to drive the LED arrays for local dimming backlighting in automotive LCD panels.

The MPQ3321 employs low headroom to regulate the LED current (I_{LEDx}, where x = 1–48). The adaptive voltage feedback function optimizes the LED voltage (V_{LEDx}, where x = 1–48), which achieves higher system efficiency.

The MPQ3321 supports independent 16-bit pulse-width modulation (PWM) and 7-bit analog dimming for each channel via the serial interface.

The configurable internal registers provide reliable and flexible application. The 25MHz serial interface clock guarantees a high data transfer rate for multiple devices operating in a daisy chain application.

Robust protections are included to guarantee safe operation of the device. Protection modes include LED open protection, LED short protection, and over-temperature protection (OTP). All fault statuses can be read through the serial interface.

The MPQ3321 is available in a QFN-68 (8mmx8mm) package, and it is available in AEC-Q100 Grade 0.

FEATURES

- Internal 48 Channels with Max 80mA per Channel
- 20V Voltage Rating
- Low Dropout Voltage (250mV at 30mA)
- Independent 16-Bit Pulse-Width Modulation (PWM) Dimming
- Independent 7-Bit Analog Dimming
- Adaptive Voltage Feedback Function
- 25MHz Serial Interface
- Supports Daisy Chain for Multiple ICs
- Improves EMI with LED Current (I_{LEDx}, where x = 1–48) Slew Rate and Phase Shift
- LED Short Protection
- LED Open Protection
- Fault Status Indicator Register
- Available in a QFN-68 (8mmx8mm) Package
- Available in AEC-Q100 Grade 0

APPLICATIONS

- Automotive Cluster LCDs
- Automotive Center Information LCDs
- General Mini LED LCDs

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TYPICAL APPLICATION

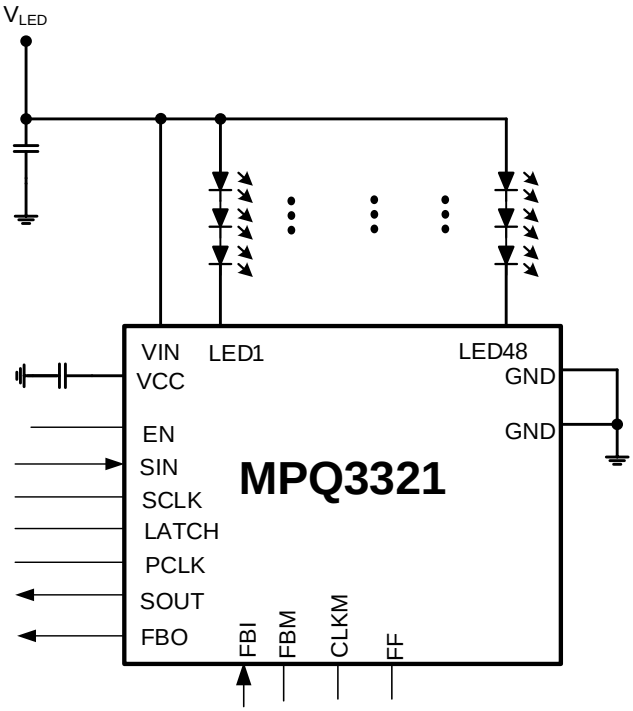

Figure 1: Typical Application

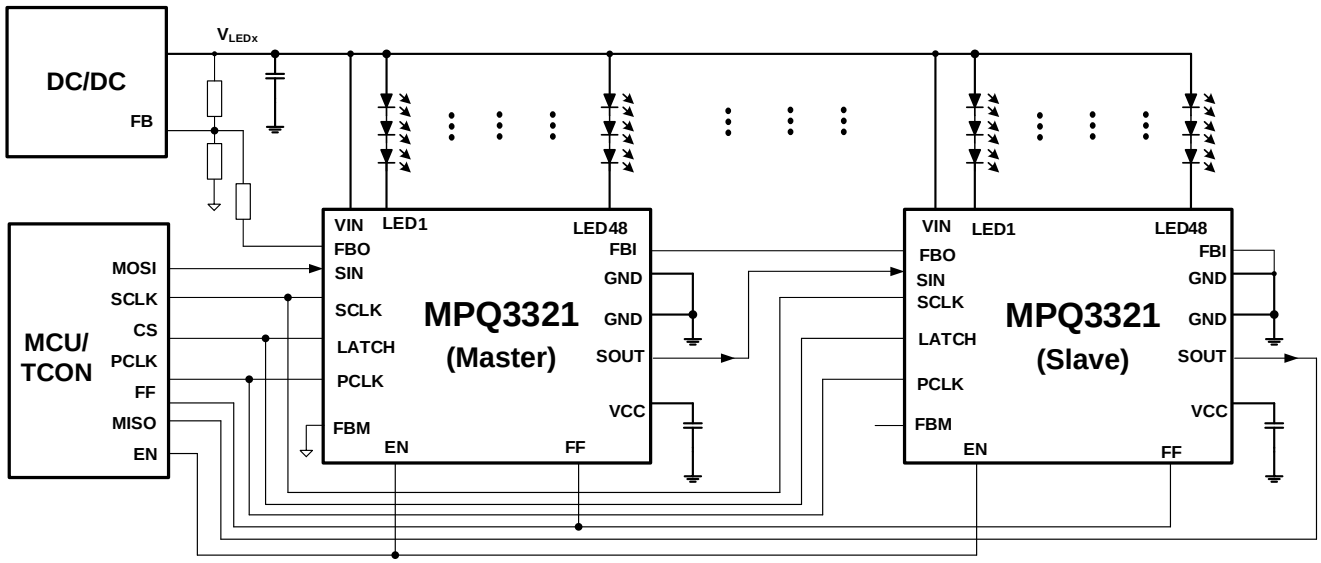

Figure 2: Typical Application (Multiple ICs in a Daisy Chain Application)

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3321GQQE-AEC1*	QFN-68 (8mmx8mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ3321GQQE-AEC1-Z).

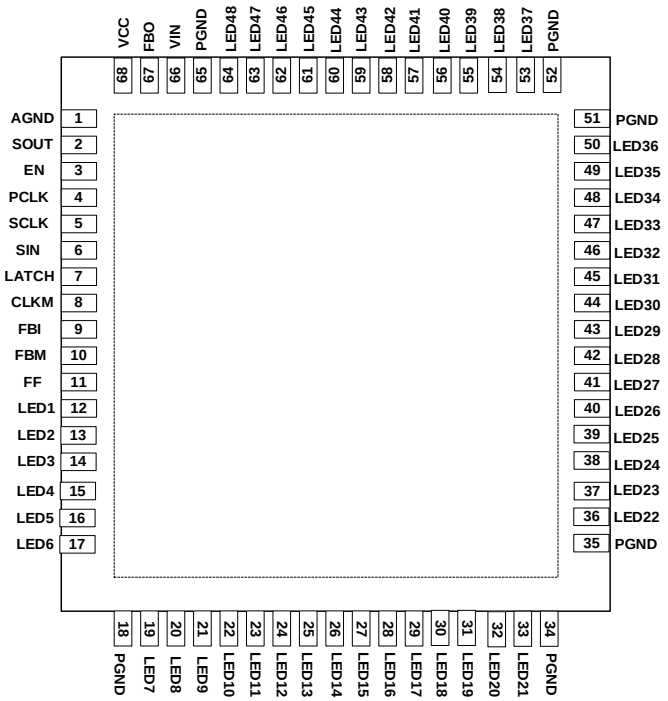
TOP MARKING

MPSYYWW
MP3321
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP3321: Part number
LLLLLLLLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE

TOP VIEW



QFN-68 (8mmx8mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog ground.**
2	SOUT	**Serial interface data output pin.**
3	EN	**Enable pin.** Pull EN to a high level to enable the IC; pull EN to a low level to disable the IC.
4	PCLK	**External PWM dimming clock input pin.**
5	SCLK	**Serial interface clock pin.**
6	SIN	**Serial interface data input pin.**
7	LATCH	**Internal register data load latch pin.**
8	CLKM	**PWM dimming clock mode select.** The CLKM pin outputs a 30μA current when IC starts up. Connect a resistor from CLKM to GND to determine the CLKM pin's voltage. The internal PWM dimming clock (IPCLK) is used when CLKM < 1.5V. • When CLKM < 0.5V, IPCLK is 5MHz. • When 0.5V < CLKM < 1V, IPCLK is 10MHz. • When 1V < CLKM < 1.5V, IPCLK is 20MHz. The external PCLK pin's clock is used when CLKM > 1.5V, or when the CLKM pin is floating.
9	FBI	**Feedback input pin.** The FBI pin is the input pin for the LEDx pin's voltage regulation information when multiple ICs are cascaded. Connect the pin to AGND if it not used.
10	FBM	**Feedback (master/slave) mode.** Float this pin for slave mode. Connect this pin to AGND for master mode.
11	FF	**Fault flag.** The FF pin is an open-drain circuit for a fault flag.
12, 13, 14, 15, 16, 17, 19–33, 36–50, 53–64	LED1~48	**LED string 1–48 current input pin.** Connect the cathodes of LED strings 1–48 to the respective LEDx pin.
18, 34, 35, 51, 52, 65	PGND	**Power ground.**
66	VIN	**Input voltage pin.** Connect an input capacitor to the VIN pin.
67	FBO	**Feedback output pin.** The FBO pin has two functions, described below: • If FBM is floating, the FBO pin is the output pin for the LEDx pin's voltage regulation information when multiple MPQ3321 devices are used. • If FBM is connected to AGND, the FBO pin is used to regulate the DC/DC converter through a resistor divider network.
68	VCC	**LDO output pin.** Connect a capacitor to the VCC pin. VCC powers the IC.
	EP	**Exposed pad.** Connect the exposed pad to PGND and AGND.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, V_{FBO} .....-0.3V to +22V
$V_{LED1–48}$ .....-0.3V to +22V
All other pins .....-0.3V to +5V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-68 (8mmx8mm) 5.55W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 20V
V_{EN}, V_{VCC}, V_{FF}, V_{PCLK}, V_{CLKM}.....0V to 3.6V
V_{SIN}, V_{SCLK}, V_{LATCH}, V_{SOUT}.....0V to 3.6V
V_{FBI}, V_{FBM}.....0V to 3.6V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-68 (8mmx8mm)……22.5…….3....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
Input voltage range	V_{IN}		3		20	V
Supply current (quiescent)	I_Q	I_{LED} = 30mA			24	mA
Supply current (shutdown)	I_{ST}	V_{IN} = 20V			2	μA
Input under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Rising edge	2.7	2.85	3	V
		Falling edge	2.5	2.65	2.8	V
VCC voltage	V_{CC}	V_{IN} > 3.5V		3.3		V
EN rising threshold	V_{EN_ON}	EN rising	1.7			V
EN falling threshold	V_{EN_OFF}	EN falling			0.8	V
EN pull-down resistor	R_{EN}	V_{EN} = 1V		1		MΩ
LED Regulator						
LED current	I_{LED}	I_{LED} = 30mA, T_J = 25°C	-5%	30	+5%	mA
		I_{LED} = 30mA, T_J = -40°C to +150°C	-8.7%	30	+8.7%	mA
		I_{LED} = 7.5mA, T_J = 25°C	-6%	7.5	+6%	mA
I_{LED} matching (5)		I_{LED} = 30mA	-3%		+3%	
Current sink headroom	V_{LEDx}	I_{LED} = 30mA		250	350	mV
		I_{LED} = 80mA		500	800	mV
FBI and FBO						
FBI voltage	V_{FBI}	Low threshold			0.6	V
		High threshold	1.3			V
FBO output voltage	V_{FBO}	FBM pin floating – Low threshold		0.3		V
		FBM pin floating – Mid threshold		0.9		V
		FBM pin floating – High threshold		1.5		V
FBO regulation voltage	V_{RFBO}	FBM pin = low, IFBO[8:0] = 0B2h, FBO output current = ±0.5mA	-5%	1.198	+5%	V
Protection						
Short LED string protection threshold	V_{SLP}	VSLP = 0b (configurable)	2	2.5	3	V
Short LED string protection time	t_{SLP}	V_{LEDx} > V_{SLP}		4		ms
Open LED string protection threshold	V_{LED_UV}			80	120	mV
Open LED string protection time	t_{LEDO}	V_{LEDx} < 80mV		4		ms
FF pull-down resistor				4.5		Ω
Thermal shutdown threshold	T_{ST}			170		°C
Thermal shutdown hysteresis	T_{ST_HYS}			20		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +150°C, typical value is at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Serial Interface						
Input logic low	V_{IL}		0		0.7	V
Input logic high	V_{IH}		1.5			V
SOUT rising time (6)	t_{SOUTR}			3	5	ns
SOUT falling time (6)	t_{SOUTF}			2.2	4	ns
SCLK frequency (6)	f_{SCLK}				25	MHz
PCLK frequency (6)	f_{PCLK}				30	MHz
SCLK high level time (6)	t_{SCLKH}		10			ns
SCLK low level time (6)	t_{SCLKL}		20			ns
PCLK high level time (6)	t_{PCLKH}		10			ns
PCLK low level time (6)	t_{PCLKL}		10			ns
LATCH high level time (6)	t_{LATH}		4			PCLK
Set-up time (6)	t_{SUSS}	SIN to SCLK rising edge	2			ns
	t_{SULS1}	LATCH falling edge to SCLK rising edge (RFRESH = 0)	1			SCLK
	t_{SULS2}	LATCH falling edge to SCLK rising edge (RFRESH = 1)	65539			PCLK
Update time (6)	t_{UTLD1}	LATCH rising edge to duty data update (RFRESH = 0)	2		3	PCLK
	t_{UTLD2}	LATCH rising edge to duty data update (RFRESH = 1, 16-bit)			65536	PCLK
	t_{UTLC}	LATCH rising edge to control data update	2		3	PCLK
Hold time (6)	t_{HOSS}	SCLK rising edge to SIN	2			ns
	t_{HOSL}	SCLK rising edge to LATCH rising edge	1			SCLK
Transmission delay (6)	t_{TDSS}	SCLK falling edge to SOUT		10	18	ns
	t_{TDPL}	PCLK to LED current rising, LED current = 30mA		100		ns
Output LED current error (6)	t_{ERR}	The difference between the time of a given PCLK count and the actual LED current on time, LED current = 30mA		100		ns

Notes:

5) Matching is defined as the difference of the maximum to minimum current divided by 2 times the average current.
6) Derived from bench characterization. Not tested in production.

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TIMING DIAGRAMS

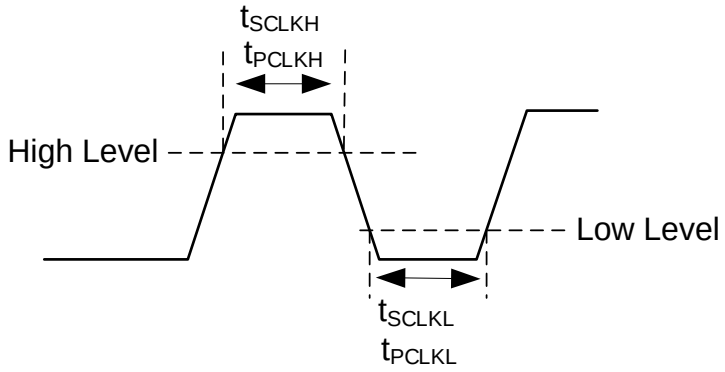

Figure 3: Timing Diagram for SCLK and PCLK

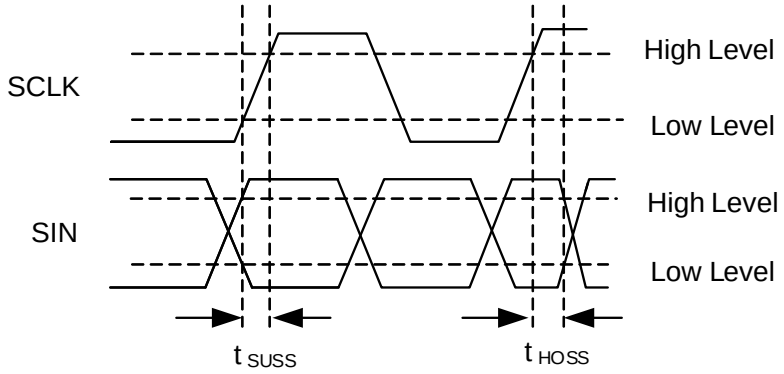

Figure 4: Timing Diagram for SCLK and SIN

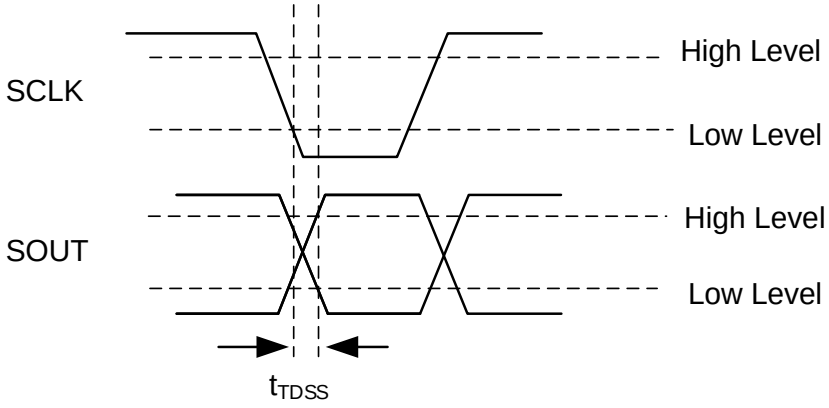

Figure 5: Timing Diagram for SCLK and SOUT

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TIMING DIAGRAMS *(continued)*

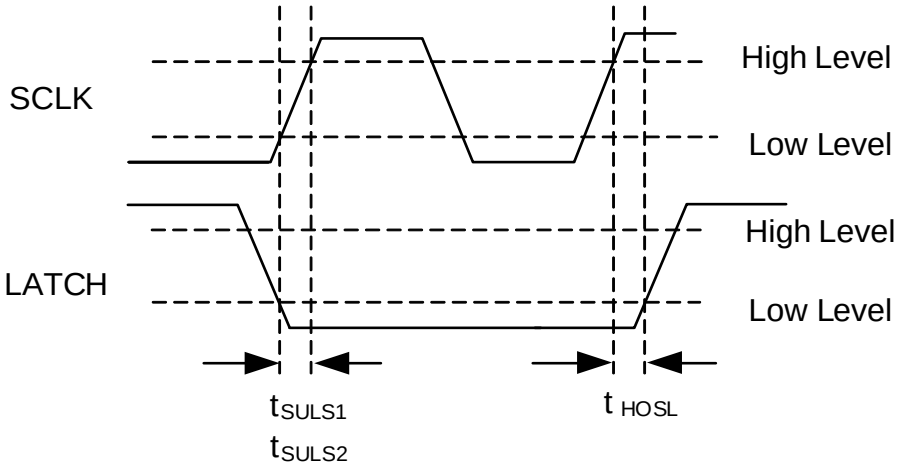

Figure 6: Timing Diagram for SCLK and LATCH

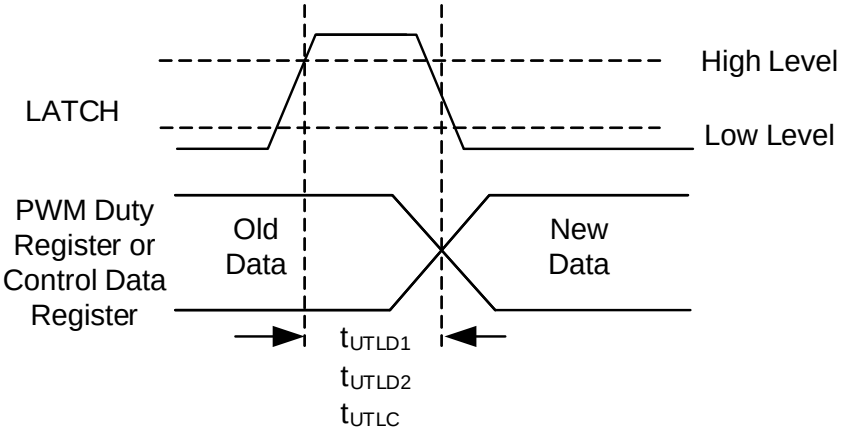

Figure 7: Timing Diagram for LATCH and PWM Duty Register or Control Data Register Update

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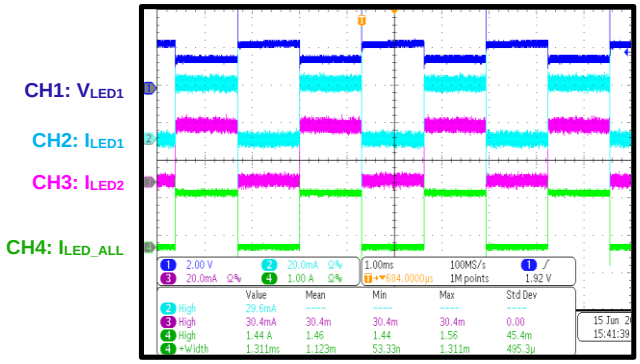
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 4V, f_{PCLK} = 25MHz, PDB = 16-bit, I_{MAX} = 30mA/ch, LED = 48P1S, T_A = 25°C, unless otherwise noted.

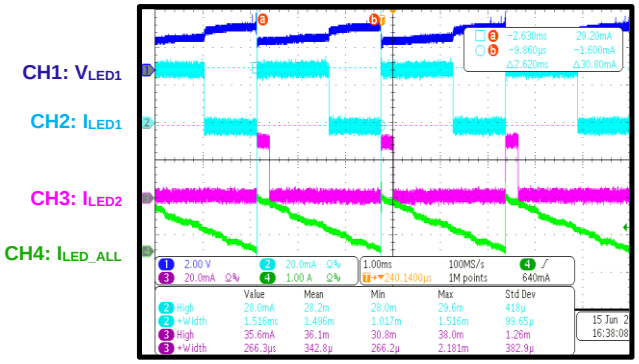
PWM Dimming

PWM duty cycle = 50% for each channel



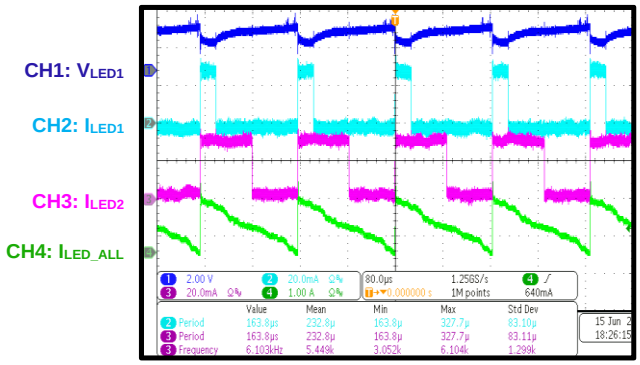
PWM Dimming

Random duty cycle for each channel



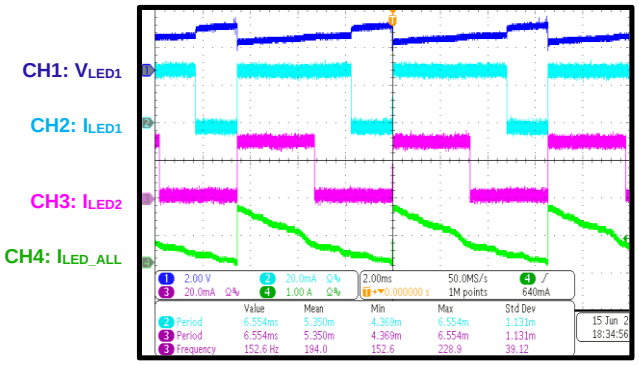
PWM Dimming

PDB = 12-bit, random duty cycle for each channel



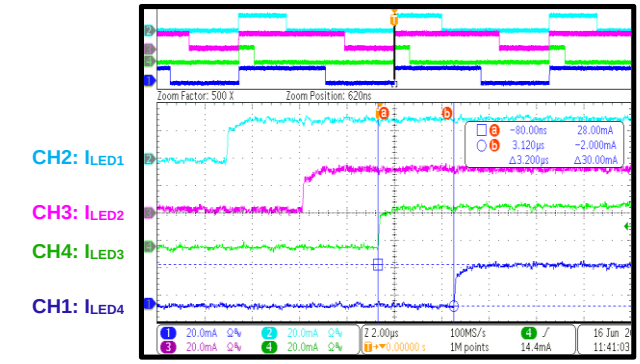
PWM Dimming

f_{PCLK} = 10MHz, random duty cycle for each channel



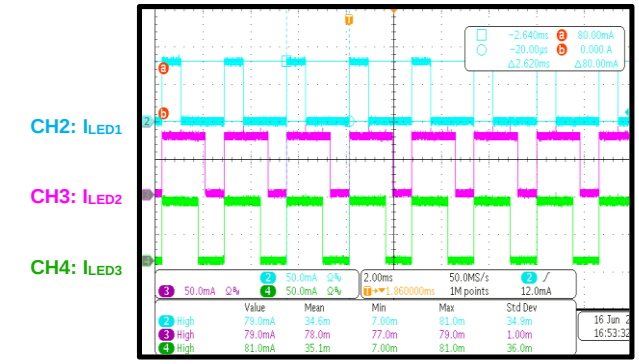
PWM Dimming

f_{PCLK} = 20MHz, phase shift = 64PCLK, time delay = 3.2µs



Analog Dimming

I_{MAX} = 80mA/ch, I_{LED} = 100% for each channel



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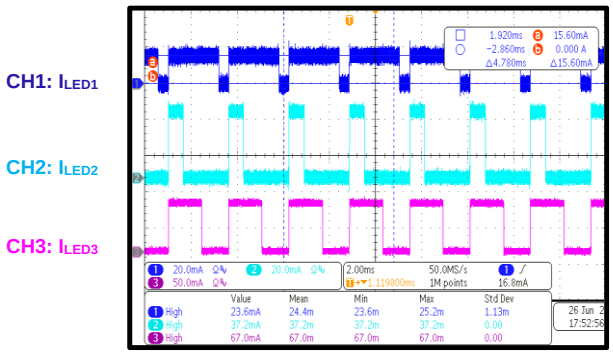
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4V, f_{PCLK} = 25MHz, PDB = 16-bit, I_{MAX} = 30mA/ch, LED = 48P1S, T_A = 25°C, unless otherwise noted.

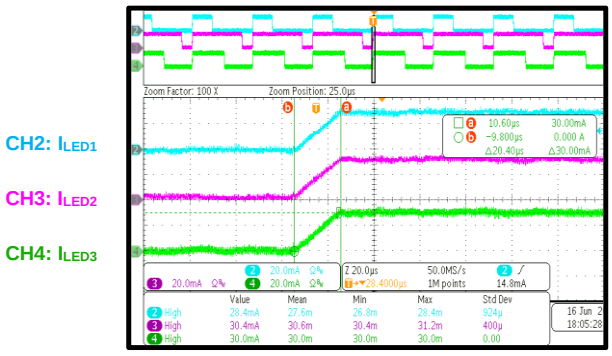
Analog Dimming

I_{MAX} = 80mA/ch, random I_{LED} for each channel



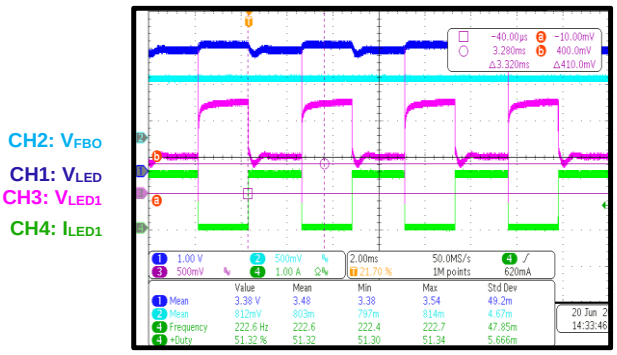
Analog Dimming

Slew rate = 4PCLK/step



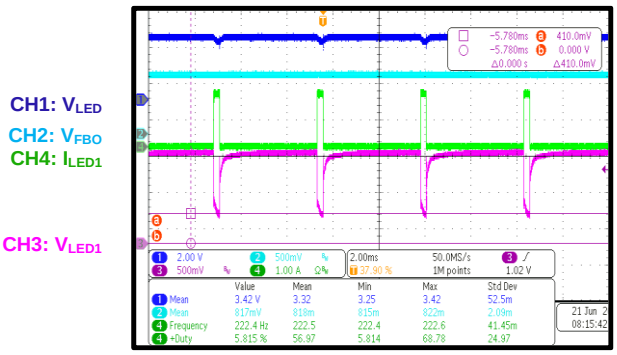
Adaptive Feedback Control (AFC)

Headroom = 300mV and hysteresis = 200mV, PWM duty cycle = 51.32%, slew rate = 1PCLK/step



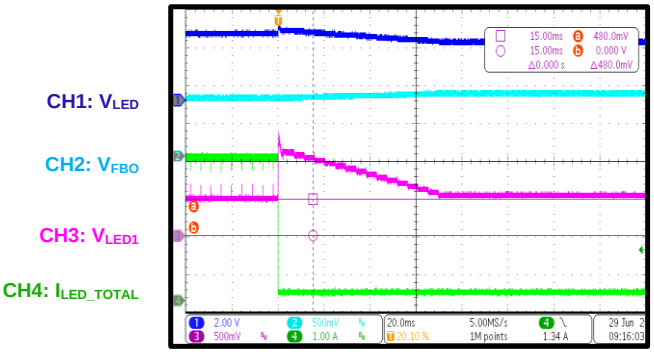
Adaptive Feedback Control (AFC)

Headroom = 300mV and hysteresis = 200mV, PWM duty cycle = 5.82%, phase shift = 1PCLK



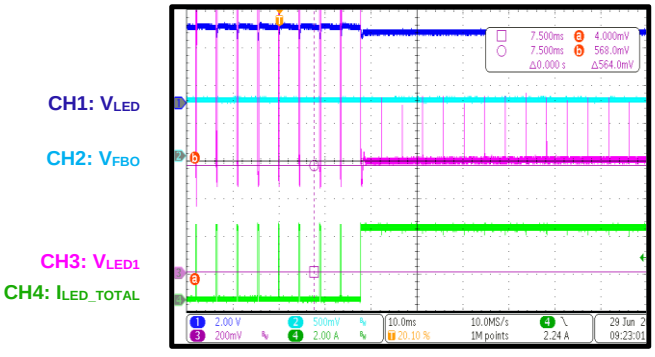
Adaptive Feedback Control (AFC)

Headroom = 300mV and hysteresis = 200mV, I_{MAX} = 80mA/string, I_{LED} from 100% to 5%



Adaptive Feedback Control (AFC)

I_{MAX} = 80mA/string, PWM duty cycle from 100% to 5%, I_{LED} = 100%



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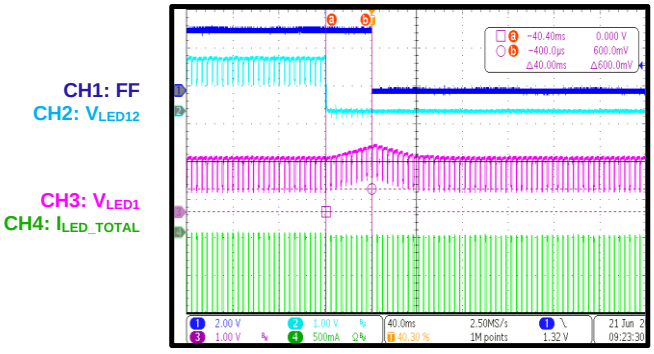
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 4V, f_{PCLK} = 25MHz, PDB = 16-bit, I_{MAX} = 30mA/ch, LED = 48P1S, T_A = 25°C, unless otherwise noted.

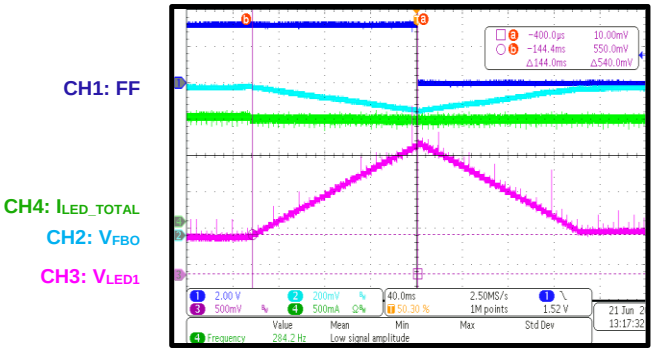
Open LED Protection

OPS = 8 steps, open channel 12



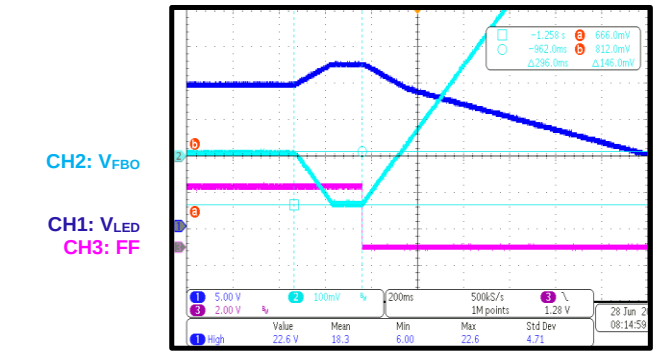
Open LED Protection

OPS = 32 steps, open channel 12



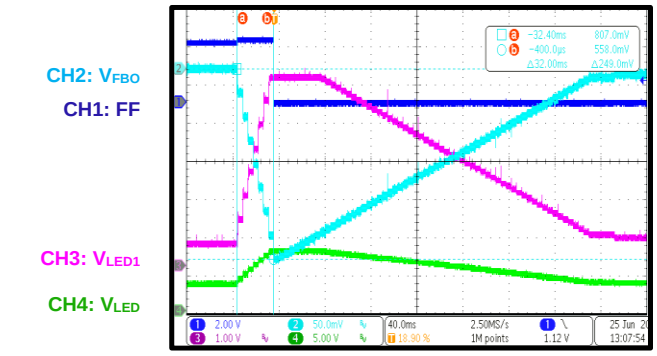
Open LED Protection

OVP = 22V, open channel 12



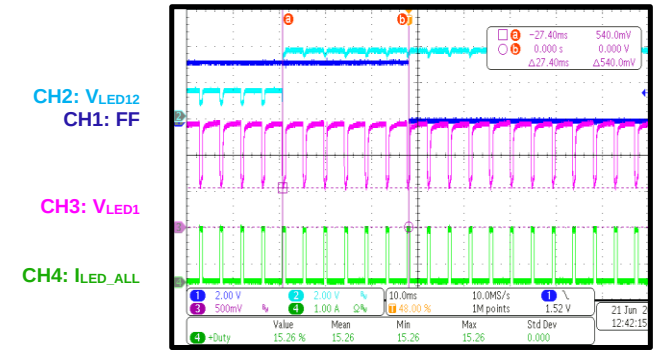
Open LED Protection

Step-up = 8 steps, open channel 12

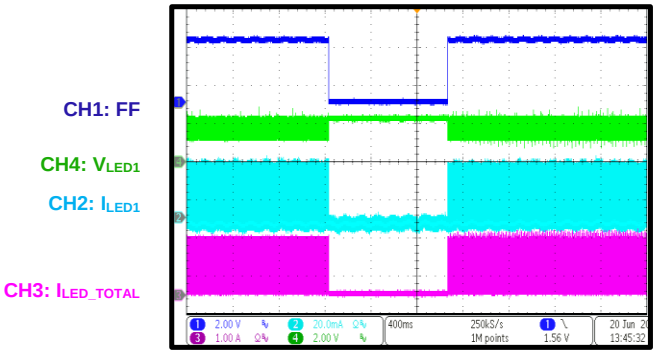


Short LED Protection

Short channel 12



Over-Temperature Protection



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FUNCTIONAL BLOCK DIAGRAM

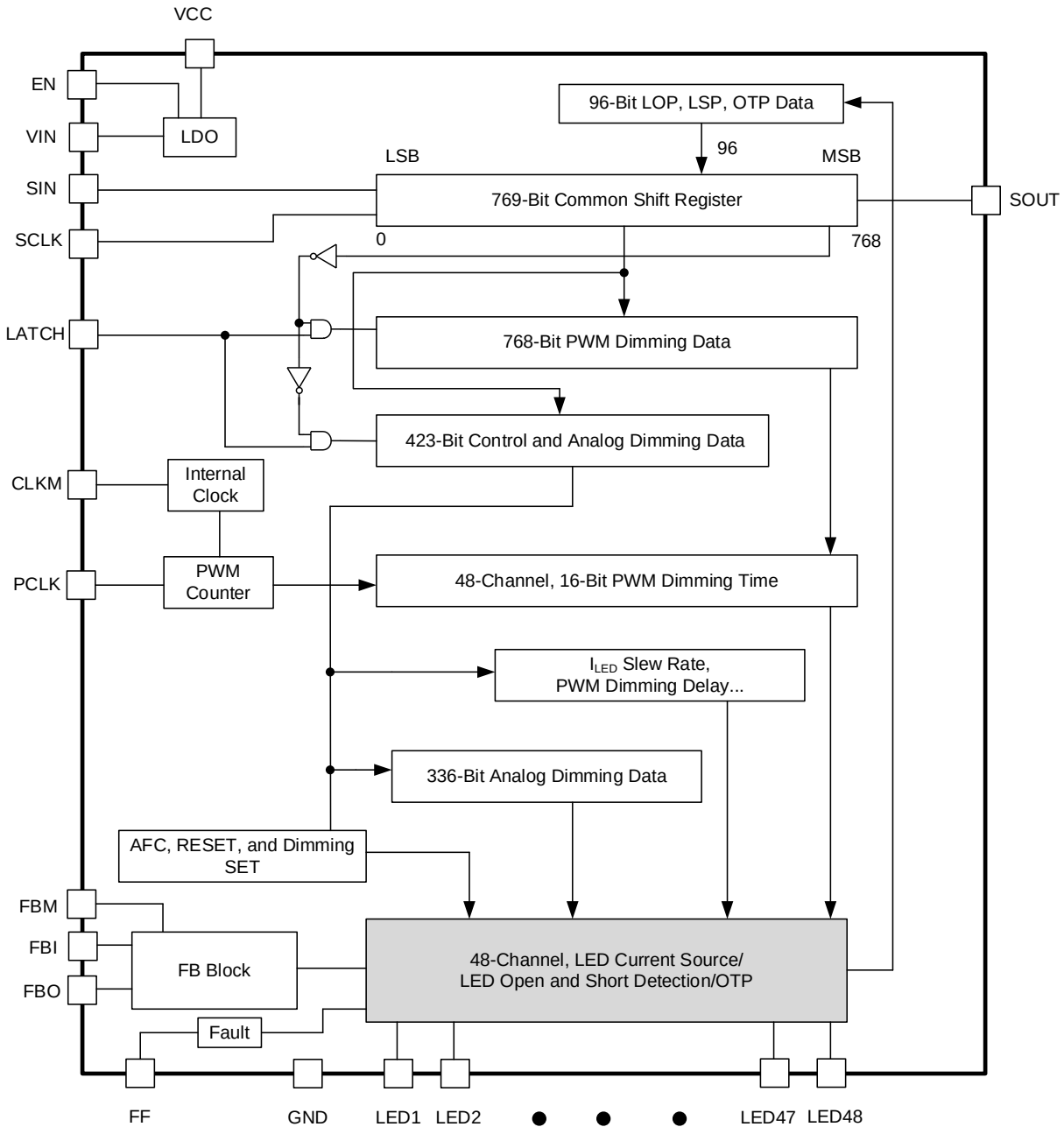

Figure 8: Functional Block Diagram

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TERMINAL-EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

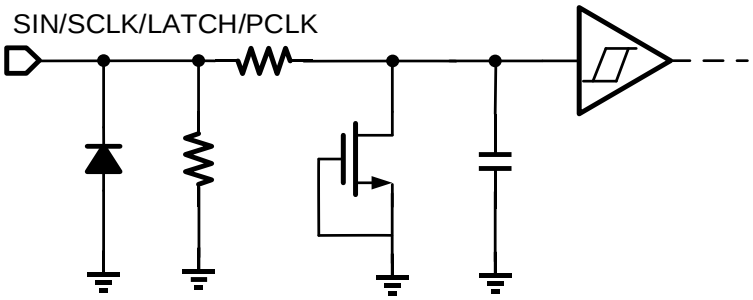

Figure 9: SIN, SCLK, LATCH, PCLK

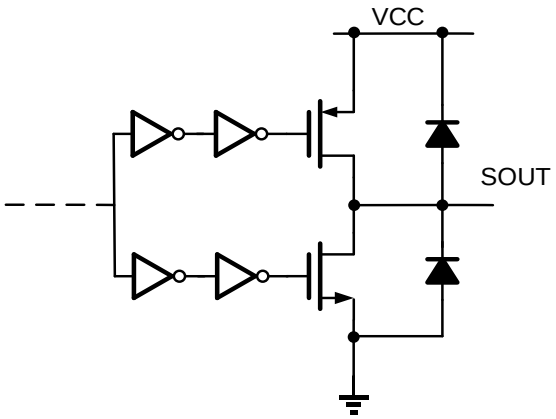

Figure 10: SOUT

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SERIAL INTERFACE AND REGISTER DESCRIPTION

(SIN, SOUT, SCLK, LATCH, PCLK)

Table 1: Common Shift Register (769 Bits)

	MSB												LSB	
SOUT	Latch Select Bit	Common Data Bit 767	Common Data Bit 766	Common Data Bit 765	Common Data Bit 764	Common Data Bit 763	-------	Common Data Bit 5	Common Data Bit 4	Common Data Bit 3	Common Data Bit 2	Common Data Bit 1	Common Data Bit 0	SIN / SCLK
	768	767	766	765	764	763	----	5	4	3	2	1	0	

Table 2: Command Format for Duty Update (1+ 16 x 48 Bits)

	MSB												LSB	
SOUT	0	Ch48 Duty [15:0]	Ch47 Duty [15:0]	Ch46 Duty [15:0]	Ch45 Duty [15:0]	Ch44 Duty [15:0]	-------	Ch6 Duty [15:0]	Ch5 Duty [15:0]	Ch4 Duty [15:0]	Ch3 Duty [15:0]	Ch2 Duty [15:0]	Ch1 Duty [15:0]	SIN / SCLK
	768	767~752	751~736	735~720	719~704	703~688	----	95~80	79~64	63~48	47~32	31~16	15~0	
	Parity Bits					Ch1~48 Duty Data Bits								

Table 3: Command Format for Control and LED Current Update (1 + 8 + 337 + 87 + 7 x 48 Bits)

	MSB					LSB	
SOUT	1	8'h96	337 Bits NC		Ch 48 ILED [6:0] ----- Ch 1 ILED [6:0]		SIN / SCLK
	768	767~760	759~423	422~336	335~329 ---- 6~0		
	Parity Bits	Parity Bits	Unused Bits	Control Register Bits	Ch 1~48 ILED Data Bits		

CH_EN [47:0]	ENOP	ENSH	SCANEN	STEPUP [1:0]	OPS [1:0]	EN_MODU	OVP [1:0]	VLEDX_HYS [1:0]	HeadR_TH [1:0]	IFBO [8:0]	PDB [1:0]	LATCH	SLEW [1:0]	REFRESH	TMRST	PDMOD	IMAX [2:0]	TDLY [3:0]	VSLP
422~375	374	373	372	371~370	369~368	367	366~365	364~363	362~361	360~352	351~350	349	348~347	346	345	344	343~341	340~337	336

Table 4: Command Format for Fault Flag Read Out (1 + 2 x 48 + 672 Bits)

	MSB			LSB	
SOUT	0	Ch 48~1 Open Fault Flag	Ch 48~1 Short Fault Flag	Common Data Bit [671:0]	SIN / SCLK
	768	767~720	719~672	671~0	
	Parity Bits	Fault Flag Bits		Previous Duty Data	

For the fault flag bits, if a channel experiences an open or short fault, the corresponding channel's fault bit = 1.

CHO48 and CHS48 are both set to 1 to indicate a bits-error fault. For a bits-error fault, the number of data bits that the IC receives is incorrect, which means the number of input SCLK pulses is not equal to *n* x 769 (where *n* is the number of MPQ3321 devices connected in a daisy chain).

CHO24 and CHS24 are both set to 1 to indicate that over-temperature protection (OTP) has occurred.

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TIMING DIAGRAMS FOR AN SPI DATA UPDATE

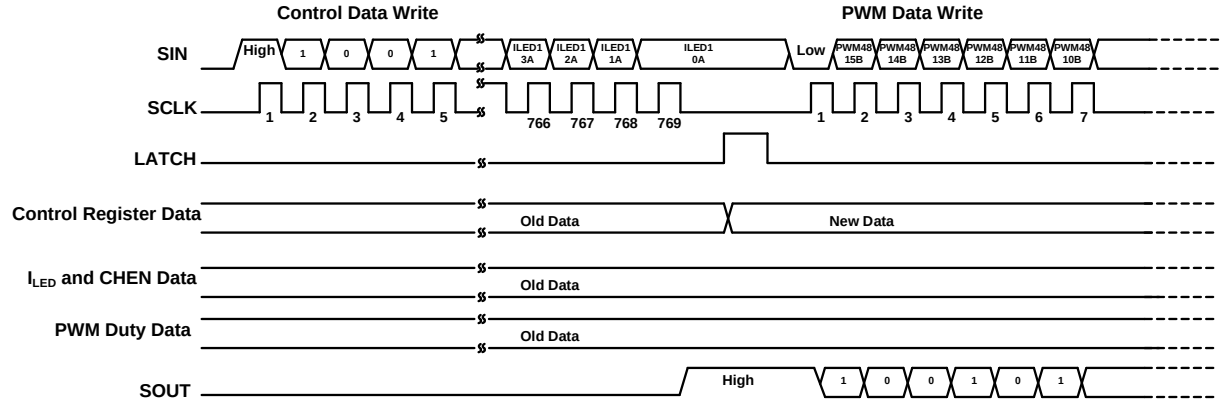

Figure 11: Timing Diagram of Control Register Update

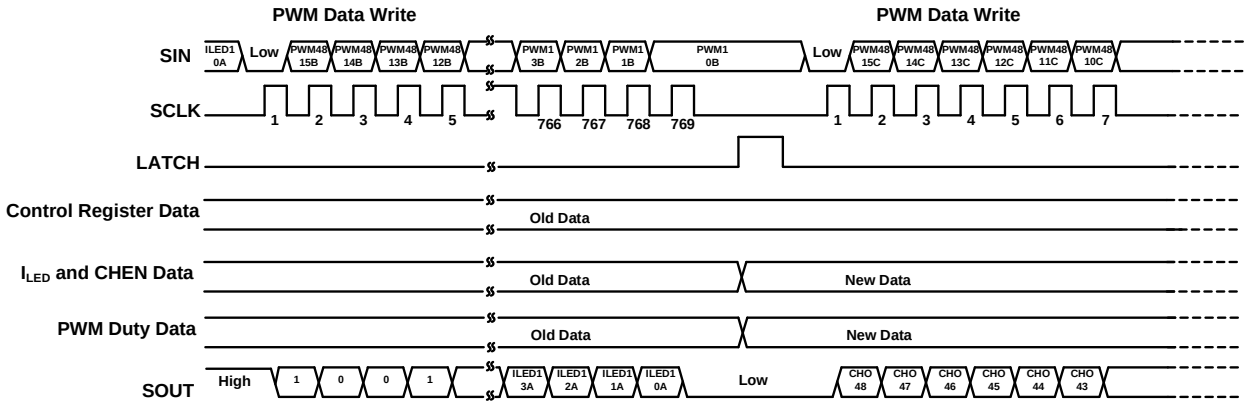

Figure 12: Timing Diagram of PWM Duty Register Update (RFRESH = 0)

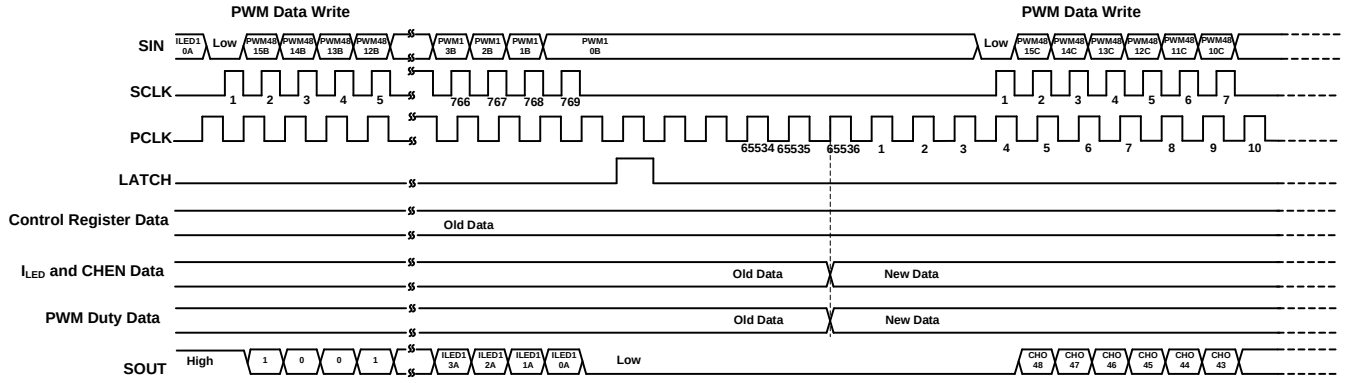

Figure 13: Timing Diagram of PWM Duty Register Update (RFRESH = 1)

To enable/disable channels 1–48, or to change the data for the ILED1[6:0]~ILED48[6:0] registers, first write the 769 bits in the control commands with the corresponding bits of the CH_EN registers (set to 1 or 0), or set the new ILED1~ILED48 data through the SPI interface.

The data for the CH_EN1~CH_EN48 bits and the ILED1~ILED48 registers are not valid immediately after sending control commands through the SPI interface.

Only when the next PWM duty data is written, the corresponding LED channels are enabled/disabled, and the new data for the ILED1~ILED48 registers is used.

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OPERATION

The MPQ3321 is a 48-channel LED driver with a 22V voltage rating and maximum 80mA current sources. It is designed to drive the LED arrays for local dimming backlighting in automotive LCD panels.

Internal 3.3V Regulator

The MPQ3321 includes an internal linear regulator (VCC). When the input voltage (V_{IN}) exceeds 3.5V, this regulator outputs a 3.3V power supply to the internal MOSFET and internal control circuitry. The VCC voltage (V_{CC}) drops to 0V when the chip shuts down. The chip remains disabled until V_{CC} exceeds the under-voltage lockout (UVLO) threshold. If the LED voltage (V_{LEDx}, where x = 1–48) is too low (e.g. <3.3V) and V_{IN} = V_{LEDx}, an external 3.3V power supply can be applied to the VCC pin. It is recommended to add a 100Ω resistor between the external 3.3V power supply and the VCC pin to limit the VCC pin's output current.

Dimming Function

The MPQ3321 supports independent 16-bit pulse-width modulation (PWM) and 7-bit analog dimming for each channel through the serial interface.

The ILEDx amplitude registers (A1~A48, ILEDx[6:0]) and ILED PWM duty registers (P1~P48, PWMx[15:0]) are configurable for reliable and flexible applications. The internal registers (IMAX[2:0]) can set the maximum LED current for all LED channels. The final ILED amplitude (I_{LEDx}, where x = 1–48) of each channel can be calculated with Equation (1):

$$I_{LEDx} = IMAX[2:0] \times ILEDx[6:0] \quad (1)$$

The final ILEDx dimming frequency depends on the external or internal PWM dimming clock (PCLK) and PWM counter bit, which is set by PDB[1:0]. The final frequency can be estimated with Equation (2):

$$f_{ILED} = f_{PCLK} / (2^{PDB[1:0]}) \quad (2)$$

The minimum on time for the current sources is about 560ns, and the minimum off time is about 60ns.

The maximum 30MHz external PWM dimming input clock and 25MHz serial interface clock guarantee excellent dimming performance and high data transfer rates for multiple devices in a daisy chain application.

To improve EMI performance, the MPQ3321 also supports an internal PWM dimming clock up to 20MHz. Enable this clock via the CLKM pin. To use the CLKM pin, connect a resistor from the CLKM pin to GND and float the PCLK pin. To select the internal clock frequency when the IC starts up, the CLKM pin outputs a 30μA current to detect the CLKM pin's voltage (see Table 5).

Table 5: PCLK Configuration

CLKM Voltage	f_{PCLK}	From
<0.5V	5MHz	Internal
>0.5V and <1V	10MHz	Internal
>1V and <1.5V	20MHz	Internal
>1.5V	Follow PCLK pin	External

Figure 14 shows the recommended start-up sequence.

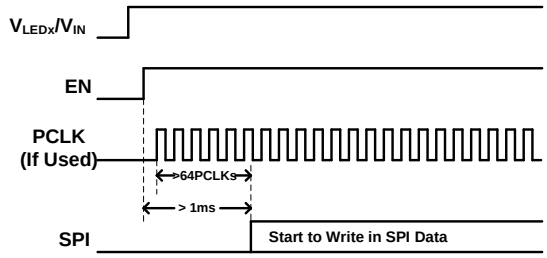

Figure 14: Recommended Start-Up Sequence

Figure 15 shows the recommended shutdown sequence.

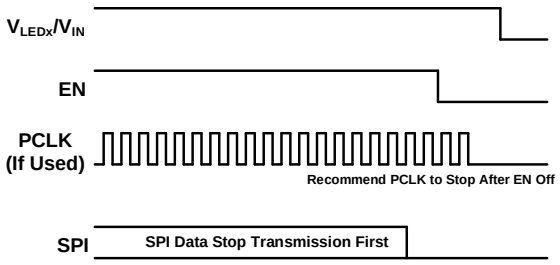

Figure 15: Recommended Shutdown Sequence

Phase-Shift Function

To reduce inrush current and eliminate audible noise during PWM dimming, the MPQ3321 employs a phase-shift function.

The internal register configures the delay time between the LEDx channel and LED(x + 1) channel.

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A maximum of 128 PCLK cycles/pulses can be set via the TDLY[3:0] bits.

LED Current (I_{LEDx}) Slew Rate Control

Changing the I_{LEDx} rising/falling slew rate when PWM dimming can sufficiently optimize EMI performance. The I_{LEDx} rising/falling slew rate is controlled by the SLEW[1:0] register:

- SLEW[1:0] = 00: No slew rate
- SLEW[1:0] = 01: 1 PCLK/step
- SLEW[1:0] = 10: 2 PCLK/step
- SLEW[1:0] = 11: 4 PCLK/step

Where each step refers to the analog dimming resolution, which is 1/127.

Adaptive Feedback Control (AFC) for the Pre-Power Stage

The MPQ3321 features adaptive feedback control (AFC) for the pre-power stage (see Figure 16).

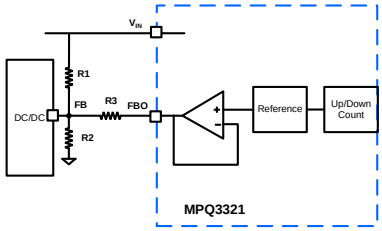

Figure 16: Regulating the DC/DC Converter's Output Voltage

When the front stage's DC/DC converter starts working, the initial V_{IN} can be set by the resistor divider (R1 and R2), calculated with Equation (3):

$$V_{IN} = V_{FB} \times (1 + \frac{R1}{R2}) \quad (3)$$

After the MPQ3321 is enabled, the FBO voltage (V_{FBO}) is regulated to a value set by IFBO[8:0]. Then V_{IN} can be estimated with Equation (4):

$$V_{IN} = V_{FB} \times (1 + \frac{R1}{R2}) + \frac{R1}{R3} \times (V_{FB} - V_{FBO}) \quad (4)$$

Where V_{FBO} ranges between 0.5V and 1.5V with an 8-bit resolution (about 3.922mV/step).

After the current source begins working, V_{IN} is regulated to a target value according to the minimum active LEDx pin voltage (V_{LEDx_MIN}) through the FBO pin. This optimizes system efficiency and improves the IC's thermal performance.

V_{LEDx_MIN} is monitored periodically. If V_{LEDx_MIN} < 0.3V (set by HEADR_TH[1:0]), V_{IN} increases; if V_{LEDx_MIN} > (HEADR_TH[1:0] + VLEDX_HYS[1:0]), then V_{IN} decreases. VLEDX_HYS[1:0] is the hysteresis voltage.

Adaptive Feedback Control (AFC) for Multiple ICs

The AFC function also supports applications with multiple ICs. The minimum active LEDx pin voltage between the multiple ICs is used to control the pre-power stage. The FBI and FBO pins deliver the V_{IN} regulation information to the ICs.

If the FBM pin is connected to GND, it is the master IC; if the FBM pin is floating, it is the slave IC. Figure 17 shows the FBO and FBI connection method.

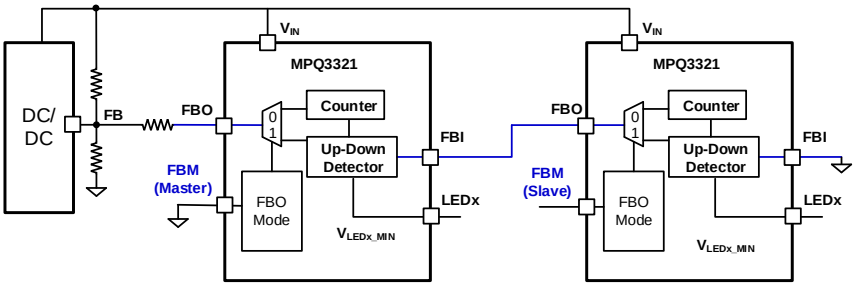

Figure 17: Circuit with Multiple ICs

For the FBI Input Detector

Connect the FBO pin of the latest IC to the FBI pin of the previous IC, as shown in figure 17.

- When the FBI voltage (V_{FBI}) < 0.6V, it means V_{IN} is too high for the latest IC.
- When 0.6V < V_{FBI} < 1.2V, it means V_{IN} does not need to change for the latest IC.

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- When V_{FBI} > 1.2V, it means V_{IN} is not sufficient for the latest IC.

Connect the final slave IC's FBI pin to GND.

For the Slave FBO Output Detector

- When V_{LEDx_MIN} < 0.3V or V_{FBI} > 1.2V, the FBO output 1.5V (V_{IN} must increase).
- When V_{LEDx_MIN} > 0.5V and V_{FBI} < 0.6V, the FBO output 0.3V (V_{IN} must decrease).

For other scenarios, the FBO pin outputs 0.9V and V_{IN} stays the same (see Table 7).

Table 7: FBI and FBO Output

FBI (Input)	<0.6V	0.6< and <1.2V	>1.2V
Slave FBO (Output)	0.3V	0.9V	1.5V
V_{IN}	Must fall	Stays the same	Must rise

For the Master FBO Output Detector

The master IC's FBO pin is connected to the FB resistor divider of the DC/DC converter to regulate V_{IN}. V_{FBO} ranges between 0.5V and 1.5V with an 8-bit resolution. Figure 17 on page 18 shows the detailed circuit. If the master IC's FBO pin is connected from one PCB to another PCB, ensure that noise is not coupled directly onto the signal. Since FBO is connected into a high-impedance feedback network, it can be more sensitive to noise if a board-to-board cable/connection is used without shielding or a poor ground return path.

Protections

The MPQ3321 includes open LED protection, short LED protection, and thermal protection. Once the protection is triggered, the FF pin pulls low and the corresponding fault bit is set to 1. After the IC recovers from the protection (in hiccup mode), the FF pin releases to high with a 750µs delay.

Open LED Protection

Open string protection is achieved by detecting the LEDx voltage (V_{LEDx}, where x = 1–48). During operation, if one string is open, the respective V_{LEDx} is low to ground (<80mV) and lasts for 8 FBO regulation steps (OPS[1:0]) if the AFC function is used; if AFC is not used, V_{LEDx} is low to ground for 4ms (duty cycle = 100%), then the corresponding LED string is marked off. Once marked, the remaining LED strings continue to feedback the output voltage information to the previous DC/DC converter. The string with the largest voltage drop determines the output regulation value. In hiccup mode, the marked-off string sends a 20µs pulse current to check whether an open fault is removed after every 20ms delay. This means that open string protection is recoverable.

Short String Protection

The MPQ3321 monitors V_{LEDx} to determine whether a short string fault has occurred. When one or more strings are shorted, the respective LEDx pins tolerate high voltage stress. If an LEDx voltage exceeds the short protection threshold, an internal counter starts. If this fault condition lasts for 4ms (D_{PWM} = 100%), the fault string is marked off. Once a string is marked off, it disconnects from the output voltage loop until the short is removed.

The short protection threshold can be set via the internal VSLP bit.

The marked-off string sends a 20µs pulse current to check if a short fault is removed after every 20ms delay. This means that short string protection is recoverable in hiccup mode.

If operating in scan mode (SCANEN = 1), the open/short fault bits and fault pin are reset at the next LATCH pin rising edge, and the short/open detection time changes to 50µs.

Thermal Shutdown

If the die temperature exceeds the upper threshold (TST), the IC shuts down and recovers to normal operation. When the temperature drops below the lower threshold, the IC recovers. The hysteresis value is typically 20°C.

The FF pin is active low, open drain. Pull FF high to an external voltage source. When the protection is triggered, the corresponding fault bit is set, and the FF pin pulls low.

In hiccup mode, the FF pin releases to high after all fault conditions are removed.

In latch-off mode, the FF pin stays low until the power is reset or the EN pin is reset.

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REGISTER MAP

Register Short Name	R/W	Bits	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PWM Duty Update (The MSB is 0)																			
PWM48	W	767:752	0000h	PWM48[15:0]															
PWM47	W	751:736	0000h	PWM47[15:0]															
…	W	…	…	…															
PWM2	W	31:16	0000h	PWM2[15:0]															
PWM1	W	15:0	0000h	PWM1[15:0]															
Control Registers and LED Current Amplitude Update (The MSB is 1)																			
CHN_EN3	W	422:407	FFFFh	CHEN48	CHEN47	CHEN46	CHEN45	CHEN44	CHEN43	CHEN42	CHEN41	CHEN40	CHEN39	CHEN38	CHEN37	CHEN36	CHEN35	CHEN34	CHEN33
CHN_EN2	W	406:391	FFFFh	CHEN32	CHEN31	CHEN30	CHEN29	CHEN28	CHEN27	CHEN26	CHEN25	CHEN24	CHEN23	CHEN22	CHEN21	CHEN20	CHEN19	CHEN18	CHEN17
CHN_EN1	W	390:375	FFFFh	CHEN16	CHEN15	CHEN14	CHEN13	CHEN12	CHEN11	CHEN10	CHEN9	CHEN8	CHEN7	CHEN6	CHEN5	CHEN4	CHEN3	CHEN2	CHEN1
CON1	W	374:368	0060h	RESERVED									ENOP	ENSH	ENSC	STEPUP[1:0]		OPS[1:0]	
CON2	W	367:352	82B2h	EN_MODU	OVP[1:0]		VLEDX_HYS[1:0]		HEADR_TH[1:0]		IFBO[8:0]								
CON3	W	351:336	2140h	PDB[1:0]		LATCH	SLEW[1:0]		FRRESH	TMRST	PDMOD	IMAX[2:0]			TDLY[3:0]				VSLP
ILED48	W	335:329	00h	RESERVED									ILED48[6:0]						
ILED47	W	328:322	00h	RESERVED									ILED47[6:0]						
…	W	…	…	…									…						
ILED2	W	13:7	00h	RESERVED									ILED2[6:0]						
ILED1	W	6:0	00h	RESERVED									ILED1[6:0]						
Open and Short Fault Flag Read (The MSB is 0)																			
FAU_OP3	R	767:752	0000h	CHO48	CHO47	CHO46	CHO45	CHO44	CHO43	CHO42	CHO41	CHO40	CHO39	CHO38	CHO37	CHO36	CHO35	CHO34	CHO33
FAU_OP2	R	751:736	0000h	CHO32	CHO31	CHO30	CHO29	CHO28	CHO27	CHO26	CHO25	CHO24	CHO23	CHO22	CHO21	CHO20	CHO19	CHO18	CHO17
FAU_OP1	R	735:720	0000h	CHO16	CHO15	CHO14	CHO13	CHO12	CHO11	CHO10	CHO9	CHO8	CHO7	CHO6	CHO5	CHO4	CHO3	CHO2	CHO1
FAU_SH3	R	719:704	0000h	CHS48	CHS47	CHS46	CHS45	CHS44	CHS43	CHS42	CHS41	CHS40	CHS39	CHS38	CHS37	CHS36	CHS35	CHS34	CHS33
FAU_SH2	R	703:688	0000h	CHS32	CHS31	CHS30	CHS29	CHS28	CHS27	CHS26	CHS25	CHS24	CHS23	CHS22	CHS21	CHS20	CHS19	CHS18	CHS17
FAU_SH1	R	687:672	0000h	CHS16	CHS15	CHS14	CHS13	CHS12	CHS11	CHS10	CHS9	CHS8	CHS7	CHS6	CHS5	CHS4	CHS3	CHS2	CHS1

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REGISTER DESCRIPTION

PWMx (Where x = 48–1) (Bits[767:0], 16 Bits/Register)

Access: Write-only

POR/Soft Reset Value: 0000h

The PWMx command sets the LED current dimming duty. See Table 2 on page 15 for more details.

Bits	Name	Description
D[15:0]	PWMx[15:0]	Sets the PWM dimming clock number. 16 bits. The clock can be the external or internal PCLK. 0000H: 0 clock … FFFFH: 65535 clocks

CHN_EN3 (Bits[422:407])

Access: Write-only

POR/Soft Reset Value: FFFFh

The CHN_EN3 command enables channels 33–48.

Bits	Name	Description
D[15]	CHEN48	0: Channel 48 disabled 1: Channel 48 enabled
D[14]	CHEN47	0: Channel 47 disabled 1: Channel 47 enabled
D[13]	CHEN46	0: Channel 46 disabled 1: Channel 46 enabled
D[12]	CHEN45	0: Channel 45 disabled 1: Channel 45 enabled
D[11]	CHEN44	0: Channel 44 disabled 1: Channel 44 enabled
D[10]	CHEN43	0: Channel 43 disabled 1: Channel 43 enabled
D[9]	CHEN42	0: Channel 42 disabled 1: Channel 42 enabled
D[8]	CHEN41	0: Channel 41 disabled 1: Channel 41 enabled
D[7]	CHEN40	0: Channel 40 disabled 1: Channel 40 enabled
D[6]	CHEN39	0: Channel 39 disabled 1: Channel 39 enabled
D[5]	CHEN38	0: Channel 38 disabled 1: Channel 38 enabled
D[4]	CHEN37	0: Channel 37 disabled 1: Channel 37 enabled
D[3]	CHEN36	0: Channel 36 disabled 1: Channel 36 enabled
D[2]	CHEN35	0: Channel 35 disabled 1: Channel 35 enabled

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D[1]	CHEN34	0: Channel 34 disabled 1: Channel 34 enabled
D[0]	CHEN33	0: Channel 33 disabled 1: Channel 33 enabled

CHN_EN2 (Bits[406:391])

Access: Write-only

POR/Soft Reset Value: FFFFh

The CHN_EN2 command enables channels 17–32.

Bits	Name	Description
D[15]	CHEN32	0: Channel 32 disabled 1: Channel 32 enabled
D[14]	CHEN31	0: Channel 31 disabled 1: Channel 31 enabled
D[13]	CHEN30	0: Channel 30 disabled 1: Channel 30 enabled
D[12]	CHEN29	0: Channel 29 disabled 1: Channel 29 enabled
D[11]	CHEN28	0: Channel 28 disabled 1: Channel 28 enabled
D[10]	CHEN27	0: Channel 27 disabled 1: Channel 27 enabled
D[9]	CHEN26	0: Channel 26 disabled 1: Channel 26 enabled
D[8]	CHEN25	0: Channel 25 disabled 1: Channel 25 enabled
D[7]	CHEN24	0: Channel 24 disabled 1: Channel 24 enabled
D[6]	CHEN23	0: Channel 23 disabled 1: Channel 23 enabled
D[5]	CHEN22	0: Channel 22 disabled 1: Channel 22 enabled
D[4]	CHEN21	0: Channel 21 disabled 1: Channel 21 enabled
D[3]	CHEN20	0: Channel 20 disabled 1: Channel 20 enabled
D[2]	CHEN19	0: Channel 19 disabled 1: Channel 19 enabled
D[1]	CHEN18	0: Channel 18 disabled 1: Channel 18 enabled
D[0]	CHEN17	0: Channel 17 disabled 1: Channel 17 enabled

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CHN_EN1 (Bits[390:375])

Access: Write-only

POR/Soft Reset Value: FFFFh

The CHN_EN1 command enables channels 1–16.

Bits	Name	Description
D[15]	CHEN16	0: Channel 16 disabled 1: Channel 16 enabled
D[14]	CHEN15	0: Channel 15 disabled 1: Channel 15 enabled
D[13]	CHEN14	0: Channel 14 disabled 1: Channel 14 enabled
D[12]	CHEN13	0: Channel 13 disabled 1: Channel 13 enabled
D[11]	CHEN12	0: Channel 12 disabled 1: Channel 12 enabled
D[10]	CHEN11	0: Channel 11 disabled 1: Channel 11 enabled
D[9]	CHEN10	0: Channel 10 disabled 1: Channel 10 enabled
D[8]	CHEN9	0: Channel 9 disabled 1: Channel 9 enabled
D[7]	CHEN8	0: Channel 8 disabled 1: Channel 8 enabled
D[6]	CHEN7	0: Channel 7 disabled 1: Channel 7 enabled
D[5]	CHEN6	0: Channel 6 disabled 1: Channel 6 enabled
D[4]	CHEN5	0: Channel 5 disabled 1: Channel 5 enabled
D[3]	CHEN4	0: Channel 4 disabled 1: Channel 4 enabled
D[2]	CHEN3	0: Channel 3 disabled 1: Channel 3 enabled
D[1]	CHEN2	0: Channel 2 disabled 1: Channel 2 enabled
D[0]	CHEN1	0: Channel 1 disabled 1: Channel 1 enabled

CON1 (Bits[374:368])

Access: Write-only

POR/Soft Reset Value: 0060h

The CON1 command sets the protection features.

Bits	Name	Description
D[15:7]	RESERVED	Reserved.
D[6]	ENOP	0: Disable LED open protection 1: Enable LED open protection

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D[5]	ENSH	0: Disable LED short protection 1: Enable LED short protection
D[4]	ENSC	If the device operates in scan mode: • The open/short fault bits and the fault pin are reset at the next LATCH pin rising • The short/open detection time is changed to 50μs 0: Disable scan mode 1: Enable scan mode
D[3:2]	STEPUP[1:0]	Sets the steps for FBO. In adaptive feedback control (AFC) mode, FBO decreases by the set number of steps in every PWM period. 00: 1 step 01: 2 steps 10: 4 steps 11: 8 steps
D[1:0]	OPS[1:0]	When one string is open and the condition lasts for the below steps of FBO regulation, the fault string is marked off. 00: 8 steps 01: 16 steps 10: 32 steps 11: 64 steps

CON2 (Bits[367:352])

Access: Write-only

POR/Soft Reset Value: 82B2h

The CON2 command sets the adaptive control features.

Bits	Name	Description
D[15]	EN_MODU	0: Disable the FBO regulation function 1: Enable the FBO regulation function
D[14:13]	OVP[1:0]	Sets the maximum regulated input voltage when adaptive feedback control (AFC) is used. 00: Reserved 01: 16.5V 10: 11V 11: 5.5V
D[12:11]	VLEDX_HY[1:0]	Sets the hysteresis for V_{LEDx} comparisons during AFC. V_{IN} decreases if the minimum V_{LEDx} exceeds (HEADR_TH[1:0] + VLEDX_HYS[1:0]). 00: 200mV 01: 300mV 10: 400mV 11: 500mV
D[10:9]	HEADR_TH[1:0]	Sets the V_{LEDx} threshold to increase V_{IN} for AFC. 00: 300mV 01: 400mV 10: 500mV 11: 600mV

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D[8:0]	IFBO[8:0]	Sets the initial FBO voltage. Ranges from 0.5V to 1.5V, with 3.922mV/step. When IFBO[8] is 1, the FBO pin voltage of the master IC can be changed to the value set by IFBO[7:0] directly. 00h: 0.5V 01h: (0.5V + 3.922mV) … B2h: 1.198V B3h: 1.202V … FFh: 1.5V

CON3 (Bits[351:336])

Access: Write-only

POR/Soft Reset Value: 2140h

The CON3 command sets the communication features.

Bits	Name	Description
D[15:14]	PDB[1:0]	Sets the PWM dimming bit/resolution. 00: 16 bits 01: 14 bits 10: 13 bits 11: 12 bits
D[13]	LATCH	0: Hiccup mode if there is a fault condition 1: Latch-off mode if there is a fault condition
D[12:11]	SLEW[1:0]	Sets the LED current slew rate. 00: No slew rate 01: 1 PCLK/step 10: 2 PCLK/step 11: 4 PCLK/step
D[10]	RFRESH	Enables automatic data refresh mode. 0: Disabled. The data in the common shift register are copied to the PWM data latch at the next LATCH signal rising edge for a PWM data write. The analog data in the control data latch are copied to the analog data latch simultaneously 1: Enabled. The data in the common shift register are copied to the PWM data latch at the 65,536th PCLK after the LATCH signal rising edge for a PWM data write. The analog data in the control data latch are copied to the analog data latch simultaneously
D[9]	TMRST	Sets whether the PWM timer resets after receiving a LATCH signal. 0: The PWM timer counter is not reset and the outputs are not forced off, even when a LATCH signal rising edge is input for a PWM dimming data write 1: The PWM dimming timer counter is reset to 0 and all outputs are forced off at the LATCH signal rising edge for a PWM dimming data write. PWM control resumes at the next PCLK rising edge
D[8]	PDMOD	0: Each constant-current output is turned on and off for one display period (one time) 1: Each output repeats the PWM control every 65,536 PCLKs (traditional PWM dimming)
D[7:5]	IMAX[2:0]	Sets the maximum I_{LEDx}. 10mA/step If the maximum current ≥ 60mA, then V_{IN} must ≥ 3.5V 000: 10mA 001: 20mA 010: 30mA … 111: 80mA

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D[4:1]	TDLY[3:0]	Sets the PWM dimming delay time. 0000: No delay time 0001: Delay 1 PCLK 0010: Delay 2 PCLKs 0011: Delay 4 PCLKs 0100: Delay 8 PCLKs 0101: Delay 16 PCLKs 0110: Delay 32 PCLKs 0111: Delay 64 PCLKs 1000~1111: Delay 128 PCLKs
D[0]	VSLP	Sets the threshold for short LED protection. 0: 2.5V 1: 5V

ILEDx (x = 48–1) (Bits[335:0], 7 Bits/Register)

Access: Write-only

POR/Soft Reset Value: 0000h

The ILEDx command sets the LED current amplitude (I_{LEDx}, where x = 1–48). See Table 3 on page 15 for more details.

Bits	Name	Description
D[15:7]	RESERVED	Reserved.
D[6:0]	ILEDx[6:0]	Sets the I_{LEDx} amplitude. 7 bits, analog dimming. 00h: 0% 7Fh: 100%

FAU_OP3 (Bits[767:752])

Access: Read-only

POR/Soft Reset Value: 0000h

The FAU_OP3 command reads whether an open fault has occurred on channels 33–48.

Bits	Name	Description
D[15]	CHO48	0: No open fault has occurred on channel 48 1: An open fault has occurred on channel 48
D[14]	CHO46	0: No open fault has occurred on channel 47 1: An open fault has occurred on channel 47
D[13]	CHO46	0: No open fault has occurred on channel 46 1: An open fault has occurred on channel 46
D[12]	CHO45	0: No open fault has occurred on channel 48 1: An open fault has occurred on channel 48
D[11]	CHO44	0: No open fault has occurred on channel 44 1: An open fault has occurred on channel 44
D[10]	CHO43	0: No open fault has occurred on channel 43 1: An open fault has occurred on channel 43
D[9]	CHO42	0: No open fault has occurred on channel 42 1: An open fault has occurred on channel 42
D[8]	CHO41	0: No open fault has occurred on channel 41 1: An open fault has occurred on channel 41
D[7]	CHO40	0: No open fault has occurred on channel 40 1: An open fault has occurred on channel 40

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D[6]	CHO39	0: No open fault has occurred on channel 39 1: An open fault has occurred on channel 39
D[5]	CHO38	0: No open fault has occurred on channel 38 1: An open fault has occurred on channel 38
D[4]	CHO37	0: No open fault has occurred on channel 37 1: An open fault has occurred on channel 37
D[3]	CHO36	0: No open fault has occurred on channel 36 1: An open fault has occurred on channel 36
D[2]	CHO35	0: No open fault has occurred on channel 35 1: An open fault has occurred on channel 35
D[1]	CHO34	0: No open fault has occurred on channel 34 1: An open fault has occurred on channel 34
D[0]	CHO33	0: No open fault has occurred on channel 33 1: An open fault has occurred on channel 33

FAU_OP2 (Bits[751:736])

Access: Read-only

POR/Soft Reset Value: 0000h

The FAU_OP2 command reads whether an open fault has occurred on channels 17–32.

Bits	Name	Description
D[15]	CHO32	0: No open fault has occurred on channel 32 1: An open fault has occurred on channel 32
D[14]	CHO31	0: No open fault has occurred on channel 31 1: An open fault has occurred on channel 31
D[13]	CHO30	0: No open fault has occurred on channel 30 1: An open fault has occurred on channel 30
D[12]	CHO29	0: No open fault has occurred on channel 29 1: An open fault has occurred on channel 29
D[11]	CHO28	0: No open fault has occurred on channel 28 1: An open fault has occurred on channel 28
D[10]	CHO27	0: No open fault has occurred on channel 27 1: An open fault has occurred on channel 27
D[9]	CHO26	0: No open fault has occurred on channel 26 1: An open fault has occurred on channel 26
D[8]	CHO25	0: No open fault has occurred on channel 25 1: An open fault has occurred on channel 25
D[7]	CHO24	0: No open fault has occurred on channel 24 1: An open fault has occurred on channel 24
D[6]	CHO23	0: No open fault has occurred on channel 23 1: An open fault has occurred on channel 23
D[5]	CHO22	0: No open fault has occurred on channel 22 1: An open fault has occurred on channel 22
D[4]	CHO21	0: No open fault has occurred on channel 21 1: An open fault has occurred on channel 21
D[3]	CHO20	0: No open fault has occurred on channel 20 1: An open fault has occurred on channel 20
D[2]	CHO19	0: No open fault has occurred on channel 19 1: An open fault has occurred on channel 19

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D[1]	CHO18	0: No open fault has occurred on channel 18 1: An open fault has occurred on channel 18
D[0]	CHO17	0: No open fault has occurred on channel 17 1: An open fault has occurred on channel 17

FAU_OP1 (Bits[735:720])

Access: Read-only

POR/Soft Reset Value: 0000h

The FAU_OP1 command reads whether an open fault has occurred on channels 1–16.

Bits	Name	Description
D[15]	CHO16	0: No open fault has occurred on channel 16 1: An open fault has occurred on channel 16
D[14]	CHO15	0: No open fault has occurred on channel 15 1: An open fault has occurred on channel 15
D[13]	CHO14	0: No open fault has occurred on channel 14 1: An open fault has occurred on channel 14
D[12]	CHO13	0: No open fault has occurred on channel 13 1: An open fault has occurred on channel 13
D[11]	CHO12	0: No open fault has occurred on channel 12 1: An open fault has occurred on channel 12
D[10]	CHO11	0: No open fault has occurred on channel 11 1: An open fault has occurred on channel 1
D[9]	CHO10	0: No open fault has occurred on channel 10 1: An open fault has occurred on channel 10
D[8]	CHO9	0: No open fault has occurred on channel 9 1: An open fault has occurred on channel 9
D[7]	CHO8	0: No open fault has occurred on channel 8 1: An open fault has occurred on channel 8
D[6]	CHO7	0: No open fault has occurred on channel 7 1: An open fault has occurred on channel 7
D[5]	CHO6	0: No open fault has occurred on channel 6 1: An open fault has occurred on channel 6
D[4]	CHO5	0: No open fault has occurred on channel 5 1: An open fault has occurred on channel 5
D[3]	CHO4	0: No open fault has occurred on channel 4 1: An open fault has occurred on channel 4
D[2]	CHO3	0: No open fault has occurred on channel 3 1: An open fault has occurred on channel 3
D[1]	CHO2	0: No open fault has occurred on channel 2 1: An open fault has occurred on channel 2
D[0]	CHO1	0: No open fault has occurred on channel 1 1: An open fault has occurred on channel 1

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FAU_SH3 (Bits[719:704])

Access: Read-only

POR/Soft Reset Value: 0000h

The FAU_SH3 command reads whether a short fault has occurred on channels 33–48.

Bits	Name	Description
D[15]	CHO48	0: No short fault has occurred on channel 48 1: A short fault has occurred on channel 48
D[14]	CHO46	0: No short fault has occurred on channel 47 1: A short fault has occurred on channel 47
D[13]	CHO46	0: No short fault has occurred on channel 46 1: A short fault has occurred on channel 46
D[12]	CHO45	0: No short fault has occurred on channel 48 1: A short fault has occurred on channel 48
D[11]	CHO44	0: No short fault has occurred on channel 44 1: A short fault has occurred on channel 44
D[10]	CHO43	0: No short fault has occurred on channel 43 1: A short fault has occurred on channel 43
D[9]	CHO42	0: No short fault has occurred on channel 42 1: A short fault has occurred on channel 42
D[8]	CHO41	0: No short fault has occurred on channel 41 1: A short fault has occurred on channel 41
D[7]	CHO40	0: No short fault has occurred on channel 40 1: A short fault has occurred on channel 40
D[6]	CHO39	0: No short fault has occurred on channel 39 1: A short fault has occurred on channel 39
D[5]	CHO38	0: No short fault has occurred on channel 38 1: A short fault has occurred on channel 38
D[4]	CHO37	0: No short fault has occurred on channel 37 1: A short fault has occurred on channel 37
D[3]	CHO36	0: No short fault has occurred on channel 36 1: A short fault has occurred on channel 36
D[2]	CHO35	0: No short fault has occurred on channel 35 1: A short fault has occurred on channel 35
D[1]	CHO34	0: No short fault has occurred on channel 34 1: A short fault has occurred on channel 34
D[0]	CHO33	0: No short fault has occurred on channel 33 1: A short fault has occurred on channel 33

FAU_SH2 (Bits[703:688])

Access: Read-only

POR/Soft Reset Value: 0000h

The FAU_SH2 command reads whether a short fault has occurred on channels 17–32.

Bits	Name	Description
D[15]	CHO32	0: No short fault has occurred on channel 32 1: A short fault has occurred on channel 32
D[14]	CHO31	0: No short fault has occurred on channel 31 1: A short fault has occurred on channel 31

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D[13]	CHO30	0: No short fault has occurred on channel 30 1: A short fault has occurred on channel 30
D[12]	CHO29	0: No open fault has occurred on channel 29 1: A short fault has occurred on channel 29
D[11]	CHO28	0: No short fault has occurred on channel 28 1: A short fault has occurred on channel 28
D[10]	CHO27	0: No short fault has occurred on channel 27 1: A short fault has occurred on channel 27
D[9]	CHO26	0: No short fault has occurred on channel 26 1: A short fault has occurred on channel 26
D[8]	CHO25	0: No short fault has occurred on channel 25 1: A short fault has occurred on channel 25
D[7]	CHO24	0: No short fault has occurred on channel 24 1: A short fault has occurred on channel 24
D[6]	CHO23	0: No short fault has occurred on channel 23 1: A short fault has occurred on channel 23
D[5]	CHO22	0: No short fault has occurred on channel 22 1: A short fault has occurred on channel 22
D[4]	CHO21	0: No short fault has occurred on channel 21 1: A short fault has occurred on channel 21
D[3]	CHO20	0: No short fault has occurred on channel 20 1: A short fault has occurred on channel 20
D[2]	CHO19	0: No open fault has occurred on channel 19 1: A short fault has occurred on channel 19
D[1]	CHO18	0: No short fault has occurred on channel 18 1: A short fault has occurred on channel 18
D[0]	CHO17	0: No short fault has occurred on channel 17 1: A short fault has occurred on channel 17

FAU_SH1 (Bits[687:672])

Access: Read-only

POR/Soft Reset Value: 0000h

The FAU_SH1 command reads whether a short fault has occurred on channels 1–16.

Bits	Name	Description
D[15]	CHO16	0: No short fault has occurred on channel 16 1: A short fault has occurred on channel 16
D[14]	CHO15	0: No short fault has occurred on channel 15 1: A short fault has occurred on channel 15
D[13]	CHO14	0: No short fault has occurred on channel 14 1: A short fault has occurred on channel 14
D[12]	CHO13	0: No short fault has occurred on channel 13 1: A short fault has occurred on channel 13
D[11]	CHO12	0: No short fault has occurred on channel 12 1: A short fault has occurred on channel 12
D[10]	CHO11	0: No short fault has occurred on channel 11 1: A short fault has occurred on channel 1

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D[9]	CHO10	0: No short fault has occurred on channel 10 1: A short fault has occurred on channel 10
D[8]	CHO9	0: No short fault has occurred on channel 9 1: A short fault has occurred on channel 9
D[7]	CHO8	0: No short fault has occurred on channel 8 1: A short fault has occurred on channel 8
D[6]	CHO7	0: No short fault has occurred on channel 7 1: A short fault has occurred on channel 7
D[5]	CHO6	0: No short fault has occurred on channel 6 1: A short fault has occurred on channel 6
D[4]	CHO5	0: No short fault has occurred on channel 5 1: A short fault has occurred on channel 5
D[3]	CHO4	0: No short fault has occurred on channel 4 1: A short fault has occurred on channel 4
D[2]	CHO3	0: No short fault has occurred on channel 3 1: A short fault has occurred on channel 3
D[1]	CHO2	0: No short fault has occurred on channel 2 1: A short fault has occurred on channel 2
D[0]	CHO1	0: No short fault has occurred on channel 1 1: A short fault has occurred on channel 1

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TYPICAL APPLICATION CIRCUIT

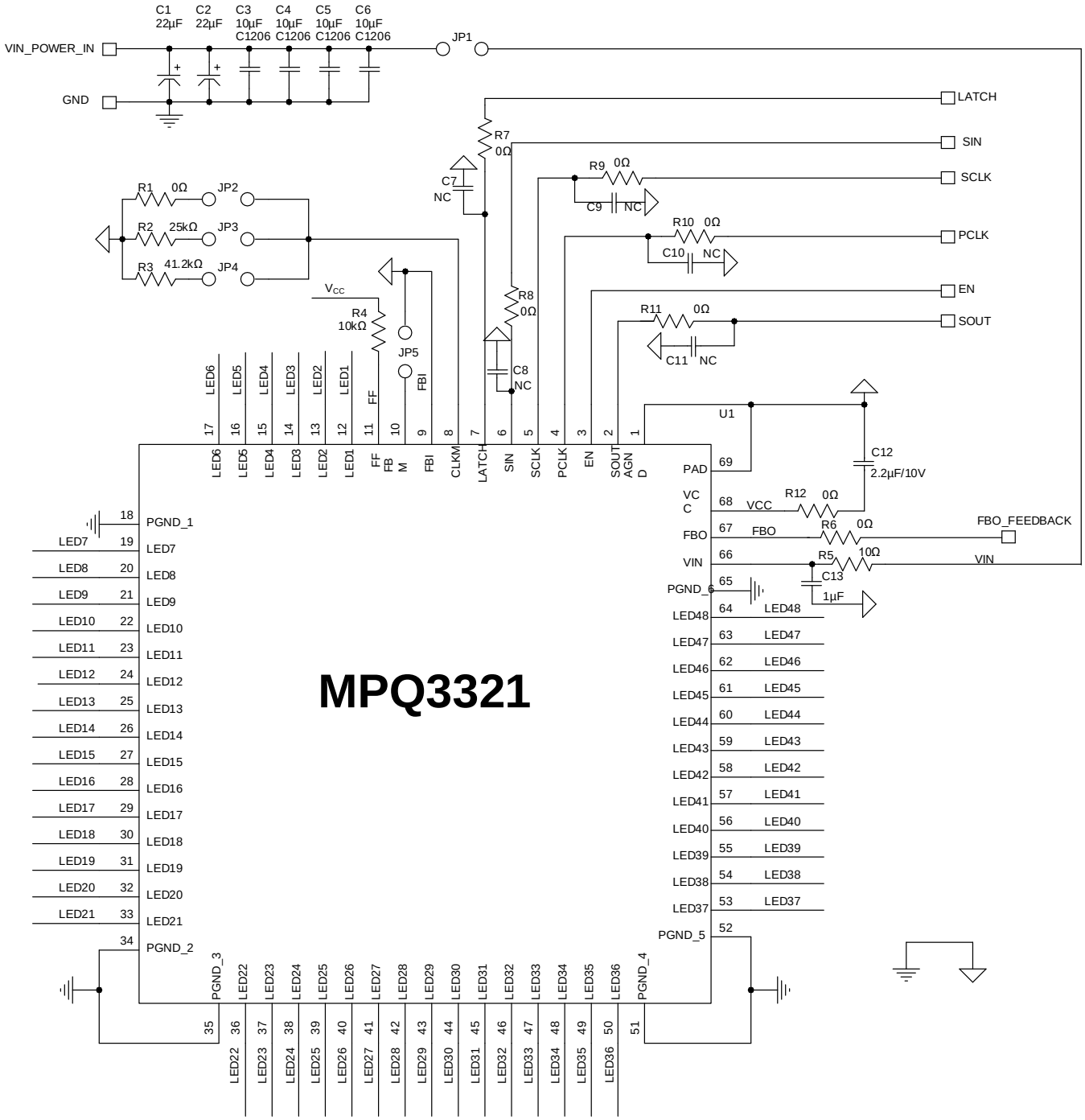

Figure 18: Typical Application Circuit

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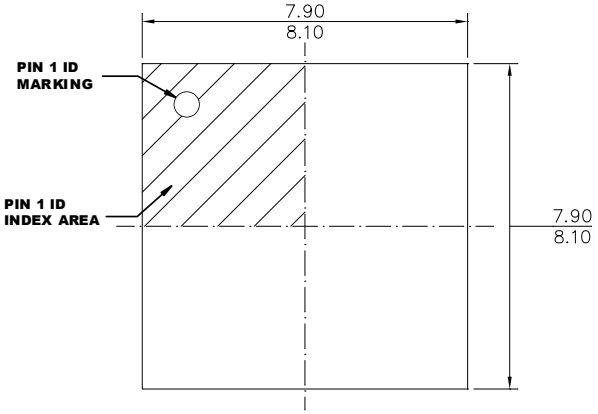
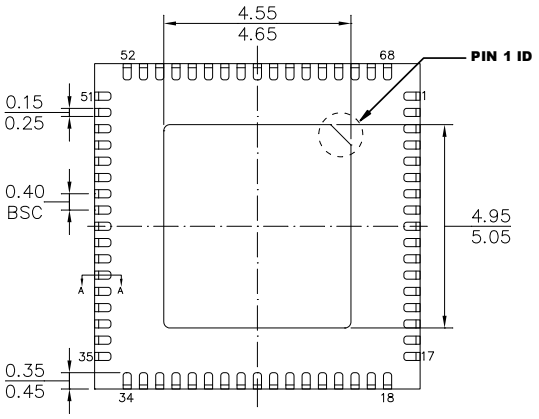
PACKAGE INFORMATION

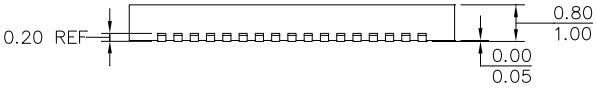
QFN-68 (8mmx8mm)
Wettable Flank



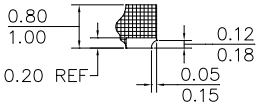
TOP VIEW



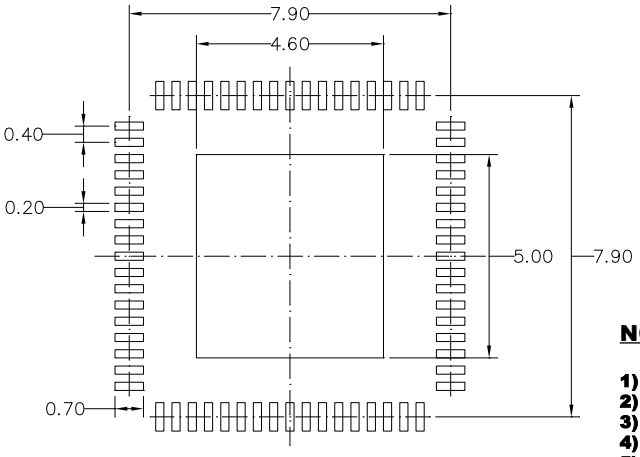
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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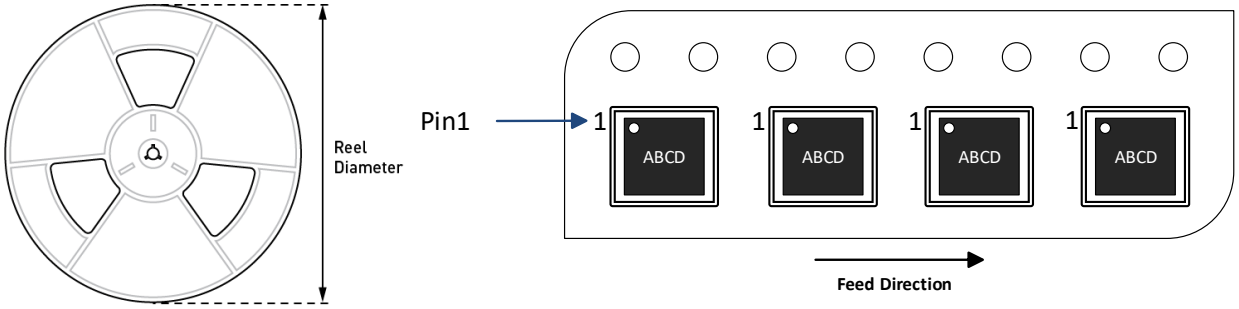
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3321GQQE-AEC1-Z	QFN-68 (8mmx8mm)	2500	N/A	N/A	13in	16mm	12mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/27/2024	Initial Release	-

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