MPQ29261

18A, Synchronous Step-Down Converter with 2-Bit VID, AEC-Q100 Qualified

DESCRIPTION

The MPQ29261 is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with 2-bit voltage identification (VID). It offers an ultra-compact solution that can achieve up to 18A of continuous output current (I_{OUT}), with an adjustable current limit (I_{LIMIT}).

MPS's proprietary switching loss reduction technique and internal low on resistance ($R_{DS(ON)}$) MOSFETs allow the device to operate at high efficiency across the wide I_{OUT} load range.

Adaptive constant-on-time (COT) control provides fast transient response and eases loop stabilization. The DC auto-tune loop works with the differential remote sense to provide excellent load and line regulation.

Full protection features include over-current limitation (OCL), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MPQ29261 requires a minimal number of standard external components, and it is available in a QFN-19 (3mmx4mm) package.

FEATURES

- Wide Operating Input Voltage (V_{IN}) Range
- 2-Bit Voltage Identification (VID)
- 190µA Low Quiescent Current (I_Q)
- 18A Continous Output Current (I_{OUT})
- IMON Function
- Selectable Load Line
- Adjustable Current Limit (I_{LIMIT})
- 800kHz Fixed Switching Frequency (f_{SW})
- Adaptive Constant-On-Time (COT) Control for Fast Transient Response
- Remote Differential Sense
- Stable with POSCAP and Ceramic Capacitors
- Internal Soft Start (SS)
- Output Discharge
- Over-Current Limitation (OCL), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), and Thermal Shutdown
- Available in a QFN-19 (3mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive System-on-Chip (SoC) Power for Advanced Driver-Assistance Systems (ADAS) and Infotainment Systems

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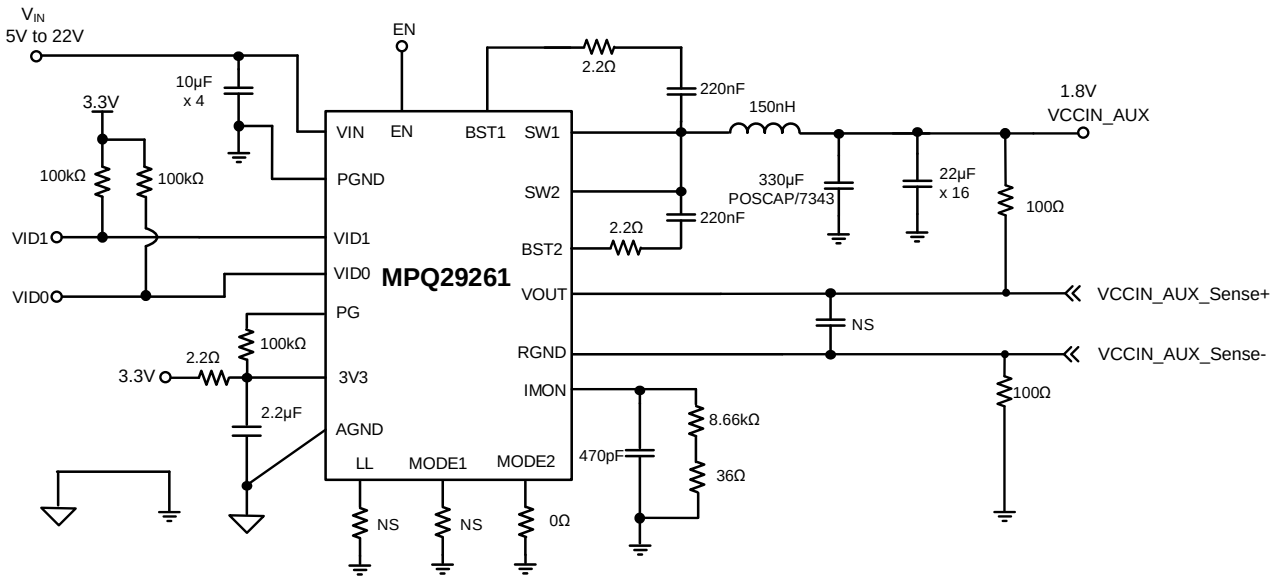
TYPICAL APPLICATION (1) (2)



Notes:

1) f_{SW} = 800kHz, I_{LIMIT} = 20.5A/phase, LL = 1.2mΩ, VID decay down mode.
2) The VID1 and VID0 pins are recommended to pulled up to 3.3V or 1.8V via 100kΩ resistors.

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ29261GLE-AEC1	QFN-19 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ29261GLE-AEC1-Z).

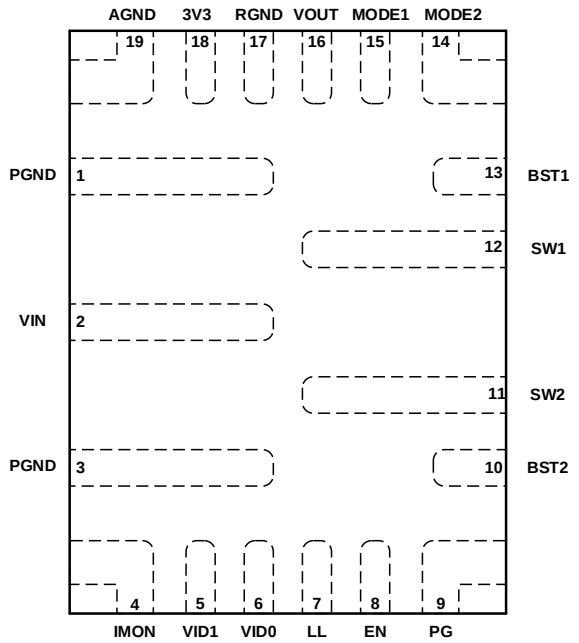
TOP MARKING

MPYW
2926
1LLL
E

MP: MPS prefix
Y: Year code
W: Week code
29261: Part number
LLL: Lot number
E: Wettable Flank

PACKAGE REFERENCE

TOP VIEW



QFN-19 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 3	PGND	**Power ground**. Connect PGND to the PCB's ground layer (GND) using wide PCB traces and multiple vias.
2	VIN	**Input voltage**. The VIN pin supplies power to the internal MOSFET and converter. The MPQ29261 operates from a 4.5V to 22V input rail. Use a decoupling input capacitor (C_{IN}) to decouple the input rail. Use wide PCB traces and multiple vias to make the VIN connection.
4	IMON	**Output current signal.** The IMON pin sources a current proportional to the sensed output load current. Connect an external resistor between the IMON pin and the GND layer to form a voltage. Do not float IMON.
5	VID1	**Bit[1] of the 2-bit VID.** The VID1 pin supports the VID table.
6	VID0	**Bit[0] of the 2-bit VID.** The VID0 pin supports the VID table.
7	LL	**Selectable load line.** Connect the LL and GND layer via a resistor to select one of the four load-line scales.
8	EN	**Enable.** The EN pin is a digital input pin that enables and disables the internal converter. Pull EN high to turn the converter on; pull EN low to turn it off.
9	PG	**Power good output.** The PG pin is an open-drain signal. If the output voltage (V_{OUT}) is within its proper range, then PG is pulled high.
10	BST2	**Bootstrap 2.** Connect a capacitor between the SW2 and BST2 pins to form a floating supply across the high-side MOSFET (HS-FET) driver.
11	SW2	**Switch output 2.** Connect SW2 to the inductor and the bootstrap capacitor (C_{BST}). SW2 is connected to VIN while the HS-FET is on, and is connected to PGND while the low-side MOSFET (LS-FET) is on. Use short and wide PCB traces to make the SW2 connection. SWx is noisy, and should be routed away from sensitive traces.
12	SW1	**Switch output 1.** Connect SW1 to the inductor and C_{BST}. SW1 is connected to VIN while the HS-FET is on, and is connected to PGND while the LS-FET is on. Use short and wide PCB traces to make the SW1 connection. SWx is noisy, and should be routed away from sensitive traces.
13	BST1	**Bootstrap 1.** Connect a capacitor between the SW1 and BST1 pins to form a floating supply across the HS-FET driver.
14	MODE2	**Mode selection 2.** The MODE2 pin selects the LS-FET valley current limit (I_{LIMIT_LS}) (17.5A or 20.5A). See Table 2 on page 16 for more details.
15	MODE1	**Mode selection 1.** The MODE1 pin selects the VID mode (decay down mode or slew down mode). See Table 1 on page 16 for more details.
16	VOUT	**Output sense+ (positive remote-sense input).** The VOUT pin is the positive remote-sense input. Connect VOUT to the VR's output directly at the load. Route VOUT with RGND differentially.
17	RGND	**Output sense- (remote-sense return input).** The RGND pin is the remote-sense return input. Connect RGND to ground directly at the load. Route RGND with VOUT differentially.
18	3V3	**External 3V3 VCC input for the controls and driver.** Place a 2.2µF decoupling capacitor close to the 3V3 and AGND pins. If connecting an external power supply, connect a 2.2Ω resistor in series to form an RC filter.
19	AGND	**Analog ground.** The internal reference is referred to the AGND pin. A Kelvin connection to PGND is required.

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ABSOLUTE MAXIMUM RATINGS (3)

Input voltage (V_{IN}) 28V
V_{SW1}, V_{SW2} (DC) .....-0.3V to +25V
V_{SW1}, V_{SW2} (25ns).....-3.6V to +28V
V_{BST1}, V_{BST2} ..... V_{SW} + 4.5V
All other pins .....-0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (4)
QFN-19 (3mmx4mm) 3.1W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (5)

Human body model (HBM) ……. Class 2
Charged-device model (CDM)……Class C2B

Recommended Operating Conditions (6)

Input voltage (V_{IN}) .....4.5V to 22V
Supply voltage (V_{CC}) .....3.15V to 3.5V
Output voltage (V_{OUT}).....0V to 1.8V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (7) θ_{JA} θ_{JC}

QFN-19 (3mmx4mm)..... 40 ..... 8.... °C/W

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{3V3} = 3.3V, R_{MODE1} = 0Ω, VID1 = 1, VID0 = 1, T_J = 25°C for typical values and T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (External 3V3)						
3V3 current	I_{3V3}	V_{EN} = 3V, V_{OUT} = 1.9V		190		µA
3V3 shutdown current	I_{3V3_SD}	V_{EN} = 0V, no load, T_J = 25°C			2	µA
MOSFET (per Phase)						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	T_J = 25°C		12		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	T_J = 25°C		5.4		mΩ
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW1} = 0V, T_J = 25°C		0	1	µA
Current Limit (per Phase)						
LS-FET valley current limit	I_{LIMIT_LS}	R_{MODE2} = 0Ω	15.5	20.5	23.5	A
		R_{MODE2} = 150kΩ		17.5		A
Frequency						
Switching frequency	f_{SW}	V_{IN} = 6V, R_{MODE2} = 0Ω		800		kHz
Constant-on-time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.8V, R_{MODE2} = 0Ω	410	475	570	ns
Minimum on time (8)	t_{ON_MIN}			40		ns
Minimum off time (8)	t_{OFF_MIN}			150		ns
Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}		2.15	2.25	2.35	V
UVP1 threshold	V_{UVP1}		70	75	80	% of V_{REF}
UVP1 foldback timer (8)	t_{UVP1}			30		µs
UVP2 threshold	V_{UVP2}		45	55	60	% of V_{REF}
IMON Accuracy						
Current-gain accuracy	I_{MON} / I_{OUT}	8A < I_{SW} < 18A, T_J = 25°C	3.85		4.09	µA/A
Reference, Soft Start (SS), and Soft Shutdown						
Reference voltage	$V_{REFERENCE}$	VID1 = 0, VID0 = 0		0		V
		VID1 = 0, VID0 = 1		1.1		V
		VID1 = 1, VID0 = 0		1.65		V
		VID1 = 1, VID0 = 1	1.764	1.8	1.82	V
Soft-start time	t_{SS}	EN rising edge to PG is pulled high			250	µs
MODE1, MODE2, and LL						
MODE1 current	I_{MODE1}		8.7	10	11.5	µA
MODE2 current	I_{MODE2}		8.7	10	11.5	µA
LL current	I_{LL}		8.7	10	11.5	µA
VID1 and VID0						
VIDx low voltage	V_{IDx_LOW}				0.3	V
VIDx high voltage	V_{IDx_HIGH}		0.6			V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{3V3} = 3.3V, R_{MODE1} = 0Ω, VID1 = 1, VID0 = 1, T_J = 25°C for typical values and T_J = -40°C to +125°C for max and min values, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable (EN) and Under-Voltage Lockout (UVLO) Protection						
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN hysteresis	V_{EN_HYS}			125		mV
EN current	I_{EN}	V_{EN} = 2V			5	µA
		V_{EN} = 0V			1	
V_{CC} UVLO rising threshold	$V_{CC_UVLO_RISING}$		2.8	2.95	3.1	V
V_{CC} UVLO hysteresis	$V_{CC_UVLO_HYS}$			250		mV
V_{IN} UVLO rising threshold	$V_{IN_UVLO_RISING}$			4.1	4.4	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			400		mV
Power Good (PG)						
PG when V_{FB} rising (good)	$V_{PG_RISING_GOOD}$	V_{FB} rising		95		% of V_{REF}
PG when V_{FB} falling (fault)	$V_{PG_FALLING_GOOD}$	V_{FB} falling		90		
PG low to high delay	t_{PG}			5	10	µs
EN low to PG low delay	t_{EN_PG}				10	µs
PG sink current capability	V_{PG_SINK}	4mA sink			0.4	V
Thermal protection						
Thermal shutdown (8)	T_{SD}			155		°C
Thermal shutdown hysteresis (8)	T_{SD_HYS}			25		°C

Note:

8) Guaranteed by design.

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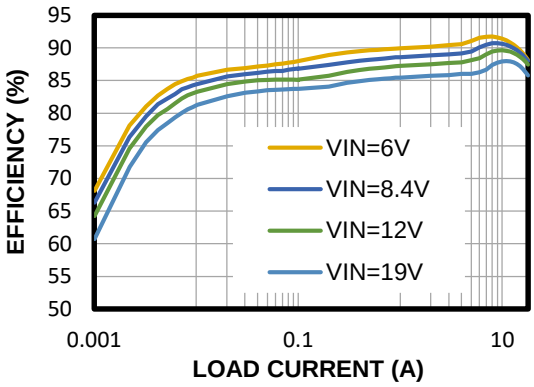
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 800kHz, L = 150nH, DCR = 1.8mΩ, C_{OUT} = 330µF POSCAP + 16 x 22µF ceramic, T_A = 25°C, unless otherwise noted.

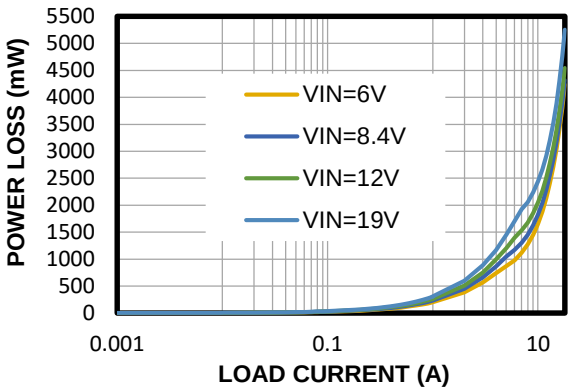
Efficiency vs. Load Current

f_{SW} = 800kHz, L = 150nH, V_{OUT} = 1.8V



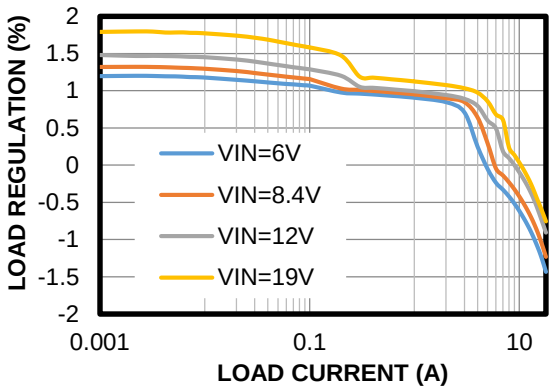
Power Loss vs. Load Current

f_{SW} = 800kHz, L = 150nH, V_{OUT} = 1.8V



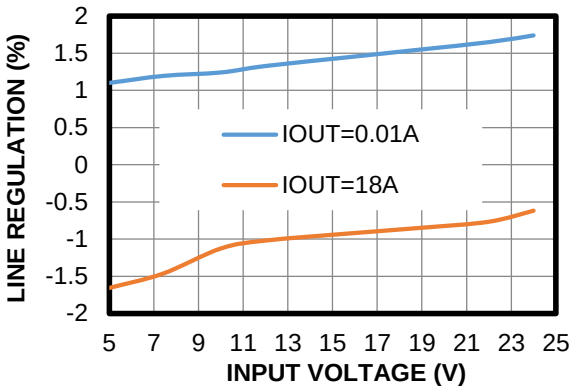
Load Regulation

f_{SW} = 800kHz, L = 150nH, V_{OUT} = 1.8V



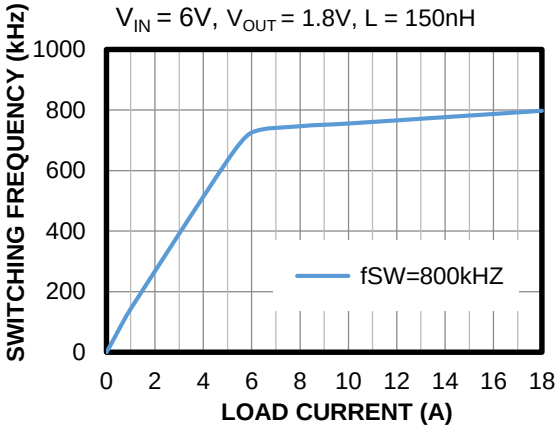
Line Regulation

f_{SW} = 800kHz, L = 150nH, V_{OUT} = 1.8V



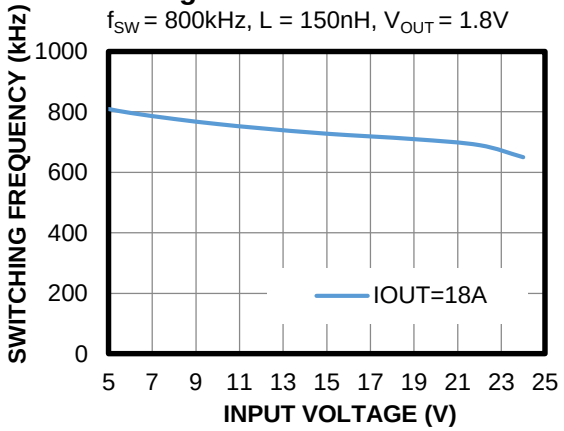
Switching Frequency vs. Load Current

V_{IN} = 6V, V_{OUT} = 1.8V, L = 150nH



Switching Frequency vs. Input Voltage

f_{SW} = 800kHz, L = 150nH, V_{OUT} = 1.8V



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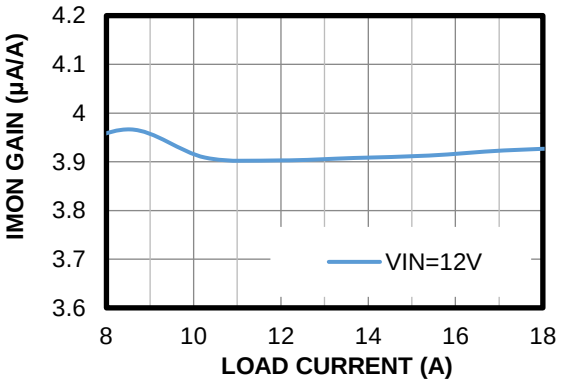
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 800kHz, L = 150nH, DCR = 1.8mΩ, C_{OUT} = 330µF POSCAP + 16 x 22µF ceramic, T_A = 25°C, unless otherwise noted.

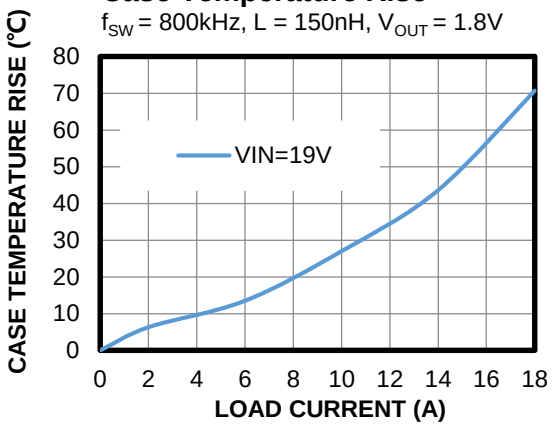
IMON Gain vs. Load Current

f_{SW} = 800kHz, L = 150nH, V_{OUT} = 1.8V



Case Temperature Rise

f_{SW} = 800kHz, L = 150nH, V_{OUT} = 1.8V



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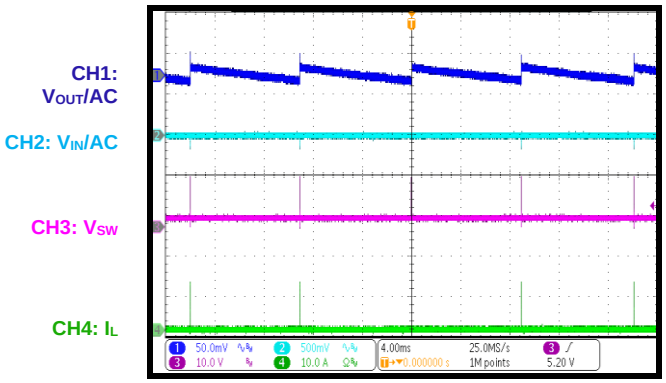
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 800kHz, L = 150nH, DCR = 1.8mΩ, C_{OUT} = 330µF POSCAP + 16 x 22µF ceramic, T_A = 25°C, unless otherwise noted.

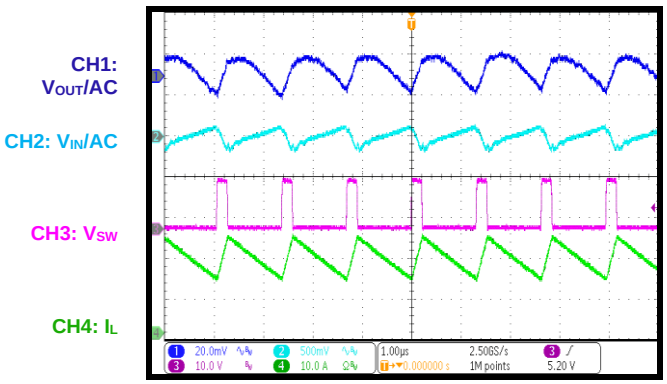
Input/Output Voltage Ripple

I_{OUT} = 0.001A



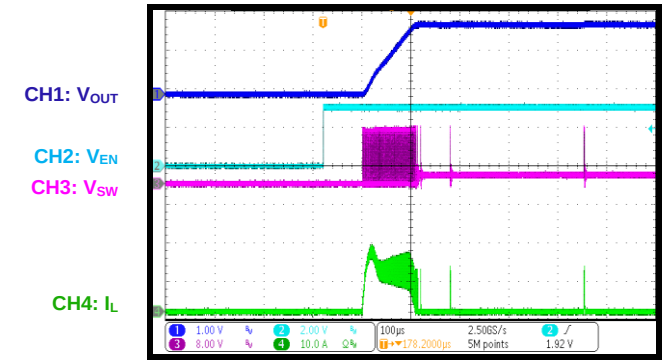
Input/Output Voltage Ripple

I_{OUT} = 18A



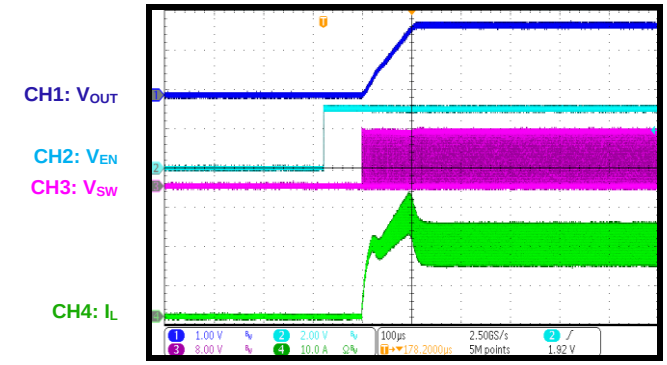
Start-Up through EN

I_{OUT} = 0A



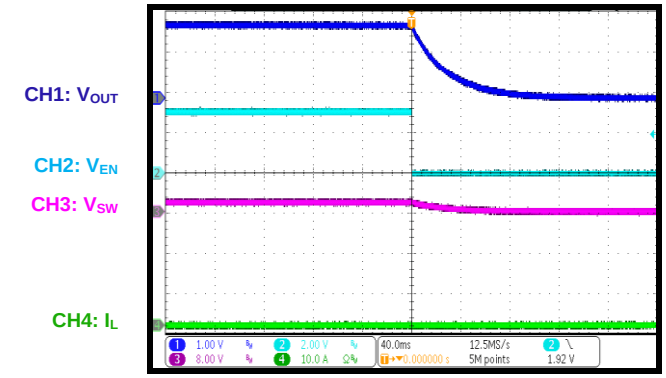
Start-Up through EN

I_{OUT} = 18A



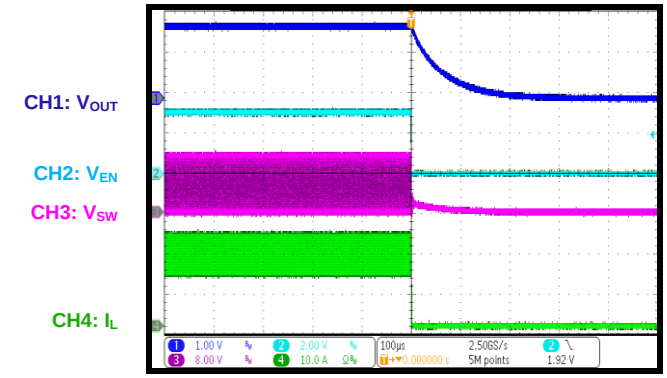
Shutdown through EN

I_{OUT} = 0A



Shutdown through EN

I_{OUT} = 18A



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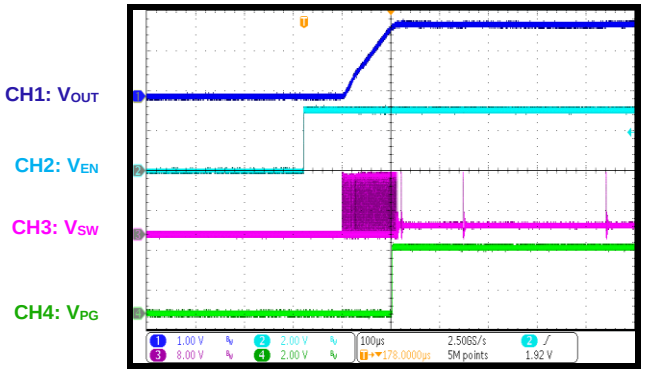
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 800kHz, L = 150nH, DCR = 1.8mΩ, C_{OUT} = 330µF POSCAP + 16 x 22µF ceramic, T_A = 25°C, unless otherwise noted.

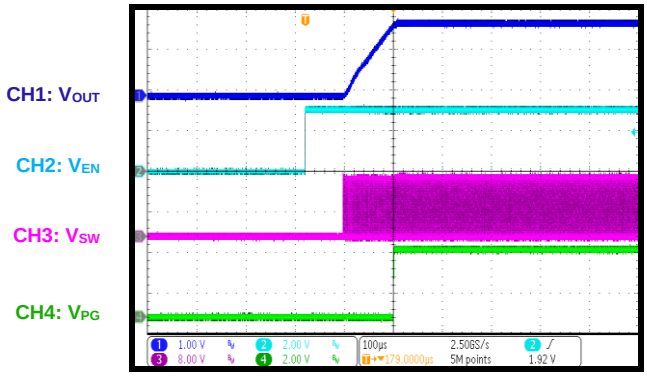
PG Start-Up through EN

I_{OUT} = 0A



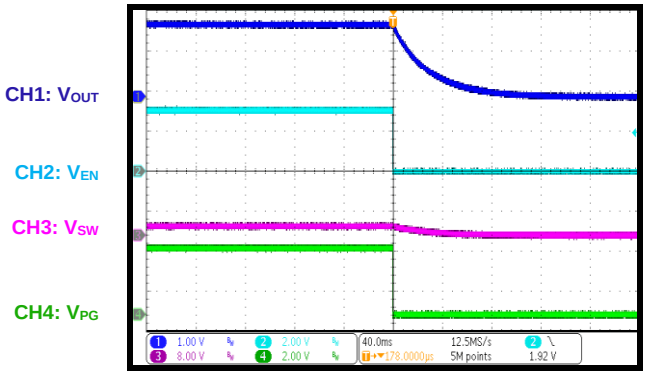
PG Start-Up through EN

I_{OUT} = 18A



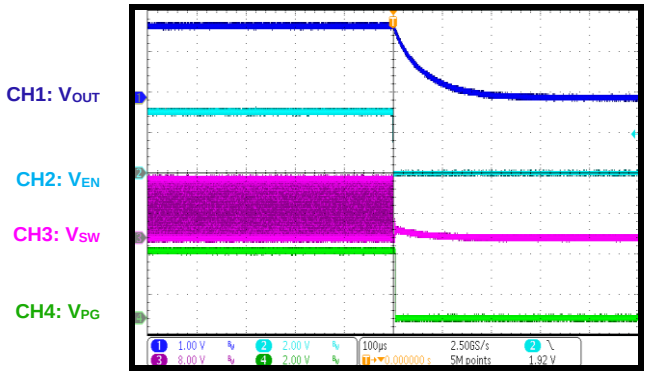
PG Shutdown through EN

I_{OUT} = 0A



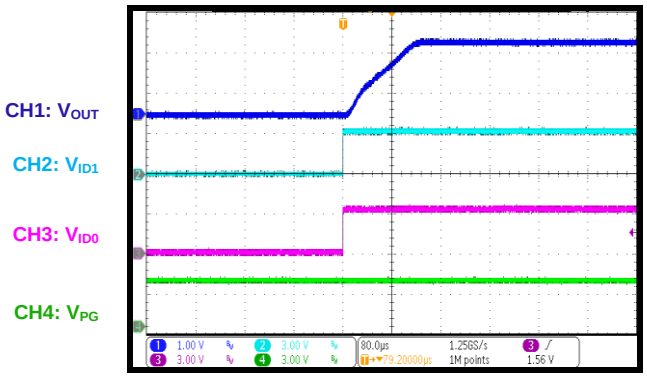
PG Shutdown through EN

I_{OUT} = 18A



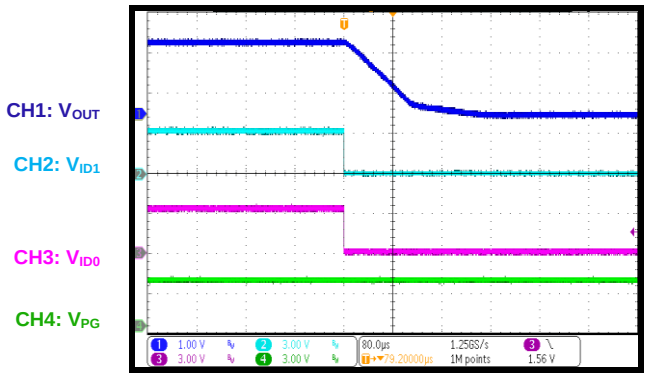
DVID

I_{OUT} = 2A, slew down mode, V_{OUT} = 0V to 1.8V, [VID1, VID0] = [0, 0] to [1, 1]



DVID

I_{OUT} = 2A, slew down mode, V_{OUT} = 1.8V to 0V, [VID1, VID0] = [1, 1] to [0, 0]



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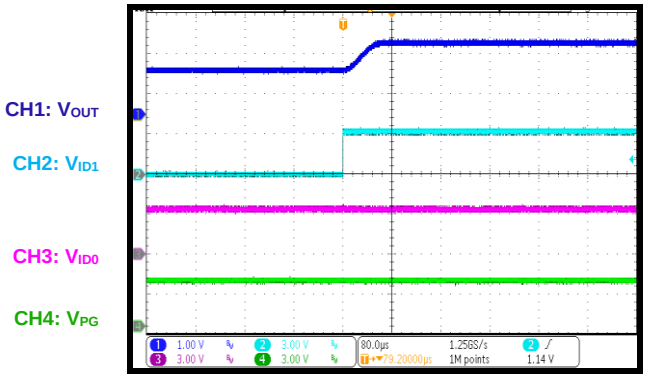
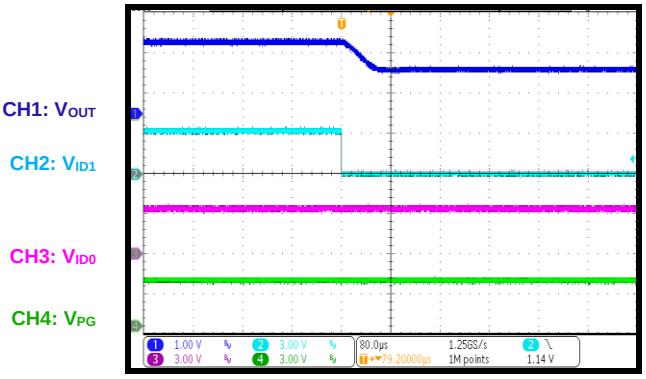
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 800kHz, L = 150nH, DCR = 1.8mΩ, C_{OUT} = 330µF POSCAP + 16 x 22µF ceramic, T_A = 25°C, unless otherwise noted.

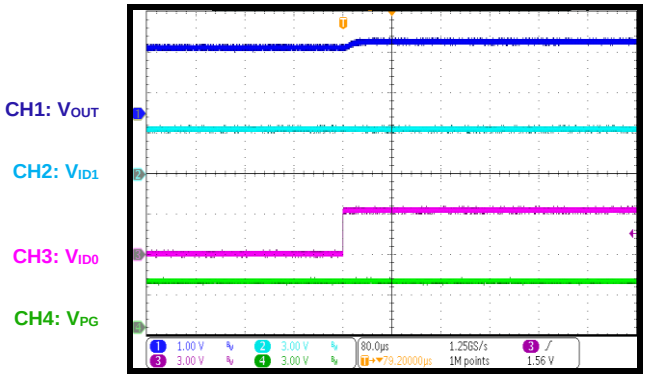
DVID
I_{OUT} = 2A, [VID1, VID0] = [0, 1] to [1, 1],
slew down mode, V_{OUT} = 1.1V to 1.8V



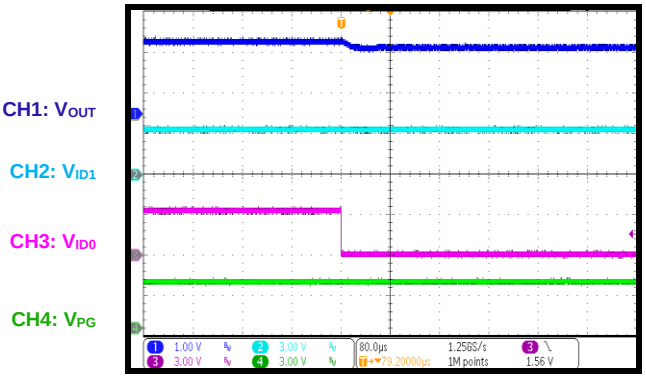
DVID
I_{OUT} = 2A, [VID1, VID0] = [1, 1] to [0, 1],
slew down mode, V_{OUT} = 1.8V to 1.1V



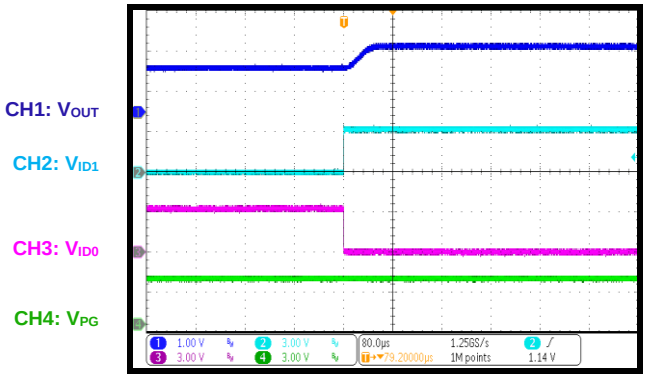
DVID
I_{OUT} = 2A, [VID1, VID0] = [1, 0] to [1, 1],
slew down mode, V_{OUT} = 1.65V to 1.8V



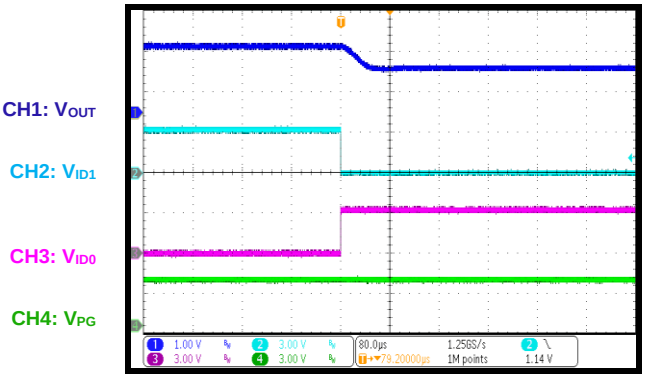
DVID
I_{OUT} = 2A, [VID1, VID0] = [1, 1] to [1, 0],
slew down mode, V_{OUT} = 1.8V to 1.65V



DVID
I_{OUT} = 2A, [VID1, VID0] = [0, 1] to [1, 0]
slew down mode, V_{OUT} = 1.1V to 1.65V



DVID
I_{OUT} = 2A, [VID1, VID0] = [1, 0] to [0, 1],
slew down mode, V_{OUT} = 1.65V to 1.1V



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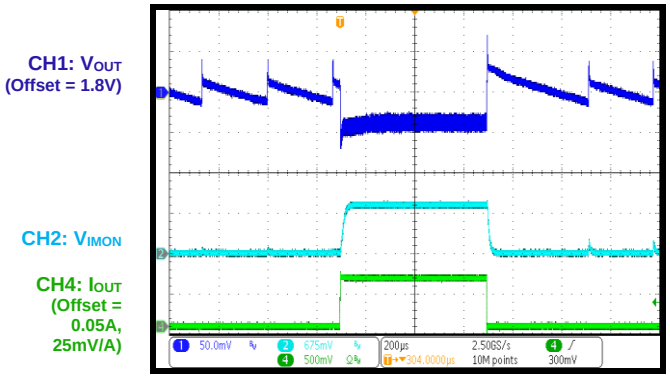
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 800kHz, L = 150nH, DCR = 1.8mΩ, C_{OUT} = 330µF POSCAP + 16 x 22µF ceramic, T_A = 25°C, unless otherwise noted.

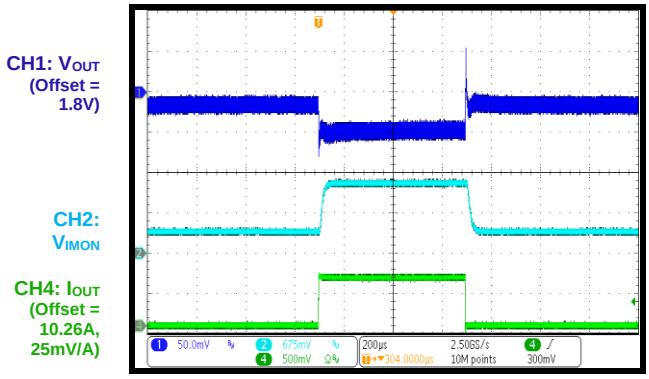
Transient Response

I_{OUT} = 0.05A to 24.01A, d_T = 250ns,
R_{IMON} = 8.66kΩ



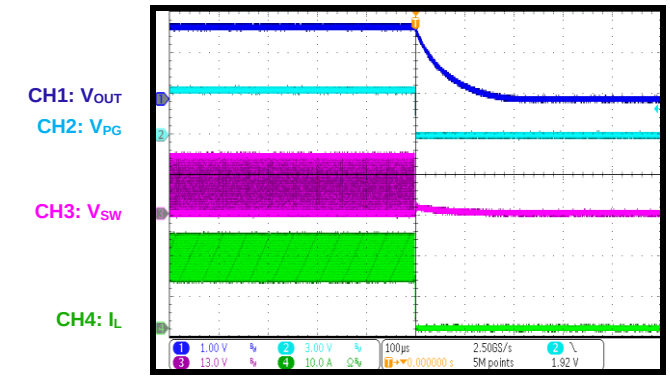
Transient Response

I_{OUT} = 10.26A to 34.2A, d_T = 250ns,
R_{IMON} = 8.66kΩ



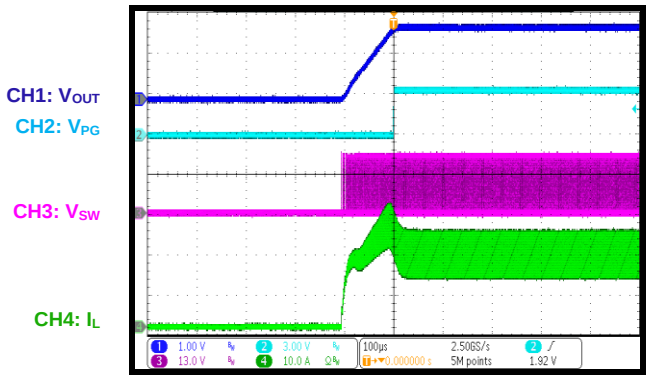
Thermal Shutdown

V_{IN} = 19V, initial current = 18A



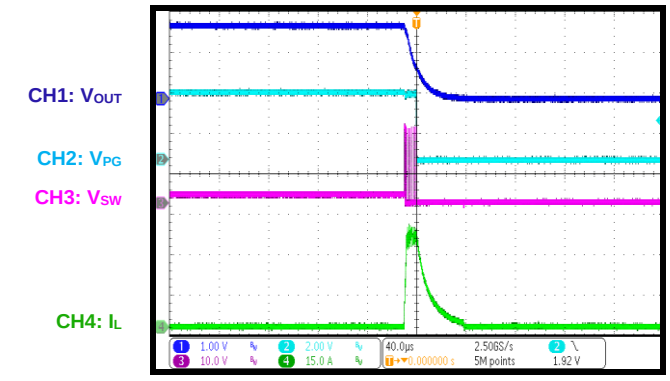
Thermal Recovery

V_{IN} = 19V, initial current = 18A



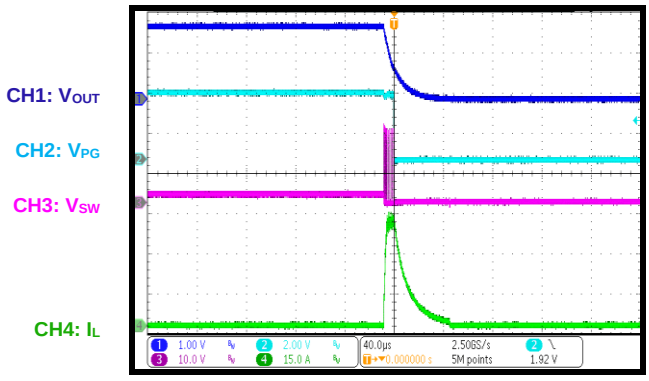
Short-Circuit Protection

V_{IN} = 19V, I_{LIMIT_LS} = 17.5A per phase



Short-Circuit Protection

V_{IN} = 19V, I_{LIMIT_LS} = 20.5A per phase



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FUNCTIONAL BLOCK DIAGRAM

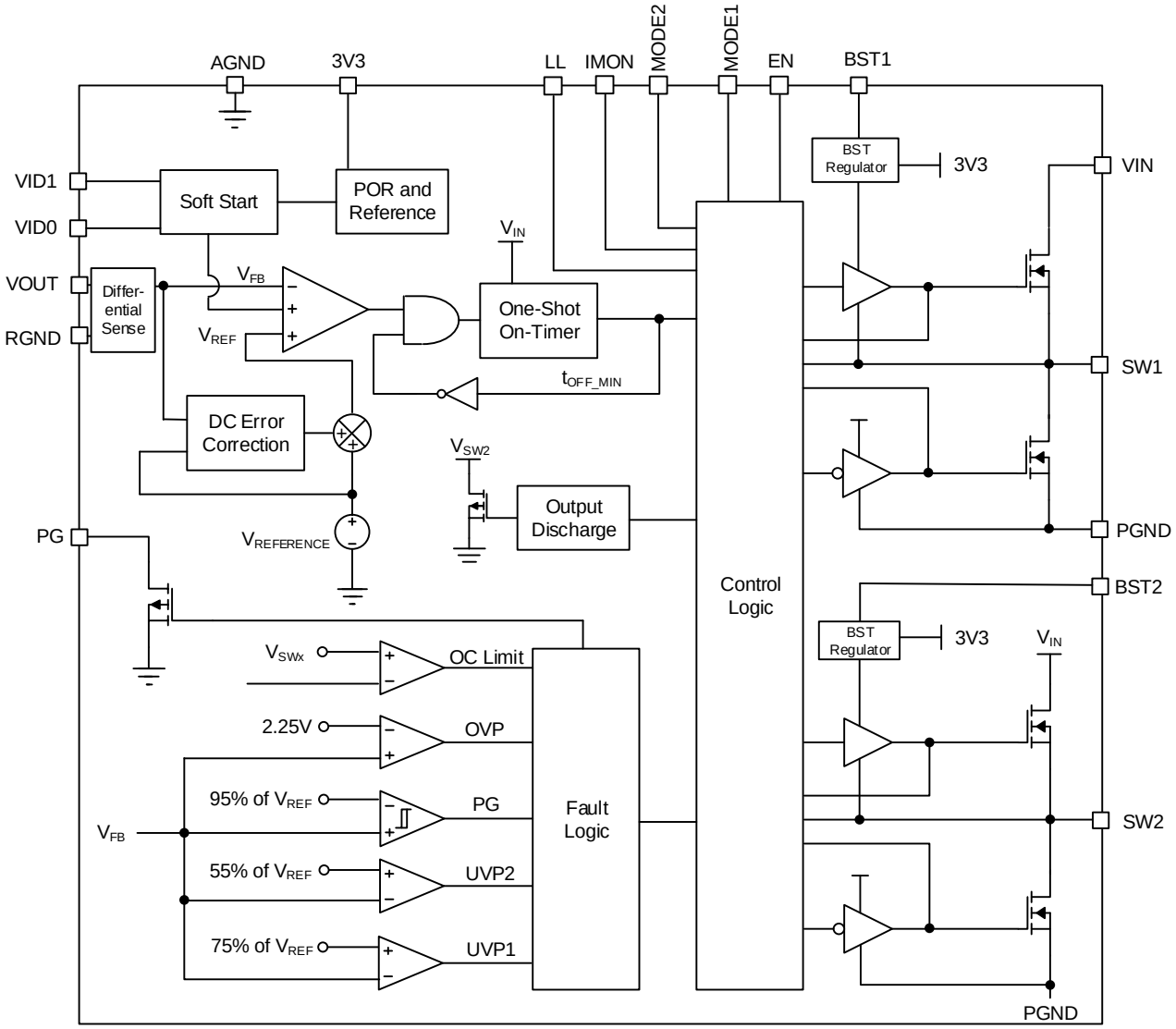

Figure 1: Functional Block Diagram

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OPERATION

Pulse-Width Modulation (PWM) Mode

The MPQ29261 is a fully integrated, synchronous, rectified, step-down switch-mode converter with 2-bit voltage identification (VID) and an adjustable current limit (I_{LIMIT}). Constant-on-time (COT) control provides fast transient response and eases loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on once the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}) due to an insufficient output voltage (V_{OUT}). The on time (t_{ON}) is determined by both the input voltage (V_{IN}) and V_{OUT} to maintain a constant switching frequency (f_{SW}) across the entire V_{IN} range.

Once t_{ON} is complete, the HS-FET turns off. It turns on again once V_{FB} drops below V_{REF}. The converter regulates V_{OUT} by repeating this operation.

To minimize conduction loss, the integrated low-side MOSFET (LS-FET) turns on once the HS-FET turns off. If both the HS-FET and the LS-FET turn on simultaneously, then a dead short occurs between the input and PGND. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off time (t_{OFF}) and the LS-FET t_{ON}, and vice versa.

COT control with internal compensation provides stable operation, even when using ceramic capacitors as output capacitors. Internal compensation reduces jitter without affecting load and line regulation.

Continuous Conduction Mode (CCM)

The part operates in continuous conduction mode (CCM) while the output current (I_{OUT}) is high and the inductor current (I_L) exceeds 0A (see Figure 2).

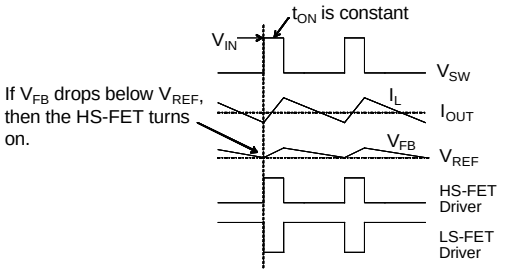

Figure 2: Continuous Conduction Mode (CCM)

If V_{FB} drops below V_{REF}, then the HS-FET turns on for a fixed interval determined by the one-shot on-timer. Once the HS-FET turns off, the LS-FET turns on until the next period. f_{SW} remains fairly constant in CCM (PWM mode).

Discontinuous Conduction Mode (DCM)

I_L decreases as the load decreases. Once the I_L reaches 0A, the MPQ29261 exits CCM and enters discontinuous conduction mode (DCM) (see Figure 3).

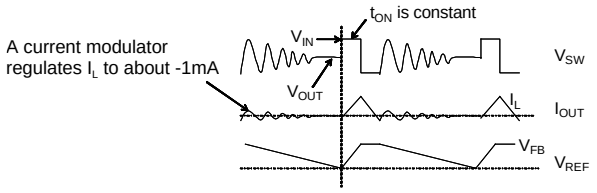

Figure 3: Discontinuous Conduction Mode (DCM)

If V_{FB} drops below V_{REF}, then the HS-FET turns on for a fixed interval determined by the one-shot on-timer. Once HS-FET turns off, the LS-FET turns on until I_L reaches 0A. In DCM, V_{FB} does not reach V_{REF} as I_L reaches 0A. The LS-FET driver enters a high-impedance (Hi-Z) state once I_L reaches 0A. A current modulator takes control of the LS-FET and limits I_L below -1mA, and the output capacitors discharge to PGND slowly via the LS-FET. This improves efficiency during light-load operation. The HS-FET does not turn on as frequently under light-load conditions as it does under heavy-load conditions.

The device achieves high efficiency at light loads and no load by dropping V_{OUT} slowly to reduce f_{SW}. As the load increases, the current modulator regulation time decreases. The HS-FET turns on more frequently, and f_{SW} increases accordingly. I_{OUT} reaches its critical level once the current modulator time reaches 0A. The critical level of I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device enters CCM once I_{OUT} exceeds its critical level. Then f_{SW} remains fairly constant across the entire CCM range.

Jitter and Feedback (FB) Ramp

Jitter occurs in both PWM mode and pulse-skip

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mode (PSM) while noise in the V_{FB} ripple propagates a delay to the HS-FET driver. Figure 4 shows jitter in PWM mode.

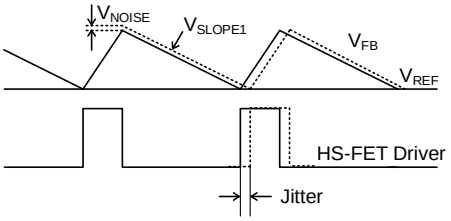

Figure 4: Jitter in PWM Mode

Figure 5 shows jitter in PSM.

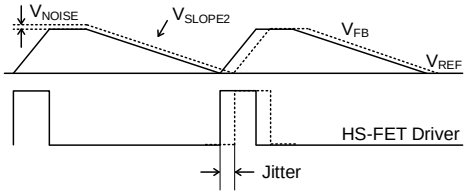

Figure 5: Jitter in PSM

Jitter affects system stability, and its noise immunity is proportional to the steepness of the V_{FB} downward slope. Jitter in DCM is typically larger than that in CCM. The V_{FB} ripple does not affect noise immunity directly.

Operation without External Ramp Compensation

Traditional COT control schemes are intrinsically unstable if the ESR of the output capacitor (C_{OUT}) is not large enough to act as an effective current-sense resistor. Ceramic capacitors cannot typically be used as output capacitors.

The MPQ29261 has built-in internal ramp compensation to ensure that the system is stable, even when using ceramic capacitors as output capacitors. This allows for a pure ceramic capacitor solution, which reduces the output voltage ripple, the total bill of materials (BOM) cost, and the required board area.

When using a large output capacitor (e.g. POSCAP), place a >10µF ceramic capacitor in parallel to minimize the effect of the equivalent series inductance (ESL).

VID Slew Down Mode and Decay Down Mode

The MODE1 pin selects the VID down mode (slew down mode or decay down mode) via a resistor (R_{MODE1}) (see Table 1).

Table 1: MODE1 Selection

State	VID Down Mode	R_{MODE1}
Option 1	Slew down mode	0Ω
Option 2	Decay down mode	>230kΩ or floating

Short SW1 and SW2 together. Do not float SW1 and SW2.

Adjustable Current Limit

The MPQ29261 valley current limit (I_{LIMIT_LS}) can be set via the MODE2 resistor (R_{MODE2}). The adjustable I_{LIMIT} allows for flexible design in application. Table 2 shows the recommended resistor values for the different current limits.

Table 2: MODE2 Selection

State	f_{SW}	I_{LIMIT_LS}	R_{MODE2}
Option 1	800kHz	20.5A	0Ω
Option 2	800kHz	17.5A	150kΩ

2-Bit Voltage Identification (VID)

The MPQ29261 employs 2-bit VID, which follows Intel specifications. The VID1 and VID0 pins are recommended to be pulled up to 3.3V or 1.8V via 100kΩ resistors. Table 3 shows the VIDx control bit logic.

Table 3: VIDx Control Bit Logic

VID1	VID0	V_{OUT} (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

VID Change Mode

VID can change from low to high (0 to 1) (VID rising) or from high to low (1 to 0). If VID rises from low to high, then V_{OUT} rises with a 15mV/µs slew rate.

There are two modes for a VID high-to-low change (slew down mode and decay down mode). The VID down mode can be selected via the MODE1 pin (see the VID Slew Down Mode and Decay Down Mode section. In slew down mode, V_{OUT} drops at 15mV/µs, which is the same slew rate at which VID rises. In decay down mode, V_{OUT} does not have a fixed slew rate, and instead drops with the output load.

Current-Sense Output (IMON)

IMON is a unidirectional current source that is proportional to I_{OUT}. Connect a resistor and a

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capacitor between the IMON pin and the PGND layer to form a voltage proportional to I_{OUT} (see Figure 6).

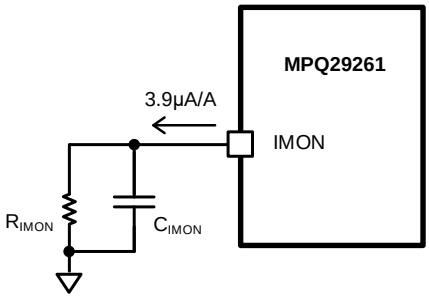

Figure 6: IMON Pin Set-Up

Choose the IMON resistor (R_{IMON}) value to set the IMON voltage (V_{IMON}) within the desired range. R_{IMON} can be calculated with Equation (2):

$$R_{IMON} = \frac{V_{IMON_MAX}}{K_{IMON} \times I_{CC_MAX}} \quad (2)$$

Where K_{IMON} is the current-sense gain proportional to I_{OUT} (3.9μA/A), and V_{IMON_MAX} is the voltage corresponding to the maximum I_{OUT} (<2.5V).

For example, if the MPQ29261 is used in design with devices (e.g. the MPQ29164) for an I_{CC_MAX} of 34.2A, then V_{IMON_MAX} is recommended to be 1.16V. This means that R_{IMON} is 8.7kΩ.

The IMON capacitor (C_{IMON}) smooths V_{IMON}. It is recommended that C_{IMON} be about 470pF.

The IMON output has two states (enabled and disabled) (see Table 4). If the VID output is 1.1V or 0V, then the IMON function is disabled. It takes about 10μs to enable the IMON function once the VID output is either in the 1.65V or 1.8V state.

Table 4: IMON Function Active

VID1	VID0	IMON
0	0	Disabled
0	1	Disabled
1	0	Enabled
1	1	Enabled

Static Load-Line (LL) Selection

The MPQ29261 has a static load line that can be selected by connecting the LL pin to ground via a resistor (R_{LL}). Table 5 shows the recommended resistor values for static load-line selection.

Table 5: Static Load-Line Selection

State	Load Line	R_{LL}
Option 1	0.8mΩ	150kΩ
Option 2	1.2mΩ	>230kΩ or floating
Option 3	1.6mΩ	0Ω
Option 4	2mΩ	90.9kΩ

Power Good (PG)

The MPQ29261 has a power good (PG) output that indicates whether V_{OUT} is ready. PG is the open drain of a MOSFET. Connect PG to VCC or another voltage source via a resistor (e.g. 100kΩ). Once V_{IN} is applied, the MOSFET turns on, and PG is pulled to ground before soft start (SS) is ready. If V_{FB} exceeds 95% of V_{REF}, then PG is pulled high after a delay time (t_{PG}) (about 10μs). If V_{FB} drops below 90% of V_{REF}, PG is pulled low.

If [VID1, VID0] changes from a non-zero VID to [0, 0], PG remains high.

Soft Start (SS)

The MPQ29261 employs soft start (SS) to ensure that V_{OUT} ramps up smoothly during start-up. The start-up slew rate is set similar to the VID rising slew rate. If the EN voltage (V_{EN}) goes high, then V_{OUT} ramps up by slowly following the internal V_{REF}. Once V_{REF} reaches the target value, soft start finishes, and the part enters steady-state operation.

Figure 7 shows the start-up sequence and the VID change.

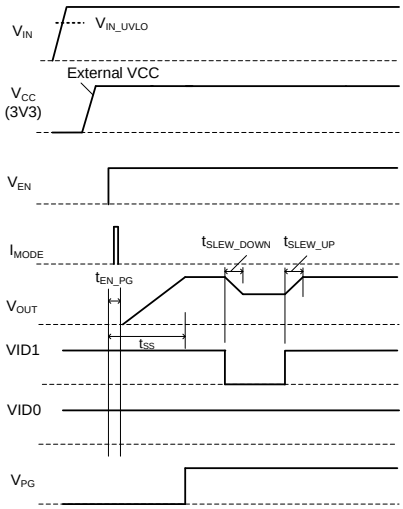

Figure 7: Start-Up Sequence and VID Change

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If the output is pre-biased to a certain voltage during start-up, both the HS-FET and the LS-FET turn off until the internal V_{REF} exceeds the sensed output voltage.

If the [VID1, VID0] = [0, 0] during start-up, then the part waits for a non-zero VID, and PG is not asserted before the V_{OUT} reaches the effective non-zero VID.

Output Discharge

If the part is shut down through EN or via a protection function (e.g. under-voltage protection (UVP), over-voltage protection (OVP), V_{IN} under-voltage lockout (UVLO), or thermal shutdown), then the device discharges the output via an internal circuit with a <50mA discharge current.

Over-Current Limitation (OCL)

The MPQ29261 has cycle-by-cycle over-current limiting for each phase. The current-limit circuit employs a valley current-sense algorithm. The part uses the LS-FET's on resistance as a current-sense element. If the magnitude of the current-sense signal exceeds I_{LIMIT_LS}, then the PWM comparator cannot initiate a new cycle, even if V_{FB} is below V_{REF}. Figure 8 shows the valley current limit control.

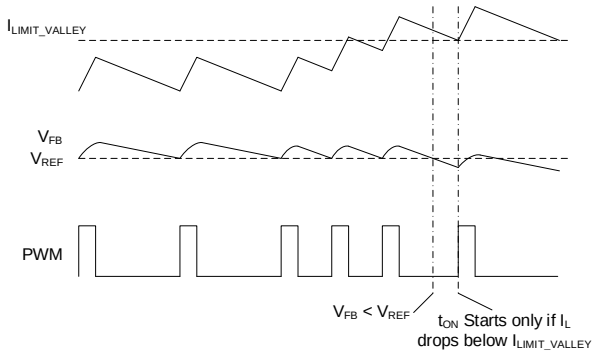

Figure 8: Valley Current-Limit Control

Since the comparison occurs while the LS-FET on, the OC trip level sets the valley level of I_L. The maximum load current (I_{LOAD_MAX}) can be calculated with Equation (3):

$$I_{LOAD_MAX} = 2 \times I_{LIMIT} + \frac{\Delta I_L}{2} \quad (3)$$

The over-current threshold (I_{OC}) limits the inductor current and does not latch off.

If an over-current fault occurs, the load current exceeds the current to C_{OUT}, and V_{OUT} drops. If V_{OUT} drops below the UVP threshold, then the part latches off. The fault latch can be reset by V_{EN} going low or by cycling the power on VIN.

Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)

The MPQ29261 monitors the V_{OUT} to detect over-voltage (OV) and under-voltage (UV) conditions. The output has an absolute OVP threshold (2.25V), which is active while the system is on. If V_{OUT} exceeds 2.25V, then the OVP comparator output goes high, and the part latches with the output discharge circuit on.

If V_{OUT} is between 55% and 75% of V_{REF}, then the UVP1 comparator output goes high. The part latches if V_{OUT} stays within this range for about 30µs (the HS-FET latches off and the LS-FET latches on). The LS-FET remains on until I_L reaches 0A. During this period, I_{LIMIT_LS} helps control I_L.

If V_{OUT} drops below 55% of V_{REF}, then the UVP2 comparator output goes high, and the part latches off after the comparator and logic delay (the HS-FET latches off and the LS-FET latches on). The LS-FET remains on until I_L reaches 0A. The fault latch can be reset by V_{EN} going low or cycling the power on VIN.

Under-Voltage Lockout (UVLO)

The MPQ29261 has two UVLO thresholds: a V_{CC} UVLO threshold (2.95V) and a V_{IN} UVLO threshold (4.1V). The part starts up once both V_{CC} and V_{IN} exceed their respective UVLO thresholds. The part shuts down if either V_{CC} or V_{IN} drops below their respective falling threshold. Both UVLO protections are non-latch protections.

If an application requires a higher UVLO threshold, adjust the V_{IN} UVLO threshold via an external resistor divider (R_{UP} + R_{DOWN}) (see Figure 9 on page 19).

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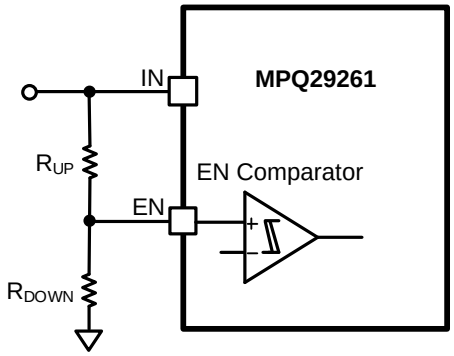

Figure 9: Adjustable UVLO Protection

Thermal Shutdown

The MPQ29261 monitors the junction temperature (T_J) internally. If T_J exceeds the thermal shutdown threshold (typically 155°C), then the converter shuts down. Once T_J drops to about 130°C, the device initiates a soft start and resumes normal operation. There is a 25°C hysteresis. Thermal shutdown is a non-latch protection.

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APPLICATION INFORMATION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for optimal performance and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors require a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs when V_{IN} = 2 x V_{OUT}, calculated with Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs when V_{IN} = 2 x V_{OUT}, calculated with Equation (7):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (7)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} + \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (8)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The voltage generated from the ESR dominates the output ripple. The output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

The maximum C_{OUT} limitation should be considered in design application. The MPQ29261 has a VID ramp-up time (t_{RAMP}, about 0.15ms). If C_{OUT} is too high, V_{OUT} cannot reach the design value during t_{RAMP}, and the device fails to regulate V_{OUT}. The maximum C_{OUT} (C_{OUT_MAX}) can be estimated with Equation (11):

$$C_{OUT_MAX} = (I_{LIMIT_AVG} - I_{OUT}) \times t_{RAMP} / V_{OUT} \quad (11)$$

Where I_{LIMIT_AVG} is the average ramp-up current during t_{RAMP}, which can be equivalent to I_{LIMIT}.

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, a larger-value inductor is physically larger, has a higher series resistance, and has a lower saturation current.

To determine the inductance value, set the peak-to-peak ripple current in the inductor to be

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between 30% to 50% of the maximum output current. Set the peak inductor current below the maximum switch current limit. The inductance can be calculated with Equation (12):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum I_{L_PEAK} (including the short current). It is recommended to have the saturation current exceed (2 x I_{LIMIT} + ΔI_L) for applications (based on the different maximum current requirements).

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 10 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SWx) as close to the IC as possible using short, direct, and wide traces.
2. Place a wide PGND trace under the IC.
3. Place the input capacitors as close to VIN and PGND pins as possible (the recommended distance is <1mm), and on the same layer as the IC, using a symmetrical routing structure.
4. Connect the VIN and PGND pads using a large copper plane to improve thermal performance.
5. Place multiple vias (10mil drill/18mil copper width) close to the VIN and PGND pads to improve thermal dissipation.
6. Place the VCC decoupling capacitor as close to the 3V3 and AGND pins as possible (the recommended distance is <1mm).
7. Connect AGND and PGND through the inner ground layer using a Kelvin connection.
8. Route the switching node (SWx) away from the feedback network using a short trace.
9. Make the BSTx voltage path as short as possible.

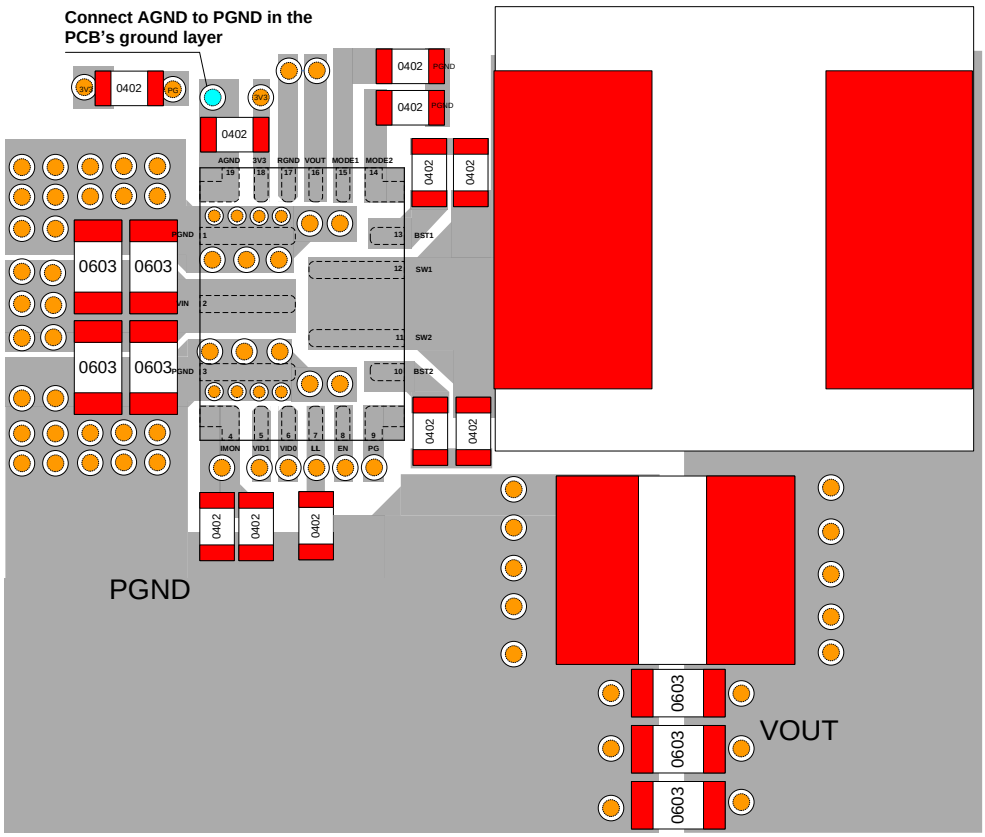

Figure 10: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

Application for I_{CCMAX} = 34.2A (9) (10)

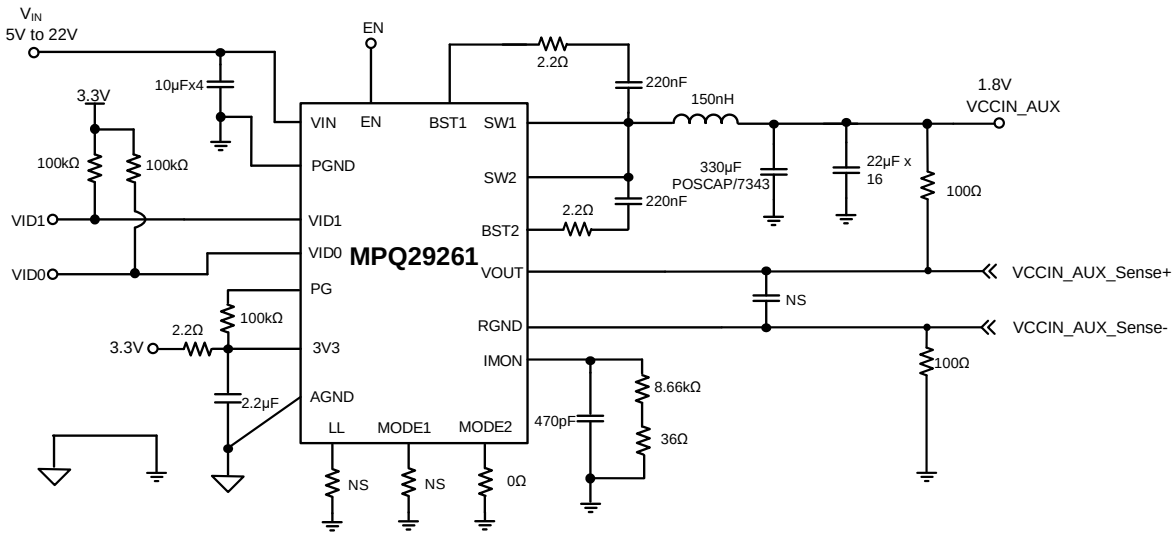

Figure 11: Typical Application Circuit (V_{OUT} = 1.8V, I_{CC_MAX} = 34.2A, f_{SW} = 800kHz, LL = 1.2mΩ, I_{LIMIT} = 20.5A/Phase, VID Decay Down Mode)

Notes:

9) Short SW1 and SW2.
10) The VID1 and VID0 pins are recommended to be pulled up to 3.3V or 1.8V via 100kΩ resistors.

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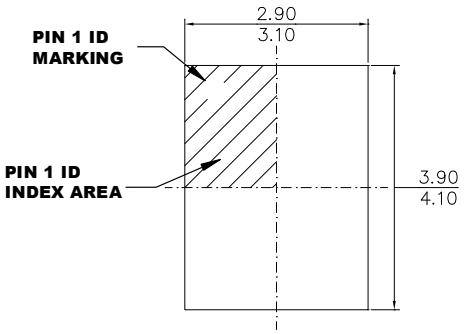
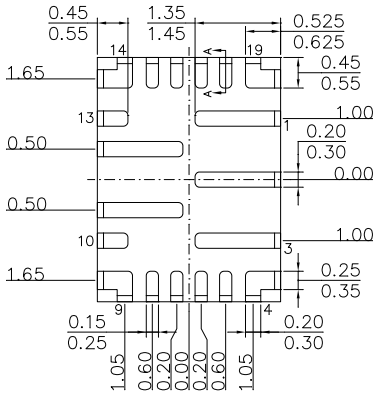
PACKAGE INFORMATION

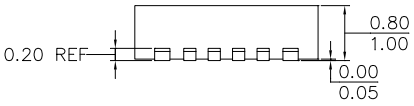
QFN-19 (3mmx4mm)



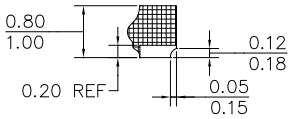
TOP VIEW



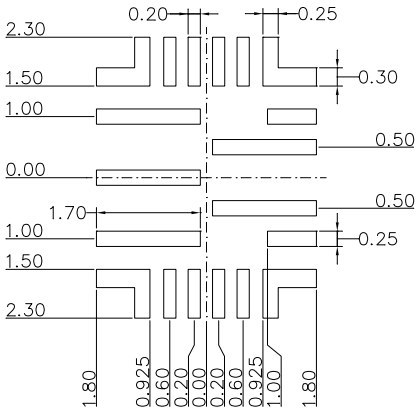
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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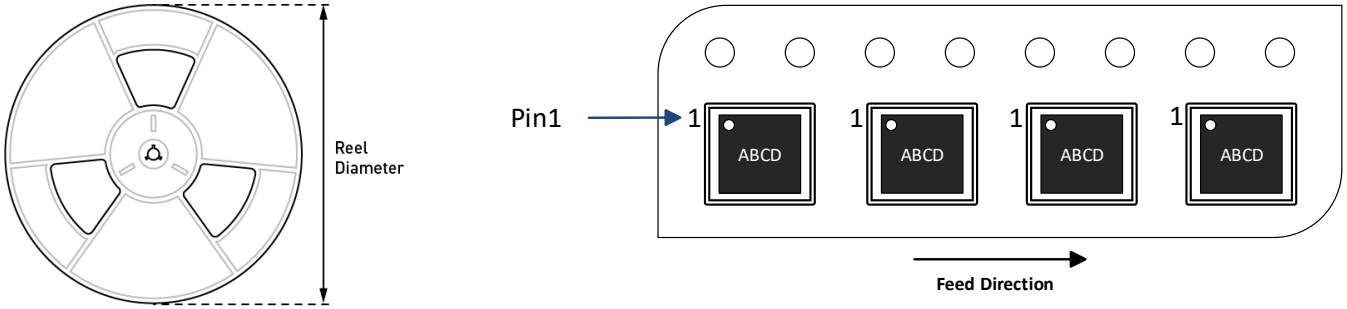
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ29261GLE-AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/7/2025	Initial Release	-

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