MPQ29164

Digital, 6-Phase Controller with I²C Interface for IMVP8/9/9.1, AEC-Q100 Qualified

DESCRIPTION

The MPQ29164 is a dual-rail, multi-phase digital voltage regulator (VR) controller, and is compliant with IMVP8/IMVP9/IMVP9.1 for Intel microprocessors.

The MPQ29164 can work with MPS's Intelli-Phase™ products to complete the multi-phase VR solution with minimal external components. The device can be configured for single-rail operation, and can operate in low quiescent current (I_Q) mode. Rail A is configurable up to 4 phases, while rail B is configurable up to 2 phases.

The on-chip, multiple-time programmable (MTP) memory stores and restores device configurations. Device configurations and fault parameters can be configured or monitored using the I²C interface. The MPQ29164 can monitor and report the output current (I_{OUT}) through the Intelli-Phase™ current-sense (CS) output.

The MPQ29164 is based on unique, digital, multi-phase nonlinear control to provide fast transient response with minimal output capacitors. With only one power loop control method for both the steady state and load transient, power loop compensation is simple to configure.

The MPQ29164 is available in a TQFN-48 (6mmx6mm) package.

FEATURES

- Configurable Phase Numbers
- Two Rails with Up to 6-Phase Operation:
- Up to 4 Phases on Rail A
- Up to 2 Phases on Rail B
- Intel IMVP8, IMVP9, and IMVP9.1 Compliant
- I²C Compliant
- Serial VID Interface for Configuring and Monitoring
- Built-In Multiple-Time Programmable (MTP) Memory to Store Customer Configurations
- Automatic Loop Compensation
- Automatic Phase-Shedding (APS) to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing
- Input Voltage (V_{IN}), Output Voltage (V_{OUT}), Power, and Output Current (I_{OUT}) Monitoring
- Low Quiescent Current (I_Q) Function
- Regulator Temperature Monitoring
- Under-Voltage Lockout (UVLO), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection (OCP), Over-Temperature Protection (OTP), and Reverse-Voltage Protection (RVP) with No Action, Latch-Off, Auto-Retry, and Hiccup Options
- Digital, Configurable Load Line
- Supports Fast-V Mode
- Available in a TQFN-48 (6mmx6mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Autonomous Driving System-On-Chips (SoCs)
- Infotainment Systems

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TYPICAL APPLICATION

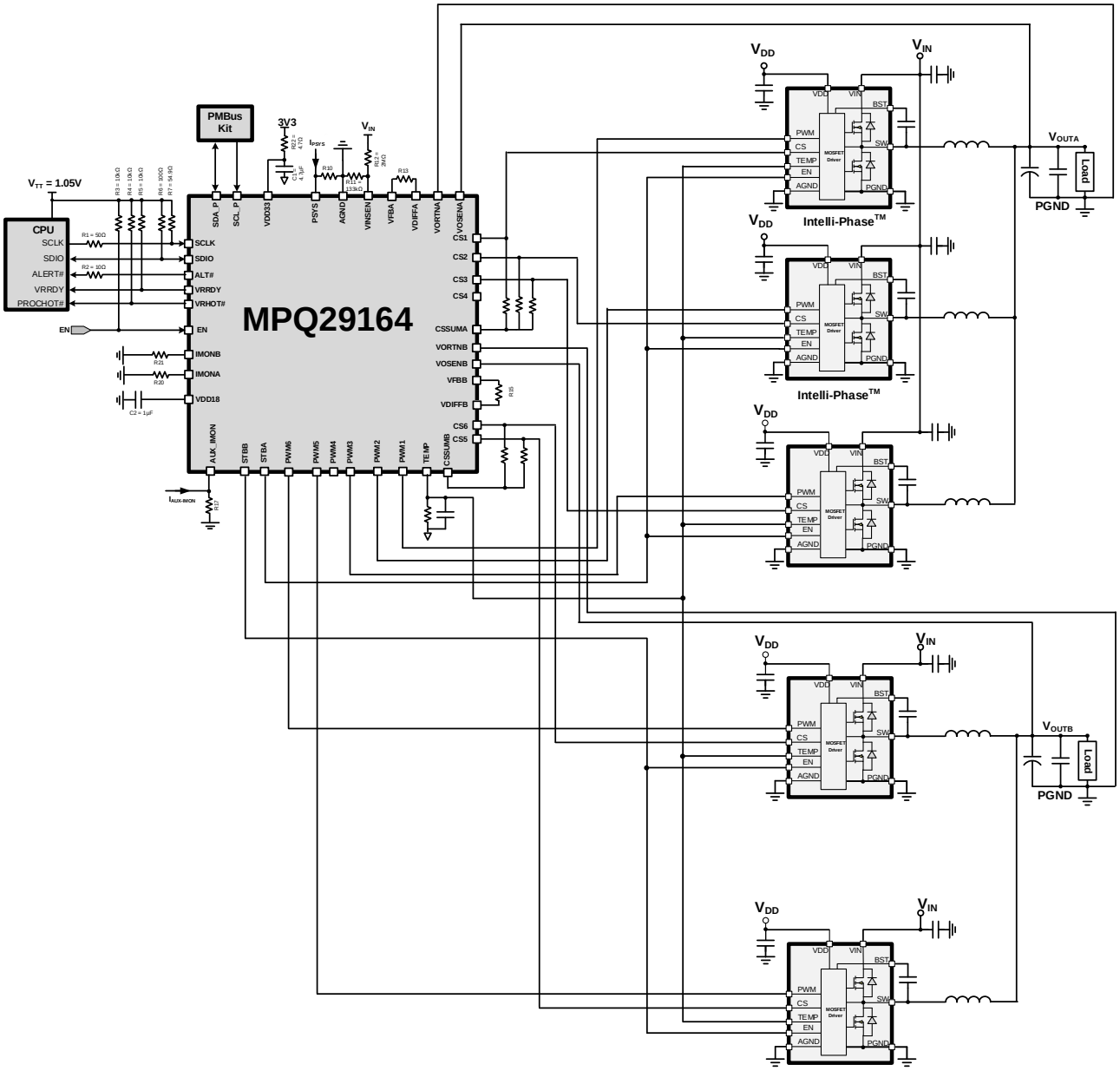

Figure 1: Dual-Rail 3 + 2 Solution

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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ29164GQKTE-xxxx-AEC1**	TQFN-48 (6mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ29164GQKTE-xxxx-AEC1-Z).

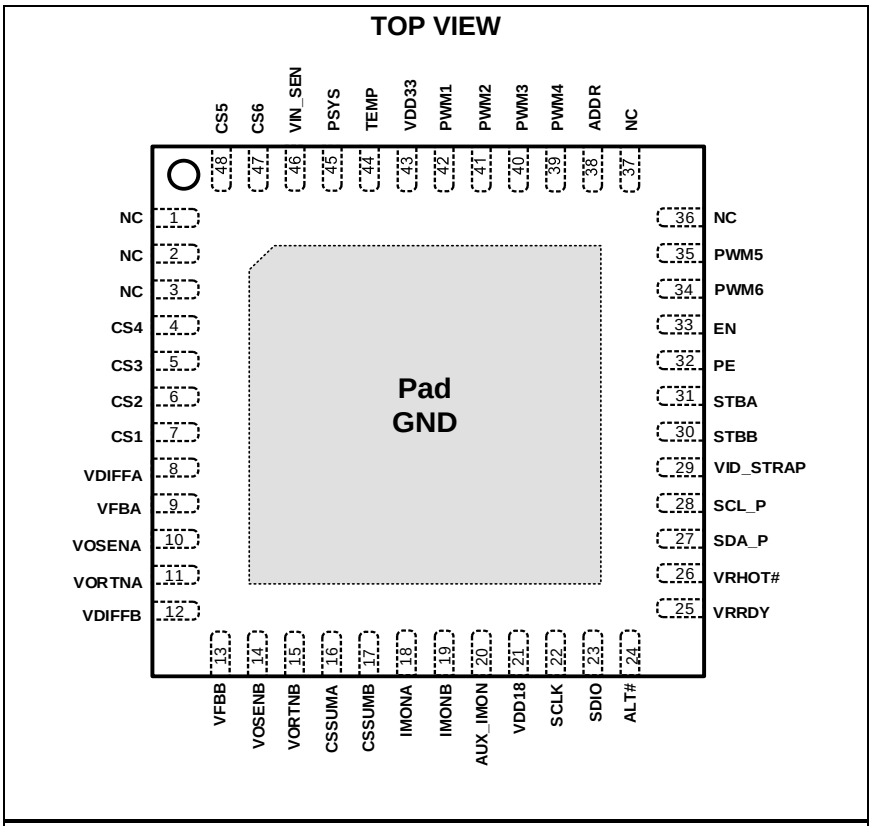
** “xxxx” is the configuration code identifier for the register settings stored in the internal non-volatile memory (NVM). Each “x” can be a hexadecimal value between 0 and F. The default code is “0000”. Work with an MPS FAE to create this unique number.

TOP MARKING

MPSYYWW
MP29164
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP29164: Part number
LLLLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



TQFN-48 (6mmx6mm)

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PIN FUNCTIONS

Pin #	Name	I/O	Description
1, 2, 3	NC		**No connection.**
4	CS4	A [I]	**Phase 4 current-sense input.** Float the CS pin of any unused phase(s).
5	CS3	A [I]	**Phase 3 current-sense input.** Float the CS pin of any unused phase(s).
6	CS2	A [I]	**Phase 2 current-sense input.** Float the CS pin of any unused phase(s).
7	CS1	A [I]	**Phase 1 current-sense input.**
8	VDIFFA	A[O]	**Differential remote-sense amplifier output for rail A.**
9	VFBA	A [I/O]	**Feedback for rail A.** VFBA sources a current proportional to the sensed output current (I_{OUT}). This current flows through the resistor between VFBA and VDIFFA to create a voltage drop that is proportional to the load current. Place a resistor between VDIFFA and VFBA to set a proper load line for rail A.
10	VOSENA	A[I]	**Positive remote voltage sense input for rail A.** Directly connect VOSENA to the VR's output voltage at the load. Route VOSENA differentially with VORTNA.
11	VORTNA	A[I]	**Remote voltage sense return input for rail A.** Directly connect VORTNA to ground at the load. Route VORTNA differentially with VOSENA.
12	VDIFFB	A [O]	**Differential remote-sense amplifier output for rail B.**
13	VFBB	A [I/O]	**Feedback of rail B.** VFBB sources a current proportional to the sensed I_{OUT}. This current flows through the resistor between VFBB and VDIFFB to create a voltage drop that is proportional to the load current. Place a resistor between VDIFFB and VFBB to set a proper load line for rail B.
14	VOSENB	A [I]	**Positive remote voltage sense input for rail B.** Directly connect VOSENB to the VR's output voltage at the load. Route VOSENB differentially with VORTNB.
15	VORTNB	A [I]	**Remote voltage sense return input for rail B.** Directly connect VORTNB to ground at the load. Route VORTNB differentially with VOSENB.
16	CSSUMA	A [I]	**Total phase current monitor for rail A AVP.** Connect the active phase's CS signal to CSSUMA through current-sense resistors.
17	CSSUMB	A [I]	**Total phase current monitor for rail B AVP.** Connect the active phase's CS signal to CSSUMB through current-sense resistors.
18	IMONA	A [I/O]	**Analog total load current signal for rail A.** IMONA sources a current proportional to the sensed total load current from CSSUMA. Connect an external resistor from IMONA to AGND to configure the I_{OUT} report gain.
19	IMONB	A [I/O]	**Analog total load current signal for rail B.** IMONB sources a current proportional to the sensed total load current from CSSUMB. Connect an external resistor from IMONB to AGND to configure the I_{OUT} report gain.
20	AUX_ IMON	A [I/O]	**Analog load current signal for AUX_RAIL.** A current proportional to the AUX_RAIL current flows out through a resistor connected to AGND at AUX_IMON.
21	VDD18	A [I/O]	**1.8V LDO output for internal digital power supply.** Connect a 1µF bypass capacitor to AGND.
22	SCLK	D [I]	**Source synchronous clock from the CPU.** The SCLK frequency ranges between 10MHz and 26.25MHz.
23	SDIO	D [I/O]	**Data signal between the CPU and VID controller.**
24	ALT#	D [O]	**Alert.** ALT# is an open-drain output. The ALT# signal is from the VR controller to the CPU.
25	VRRDY	D [O]	**VR ready output of the controller.** VRRDY goes high when the SVID interface is ready (in IMVP8 mode) or high when the boot ramp finishes (in IMVP9.1 mode). VRRDY only de-asserts if a protection is triggered or EN goes low.

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PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
26	VRHOT#	D [O]	**Voltage regulator thermal throttling logic output.** VRHOT# is an open-drain output. VRHOT# pulls low actively if the monitored temperature exceeds the configured VRHOT# temperature threshold, or if PSYS exceeds the critical level in IMVP9.1. Pull VRHOT# up to 1V through a 10kΩ resistor.
27	SDA_P	D [I/O]	**Data signal between the I²C controller and VID controller.**
28	SCL_P	D [I]	**Source synchronous clock from the I²C controller.**
29	VID_ STRAP	D [I]	**VID step scale pin.** The VID_STRAP pin is the input pin for the VID step scale.
30	STBB	D [O]	**Digital output to tell the Intelli-Phase™ of rail B to enter low-power mode.**
31	STBA	D [O]	**Digital output to tell the Intelli-Phase™ of rail A to enter low-power mode.**
32	PE	D [I]	**Program enable.** PE is the program enable input for system configuration through the I²C when EN is off. Pull PE low to AGND with a 0Ω resistor if it is not being used.
33	EN	D [I]	**Enable control for the controller.**
36, 37	NC	N/A	**No connection.**
38	ADDR	A [I]	**I²C address setting.**
34	PWM6	D [O]	**Tri-state logic level PWM outputs.** Each output is connected to the input of the Intelli-Phase's™ PWM pin. The logic levels are 0V for logic low and 3.3V for logic high. The output is set to tri-state to shut down both the high-side MOSFET (HS-FET) and low-side MOSFET (HS-FET) of the Intelli-Phase™.
35	PWM5	D [O]	
39	PWM4	D [O]	
40	PWM3	D [O]	
41	PWM2	D [O]	
42	PWM1	D [O]	
43	VDD33	A [I]	**3.3V power supply input.** Connect a 4.7µF bypass capacitor from VDD33 to AGND.
44	TEMP	A [I]	**Analog signal from the VR to the VID controller.** TEMP indicates the power stage temperature. Connect all of the Intelli-Phase's™ VTEMP pins together to produce the maximum junction temperature (T_J). Then connect these VTEMP pins to the MPQ29164's TEMP pin. To discharge the TEMP voltage, place a 49.9kΩ resistor in parallel with a 1µF capacitor from TEMP to AGND.
45	PSYS	A [I]	**System total input power sensing.** A current proportional to the system power flows out from a sensor and goes to ground through a resistor connected to the PSYS pin (R_{PSYS}) and AGND.
46	VIN_SEN/ VSYS	A [I]	**Input voltage sense or V_{SYS} sense.** When this pin functions as VIN_SEN, connect VIN_SEN to VIN through a 1/16 divider network. When this pin functions as VSYS, it is the system's voltage function.
47	CS6	A [I]	**Phase 6-current sense input.** Float the CS pin of any unused phase(s).
48	CS5	A [I]	**Phase 5-current sense input.** Float the CS pin of any unused phase(s).
Pad	AGND	I/O	**Analog ground.**

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ABSOLUTE MAXIMUM RATINGS (1)

VDD33.....-0.3V to +4V
VDD18.....-0.3V to +2.2V
VORTNA/B.....-0.3V to +0.3V
CS1~6, PWM1~6, VFBA, VDIFFA, VOSENA, VFBB, VDIFFB, VOSENB, VRRDY, VRHOT#, SCL_P, SDA_P, PE, EN, SCLK, SDIO, TEMP, STBA, STBB,VID_STRAP……..
..... -0.3V to +4V
All other pins..... -0.3V to +2.2V
Continuous power dissipation (T_A = 25°C) (2)
……..…….... 5.2W
Junction temperature (T_J)..... 150°C
Lead temperature ..... 260°C
Storage temperature.....-65°C to +150°C

ESD Ratings (3)

Human body model (HBM) .....Class 2
Charged-device model (CDM) .....Class C2B

Recommended Operating Conditions (4)

VDD33 .....3.15V to 3.4V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TQFN-48 (6mmx6mm) ..... 24 ..... 1.5 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature.
3) Followed ANSI/ESDA/JEDEC JS-001 for HBM and ANSI/ESDA/JEDEC JS-002 for CDM
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VDD33 = 3.3V, EN = 1V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Remote-Sense Amplifier						
Bandwidth (6)	$GBW_{(RSA)}$			20		MHz
VORTN current	$I_{RTNA/B}$	EN = 1V, V_{OSEN} = 3V, V_{ORTN} = 0V		-25	-50	µA
VOSEN current	$I_{VOSENA/B}$	EN = 1V, V_{ORTN} = 0V, V_{OSEN} = 3V		50	100	µA
Oscillator						
Frequency	f_{OSC}	T_A = 25°C	1.5	1.5625		MHz
System Interface Control Inputs						
EN/PE						
Input low voltage	$V_{IL(EN)}$				0.4	V
Input high voltage	$V_{IH(EN)}$	T_A = 25°C	0.8			V
Enable high leakage	$I_{IH(EN)}$	EN = 2V			3.6	µA
Input low voltage	$V_{IL(PE)}$				0.8	V
Input high voltage	$V_{IH(PE)}$		2.4			V
PE high leakage	$I_{IH(PE)}$	PE = 3.6V			2	µA
Enable delay	T_A	EN high to SVID ready		1		ms
Thermal Throttling Control						
VRHOT# low output impedance		$I_{VRHOT\#}$ = 20mA, T_A = 25°C		8	12	Ω
VRHOT# high leakage current		$V_{RHOT\#}$ = 1.8V	-3		+3	µA
IMON Output						
Current gain accuracy	I_{MON}/ I_{CS_SUM}	Measured from I_{CS_SUM} to I_{MON}, I_{CS_SUM} = 1.2mA		1:32		A/A
Comparator (PWM)						
Propagation delay (6)	t_{PD}			10		ns
Common-mode range (6)			0		2.74	V
Comparator (Protection)						
Under-voltage (UV) threshold	$V_{DIFF(UV)}$	Relative to reference digital-to-analog converter (DAC) voltage		-300 / -600		mV
Over-voltage (OV) threshold	$V_{DIFF(OV2)}$	Relative to reference DAC voltage		400		mV
	$V_{DIFF(OV1)}$	Over-voltage protection (OVP1) DAC voltage		2.54		V
		Resolution/LSB(6)		20		mV
PWM1~6, STBA, STBB Outputs						
Output low voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA		10	200	mV
Output high voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	3.15			V
Rising and falling time (6)		C = 10pF		10		ns
PWM/STB tri-state leakage		PWM = 1.5V, EN = 0V	-1		+1	µA
Internal LDO Output						
LDO output voltage	VDD18	Load = 0mA		1.8		V
	$VDD18_{30mA}$	Load = 30mA, T_A = 25°C	1.76			V

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ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 1V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VDD33 Supply						
Supply voltage range	VDD33		3.15	3.3	3.4	V
Supply current	I_{VDD33}	EN = PE = high, VDD33 = 3.3V, PS0, T_A = 25°C		8		mA
		EN = PE = low, VDD33 = 3.3V		100		µA
		EN = PE = high, VDD33 = 3.3V, PS4, T_A = 25°C		120		µA
		EN = PE = high, VDD33 = 3.3V, PS2/PS3, T_A = 25°C		8		mA
Under-voltage lockout (UVLO) threshold voltage	$VDD33_{UVLO}$	VDD33 is rising, T_A = 25°C		2.88	3.05	V
UVLO hysteresis (6)	$VDD33_{UVLO_HYS}$	VDD33 is falling		75		mV
SVID Interface (6)						
CPU interface voltage (SDIO, SCLK)	V_{IL}	Logic low			0.45	V
	V_{IH}	Logic high	0.65			V
Termination resistance (SDIO, SCLK, ALT#)	R_{PU}		50	55		Ω
Leakage current (SDIO, SCLK, ALT#)	I_L	0V to V_{TT}	-10		+10	µA
Pad capacitance (SDIO, SCLK, ALT#)	C_{PAD}				4	pF
Pin capacitance (SDIO, SCLK, ALT#)	C_{PIN}				5	pF
Buffer on resistance (SDIO, SCLK, ALT#)	R_{ON}		4		13	Ω
Maximum voltage (SDIO, SCLK, ALT#)	V_{MAX}	Transient voltage, including ringing	-0.3		+2.1	V
Slew rate (SDIO, SCLK, ALT#)		2nH, 4pF load	0.5		2	V/ns
Analog-to-Digital Converter (ADC)						
ADC voltage reference		T_A = 25°C	1.595	1.6	1.605	V
ADC resolution (6)				10		bits
DNL (6)				1		LSB
Sample rate (6)				780		kHz
DAC (Reference Voltage for V_{OUT})						
Range				1.6		V
Resolution/LSB (6)				5		mV
DAC (V_{OUT} Calibration)						
Range				320		mV
Resolution (6)				8		bits

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ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 1V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DAC (Protection for per-Phase Over-Current Protection (OCP))						
Range		Adjustable via the I²C		1.28 to 2.54		V
Resolution/LSB				10		mV
I²C DC Characteristics (SDA_P, SCL_P)						
Input high voltage	V_{IH_I2C}	SCL_P, SDA_P	2.3			V
Input low voltage	V_{IL_I2C}	SCL_P, SDA_P			0.8	V
Input leakage current		SCL_P, SDA_P	-10		+10	µA
Maximum voltage (6)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	+3.6	V
Pin capacitance (6)	C_{PIN}				10	pF
I²C Timing Characteristics (6)						
Operating frequency range			10		1000	kHz
Bus free time		Between a stop and start command	0.5			µs
Hold time			0.26			µs
Repeated start command set-up time			0.26			µs
Stop command set-up time			0.26			µs
Data hold time			0			ns
Data set-up time			50			ns
Clock low timeout			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data falling time					120	ns
Clock/data rising time					120	ns
VID Strap Input						
Input high voltage (6)	$V_{IH_VID_STRAP}$	VID_STRAP	2.4			V
Input low voltage (6)	$V_{IL_VID_STRAP}$	VID_STRAP			0.7	V

Notes:

6) Guaranteed by design or characterization data. Not tested in production.

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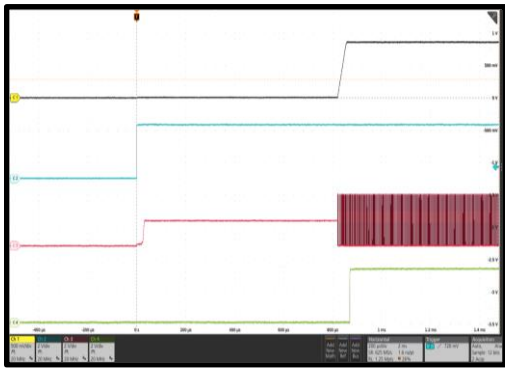
TYPICAL PERFORMANCE CHARACTERISTICS

EN On

Rail B enable on, V_{IN} = 12V, V_{BOOT} = 0.9V, I_{OUT} = 0A

CH1: V_{OUTB} 500mV/div.
CH2: V_{EN} 2V/div.
CH3: PWM6 2V/div.
CH4: VRRDY 2V/div.

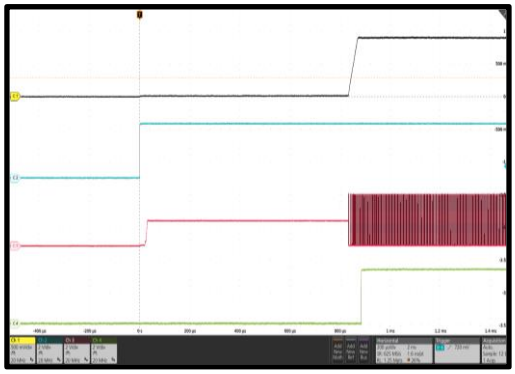


200µs/div.

EN On

Rail A enable on, V_{IN} = 12V, V_{BOOT} = 0.9V, I_{OUT} = 0A

CH1: V_{OUTA} 500mV/div.
CH2: V_{EN} 2V/div.
CH3: PWM1 2V/div.
CH4: VRRDY 2V/div.

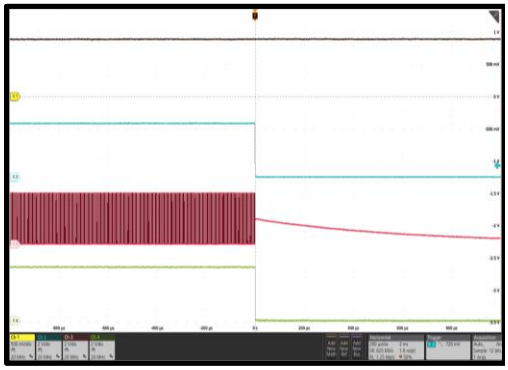


200µs/div.

EN Off

Rail B enable off, V_{IN} = 12V, V_{BOOT} = 0.9V, I_{OUT} = 0A

CH1: V_{OUTB} 500mV/div.
CH2: V_{EN} 2V/div.
CH3: PWM6 2V/div.
CH4: VRRDY 2V/div.

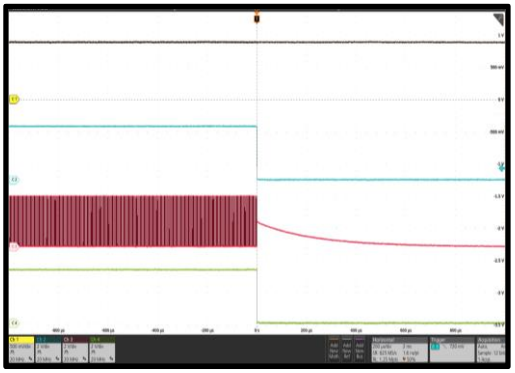


200µs/div.

EN Off

Rail A enable off, V_{IN} = 12V, V_{BOOT} = 0.9V, I_{OUT} = 0A

CH1: V_{OUTA} 500mV/div.
CH2: V_{EN} 2V/div.
CH3: PWM1 2V/div.
CH4: VRRDY 2V/div.

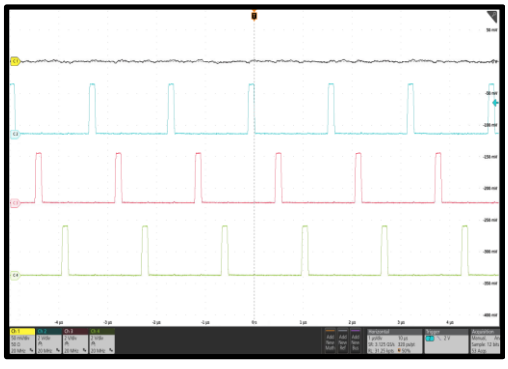


200µs/div.

Steady State

V_{IN} = 12V, V_{OUTA} = 0.9V, PS0, 3-phase CCM, f_{SW} = 600kHz, I_{OUT} = 30A

CH1: $V_{OUTA/AC}$ 50mV/div.
CH2: PWM1 2V/div.
CH3: PWM2 2V/div.
CH4: PWM3 2V/div.

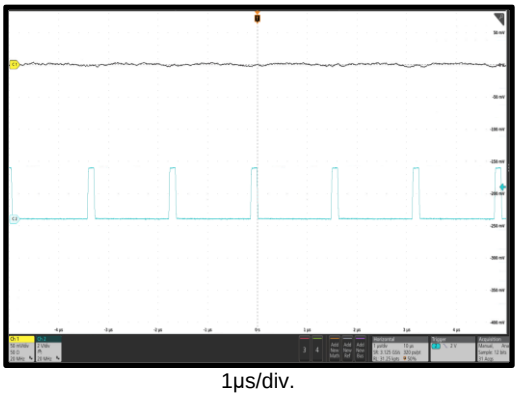


1µs/div.

Steady State

V_{IN} = 12V, V_{OUTA} = 0.9V, PS1, 1-phase CCM, f_{SW} = 600kHz, I_{OUT} = 10A

CH1: $V_{OUTA/AC}$ 50mV/div.
CH2: PWM1 2V/div.



1µs/div.

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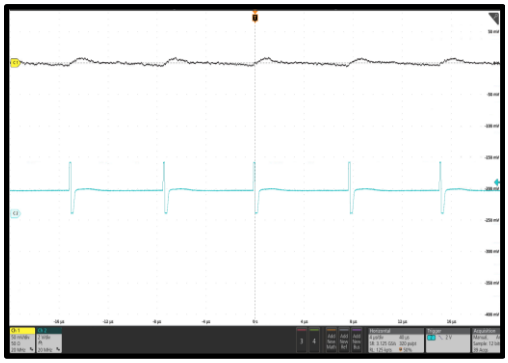
TYPICAL PERFORMANCE CHARACTERISTICS

Steady State

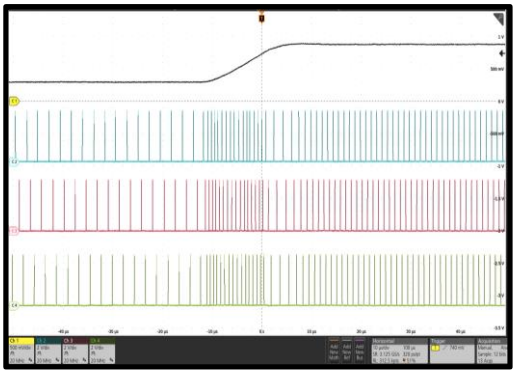
V_{IN} = 12V, V_{OUTA} = 0.9V, PS2, 1-phase DCM, I_{OUT} = 1A



4µs/div.

DVID Ramping Up

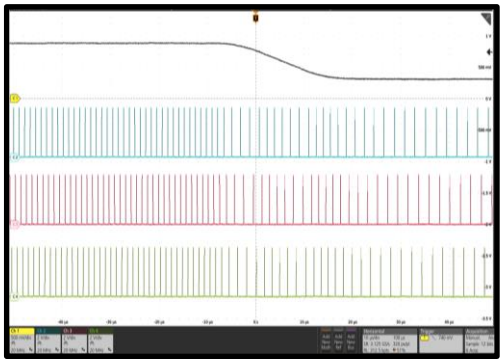
DVID up, DVID from 0.3V to 0.9V, I_{OUT} = 5A



10µs/div.

DVID Ramping Down

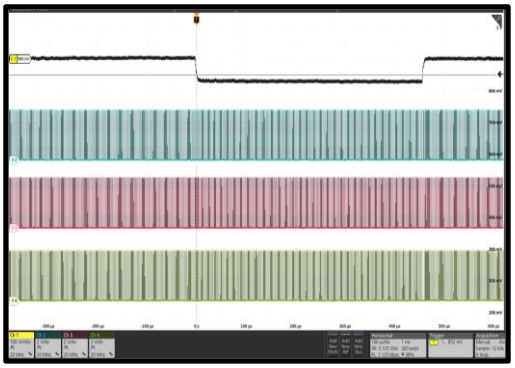
DVID down, DVID from 0.9V to 0.3V, I_{OUT} = 5A



10µs/div.

Transient

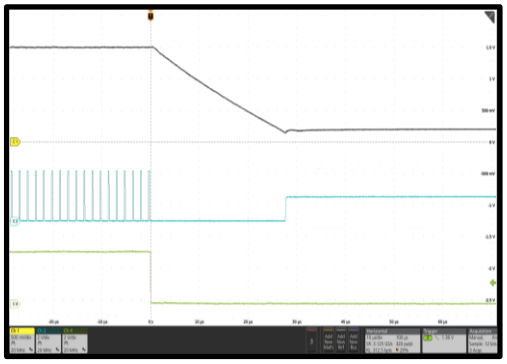
Load transient with DC load line, V_{IN} = 12V, V_{OUTA} = 0.9V, R_{LL_DC} = 2.3mΩ, 2A to 32A at 300A/µs



100µs/div.

Over-Voltage Protection (OVP)

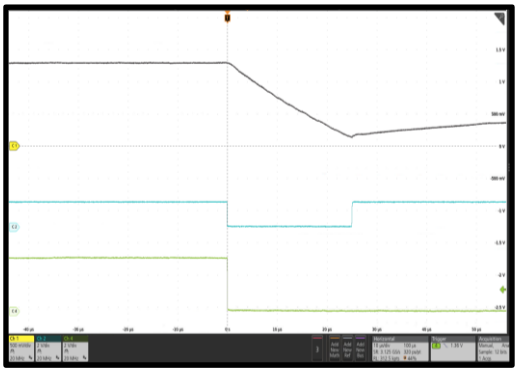
OVP1, V_{IN} = 12V, VIDA = 1.5V, then set OVP1 level = 1.4V, latch-off mode



10µs/div.

Over-Voltage Protection (OVP)

OVP2, VIN = 12V, VIDA = 0.9V, then add 1.5V to V_{OUTA}, OV VID delay = 0.2µs, latch-off mode



10µs/div.

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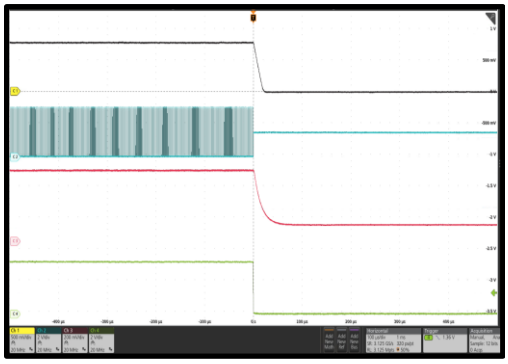
TYPICAL PERFORMANCE CHARACTERISTICS

Over-Current Protection (OCP)

V_{IN} = 12V, V_{OUTA} = 0.9V, OCP_Level = 40A,
OCP action delay = 500µs, latch-off mode



100µs/div.

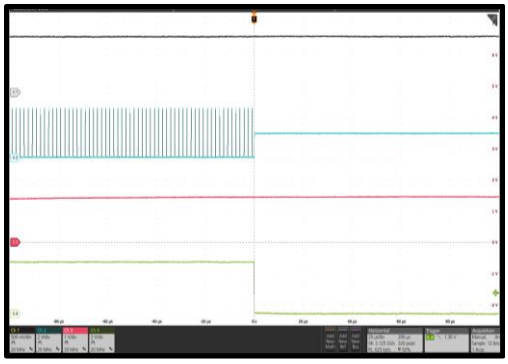
Under-Voltage Protection (UVP)

V_{IN} = 12V, V_{OUTA} = 0.9V, UVP_Level = 600mV,
UVP delay time = 500µs, latch off mode

100µs/div.

Over-Temperature Protection (OTP)

V_{IN} = 12V, V_{OUTA} = 0.9V, latch-off mode,
T_J = (VTEMP + 100mV) / (10mV/°C) °C,
OTP threshold = 150°C, latch off mode



20µs/div.

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FUNCTIONAL BLOCK DIAGRAM

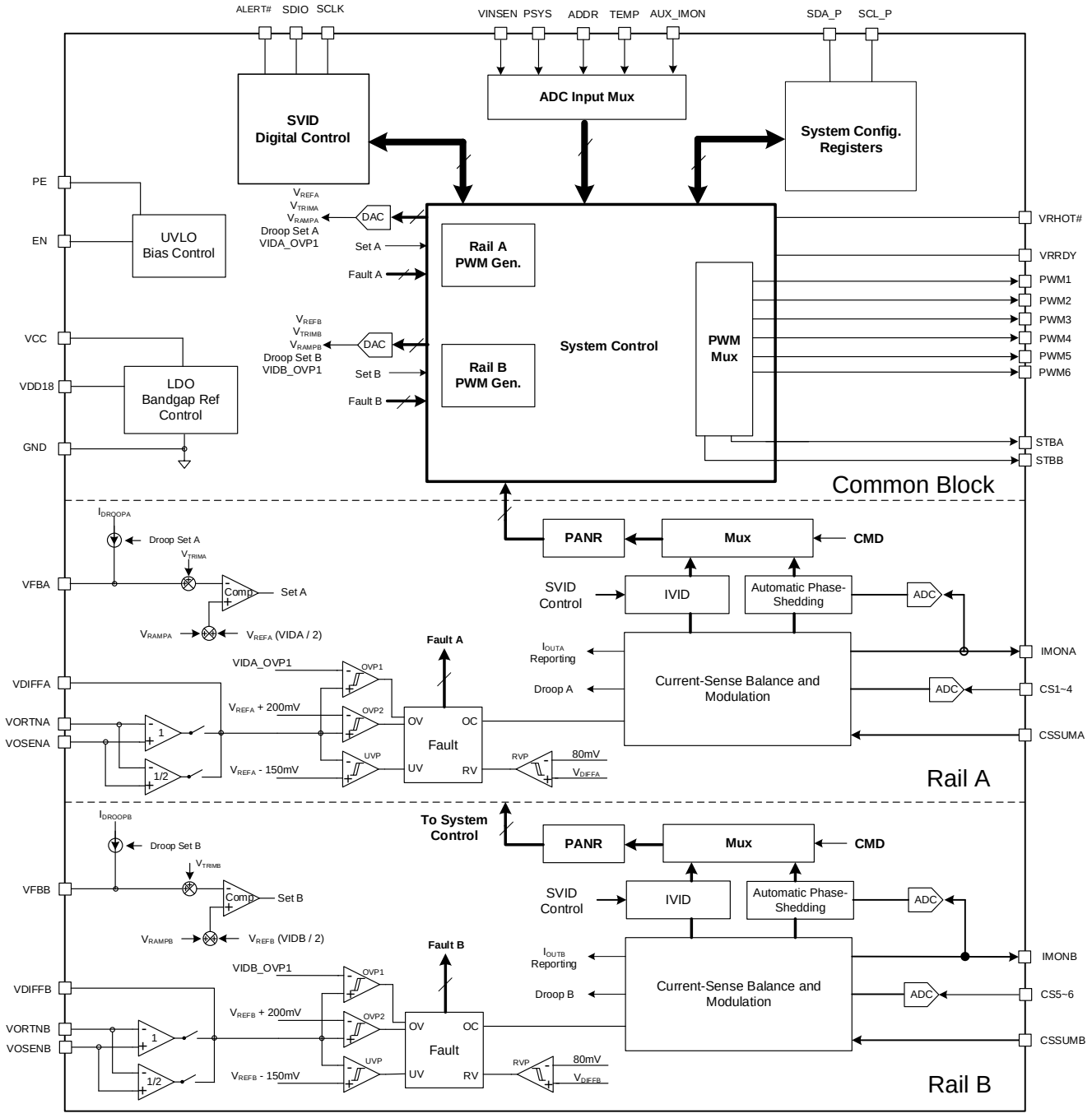

Figure 2: System Functional Block

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OPERATION

The MPQ29164 is a dual-rail, digital, multi-phase voltage regulator (VR) controller, and is compliant with IMVP8/IMVP9/IMVP9.1 for Intel microprocessors. Automatic phase-shedding (APS) and phase-adding are accomplished according to the load current to improve VR efficiency.

The MPQ29164 contains blocks for the I²C and SVID interface, including a precision digital-to-analog converter (DAC) and analog-to-digital converter (ADC), multiple-time programmable (MTP) memory for custom configuration, differential remote voltage-sense amplifiers, current-sense amplifiers, internal slope compensation, VR_READY monitoring, and temperature monitoring.

Fault protection features include input voltage (V_{IN}) under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), over-temperature protection (OTP), and reverse-voltage protection (RVP).

Phase Configuration

The MPQ29164 supports multiple phases for different applications and platforms. The device can be configured for up to 4-phase operation on rail A and up to 2-phase operation on rail B. The phases can be set via I²C register MFR_PHASE_NUM (29h on Page 0), bits[3:0] or MFR_PHASE_NUM (29h on Page 1), bits[2:0].

For example, for 4-phase operation on rail A and 2-phase operation on rail B, set MFR_PHASE_NUM (29h on Page 0), bits[3:0] to 0100b, then set MFR_PHASE_NUM (29h on Page 1), bits[2:0] to 010b.

Table 1 shows the phase configurations for rail A.

Table 1: Rail A Phase Configuration and Active PWM Pins

MFR_PHASE_NUM (on Page 0), Bits[3:0]	Active PWM Pins (Rail A)
0100	PWM1~4
0011	PWM1~3
0010	PWM1~2
0001	PWM1
0000	-

Table 2 shows the phase configurations for rail B.

Table 2: Phase Configuration and Active PWM Pins (Rail B)

MFR_PHASE_NUM (on Page 1), Bits[2:0]	Active PWM Pins (Rail B)
010	PWM 6~5
001	PWM 6
000	-

Note that one PWM pin cannot be used for both rails simultaneously.

I²C Address Configuration

To support multiple VR devices using the same I²C interface, there is a I²C address for every device. The I²C address is a 7-bit code. The 4 MSB are set via the register, and the lower 3 bits can be set by either the register or a resistor connected to the ADDR pin.

The register MFR_ADDR_I2C (C0h), bits[6:0] and the ADDR pin can be used to configure the I²C address (see Figure 3). Use two resistor dividers connected from VDD18 and ground to obtain the target voltage for the corresponding address.

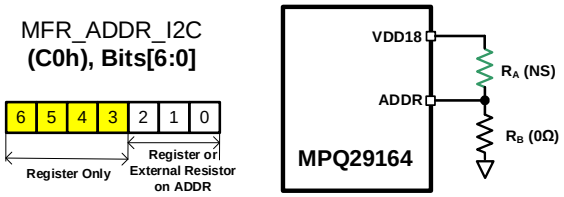

Figure 3: I2C Address Configuration

Table 3 on page 15 shows the ADDR pin voltage setting for different I²C addresses. By default, MFR_ADDR_I2C (C0h), bits[6:4] is set to 0100b. The default setting on the external resistors are R_A = NS and R_B = 0Ω, where the default I²C address is 20h.

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Table 3: I²C Address Setting via the ADDR Voltage

I²C Address	Recommended Setting Voltage (V)	Min Setting Voltage (V)	Max Setting Voltage (V)
x0h	0	0	0.2
x1h	0.3	0.2	0.4
x2h	0.5	0.4	0.6
x3h	0.7	0.6	0.8
x4h	0.9	0.8	1.0
x5h	1.1	1.0	1.2
x6h	1.3	1.2	1.4
x7h	1.5	1.4	1.6

Start-Up Sequence

The MPQ29164 is supplied with a 3.3V voltage for the analog circuit. The system is reset by the internal power-on reset (POR) signal. After the system exits POR, the data in the MTP is loaded into the registers to configure the VR's operation. The initialization process takes about 0.5ms plus a delay time (marked as EN Delay A/B in Figure 4). Then the MPQ29164 initiates soft start (SS) to charge the output capacitor with the SETVID_SLOW slew rate until the reference reaches the target boot voltage (V_{BOOT}). t_B is set by V_{BOOT} / slow slew rate.

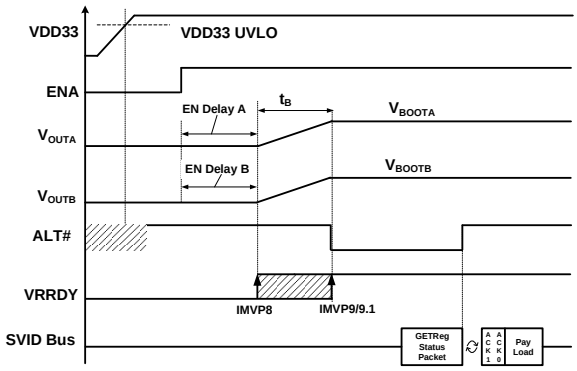

Figure 4: Start-Up Sequence

The MPQ29164 supports both IMVP8 and IMVP9/IMVP9.1, with different VRRDY assertion time settings. The VRRDY signal asserts either when the SVID interface is ready to receive CPU commands (IMVP8), or when the VR reaches the V_{BOOT} level (IMVP9/IMVP9.1).

The MPQ29164 also provides an additional, configurable EN delay via the MFR_EN_DLY (3Eh on Page 0) and MFR_EN_SEQUENCE_CFG (3Eh on Page 1) registers. This delay time (t_A) can be set to be longer than 0.5ms, and is equal to 0.5ms + MFR_EN_DLY + MFR_PRECHECK_TIME. See the MFR_EN_DLY (3Eh) section on page 95 and the MFR_EN_SEQUENCE_CFG (3Eh) section on page 51 to configure the delay time.

When V_{BOOT} is set to 0V, pulse-width modulation (PWM) remains in tri-state until a valid SVID voltage is received. The controller then ramps the voltage to the target value and asserts ALT#.

Steady State and Switching Frequency (f_{SW})

The MPQ29164 applies digital nonlinear control to provide fast transient response and easy loop compensation. The duty cycle of each active phase's PWM updates in real time according to V_{IN} and the reference voltage (V_{REF}) under the set switching frequency (f_{SW}). The active phases are automatically interleaved during steady state. In steady state, f_{SW} is set by MFR_FS (28h), bits[6:0].

The MPQ29164 adaptively changes each individual phase's f_{SW} during load transient to achieve fast transient performance with minimal BOM cost.

Power State (PS) Change

The SVID bus can change the VR to different power states (PS0, PS1, PS2, PS3, or PS4) to optimize efficiency under various load conditions. These states are entered by configuring the power state register using the SVID's SETPS command. The VR uses the power state commands issued by the processor to optimize power loss and flatten the efficiency curve across the entire operating current range.

In PS0 mode, all phases run in continuous conduction mode (CCM). In PS1 mode, one phase runs in CCM, while all other phases are in tri-state. In PS2 mode, one phase runs in diode emulation mode, and f_{SW} drops automatically to reduce power loss under light-load conditions. Table 4 on page 16 show how the phases act at different power states.

During the dynamic VID transition issued by the SVID commands (e.g. SETVID_FAST or SETVID_SLOW), the power state changes to PS0 by default and runs in full-phase PWM mode. After V_{OUT} is regulated to the new target voltage, the power state remains in PS0 until the

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processor sends a new command to change the power state.

Table 4: Power State and Phase Activities

PS State	Active Phase	CCM/DCM
PS0	Full-phase PWM	CCM
PS1	1-phase PWM	CCM
PS2	1-phase PWM	DCM
PS3	1-phase PWM	DCM
PS4	All phases off	-

Reference

The MPQ29164 supports both 5mV VID steps and 10mV VID steps for IMVP8, IMVP9, and IMVP9.1, with only one DAC to generate V_{REF}. There is a control bit (MFR_VID_STEP_SEL) in MFR_VR_CONFIG (39h) that chooses the VID step. If this bit is set to 1, then the DAC's V_{REF} can be calculated with Equation (1):

$$V_{REF} = (VID + 49) / 2 \times 5mV \quad (1)$$

If this bit is set to 0, then the output (V_{REF}) of the DAC can be calculated with Equation (2):

$$V_{REF} = (VID + 19) / 2 \times 10mV \quad (2)$$

Output Voltage (V_{OUT}) Sense

The output voltages are sensed remotely with a half-gain differential amplifier. The sensed output voltages are used for closed-loop compensation, OVP, UVP, and I²C monitoring. A package sense is recommended to enclose the board parasitic within the VR's feedback loop (see Figure 5). This reduces noise and optimizes performance.

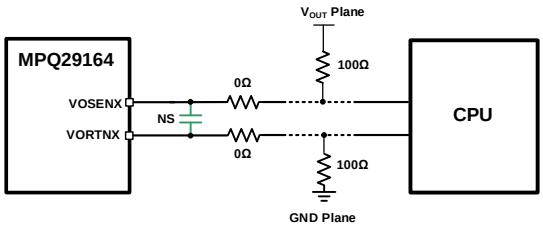

Figure 5: Output Remote Sense

Two 0Ω resistors are placed close to the MPQ29164. To avoid errant operation or board damage if the CPU is absent, connect two 100Ω catch-up resistors to the V_{OUT} and PGND planes to obtain the output feedback even when the CPU is absent.

Input Voltage (V_{IN}) Sense

The power supply input voltage (V_{IN}) is sampled at the VIN_SEN pin. This voltage is used as the feed-forward control for V_{OUT} regulation, V_{IN} UVLO, V_{IN} OVP, VSYS signaling, and I²C monitoring. Connect two resistors to the input, and use a bypass capacitor to obtain a 1/16 divider for VIN_SEN (see Figure 6). The default value for R_{VIN_1} is 2MΩ, and the default value for R_{VIN_2} is 133kΩ. The maximum voltage for VIN_SEN is 1.6V, which corresponds to a maximum V_{IN} of 25.6V.

Route the VIN_SEN trace away from noisy sources.

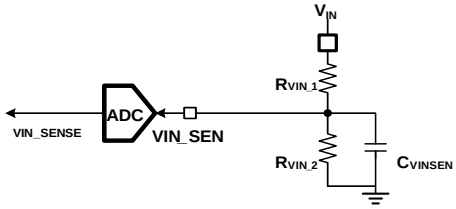

Figure 6: V_{IN} Sense Network

Current Sense

The MPQ29164 works with MPS's Intelli-Phase™ to sense the per-phase inductor current and total current (see Figure 7). The cycle-by-cycle current information is used for phase current balancing, OCP, and load-line setting. K_{CS} is the current-sense gain for Intelli-Phase™ products. A resistor (R_{CS}) is connected from CS to CSSUM. CSSUM has a constant voltage (typically 1.23V) that can sink small currents to provide voltage shifts that meet the CS operating voltage range.

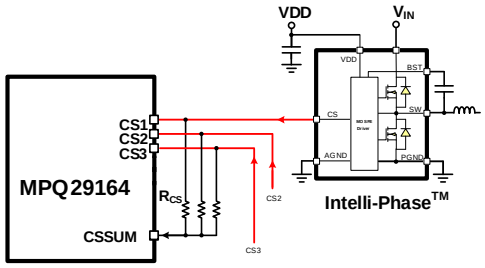

Figure 7: Phase Current Sense with 3-Phase Configuration

Different Intelli-Phase™ products have different operating voltage ranges for CS: V_{CS_MIN} and V_{CS_MAX}. Refer to each Intelli-Phase's™ datasheet to determine the minimum and maximum operating voltage range.

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Calculate R_{CS} with Equation (3):

$$V_{CS_MIN} < I_{CS} \times R_{CS} + 1.23V < V_{CS_MAX} \quad (3)$$

Where I_{CS} can be estimated with Equation (4):

$$I_{CS} = I_L \times K_{CS} \quad (4)$$

By pairing the MPQ29164 with an Intelli-Phase™ product, an accurate current sense can be achieved without temperature compensation or impedance matching.

IMON and I_{DROOP}

The current flowing out from IMON is 1/32 of the filtered CS_SUM, plus a 5μA bias current. This total current is called I_{SUM}. Place a resistor from IMON to ground to generate a voltage proportional to the output current (I_{OUT}). The IMON voltage (V_{IMON}) is sampled and converted by the ADC and then stored in the I_{OUT} register, which is scaled to I_{CCMAX} = the ADC's full range (FFh). The IMON voltage reaches to its maximum (V_{IMON_MAX}) when I_{OUT} reaches I_{CCMAX}.

V_{IMON} can be calculated with Equation (5):

$$V_{IMON} = \left(\frac{I_{OUT} \times K_{CS}}{32} + I_{BIAS} \right) \times R_{IMON} \quad (5)$$

Where K_{CS} is the Intelli-Phase™ current-sense gain, I_{OUT} is the output current, R_{IMON} is the IMON resistor, V_{IMON_MAX} is (1.6 x 8 / 11V), and I_{BIAS} is 5μA.

R_{IMON} can be set with I_{OUT} = I_{CCMAX}, and V_{IMON} = V_{IMON_MAX}. Estimate R_{IMON} with Equation (6):

$$R_{IMON} = \frac{V_{IMON_MAX}}{\frac{I_{CCMAX} \times K_{CS}}{32} + I_{BIAS}} \quad (6)$$

Figure 8 shows the MPQ29164's IMON sense and the I_{DROOP} block diagram.

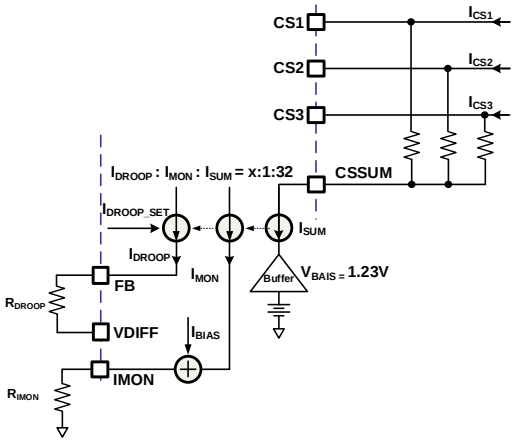

Figure 8: Current Sense IMON/I_{DROOP}

Static Load Line Setting

A droop resistor (R_{DROOP}) between VFB and VDIFF sets the static load line. The droop current (default 1/8 of I_{SUM}) flowing through the droop resistor from VFB to VDIFF generates the droop voltage. Consider the application requirements for load-line regulation (R_{LL}). If there is a half-gain on the output remote sense, calculate R_{DROOP} with Equation (7):

$$R_{DROOP} = \frac{R_{LL}}{2 \times K_{CS} \times K_{DROOP}} \quad (7)$$

Where the K_{CS} is the Intelli-Phase™ current-sense gain (default value is 10μA/A), and K_{DROOP} is the gain of the droop current mirror (the default is 8/8 x 1/8).

Digital Programmable Load Line

In addition to the load-line setting from R_{DROOP}, the MPQ29164 also provides a digital, configurable load-line trim, which is set by MFR_IDROOP_CTRL (1Bh), bits[3:0]. Table 5 on page 18 shows the MPQ29164's droop current mirror gain. The load line can be changed via the I²C, and is stored in the MTP. With a digital load line, the droop can be changed without replacing R_{DROOP}. The default value of IDROOP_SET is 0101b, which represents a 1/8 gain to I_{SUM}.

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Table 5: Digital Load-Line Trim

IDROOP_SET, Bits[3:0]	I_{DROOP} Gain
0000 b	0
0001 b	4/8 x 1/8 x I_{SUM}
0010 b	5/8 x 1/8 x I_{SUM}
0011 b	6/8 x 1/8 x I_{SUM}
0100 b	7/8 x 1/8 x I_{SUM}
0101 b (default)	8/8 x 1/8 x I_{SUM}
0110 b	9/8 x 1/8 x I_{SUM}
0111 b	10/8 x 1/8 x I_{SUM}
1000 b	11/8 x 1/8 x I_{SUM}
1001 b	12/8 x 1/8 x I_{SUM}
1010 b	13/8 x 1/8 x I_{SUM}
1011b	14/8 x 1/8 x I_{SUM}
1100 b	15/8 x 1/8 x I_{SUM}
1101 b	16/8 x 1/8 x I_{SUM}
1110 b	17/8 x 1/8 x I_{SUM}
1111 b	18/8 x 1/8 x I_{SUM}

I_{OUT} Reporting

The I_{OUT} register (15h) in the SVID register reports to the processor to prevent the device from exceeding its thermal design point and maximum current capability.

The MPQ29164 has a user-configurable register that contains the gain (MFR_IMON_SVIDx (E8h~F0h), bits[7:0]) and a signed current offset, (MFR_IMON_SVIDx (E8h~F0h), bits[14:8]) for the SVID I_{OUT} report.

These configurable parameters allow users to match the IMON scale to the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current report across the entire load range, and maximizes the Intel turbo performance. The gain can be reduced or offset to underreport the total current to the CPU for improved performance. See the MFR_IMON_SVIDx (E8h~F0h) sections starting on page 78 for details on how to configure the register.

The I²C I_{OUT} register READ_IOUT (8Ch) is also used for total current protection. If automatic phase-shedding (APS) is enabled via the I²C, the total current report determines whether to enter or exit phase-shedding to flatten the overall efficiency across the operating current range. IOUT_CAL_GAIN_SET (38h), bits[9:0] and IOUT_CAL_GAIN_SET (38h), bits[15:10] configure the I²C I_{OUT} report gain and offset, respectively. This ensures that the MPQ29164 tracks the load current (see Figure 9).

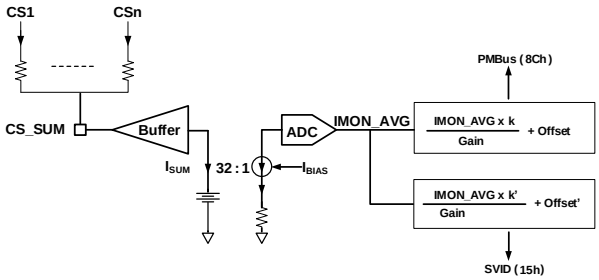

Figure 9: Total Current Sense and Report

Temperature Sense

The MPQ29164 measures the external temperature by connecting all the Intelli-Phase™ VTEMP pins together (see Figure 10).

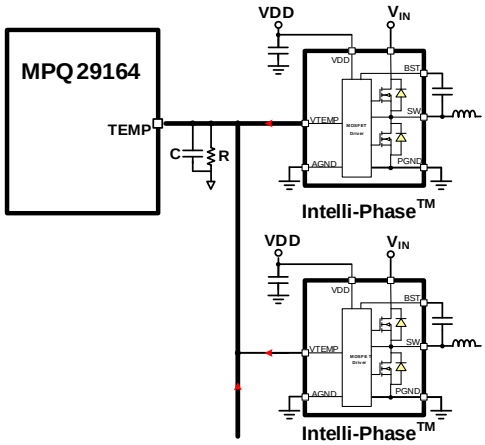

Figure 10: External Temperature Sense

The voltage on the MPQ29164's TEMP pin is the highest voltage among the Intelli-Phase™ devices, which indicates the highest temperature of the VR power system. The sensed temperature is used for OTP and to assert the SVID thermal alert (or VRHOT# signal) for the processor. To discharge TEMP, connect a 20kΩ resistor in parallel with a 10nF capacitor from TEMP to GND.

The Intelli-Phase™'s V_{TEMP} is a voltage output proportional to the junction temperature (T_J). T_J can be calculated with Equation (8):

$$T_{JUNCTION} = \frac{V_{TEMP} - 600mV}{8mV/^{\circ}C} \quad (8)$$

For example, if V_{TEMP} is 1240mV, the T_J for that Intelli-Phase™ is 80°C.

Dynamic VID (DVID)

The MPQ29164 supports dynamic VID changes when it receives one of three SVID commands:

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SETVID_FAST, SETVID_SLOW, or SETVID_DECAY.

The SETVID_FAST slew rate is set via MFR_TRANS_FAST (3Dh), bits[7:6], which is equal to the VID increase or decrease per step. MFR_TRANS_FAST (3Dh), bits[5:0] defines the VID change duration time. The fast slew rate can be calculated with Equation (9):

$$SlewRate = \frac{(VID_STEP_NUM+1)\times VID_STEP}{VID_SR_CNT\times 100ns} \quad (9)$$

Where VID_STEP_NUM can be configured to be between 0 and 3, VID_STEP is 5mV or 10mV depending on the CPU requirement, and VID_SR_CNT can be set to be between 1 and 63.

If VID_STEP_NUM is 1, VID_STEP is 5mV, and VID_SR_CNT is 3, then the slew rate is 33.3mV/µs.

The SETVID_SLOW slew rate is determined by MFR_FILTER_SET (3Ch), bits[3:0], which can be configured to 1/2, 1/4, 1/8, or 1/16 of SETVID_FAST. The SETVID_DECAY slew rate is determined by the load current and output capacitor bank.

MFR_ALT_SET (3Fh) sets the ALT# assertion time for DVID. A delay time can be added to help the MPQ29164 meet Intel specifications. See the MFR_ALT_SET (3Fh) sections on page 51 and page 96 for more details.

When DVID rises, the inductor current rises to charge the output capacitors. This current introduces a large positive droop voltage due to the load line. V_{OUT} may drop below the target voltage, which may cause V_{OUT} to exceed the minimum regulation tolerance budget (TOB) 3µs after ALT# asserts.

The MPQ29164 can be configured to ramp up more VID steps via MFR_TRANS_FAST (3Dh), bits[10:8] after VID ramps to the target voltage. The MPQ29164 remains at this VID voltage for the time set by MFR_PLATFORM_TIME_SET (2Eh), bits[5:0]. Then VID falls back to the target VID voltage, which causes V_{OUT} to rise to within the regulation TOB as required by Intel specifications.

When V_{OUT} is ramping down, the inductor current drops to discharge the output capacitors. The output capacitors are discharged until ramping ends, which may lead to V_{OUT} undershoot. There is a time window during which the inductor current must balance the load current to avoid output voltage (V_{OUT}) undershoot.

The MPQ29164 applies a low-pass filter for the VID_DAC to smooth V_{REF} when V_{OUT} is ramping down. Figure 11 shows V_{OUT} when SETVID_FAST rises after the previous SETVID_FAST cycle has finished falling.

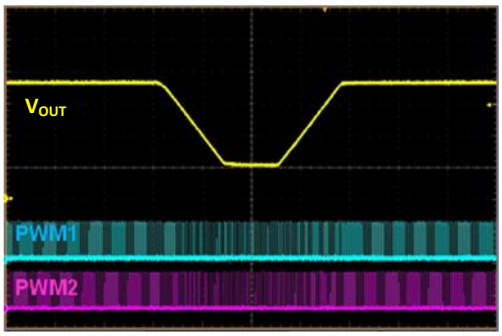

Figure 11: DVID Rising and Falling

Programmable Audible Noise Reduction (PANR)

Audible noise is an issue that mostly occurs when the capacitor flexes within the voltage fluctuation at a certain frequency. The MPQ29164 provides a control algorithm for programmable audible noise reduction (PANR) to mitigate voltage fluctuations within the audible frequency range. This function is activated by an enable bit.

Two registers are available to configure this function. If a SETVID down step exceeds the amplitude defined by register MFR_AUDIBLE_REDUCE (3Ah), bits[7:0], then this command is delayed for a certain time, set by MFR_VID_DOWN_DELAY (3Bh), bits[15:0].

Automatic Phase-Shedding (APS)

The MPQ29164 provides APS to improve efficiency in PS0 according to the comparison between the total current report and the configurable threshold.

If a SETPS command is received to enter PS1, PS2, or PS3, then the VR exits the automatic mode and changes the phase number to the value that is commanded by that particular power state.

There are three registers to configure the APS function:

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- MFR_APS_PHASE_HYS (4Bh), bits[8:4] set the phase-shedding level for 1-phase in CCM. The phase-shedding level for 2-phase to 4-phase CCM is MFR_1PHL multiplied by the phase number. MFR_APS_PHASE_HYS (4Bh), bits[12:9] set the level from 1-phase CCM to DCM.
- MFR_APS_PHASE_HYS (4Bh), bits[3:0] set the hysteresis current value during phase-adding.
- MFR_APSI_CTRL (30h), bits[7:5] sets the delay time for phase-shedding after the system's total detected current drops below the phase-shedding threshold. Once the total current exceeds the phase-adding threshold, the idle phases are added immediately (see Figure 12). See the MFR_APSI_CTRL (30h) section on page 89 for more details.

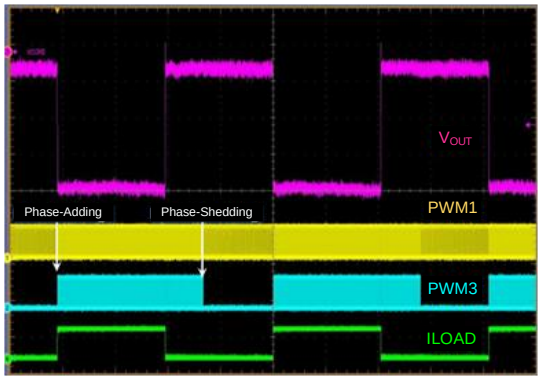

Figure 12: Phase-Shedding and Phase-Adding Process

Table 6 and Table 7 list the phase-shedding and phase-adding entry conditions based on the current report.

Table 6: Phase Number during Phase-Adding Based on the Output Current (I_{OUT}) Report

Condition	Phase Number
3 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT}	4-phase CCM or full-phase (<4) CCM
2 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT} < 3 x MFR_1PHL + MFR_PHASE_HYS	3-phase CCM or full-phase (<3) CCM
1 x MFR_1PHL + MFR_PHASE_HYS ≤ I_{OUT} < 2 x MFR_1PHL+ MFR_PHASE_HYS	2-phase CCM or full-phase (<2) CCM
MFR_0PHL + MFR_PHASE_HYS ≤ I_{OUT} < 1 x MFR_1PHL+ MFR_PHASE_HYS	1 phase CCM
I_{OUT} < MFR_0PHL + MFR_PHASE_HYS	1 phase DCM

Table 7: Phase Number during Phase-Shedding Based on the Output Current (I_{OUT}) Report

Condition	Phase Number
3 x MFR_1PHL < I_{OUT}	4-phase CCM or full-phase (<4) CCM
2 x MFR_1PHL < I_{OUT} ≤ 3 x MFR_1PHL	3-phase CCM or full-phase (<3) CCM
1 x MFR_1PHL < I_{OUT} ≤ 2 x MFR_1PHL	2-phase CCM or full-phase (<2) CCM
MFR_0PHL < I_{OUT} ≤ 1 x MFR_1PHL	1-phase CCM
I_{OUT} ≤ MFR_0PHL	1-phase DCM

In addition to the basic requirements listed in Table 6 and Table 7, follow the instructions below to improve the transient condition:

- When the configured full-phase number is smaller than the phase-adding number, the system runs with full phase.
- The DVID process runs with full phase if the VR receives a SETVID_FAST or SETVID_SLOW command from the processor, regardless of whether APS is enabled or disabled. Phase-shedding begins after the VR settles.
- Load step-up causes a high f_{SW}, which forces the VR to run with full phase to avoid triggering V_{OUT} undershoot.

I²C and SVID Communication

The MPQ29164 supports real-time monitoring for the VR operation parameters, as well as status monitoring via the I²C and SVID interfaces (see Table 8 on page 21).

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Table 8: I²C and SVID-Monitored Parameters

Parameter	I²C	SVID
V_{OUT}	✓	✓
I_{OUT}	✓	✓
Temperature	✓	✓
V_{IN}	✓	✓
Input power (P_{IN})	✓	✓
Phase current	✓	-
Over-voltage (OV)	✓	-
Over-current (OC)	✓	✓
Under-voltage (UV)	✓	-
Over-temperature (OT)	✓	✓
CML	✓	-

V_{IN} Protections

The MPQ29164 features configurable V_{IN} protections with the following thresholds, configured via the related I²C registers:

- If the sensed V_{IN} drops below VIN_OFF (36h), bits[7:0], then the VR tri-state shuts down immediately. The device restarts when the sensed V_{IN} exceeds VIN_ON (35h), bits[7:0] if the V_{IN} UVLO mode is set for non-latch mode.
- If the sensed V_{IN} exceeds the threshold set via MFR_VIN_OV_UV_LIMIT (C1h), bits[7:0] and the V_{IN} OVP mode is set to latch-off mode, then the VR latches.
- If V_{IN} drops below the threshold set via MFR_VIN_OV_UV_LIMIT (C1h), bits[15:8], then the VR receives a warning.

Over-Voltage Protection (OVP)

The OVP circuit monitors V_{OUT} for an OV condition. Figure 13 shows the OV signal generation.

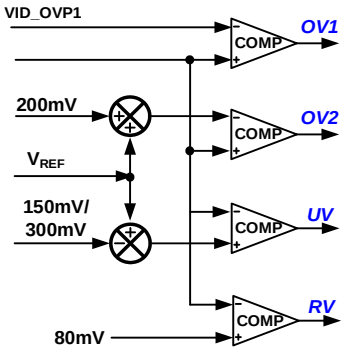

Figure 13: OVP and RVP Trigger Threshold

There are two levels of OVP, described below.

The first type is OVP1, which is set by MFR_OCP_OVP_DAC_LIMIT (60h), bits[7:0]. This is an absolute OV threshold, and it is active whenever the controller is enabled, regardless of the operation/fault conditions. In the event of an OVP1 condition, the PWMs are latched low to turn off the high-side MOSFETs (HS-FETs). The low-side MOSFETs (LS-FETs) turn on to discharge V_{OUT}. The OVP1 latch can only be reset by toggling EN or VCC.

The second type is OVP2. If the detected V_{OUT} exceeds V_{REF} by 400mV, then the controller triggers OVP after a set delay time. OVP2 latches PWM low to discharge V_{OUT} until it drops below 160mV (at this point, RVP is triggered). OVP2 is defined as V_{REF} + 200mV for the half-gain of V_{OUT} to the VDIFF voltage (V_{DIFF}). Figure 14 shows the VR's behavior when OVP2 is triggered.

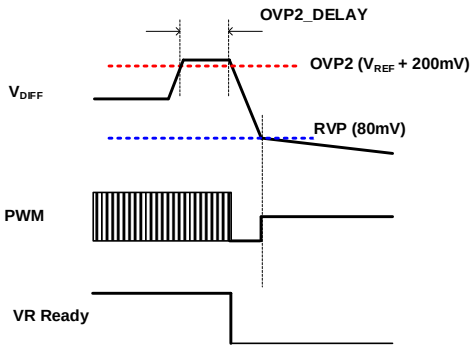

Figure 14: OVP and RVP

To avoid a false trigger, the OVP2 function is blanked during soft start and shutdown, as well as during the VID transition period (including SETVID_FAST/SLOW/DECAY). In addition, OVP2 is disabled in PS4.

OVP2 is latch-off by default in normal IMVP8/9/9.1 applications. Additional modes, such as retry and hiccup mode, can be set via MFR_PROTECT_MODE (34h), bits[5:4]. The OVP delay time is set via MFR_OVP_UVP_SET (61h), bits[11:6].

Reverse-Voltage Protection (RVP)

During OVP, the LS-FET remains on to drive the inductor current negative. A large reverse inductor current can produce negative output voltages that may damage the processor and other output components. In addition to OVP, the MPQ29164 implements RVP prevent negative voltage ringing after the OV logic is triggered.

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If V_{DIFF} drops below 80mV, the MPQ29164 triggers RVP by latching all PWM outputs to tri-state. The reverse inductor current is quickly reset to 0A by dissipating the energy in the inductor to the input DC voltage source through a forward-biased body diode of the HS-FETs (see Figure 14 on page 21).

Over-Current Protection (OCP)

The MPQ29164 provides configurable total current protection for each rail to prevent the VR from working at extremely heavy loads. If the sensed average total I_{OUT} exceeds the over-current (OC) threshold set via MFR_OCP_SET (62h), bits[6:0], then OCP is triggered.

If the sensed I_{OUT} exceeds the OCP threshold for the delay time set via MFR_OCP_SET (62h), bits[12:7], then the device turns off both the HS-FETs and LS-FETs by setting the PWM to tri-state. Figure 15 shows the OCP process for total current protection.

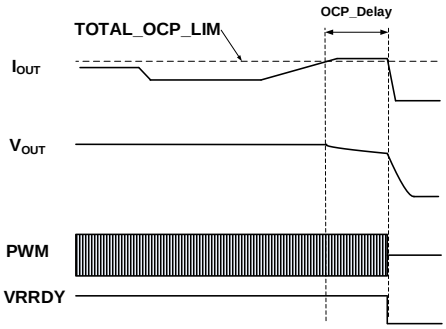

Figure 15: Total Current OCP

The total OCP limit and delay time are set by MFR_OCP_SET (62h). Set the OCP threshold to be about 130% of the maximum output current (I_{CCMAX}). The OCP delay is recommended to be about 500µs.

Phase Current Limit Protection

In addition to the total OC limit based on the sensed I_{OUT}, the MPQ29164 also utilizes a cycle-by-cycle valley point OC limit method to limit each phase current.

If the phase current exceeds the set valley point for 80ns, this phase does not turn on. The next phase turns on when its own PWM is on, which regulates V_{OUT} at the set point. The phase current limit does not trigger latch-off mode. Latch-off mode is triggered only if the phase current limit is triggered by OCP or UVP.

The valley point OC level can be configured via MFR_OCP_OVP_DAC_LIMIT (60h), bits[15:8] to limit the per-phase current.

Figure 16 shows the process when V_{OUT} is shorted to ground. During this process, the per-phase OCP limits the phase current immediately. The VR shuts down after a set time.

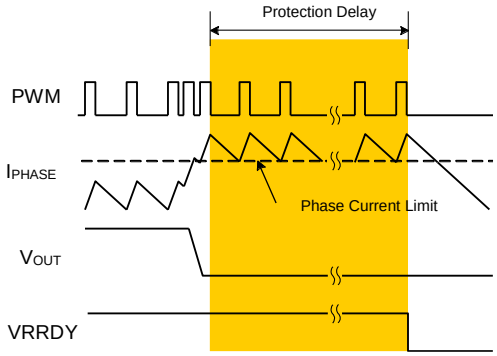

Figure 16: Phase Current Limit Protection during Output Dead Short

The MPQ29164 supports Fast-V mode VRHOT# behavior during cycle-by-cycle current limiting. The MPQ29164 asserts VRHOT# if either of the following occurs:

- The VR receives a SETVID slew command to a high voltage while the VR is in cycle-by-cycle limiting.
- VR cycle-by-cycle limiting is triggered while the VR is actively slewing the output to a higher voltage.

If VRHOT# asserts due to one of the above events, the PWM controller asserts VRHOT# until the SETVID slew target voltage is reached; at this point, VRHOT# can de-assert.

Under-Voltage Protection (UVP)

If the sensed V_{OUT} drops below V_{REF} - (150mV or 300mV) for a set time, then the system triggers UVP and immediately shuts down. All phases set by the PWM go into tri-state (see Figure 17 on page 23). Typically, UVP is triggered when OCP is reached.

The UVP model (set to latch-off by default) can be set via MFR_PROTECT_MODE (34h), bits[7:6]. The UVP delay time is set via MFR_OVP_UVP_SET (61h), bits[5:0].

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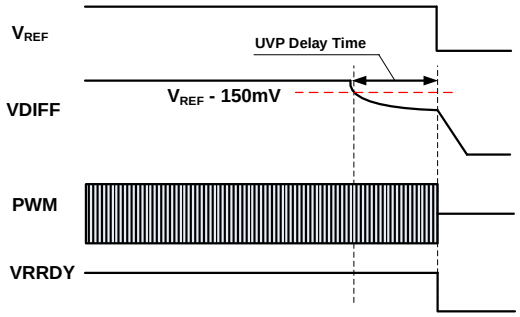

Figure 17: Under-Voltage Protection

VRHOT#

The VRHOT# fault asserts if the sensed external temperature exceeds the maximum temperature threshold. This is used for fault reporting only, and cannot shut down the system. VRHOT# has a fixed 3°C hysteresis if VRHOT# asserts. The VRHOT# pin also asserts if the PSYS pin exceeds its critical value. VRHOT# is initialized in tri-state when the device starts up.

Phase Current Balancing/Thermal Balancing

The MPQ29164 phase current is sensed and calculated with the current reference in the slow current proportion integrate (PI) loop. Each phase's PWM on time is adjusted individually to balance the currents by applying sigma-delta (Σ-Δ) modulation and delay line-loop (DLL) technology in the current balance modulation. This balances the current and greatly reduces jitter.

Each current balance loop can also include a configurable phase current offset to achieve thermal balance among the phases. The phase that has the worst cooling capability can be set to take less phase current by adding an offset on the CS sample value. This helps thermally balance the phases.

SVID Interface

To support using multiple VR devices on the same SVID bus, the SVID address can be configured independently via MFR_ADDR_SVID_CTRL (52h), bits[3:0]. The SVID address is a 4-bit code. There are 14 addresses for up to 14 VR controllers. The final addresses (0Eh and 0Fh) are all call addresses, meaning that all of the VR controllers respond to those addresses.

The all call address is only used with SETVID or SETPS commands. It cannot be used with GETREG, SETREGADR, or SETREGDAT commands. The VR does not acknowledge those commands with an all call address. The VR acknowledges an all call address similarly to how it responds to a single address.

Input Power Sense

The SVID address 0Dh domain reports the system input power (P_{IN}). When the PSYS voltage (V_{PSYS}) reaches V_{PSYS_MAX}, the platform P_{IN} has reached $P_{WR_IN_MAX}$. Then the VR reports to the CPU that the value for SVID's 1Bh register is FFh. V_{PSYS_MAX} is 1.6V.

The P_{IN} sense device sends out a current signal to the MPQ29164. This current is proportional to P_{IN}. A resistor (R_{PSYS}) connected from PSYS to GND converts the current into a voltage. A bypass capacitor is required. R_{PSYS} can be estimated with Equation (10):

$$R_{PSYS} = \frac{V_{PSYS_MAX}}{P_{WR_IN_MAX} \times I_{SYS}} \quad (10)$$

Where I_{SYS} is the current gain of the P_{IN} sensor (in μA/W), and $P_{WR_IN_MAX}$ is the maximum input power (in W).

Figure 18 shows the PSYS connection.

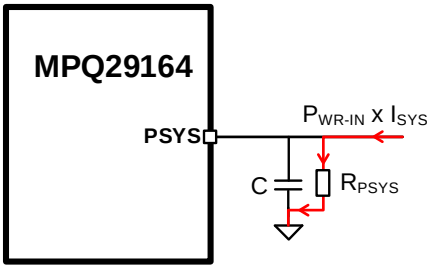

Figure 18: PSYS Connection

The averaging interval for the P_{IN} sense is 1ms, and the register updates every 500μs.

PS4 Enter/Exit Mechanism

The VR enters PS4 mode after receiving a SETPS4 command. In PS4 mode, the VR changes the VID of the rail to 00h and halts the VR's PWM(s) immediately. ALT# de-asserts in PS4, and the chip turns off PLL and disables as many analog circuits as possible to save power (except for the SVID interface).

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The SETVID or SETPS0/1/2/3 commands are used to wake up the VR from PS4 mode. Any rail that receives the SETVID or SETPS0/1/2/3 command enables the internal PLL and analog circuits. The PS4 exit latency is shorter than 80µs, and begins counting after the acknowledgement of the PS4 exit command. The timer counts until VID is ready to ramp (SETPS), or until SETVID starts ramping.

STBA and STBB Function

The STB function sets the MPS Intelli-Phase™ to standby mode by connecting STB to the Intelli-Phase™'s EN pin. In PS4 mode, STB goes to tri-state, and the Intelli-Phase™ enters low-power mode to save power. During normal operation, STB is logic high. Figure 19 shows the connection between the MPQ29164's STBA/B pin and the Intelli-Phase™'s EN pin.

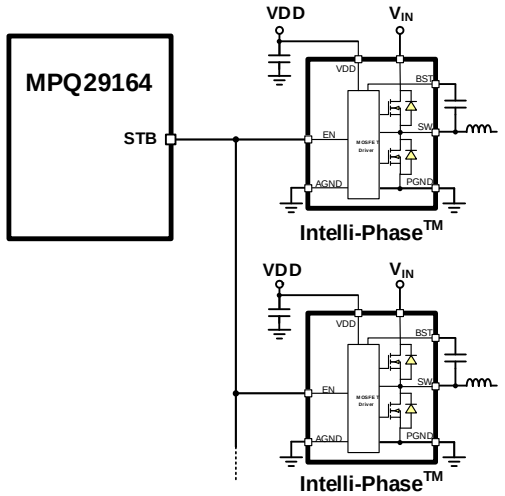

Figure 19: STB Connection between the MPQ29164 and the Intelli-Phase™

On-Time Separate Setting

The on time (t_{ON}) can be set separately in PS1 and PS2/3. This function ensures that the controller optimizes f_{SW} for efficiency at different power stages. In PS1 and PS2/3, f_{SW} can be lower to reduce switching loss, and a larger-value inductor can be used to maintain the ripple. If t_{ON} is 100% in PS0, the register setting options for PS1, PS2, and PS3 are as follows: 75%, 100%, 125%, 150%, 175%, 200%, 225%, or 250%.

AUX IMON Report

The SVID address domain (0Dh) is also defined to report the AUX power output. When the voltage on AUX_IMON reaches $V_{AUX_IMON_MAX}$, this means that the AUX rail's output current has reached AUX_ICCMAX. Then the VR reports to the CPU that the value for SVID's 15h register is FFh.

The AUX rail power device sends a current signal to the MPQ29164. This current is proportional to the AUX output current. A resistor (R_{AUX_IMON}) connected from AUX_IMON to GND converts the current into a voltage. A bypass capacitor is required. R_{AUX_IMON} can be calculated with Equation (11):

$$R_{AUX_IMON} = \frac{V_{AUX_IMON_MAX}}{K_{CS_AUX} \times AUX_ICCMAX} \quad (11)$$

Where K_{CS_AUX} is the current-sense gain of the AUX rail, AUX_ICCMAX is the is the maximum output current (in A), and $V_{AUX_IMON_MAX}$ = 1.6 x 8 / 11V.

Figure 20 shows the AUX IMON connection.

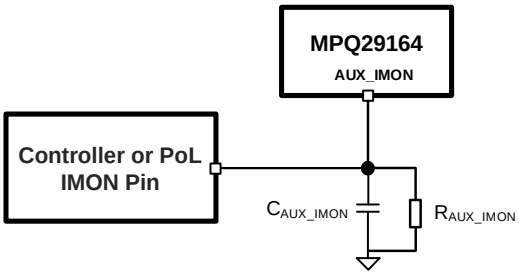

Figure 20: AUX IMON Connection

VID Strap

MFR_PSI_ICC_CTRL (4Ah), bit[13] determines if the VID step is selected by the VID strap pin or MFR_VID_STEP_SEL (39h), bit[7]. Table 9 shows the VID step when it is selected by the VID strap pin.

Table 9: VID Strap Level and VID Step

VID_STRAP Level	Pull High to 3V3	Pull Low to GND
VID step	5mV	10mV

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SVID REGISTERS

Table 10 shows the data and configuration registers for the SVID protocol.

Table 10: SVID Data and Configuration Registers

Index	Register Name	Access	Default	Note
00h	VENDOR_ID	Read-only by the initiator, write by the vendor	25h	Configurable via the I²C.
01h	PRODUCT_ID		6Ch	
02h	PRODUCT_REVISION		00h	
05h	PROTOCOL_ID		0Eh	
06h	CAPABILITY		81h	
10h	STATUS_1	Read by the initiator, write by the PWM	00h	These registers depend on the operating conditions. The register values vary with the operating conditions.
11h	STATUS_2		00h	
12h	TEMPERATURE_ZONE		00h	
15h	OUTPUT_CURRENT (IOUT)		00h	
17h	VR_TEMPERATURE		00h	
1Ah	INPUT_VOLTAGE		00h	
1Bh	INPUT_POWER		00h	
1Ch	STATUS2_LAST_READ		00h	
1Fh	ICC_LIMIT	Read and write by the initiator	00h	Can only be configured via the CPU.
21h	ICC_MAX	Read-only, configured by the platform	00h	Configurable via the I²C.
22h	TEMP_MAX		7Dh	
24h	SR-FAST		30mV/µs	
25h	SR-SLOW		15mV/µs	
26h	VBOOT		00h	
27h	VR_TOLERANCE		0Ah	
2Ah	SLOW_SLEW_SELECTOR		01h	Can only be configured via the CPU.
2Bh	PS4_EXIT_LATENCY		00h	Configurable via the I²C.
2Ch	PS3_EXIT_LATENCY		00h	
2Dh	ENABLE_TO_READY_FOR_SVID		00h	
2Eh	POWER_IN_MAX		FFh	
30h	VOUT_MAX	Read and write be the initiator	FFh	Can only be configured via the CPU.
31h	VID_SETTING		00h	
32h	PWR_STATE		00h	
33h	VID_OFFSET		00h	
34h	MULTI_VR_CONFIGURE	Read and write by the initiator	01h	Configurable via the I²C.
49h	PSYS_CRITICAL_DEASSERTION_ DEBOUNCE_TIME	Read and write by the initiator	00h	Can only be configured via the CPU.
4Ah	PSYS_CRIT_THRESHOLD		00h	
4Bh	PSYS_WARN2_THRESHOLD		00h	
4Ch	PSYS_WARN1_THRESHOLD		00h	
4Dh	PSYS_WARNING_2_COUNTER	Read-only by the initiator	00h	These registers depend on the operating conditions. The register values vary with the operating conditions.
4Eh	PSYS_WARNING_1_COUNTER		00h	
4Fh	PSYS_CRITICAL_ASSERTION_ DEBOUNCE_TIME	Read and write by the initiator	00h	Can only be configured via the CPU.
50h	HIGH_CURRENT_CAPABILITY	Read-only, configured by the platform	00h	Configurable via the I²C.
5Ch	I_LIMIT_COUNT	Read-only by the initiator	00h	This register depends on the operating conditions. The register values vary with the operating conditions.

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VID RANGE

The MPQ29164 covers the full IMVP8/IMVP9 VID range. The IMVP8 VID is 0V, and ranges between 0.25V and 1.52V. If VID is between 0.25V and 1.52V, the voltage step is 5mV/step. The IMVP9 VID step is 5mV or 10mV; the voltage for the 5mV VID step matches the IMVP8 values. The 10mV/step for the IMVP9 VID is 0V, and ranges between 0.2V and 2.74V. If VID is between 0.2V and 2.74V, the voltage step is 10mV/step. Table 11 shows the 5mV VID in IMVP8. Table 12 on page 27 shows the 10mV VID in IMVP9.

Table 11: IMVP8 5mV VID Step VID Table

VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)	VID (Hex)	V_{OUT} (V)
00	0	40	0.565	80	0.885	C0	1.205
01	0.25	41	0.57	81	0.89	C1	1.21
02	0.255	42	0.575	82	0.895	C2	1.215
03	0.26	43	0.58	83	0.9	C3	1.22
04	0.265	44	0.585	84	0.905	C4	1.225
05	0.27	45	0.59	85	0.91	C5	1.23
06	0.275	46	0.595	86	0.915	C6	1.235
07	0.28	47	0.6	87	0.92	C7	1.24
08	0.285	48	0.605	88	0.925	C8	1.245
09	0.29	49	0.61	89	0.93	C9	1.25
0A	0.295	4A	0.615	8A	0.935	CA	1.255
0B	0.3	4B	0.62	8B	0.94	CB	1.26
0C	0.305	4C	0.625	8C	0.945	CC	1.265
0D	0.31	4D	0.63	8D	0.95	CD	1.27
0E	0.315	4E	0.635	8E	0.955	CE	1.275
0F	0.32	4F	0.64	8F	0.96	CF	1.28
10	0.325	50	0.645	90	0.965	D0	1.285
11	0.33	51	0.65	91	0.97	D1	1.29
12	0.335	52	0.655	92	0.975	D2	1.295
13	0.34	53	0.66	93	0.98	D3	1.3
14	0.345	54	0.665	94	0.985	D4	1.305
15	0.35	55	0.67	95	0.99	D5	1.31
16	0.355	56	0.675	96	0.995	D6	1.315
17	0.36	57	0.68	97	1	D7	1.32
18	0.365	58	0.685	98	1.005	D8	1.325
19	0.37	59	0.69	99	1.01	D9	1.33
1A	0.375	5A	0.695	9A	1.015	DA	1.335
1B	0.38	5B	0.7	9B	1.02	DB	1.34
1C	0.385	5C	0.705	9C	1.025	DC	1.345
1D	0.39	5D	0.71	9D	1.03	DD	1.35
1E	0.395	5E	0.715	9E	1.035	DE	1.355
1F	0.4	5F	0.72	9F	1.04	DF	1.36
20	0.405	60	0.725	A0	1.045	E0	1.365
21	0.41	61	0.73	A1	1.05	E1	1.37
22	0.415	62	0.735	A2	1.055	E2	1.375
23	0.42	63	0.74	A3	1.06	E3	1.38
24	0.425	64	0.745	A4	1.065	E4	1.385
25	0.43	65	0.75	A5	1.07	E5	1.39
26	0.435	66	0.755	A6	1.075	E6	1.395
27	0.44	67	0.76	A7	1.08	E7	1.4
28	0.445	68	0.765	A8	1.085	E8	1.405
29	0.45	69	0.77	A9	1.09	E9	1.41
2A	0.455	6A	0.775	AA	1.095	EA	1.415
2B	0.46	6B	0.78	AB	1.1	EB	1.42

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Table 11: IMVP8 5mV VID Step VID Table *(continued)*

VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)
2C	0.465	6C	0.785	AC	1.105	EC	1.425
2D	0.47	6D	0.79	AD	1.11	ED	1.43
2E	0.475	6E	0.795	AE	1.115	EE	1.435
2F	0.48	6F	0.8	AF	1.12	EF	1.44
30	0.485	70	0.805	B0	1.125	F0	1.445
31	0.49	71	0.81	B1	1.13	F1	1.45
32	0.495	72	0.815	B2	1.135	F2	1.455
33	0.5	73	0.82	B3	1.14	F3	1.46
34	0.505	74	0.825	B4	1.145	F4	1.465
35	0.51	75	0.83	B5	1.15	F5	1.47
36	0.515	76	0.835	B6	1.155	F6	1.475
37	0.52	77	0.84	B7	1.16	F7	1.48
38	0.525	78	0.845	B8	1.165	F8	1.485
39	0.53	79	0.85	B9	1.17	F9	1.49
3A	0.535	7A	0.855	BA	1.175	FA	1.495
3B	0.54	7B	0.86	BB	1.18	FB	1.5
3C	0.545	7C	0.865	BC	1.185	FC	1.505
3D	0.55	7D	0.87	BD	1.19	FD	1.51
3E	0.555	7E	0.875	BE	1.195	FE	1.515
3F	0.56	7F	0.88	BF	1.2	FF	1.52

Table 12: IMVP9 10mV VID Step VID Table

VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)
00	0	40	0.83	80	1.47	C0	2.11
01	0.2	41	0.84	81	1.48	C1	2.12
02	0.21	42	0.85	82	1.49	C2	2.13
03	0.22	43	0.86	83	1.5	C3	2.14
04	0.23	44	0.87	84	1.51	C4	2.15
05	0.24	45	0.88	85	1.52	C5	2.16
06	0.25	46	0.89	86	1.53	C6	2.17
07	0.26	47	0.9	87	1.54	C7	2.18
08	0.27	48	0.91	88	1.55	C8	2.19
09	0.28	49	0.92	89	1.56	C9	2.2
0A	0.29	4A	0.93	8A	1.57	CA	2.21
0B	0.3	4B	0.94	8B	1.58	CB	2.22
0C	0.31	4C	0.95	8C	1.59	CC	2.23
0D	0.32	4D	0.96	8D	1.6	CD	2.24
0E	0.33	4E	0.97	8E	1.61	CE	2.25
0F	0.34	4F	0.98	8F	1.62	CF	2.26
10	0.35	50	0.99	90	1.63	D0	2.27
11	0.36	51	1	91	1.64	D1	2.28
12	0.37	52	1.01	92	1.65	D2	2.29
13	0.38	53	1.02	93	1.66	D3	2.3
14	0.39	54	1.03	94	1.67	D4	2.31
15	0.4	55	1.04	95	1.68	D5	2.32
16	0.41	56	1.05	96	1.69	D6	2.33
17	0.42	57	1.06	97	1.7	D7	2.34
18	0.43	58	1.07	98	1.71	D8	2.35
19	0.44	59	1.08	99	1.72	D9	2.36
1A	0.45	5A	1.09	9A	1.73	DA	2.37
1B	0.46	5B	1.1	9B	1.74	DB	2.38
1C	0.47	5C	1.11	9C	1.75	DC	2.39

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Table 12: IMVP9 10mV VID Step VID Table *(continued)*

VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)	VID (Hex)	VOUT (V)
1D	0.48	5D	1.12	9D	1.76	DD	2.4
1E	0.49	5E	1.13	9E	1.77	DE	2.41
1F	0.5	5F	1.14	9F	1.78	DF	2.42
20	0.51	60	1.15	A0	1.79	E0	2.43
21	0.52	61	1.16	A1	1.8	E1	2.44
22	0.53	62	1.17	A2	1.81	E2	2.45
23	0.54	63	1.18	A3	1.82	E3	2.46
24	0.55	64	1.19	A4	1.83	E4	2.47
25	0.56	65	1.2	A5	1.84	E5	2.48
26	0.57	66	1.21	A6	1.85	E6	2.49
27	0.58	67	1.22	A7	1.86	E7	2.5
28	0.59	68	1.23	A8	1.87	E8	2.51
29	0.6	69	1.24	A9	1.88	E9	2.52
2A	0.61	6A	1.25	AA	1.89	EA	2.53
2B	0.62	6B	1.26	AB	1.9	EB	2.54
2C	0.63	6C	1.27	AC	1.91	EC	2.55
2D	0.64	6D	1.28	AD	1.92	ED	2.56
2E	0.65	6E	1.29	AE	1.93	EE	2.57
2F	0.66	6F	1.3	AF	1.94	EF	2.58
30	0.67	70	1.31	B0	1.95	F0	2.59
31	0.68	71	1.32	B1	1.96	F1	2.6
32	0.69	72	1.33	B2	1.97	F2	2.61
33	0.7	73	1.34	B3	1.98	F3	2.62
34	0.71	74	1.35	B4	1.99	F4	2.63
35	0.72	75	1.36	B5	2	F5	2.64
36	0.73	76	1.37	B6	2.01	F6	2.65
37	0.74	77	1.38	B7	2.02	F7	2.66
38	0.75	78	1.39	B8	2.03	F8	2.67
39	0.76	79	1.4	B9	2.04	F9	2.68
3A	0.77	7A	1.41	BA	2.05	FA	2.69
3B	0.78	7B	1.42	BB	2.06	FB	2.7
3C	0.79	7C	1.43	BC	2.07	FC	2.71
3D	0.8	7D	1.44	BD	2.08	FD	2.72
3E	0.81	7E	1.45	BE	2.09	FE	2.73
3F	0.82	7F	1.46	BF	2.1	FF	2.74

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SUPPORTED PMBUS COMMANDS

Command Code	Command Name	Type	Bytes	Page 0	Page 1
00h	PAGE	R/W	1	✓	✓
01h	OPERATION	R/W	1	✓	✓
03h	CLEAR_FAULTS	W	1	✓	✓
07h	LAST_FAULT_BLOCK	R/W	2	✓	-
08h	CLEAR_LAST_FAULT	W	1	✓	✓
09h	SINGLE_READ_TRIG	W	1	✓	✓
0Ah	MFR_SINGLE_RW_ADDR	R/W	2	✓	-
0Bh	MFR_SINGLE_WR_DATA	R/W	2	✓	-
0Ch	SINGLE_WRITE_TRIG	W	1	✓	✓
15h	STORE_USER_ALL	W	1	✓	✓
16h	RESTORE_USER_ALL	W	1	✓	✓
19h	TM_MTP_WRITE_TRIG	W	1	✓	✓
1Ah	MFR_GATECLK_DIS	R/W	2	✓	-
1Bh	MFR_IDROOP_CTRL	R/W	2	✓	✓
1Dh	MFR_MTP_CTRL	R/W	2	✓	-
1Eh	MFR_PSYS_WARN_FILT_CNT	R/W	2	✓	-
1Fh	MFR_LOW_VOUT_TRIM	R/W	2	✓	✓
21h	VOUT_COMMAND	R/W	2	✓	✓
22h	MFR_VOUT_TRIM	R/W	2	✓	✓
23h	VOUT_CAL_OFFSET	R/W	2	✓	✓
24h	MFR_VOUT_MAX	R/W	2	✓	✓
25h	VOUT_MARGIN_HIGH	R/W	2	✓	✓
26h	VOUT_MARGIN_LOW	R/W	2	✓	✓
27h	MFR_VBOOT	R/W	2	✓	✓
28h	MFR_FS	R/W	2	✓	✓
29h	MFR_PHASE_NUM	R/W	2	✓	✓
2Ah	MFR_DBG_ADC_CHANNEL	R/W	2	✓	-
2Bh	MFR_CONFIG1	R/W	2	✓	✓
2Ch	MFR_IMON_SNS_OFFS	R/W	2	✓	✓
2Dh	MFR_ADC_HOLD_TIME	R/W	2	✓	-
2Eh	MFR_PLATFORM_TIME_SET	R/W	2	✓	✓
2Fh	MFR_DEBUG	R/W	2	✓	-
30h	MFR_APSI_CTRL	R/W	2	✓	✓
31h	MFR_FS_LOOP_CYC_RIPPLE_SET	R/W	2	✓	✓
32h	MFR_DC_CB_DYNC_SET	R/W	2	✓	✓
33h	MFR_VOUT_CMPS_SET	R/W	2	✓	✓
34h	MFR_PROTECT_MODE	R/W	2	✓	✓
35h	VIN_ON	R/W	2	✓	-
36h	VIN_OFF	R/W	2	✓	-
37h	MFR_VCAL_FS_PI	R/W	2	✓	✓
38h	IOUT_CAL_GAIN_SET	R/W	2	✓	✓
39h	MFR_VR_CONFIG	R/W	2	✓	✓
3Ah	MFR_AUDIBLE_REDUCE	R/W	2	✓	✓
3Bh	MFR_VID_DOWN_DELAY	R/W	2	✓	✓
3Ch	MFR_FILTER_SET	R/W	2	✓	✓
3Dh	MFR_TRANS_FAST	R/W	2	✓	✓
3Eh	MFR_EN_SEQUENCE_CFG	R/W	2	✓	-
	MFR_EN_DLY	R/W		-	✓
3Fh	MFR_ALT_SET	R/W	2	✓	✓
40h	MFR_SW_LF_SET	R/W	2	✓	✓
41h	MFR_SW_HF_SET	R/W	2	✓	✓
42h	MFR_TON_ADJ_PS1_SW_LF_TH	R/W	2	✓	✓
43h	MFR_PS2_OFFSLOPE_TON_TH	R/W	2	✓	✓
44h	MFR_TON_ADJ_PS1_SW_HF_TH	R/W	2	✓	✓

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SUPPORTED PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
45h	MFR_TON_ADJ_PS2_SW_HF_TH	R/W	2	✓	✓
46h	MFR_SLOPE_CNT_SETPS1	R/W	2	✓	✓
47h	MFR_SLOPE_SR_SETPS1	R/W	2	✓	✓
48h	MFR_CONFIG2	R/W	2	✓	✓
49h	MFR_CONFIG3	R/W	2	✓	✓
4Ah	MFR_PSI_ICC_CTRL	R/W	2	✓	✓
4Bh	MFR_APS_PHASE_HYS	R/W	2	✓	✓
4Ch	MFR_VOUT_MAX_9BIT	R/W	2	✓	✓
4Dh	MFR_SLOPE_CNT_DCM_SET	R/W	2	✓	✓
4Eh	MFR_SLOPE_SR_DCM	R/W	2	✓	✓
4Fh	MFR_SHUTDOWN_LEVEL	R/W	2	✓	✓
50h	MFR_SYS_PASSWORD	R/W	2	✓	-
51h	MFR_INPUT_PASSWORD	R/W	2	✓	-
52h	MFR_ADDR_SVID_CTRL	R/W	2	✓	✓
53h	MFR_ICC_MAX_SET	R/W	2	✓	✓
54h	MFR_CYC_OCP_FACTOR	R/W	2	✓	✓
55h	MFR_PWR_INDUCTOR_GAIN	R/W	2	✓	✓
60h	MFR_OCP_OVP_DAC_LIMIT	R/W	2	✓	✓
61h	MFR_OVP_UVP_SET	R/W	2	✓	✓
62h	MFR_OCP_SET	R/W	2	✓	✓
70h	READ_VFB_SENSE	R	2	✓	✓
71h	READ_AD_RESULT	R	2	✓	✓
72h	SVID_REG_80H_81H	R	2	✓	-
73h	SYS_STATE_AND_SVID_REG_82H	R	2	✓	-
74h	MFR_SLAVE_ADDR	R	2	✓	-
75h	READ_RAIL_STATE	R	2	✓	✓
76h	READ_VCOMP	R	2	✓	✓
77h	CHECK_SUM_USER	R	2	✓	-
78h	STATUS_BYTE	R	1	✓	✓
79h	STATUS_WORD	R	2	✓	✓
7Ah	STATUS_VOUT	R	1	✓	✓
7Bh	STATUS_IOUT	R	1	✓	✓
7Ch	STATUS_INPUT	R	1	✓	-
7Dh	STATUS_TEMPERATURE	R	1	✓	-
7Eh	STATUS_CML	R	2	✓	-
80h	READ_VREF_PS	R	2	✓	✓
88h	READ_VIN	R	2	✓	-
8Bh	READ_VOUT	R	2	✓	✓
8Ch	READ_IOUT	R	2	✓	✓
8Dh	READ_TEMPERATURE	R	2	✓	-
90h	PROTOCOL_ID_EN_RDY	R/W	2	✓	-
91h	MFR_SVID_CFG	R/W	2	✓	-
92h	VENDOR_ID_PRODUCT_ID	R/W	2	✓	-
93h	PRODUCT_DATA_CODE	R/W	2	✓	-
94h	LOT_CODE_VR	R/W	2	✓	-
95h	PS3_PS4_EXIT_DELAY	R/W	2	✓	✓
96h	MFR_SR_FAST_TOLERANCE	R/W	2	✓	✓
97h	MFR_SVID_06H_34H_VR	R/W	2	✓	✓
98h	MFR_SVID_06H_34H_PSYS	R/W	2	✓	-
99h	MFR_STANDBY_HOT_SET	R/W	2	✓	-
9Ah	MFR_SVID_OFFSET	R/W	2	✓	✓
A0h	MFR_MIN_ON_TIME	R/W	2	✓	-
A1h	MFR_MIN_OFF_TIME	R/W	2	✓	-
A2h	MFR_MIN_HIZ_TIME	R/W	2	✓	-

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SUPPORTED PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
A3h	MFR_BLANK_TIME	R/W	2	✓	✓
B0h	MFR_PSI_TRIM4	R/W	2	✓	✓
B1h	MFR_PSI_TRIM1	R/W	2	✓	-
B2h	MFR_PSI_TRIM2	R/W	2	✓	-
B3h	MFR_PSI_TRIM3	R/W	2	✓	-
B4h	MFR_CS_READ1	R	2	✓	-
B5h	MFR_CS_READ2	R	2	✓	-
B6h	MFR_CS_READ3	R	2	✓	-
B7h	RESERVED	R	2	✓	-
B8h	MFR_CS_READ5	R	2	✓	-
B9h	READ_AUXIMON	R	2	✓	-
BAh	READ_PIN	R	2	✓	-
BBh	MFR_VIN_HYS_OFFS_SET	R/W	2	✓	-
BCh	MFR_PIN_MAX	R/W	2	✓	-
BDh	MFR_AUXIMON_MAX_SET	R/W	2	✓	-
C0h	MFR_ADDR_PMBUS	R/W	2	✓	-
C1h	MFR_VIN_OV_UV_LIMIT	R/W	2	✓	-
C2h	MFR_OTP_SET	R/W	2	✓	-
D2h	MFR_SLOPE_CNT_1P	R/W	2	✓	-
D3h	MFR_SLOPE_SR_1P	R/W	2	✓	-
D4h	MFR_SLOPE_CNT_2P	R/W	2	✓	-
D5h	MFR_SLOPE_SR_2P	R/W	2	✓	-
D6h	MFR_SLOPE_CNT_3P	R/W	2	✓	-
D7h	MFR_SLOPE_SR_3P	R/W	2	✓	-
D8h	MFR_SLOPE_CNT_4P	R/W	2	✓	-
D9h	MFR_SLOPE_SR_4P	R/W	2	✓	-
DAh	RESERVED1	R/W	2	✓	-
DBh	RESERVED2	R/W	2	✓	-
DCh	RESERVED3	R/W	2	✓	-
DDh	RESERVED4	R/W	2	✓	-
DEh	RESERVED5	R/W	2	✓	-
DFh	RESERVED6	R/W	2	✓	-
E0h	MFR_SLOPE_CNT_5P	R/W	2	✓	-
E1h	MFR_SLOPE_SR_5P	R/W	2	✓	-
E2h	MFR_SLOPE_CNT_6P	R/W	2	✓	-
E3h	MFR_SLOPE_SR_6P	R/W	2	✓	-
E4h	MFR_CS_OFFSET2_3	R/W	2	✓	-
E5h	MFR_CS_OFFSET4	R/W	2	✓	-
E6h	RESERVED7	R/W	2	✓	-
E7h	MFR_CS_OFFSET5_6	R/W	2	✓	-
E8h	MFR_IMON_SVID1	R/W	2	✓	-
E9h	MFR_IMON_SVID2	R/W	2	✓	-
EAh	MFR_IMON_SVID3	R/W	2	✓	-
EBh	MFR_IMON_SVID4	R/W	2	✓	-
ECh	RESERVED8	R/W	2	✓	-
EDh	RESERVED9	R/W	2	✓	-
EEh	RESERVED10	R/W	2	✓	-
EFh	MFR_IMON_SVID5	R/W	2	✓	-
F0h	MFR_IMON_SVID6	R/W	2	✓	-
F1h	MFR_CB_PI_SET	R/W	2	✓	-
F2h	MFR_VIN_GAIN_SET	R/W	2	✓	-
F3h	MFR_AUXIMON_SVID	R/W	2	✓	-
F4h	MFR_PSYS_SVID	R/W	2	✓	-
F5h	MFR_TEMPERATURE_GAIN_SET	R/W	2	✓	-

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SUPPORTED PMBUS COMMANDS *(continued)*

Command Code	Command Name	Type	Bytes	Page 0	Page 1
F6h	MFR_PSYS_GAIN_SEL	R/W	2	✓	-
FEh	CLEAR_EEPROM_FAULTS	W	1	✓	✓

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PAGE 0 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 0 sets the register page. The MPQ29164 has three register pages: Page 0, Page 1, and Page 3. Page 0 and Page 1 are the common commands that are used in application; these values are stored in the multiple-time programmable (MTP) memory. Page 3 is the debugging register that is used for ATE testing; debugging information is not stored in MTP. Do not write to the registers on Page 3.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
1:0	R/W	PAGE	Selects the Page register. 2'b11: Page 3 (debugging page) 2'b10: None 2'b01: Page 1 (rail B and trim registers) 2'b00: Page 0 (rail A registers and some registers for rail B)

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 0 configures the converter's operational state.

Bits	Access	Bit Name	Description
7	R/W	ON_OFF_STATE	Controls whether the PMBus device output is on or off. 1'b0: The output is off 1'b1: The output is on
6	R/W	RESERVED	Reserved.
5:4	R/W	VOLT_CMD_ SOURCE	Controls the basic source of V_{OUT} command when the PMBus device output is on (bit[7] of this command = 1). 2'b00: The nominal V_{OUT} is set by the PMBus VOUT_COMMAND data 2'b01: The nominal V_{OUT} is set by the PMBus VOUT_MARGIN_LOW data 2'b10: The nominal V_{OUT} is set by the PMBus VOUT_MARGIN_HIGH data 2'b11: Not supported
3:2	R/W	MARGIN_FAULT_ RESPONSE	Selects whether a fault is generated if a margin command causes V_{OUT} to exceed VOUT_OV_FAULT_LIMIT or drop below VOUT_UV_FAULT_LIMIT. Effective when the PMBus device output is on (bit[7] of this command = 1). 2'b01: Faults caused by selecting VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW as the nominal V_{OUT} source are ignored 2'b10: Faults caused by selecting VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW as the V_{OUT} source can be triggered
1:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

Format: Unsigned binary

The CLEAR_FAULTS command on Page 0 clears any fault bits that have been set on the rails. This command clears all bits in all status registers simultaneously.

This command is write-only. There is no data byte for this command.

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LAST_FAULT_BLOCK (07h)

Format: Unsigned binary

The LAST_FAULT_BLOCK command on Page 0 records any protection, regardless of the rail, if any of the following faults occur: over-voltage protection (OVP1 or OVP2), over-current protection (OCP), under-voltage protection (UVP), V_{IN} OVP, V_{IN} under-voltage lockout (UVLO), over-temperature protection (OTP), or TEMP_FAULT.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11	R/W	OVP1_R2	Rail B's over-voltage protection (OVP1; OVP_VMAX) flag.
10	R/W	OVP2_R2	Rail B's OVP2 (OVP_VID) flag.
9	R/W	OCP_R2	Rail B's over-current protection (OCP) flag.
8	R/W	UVP_R2	Rail B's under-voltage protection (UVP) flag.
7	R/W	OVP1_R1	Rail A's OVP1 (OVP_VMAX) flag.
6	R/W	OVP2_R1	Rail A's OVP2 (OVP_VID) flag.
5	R/W	OCP_R1	Rail A's OCP flag.
4	R/W	UVP_R1	Rail A's UVP flag.
3	R/W	VIN_OVP	V_{IN} OVP flag.
2	R/W	VIN_UVLO	V_{IN} under-voltage lockout (UVLO) flag.
1	R/W	OTP	Over-temperature protection (OTP) flag.
0	R/W	TEMP_FLT	TEMP_FAULT flag.

CLEAR_LAST_FAULT (08h)

Format: Unsigned binary

The CLEAR_LAST_FAULT command on Page 0 clears the fault information on LAST_FAULT_BLOCK (07h on Page 0).

This command is write-only. There is no data byte for this command.

SINGLE_READ_TRIG (09h)

Format: Unsigned binary

The SINGLE_READ_TRIG command on Page 0 reads data from the MTP by addressing MFR_SINGLE_RW_ADDR (0Ah on Page 0), bits[7:0].

This command is write-only. There is no data byte for this command.

MFR_SINGLE_RW_ADDR (0Ah)

Format: Unsigned binary

The MFR_SINGLE_RW_ADDR command on Page 0 returns the MTP-stored information for SINGLE_READ_TRIG (09h) and SINGLE_WRITE_TRIG (0Ch).

Bits	Access	Bit Name	Description
15:8	R/W	MFR_SINGLE_WR_ADDR	Address for SINGLE_WR_TRIG.
7:0	R/W	MFR_SINGLE_RD_ADDR	Address for SINGLE_READ_TRIG.

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MFR_SINGLE_WR_DATA (0Bh)

Format: Unsigned binary

The MFR_SINGLE_WR_DATA command on Page 0 has information for the MTP. The SINGLE_WRITE_TRIG (0Ch) command writes this data to the MTP.

Bits	Access	Bit Name	Description
15:0	R/W	MFR_SINGLE_WR_DATA	Information that can be written to the MTP.

SINGLE_WRITE_TRIG (0Ch)

Format: Unsigned binary

The SINGLE_WRITE_TRIG command on Page 0 writes the data from MFR_SINGLE_WR_DATA (0Bh on Page 0) to the MTP address in MFR_SINGLE_RW_ADDR (0Ah on Page 0), bits[15:8].

This command is write-only. There is no data byte for this command.

STORE_USER_ALL (15h)

Format: Unsigned binary

The STORE_USER_ALL command on Page 0 instructs the PMBus device to copy the Page 0 to Page 1 contents (not including the read-only registers) from the operating memory to the matching locations in the MTP, regardless of the current PMBus register page. This command can be used while the device is outputting power.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

Format: Unsigned binary

The RESTORE_USER_ALL command on Page 0 instructs the PMBus device to copy the Page 0 to Page 1 contents from the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have matching locations in the operating memory are ignored. This command cannot be used while the device is outputting power unless MFR_EEPROM_COPY_EN (1Dh on Page 0), bit[1] is set to 1.

This command is write-only. There is no data byte for this command.

TM_MTP_WRITE_TRIG (19h)

Format: Unsigned binary

The TM_MTP_WRITE_TRIG command on Page 0 is used for the MTP auto-test function.

This command is write-only. There is no data byte for this command.

MFR_GATECLK_DIS (1Ah)

Format: Unsigned binary

The MFR_GATECLK_DIS command on Page 0 enables the gate clock functions.

Bits	Access	Bit Name	Description
15	R/W	MFR_SVID_DET_GTCLK_DIS	Enables the gate clock to turn off if the SVID detection function stays in an idle state. 1’b1: Disable the gate clock 1’b0: Enable the clock to turn off if the SVID detection function stays in an idle state
14	R/W	MFR_OFF_RAIL_ANA_PS2_DIS	Turns off the rail circuit if VID = 0 in a PS2 state. 1’b1: Disabled 1’b0: Only enable the rail circuit to turn off if VID = 0 in a PS2 state

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13	R/W	MFR_OFF_RAIL_ANA_DIS	Turns off the rail circuit if the rail VID = 0. 1'b1: Disabled 1'b0: Enabled. Turn off the rail circuit if the rail VID = 0
12	R/W	RESERVED	Reserved. Set to 1 by default.
11	R/W	PS1_CTRL_GTCLK_DIS_R2	Enables rail B's gate clock for the CTRL module in PS1. 1'b1: Disabled 1'b0: Enabled
10	R/W	PS1_CTRL_GTCLK_DIS_R1	Enables rail A's gate clock for the CTRL module in PS1. 1'b1: Disabled 1'b0: Enabled
9	R/W	CLK_CHIP_GTCLK_DIS	Enables the gate clock for the CHIP_CTRL module. 1'b1: Disabled 1'b0: Enabled
8	R/W	CLK_ADC_GTCLK_DIS	Enables the gate clock for the ADC_SAMPLE module. 1'b1: Disabled 1'b0: Enabled
7	R/W	CLK_ANA_CTRL_GTCLK_DIS	Enables the gate clock for the ANALOG_CTRL module. 1'b1: Disabled 1'b0: Enabled
6	R/W	CLK_RAIL_CTRL_GTCLK_DIS	Enables the gate clock for the RAIL_CTRL module. 1'b1: Disabled 1'b0: Enabled
5	R/W	CLK_CALC_GTCLK_DIS	Enables the gate clock for the calculation module. 1'b1: Disabled 1'b0: Enabled
4	R/W	CLK_PSYS_GTCLK_DIS	Enables the gate clock for the PSYS_COUNTER module. 1'b1: Disabled 1'b0: Enabled
3	R/W	CLK_MEM_GTCLK_DIS	Enables the gate clock for the MEM_CTRL module. 1'b1: Disabled 1'b0: Enabled
2	R/W	CLK_RAIL_OPR_GTCLK_DIS	Enables the gate clock for the entire RAIL_CTRL module. 1'b1: Disabled 1'b0: Enabled
1	R/W	CLK_ANALOG_GTCLK_DIS	Enables the gate clock for the entire ANALOG_CTRL module. 1'b1: Disabled 1'b0: Enabled
0	R/W	CLK_REG_SLAVE_GTCLK_DIS	Enables the gate clock for the memory (PMBus registers) module. 1'b1: Disabled 1'b0: Enabled

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MFR_IDROOP_CTRL (1Bh)

Format: Unsigned binary

The MFR_IDROOP_CTRL command on Page 0 sets the I_{DROOP} function.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:7	R/W	AC_DROOP_COMP	Selects the bandwidth and biased current for the AC droop.
6	R/W	DAC_CMP_EN	Enables the DAC_CMP function (compared to VREF_FILTER and VREF_DAC). For this bit to be effective, the MFR_DAC_CMP_EN bit must be set to 1'b1. 1'b1: Enabled 1'b0: Disabled
5	R/W	IDROOP_BW_SET	Selects the I_{DROOP} bandwidth. 1'b0: Low bandwidth 1'b1: High bandwidth
4	R/W	IDROOP_EN	Enables the DC I_{DROOP} or the AC I_{DROOP}. 1'b0: Enables DC I_{DROOP} 1'b1: Enables AC I_{DROOP}
3:0	R/W	IDROOP_SET	Sets the I_{DROOP} DC gain to set the digital load-line gain. 4'h0: 0 4'h1: 4/8 x 1/8 4'h2: 5/8 x 1/8 4'h3: 6/8 x 1/8 4'h4: 7/8 x 1/8 4'h5: 8/8 x 1/8 4'h6: 9/8 x 1/8 4'h7: 10/8 x 1/8 4'h8: 11/8 x 1/8 4'h9: 12/8 x 1/8 4'hA: 13/8 x 1/8 4'hB: 14/8 x 1/8 4'hC: 15/8 x 1/8 4'hD: 16/8 x 1/8 4'hE: 17/8 x 1/8 4'hF: 18/8 x 1/8

MFR_MTP_CTRL (1Dh)

Format: Unsigned binary

The MFR_MTP_CTRL command on Page 0 controls MTP operation and the LAST_FAULT_BLOCK (07h) function.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_MTP_ PASSWRD	If bit[15] = 0, or if 2Dh (on Page 3), bits[6:0] = bits[14:8] of this command, then the user can write to the special registers or store them to the MTP. Otherwise, the special registers (e.g. E0h~F6h on Page 1) and Page 3 registers cannot be written to the MTP.
7	R/W	MFR_CLR_MTP_ LST_FLT_EN	Enables the device to clear the last fault in the MTP after a CLEAR_LAST_FAULT (08h) command takes effect. 1'b0: Disabled 1'b1: Enabled

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6	R/W	MFR_LST_FLT_BLC_PWR_EN	Enables the device to block start-up if a protection occurred during the last operating cycle. 1'b0: Disabled 1'b1: Enabled
5	R/W	IGNORE_NO_VIN_TEMP_FAULT	Ignores V_{IN} or temperature-related faults during system start-up.
4	R/W	CLR_EEPROM_LAST_FAULT_EN	Enables the CLEAR_LAST_FAULT command (08h). 1'b0: Disabled 1'b1: Enabled
3	R/W	PROTECT_FAULT_RECORD_EN	Enables the device to record protection information to the MTP. 1'b0: Disabled 1'b1: Enabled. If a protection occurs, the VR records the protection information to the MTP automatically
2	R/W	MFR_TRIM_REG_STORE_EN	1'b1: Store trim registers, regardless of whether 1Dh, bit[15] and the password are wrong 1'b0: Disable storing some trim registers to the MTP if 1Dh, bit[15] = 1 and the password is wrong
1	R/W	MFR_MTP_COPY_EN	Enables reading (restoring) the MTP while outputting power. 1'b0: Disabled 1'b1: Enabled
0	R/W	MFR_CRC_PROTECT_EN	Enables cyclic redundancy check (CRC) protection. 1'b0: Disabled 1'b1: Enabled

MFR_PSYS_WARN_FILT_CNT (1Eh)

Format: Unsigned binary

The MFR_PSYS_WARN_FILT_CNT command on Page 0 sets the filter counter for PSYS_WARN1 and PSYS_WARN2.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
2:0	R/W	MFR_PSYS_WARN_FILT_CNT	Sets the filter time for PSYS_WARN2 and PSYS_WARN1. 0: Use the ordinary 2-level FF synchronization (the delay is 100ns to 200ns) Others: The positive edge delays will be (bits[2:1] of this command+ 1) x 100ns, and the negative edge delays are 100ns based on the 2-level FF synchronization

MFR_LOW_VOUT_TRIM (1Fh)

Format: Unsigned binary

This MFR_LOW_VOUT_TRIM command on Page 0 applies a fixed offset voltage to the V_{OUT} command value for different power states when V_{OUT} undergoes DVID to a lower value. Typically, this command is used by the end user to trim V_{OUT} when the PMBus device is assembled into the end user's system.

Bits	Access	Bit Name	Description
15:12	R/W	LOW_VOUT_TRIM_TH	Sets the level to apply LOW_VOUT_TRIM. If the V_{OUT} gain = 2:1, then 0.1V/LSB. If the V_{OUT} gain = 1:1, then 0.05V/LSB.
11:8	R/W	LOW_VOUT_TRIM_2_CCM	Applies a fixed offset voltage to V_{OUT} in multi-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.

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7:4	R/W	LOW_VOUT_TRIM_1_CCM	Applies a fixed offset voltage to V_{OUT} in 1-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
3:0	R/W	LOW_VOUT_TRIM_DCM	Applies a fixed offset voltage to V_{OUT} in 1-phase DCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 0 sets rail A's V_{OUT} when the PMBus controls the output.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_COMMAND	Sets the rail reference voltage (VID_DAC output voltage) in PMBus mode. In 5mV VID step mode: if RMS_GAIN = 2:1 (4Ah, bit[11] = 0), V_{REF} = (VID + 49) / 2 x 5mV if RMS_GAIN = 1:1 (4Ah, bit[11] = 1), V_{REF} = (VID + 49) / 2 x 10mV In 10mV VID step mode: V_{REF} = (VID + 19) / 2 x 10mV

MFR_VOUT_TRIM (22h)

Format: Unsigned binary

The MFR_VOUT_TRIM command on Page 0 applies a fixed offset voltage to the commanded V_{OUT} for different power states when V_{OUT} exceeds the value set by MFR_LOW_VOUT_TRIM (1Fh), bits[15:12]. Typically, this command is used by the end user to trim V_{OUT} when the PMBus device is assembled into the end user's system.

Bits	Access	Bit Name	Description
15:12	R/W	VOUT_TRIM_3_CCM	Applies a fixed offset voltage to V_{OUT} in ≥3-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
11:8	R/W	VOUT_TRIM_2_CCM	Applies a fixed offset voltage to V_{OUT} in 2-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
7:4	R/W	VOUT_TRIM_1_CCM	Applies a fixed offset voltage to V_{OUT} in 1-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
3:0	R/W	VOUT_TRIM_DCM	Applies a fixed offset voltage to V_{OUT} in 1-phase DCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.

VOUT_CAL_OFFSET (23h)

Format: Unsigned binary

The VOUT_CAL_OFFSET command on Page 0 offers an offset VID for the rail A target determined by VOUT_COMMAND (21h), VOUT_MARGIN_HIGH (25h), and VOUT_MARGIN_LOW (26h). This command is the initial value of the SVID offset.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

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7:0	R/W	VOUT_CAL_OFFSET	Sets the VID offset in PMBus mode. It is also the initial value for the SVID offset register (SVID 33h). 5mV/LSB or 10mV/LSB according to MFR_VR_CONFIG (39h), bit[7]. -80h ~ +7Fh.

MFR_VOUT_MAX (24h)

Format: Unsigned binary

The MFR_VOUT_MAX command on Page 0 sets the initial value of SVID VOUT_MAX (SVID 30h) for rail A, which sets an upper limit on the VID target (not including the offset) of SVID to prevent V_{OUT} from being set to a possibly dangerous level. If an attempt is made to set the VID target above MFR_VOUT_MAX, the command is rejected. The PMBus VID target is not constrained by MFR_VOUT_MAX.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_VOUT_MAX	Sets an upper limit on the rail A VID target (not including the offset) of SVID.

VOUT_MARGIN_HIGH (25h)

Format: Unsigned binary

The VOUT_MARGIN_HIGH command on Page 0 sets rail A's reference voltage (VID_DAC V_{OUT}) at the command margin high state.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_MARGIN_HIGH	Sets the reference voltage (VID_DAC V_{OUT}) at the command margin high state.

VOUT_MARGIN_LOW (26h)

Format: Unsigned binary

The VOUT_MARGIN_LOW command on Page 0 sets rail A's reference voltage (VID_DAC output voltage) at the command margin low state.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_MARGIN_LOW	Sets the reference voltage (VID_DAC V_{OUT}) at the command margin low state.

MFR_VBOOT (27h)

Format: Unsigned binary

The MFR_VBOOT command on Page 0 sets the boot-up voltage (V_{BOOT}) for rail A.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_VBOOT	Sets V_{BOOT} for rail A (following the VID table). For example, to set V_{BOOT} to 0.9V using the 5mV VID table, set these bits to 0x83h.

MFR_FS (28h)

Format: Unsigned binary

The MFR_FS command on Page 0 sets rail A's frequency.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	MFR_FS	Sets rail A's operating frequency. 50kHz/LSB.

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MFR_PHASE_NUM (29h)

Format: Unsigned binary

The MFR_PHASE_NUM command on Page 0 sets the phase number for rail A.

Bits	Access	Bit Name	Description
15:4	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
3:0	R/W	MFR_PHASE_NUM	Sets the phase number for rail A.

MFR_DBG_ADC_CHANNEL (2Ah)

Format: Unsigned binary

The MFR_DBG_ADC_CHANNEL command on Page 0 sets the ADC sample channel that must be observed.

Bits	Access	Bit Name	Description
15:5	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
4:0	R/W	MFR_DBG_ADC_ CHANNEL	5'd0: CHANL_VIN 5'd1: CHANL_I1 5'd2: CHANL_I2 5'd3: CHANL_I3 5'd4: CHANL_I4 5'd5: CHANL_I5 5'd6: CHANL_I6 5'd7: CHANL_I7 5'd8: CHANL_I8 5'd9: CHANL_I9 5'd10: CHANL_VFB_R1 5'd11: CHANL_VFB_R2 5'd12: CHANL_VOUT_R1 5'd13: CHANL_VOUT_R2 5'd14: CHANL_IMON_R1 5'd15: CHANL_IMON_R2 5'd16: CHANL_AUXIMON 5'd17: CHANL_ADDR_PL 5'd18: CHANL_PWR_IN 5'd19: CHANL_TEMP

MFR_CONFIG1 (2Bh)

Format: Unsigned binary

The MFR_CONFIG1 command on Page 0 sets some functions for rail A.

Bits	Access	Bit Name	Description
15	R/W	MFR_OFF_IMON_ BIAS_R1	1'b0: Enable the IMON bias current 1'b1: Disable the IMON bias current
14:13	R/W	MFR_CYC_MODE_ R1	Keep both of these bits set to 1.
12	R/W	MFR_ADAP_CLK_ EN_R1	Enables switching to low clock running in PS2/PS1 (if DLL is enabled off in PS2/PS1). 1'b1: Enabled 1'b0: Disabled
11	R/W	MFR_PS1_OFF_ DLL_EN_R1	Enables DLL to turn off in PS1. 1'b1: Enabled 1'b0: Disabled

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10	R/W	MFR_ECOV2_ DYNAMIC_FLT_OC_ R1	Enables the OC pre-phase signal to hold the current balance (CB) loop. This function must be enabled if the CB loop is enabled. 1'b0: Disabled 1'b1: Enabled
9:8	R/W	MFR_LL_MINUS_R1	Sets the fast slew rate function when receiving a SETVID_FAST command. Reduces I_{DROOP} when VID_Fast occurs at a large LL. I_{DROOP} gain-X cannot be set bellow 0. MFR_CONFIG3 (49h), bit[8] enables this function. 2'b00: I_{DROOP} gain (1Bh (on Page 0), bits[3:0]) - 4 2'b01: I_{DROOP} gain (1Bh (on Page 0), bits[3:0]) - 3 2'b10: I_{DROOP} gain (1Bh (on Page 0), bits[3:0]) - 2 2'b11: I_{DROOP} gain (1Bh (on Page 0), bits[3:0]) - 1
7	R/W	MFR_BLK_SET_EN_ R1	1'b0: Disables the shield PWM_SET signal when the slope saturates and enables the slope leakage reduction function 1'b1: Enables the shield PWM_SET signal when the slope saturates and enables the slope leakage reduction function
6:4	R/W	MFR_BLK_SET_ POS_RANGE_R1	Sets the shield time for PWM_SET after the slope saturates. The shield time can be calculated with the following equation: Shield time = MFR_BLK_SET_POS_RANGE_R1 x 20 + 10ns
3	R/W	MFR_BLK_SET_ PRE_RANGE_EN_ R1	1'b0: Disable the shield PWM_SET signal before the slope saturates 1'b1: Enable the shield PWM_SET signal before the slope saturates; the shield time can be set by bits[2:0] of this command
2:0	R/W	MFR_BLK_SET_ PRE_RANGE_R1	If bit[2] = 0, then bits[1:0] have the following options: 2'b00: 280ns 2'b01: 200ns 2'b10: 120ns 2'b11: 40ns If bit[2] = 1: then bits[1:0] have the following options: 2'b00: 140ns 2'b01: 100ns 2'b10: 60ns 2'b11: 20ns

MFR_IMON_SNS_OFFS (2Ch)

Format: Unsigned binary

The MFR_IMON_SNS_OFFS on Page 0 applies a constant offset on the IMONA ADC sample result due to a 5µA IMON bias current.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_IMON_SNS_ OFFS	The value should be -(5µA x R_{IMON} x 1023 / 1.6). Convert this value to a two's complement number.

MFR_ADC_HOLD_TIME (2Dh)

Format: Unsigned binary

The MFR_ADC_HOLD_TIME command on Page 0 holds the ADC trig for a certain time.

Bits	Access	Bit Name	Description
15:5	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
4:0	R/W	MFR_ADC_HOLD_ TIME	100ns/LSB.

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MFR_PLATFORM_TIME_SET (2Eh)

Format: Unsigned binary

The MFR_PLATFORM_TIME_SET command on Page 0 sets the rail A period after VID_PRES has added the rising step, and before VID_PRES starts to subtract the rising step. It also sets the time delay for one rail to exit PS4 while another rail is not in PS4.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:6	R/W	MFR_SGL_PS4_DLY	Sets the time delay when rail A exits PS4 while rail B is not in PS4. 1μs/LSB.
5:0	R/W	MFR_PLATFORM_TIME	Sets the VREF hold time from when VREF rises to the target VID plus an additional step x VID step, when DVID ramps up. 1μs/LSB.

MFR_DEBUG (2Fh)

Format: Unsigned binary

The MFR_DEBUG command on Page 0 configures some special functions for the MPQ29164.

Bits	Access	Bit Name	Description
15	R/W	MFR_PS2_OFF_DLLANA_EN	Enables the delay line loop (DLL) circuit when all rails are in PS2/3. 1'b1: Enabled 1'b0: Disabled
14	R/W	MFR_PS1_EXIT_TO_FULL_PHASE	Enables the device to run with full phase after detecting a high frequency (f_{SW_HIGH}) in PS1. If PS1 APS is not enabled, the controller enters 1-phase operation and f_{SW_HIGH} goes low. 1'b1: Enabled 1'b0: Disabled
13	R/W	MFR_PS2_OFF_PWM_FALL	Enables the PWM_FALL/PWM_SET signal in PS2/3. 1'b1: Enabled 1'b0: Disabled
12	R/W	MFR_FAST_CMPSET_SYNC	Enables the fast sync for the CMP_SET signal from the analog. 1'b1: Enabled. The sync delay is about 10ns 1'b0: Disabled. The sync delay is between 10ns and 20ns
11	R/W	PACKAGE_SEL	This bit is set to 0 by default.
10	R/W	FLT_SINGLE_CELL_WR_EN	Enables the device to write to a single cell for the fault address of the MTP. When enabled, this function will reduce the MTP lifetime. 1'b1: Enabled 1'b0: Disabled
9	R/W	MFR_STORE_SVID_CMD_EN	Enables the device to store the SVID CMD from 8'h80, 8'h81, and 8'h82. 8'h80: Receive the target address of SVID, bits[3:0] 8'h81: FLAG_XMT, FLAG_PARITY, PARITY, RECEIVE COMMAND, bits[4:0] 8'h82: Receive payload, bits[7:0] 1'b1: Enabled 1'b0: Disabled
8	R/W	MFR_DLL_EN	Enables the DLL function. 1'b1: Enabled 1'b0: Disabled
7	R/W	MFR_INPUT_DOMAIN_EN	Enables the P_{IN} domain (0Dh) for SVID. 1'b1: Enabled 1'b0: Disabled

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6	R/W	BG_CHOP	Used for debugging.
5	R/W	MFR_SDM_FRAC_EN	Enables the sigma-delta function for t_{ON}'s fraction bits. 1'b1: Enabled 1'b0: Disabled
4:0	R/W	MFR_TRI_STATE_DELAY	Sets the time delay from the PWM off state to PWM to Hi-Z. 10ns/LSB.

MFR_APSI_CTRL (30h)

Format: Unsigned binary

The MFR_APSI_CTRL command on Page 0 controls the automatic phase-shedding (APS) behaviors and t_{ON} extension for rail A.

Bits	Access	Bit Name	Description
15:13	R/W	MFR_PS23_TON_FACTOR	Sets the t_{ON} extended factor in PS2/PS3 (not in APS). 3'd0: 75% 3'd1: 100% 3'd2: 125% 3'd3: 150% 3'd4: 175% 3'd5: 200% 3'd6: 225% 3'd7: 250%
12:10	R/W	MFR_PS1_TON_FACTOR	Sets the t_{ON} extended factor in PS1 (not in APS). 3'd0: 75% 3'd1: 100% 3'd2: 125% 3'd3: 150% 3'd4: 175% 3'd5: 200% 3'd6: 225% 3'd7: 250%
9	R/W	MFR_ADP_PSI_BYPASS	Disables the SETPS command when APS is enabled. Active high.
8	R/W	MFR_ADP_OC_EXIT_EN	Enables the 1-phase CCM/DCM rail to exit to full-phase running when there is a per-phase over-current (OC) condition in APS mode. Active high.
7:5	R/W	PHASE_DROP_DELAY	Sets the delay time to drop phases after detecting that the total current is smaller than the phase-shedding threshold. About 120μs/LSB.
4	R/W	APS_VID_CHANGE	Holds APS for a set time after DVID.
3	R/W	LOAD_STEP_FSW_DET	Enables the VR to enter full-phase operation when f_{SW} is high during APS. 1'b0: Disabled 1'b1: Enabled
2:0	R/W	APS_DELAY_TIME	Sets the delay time to enable APS after high/low frequency detection or DVID.

MFR_FS_LOOP_CYC_RIPPLE_SET (31h)

Format: Unsigned binary

The MFR_FS_LOOP_CYC_RIPPLE_SET command on Page 0 sets rail A's ripple parameters for fast-V mode in SVID mode, as well as the frequency loop parameters.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

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8	R/W	MFR_CYC_RIPPLE_FILT	Enables the device to hold the phase current ripple when DVID or the cycle over-current protection (OCP) limit is updated. 1'b1: Enabled 1'b0: Disabled
7:6	R/W	MFR_CYC_RIPPLE_GAIN	Sets the ripple current gain, which can be used to reduce the cycle current limit. 2'b00: 0%. No ripple current offset 2'b01: 25% ripple current offset 2'b10: 50% ripple current offset 2'b11: 100% ripple current offset
5:3	R/W	MFR_FS_LOOP_CNT	Sets the delay time to hold the frequency loop. ADC sample period/LSB.
2:0	R/W	MFR_FS_LOOP_CTRL	Enables the device to hold the frequency loop when there are changes due to DVID, high or low frequencies (HF/LF), or the power state (PS). Bit[2]: DVID Bit[1]: PS changes Bit[0]: HF/LF detection

MFR_DC_CB_DYNC_SET (32h)

Format: Unsigned binary

The MFR_DC_CB_DYNC_SET command on Page 0 controls rail A's dynamic behavior for the DC loop and current balance loop.

Bits	Access	Bit Name	Description
15:13	R/W	MFR_PANR_RAND_BW	Selects a range of random numbers. It is valid when PANR is enabled (set via MFR_AUDIBLE_REDUCE (3Ah on Page 0), bit[8]) and the random delay is enabled (set via MFR_AUDIBLE_REDUCE (3Ah on Page 0), bit[9]). RAND_A = MFR_AUDIBLE_REDUCE (3Ah on Page 0), bits[15:10] RAND_C = MFR_VID_DOWN_DELAY (3Bh on Page 0), bits[15:0] RAND_x0 = {2'd0, MFR_TRANS_FAST (3Dh on Page 0), bits[13:0] RAND_DELAY = rem(RAND_A x RAND_x0 + RAND_C, 65536) Where rem is used to take the remainder, and USED_RAND_DELAY is the actual delay time for PANR. 3'b000: USED_RAND_DELAY = {10'd0, RAND_DELAY bits[5:0]} 3'b001: USED_RAND_DELAY = {8'd0, RAND_DELAY, bits[7:0]} 3'b010: USED_RAND_DELAY = {6'd0, RAND_DELAY, bits[9:0]} 3'b011: USED_RAND_DELAY = {4'd0, RAND_DELAY, bits[11:0]} 3'b100: USED_RAND_DELAY = {2'd0, RAND_DELAY, bits[13:0]} 3'b101: USED_RAND_DELAY = {4'd0, RAND_DELAY, bits[15:4]} 3'b110: USED_RAND_DELAY = {2'd0, RAND_DELAY, bits[15:2]} 3'b111: USED_RAND_DELAY = {RAND_DELAY, bits[15:0]}
12:10	R/W	MFR_DC_CAL_CNT	Sets the delay time to hold the DC loop. ADC sample period/LSB.
9	R/W	MFR_PFM_CTRL	Disables the low-frequency signal when the optimal t_{ON} is shorter than MIN_ON_TIME. Active low. 1'b1: Enabled 1'b0: Disabled
8:6	R/W	MFR_DC_CAL_CTRL	Enables the device to hold the DC loop when there are changes due to DVID, high or low frequencies (HF/LF), and the power state (PS). Bit[8]: DVID Bit[7]: PS changes Bit[6]: HF/LF detection

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5:3	R/W	MFR_CB_CAL_CTRL	Enables the device to hold the current balance loop when there are changes due to DVID, high or low frequencies (HF/LF), and the power state (PS). Bit[5]: DVID Bit[4]: PS changes Bit[3]: HF/LF detection
2:0	R/W	MFR_CB_CAL_CNT	Sets the delay time to hold the current balance loop. ADC sample period/LSB.

MFR_VOUT_CMPS_SET (33h)

Format: Unsigned binary

The MFR_VOUT_CMPS_SET command on Page 0 sets the V_{OUT} compensation behaviors for rail A.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_VOUT_CMPS_MAX	Sets the rails' maximum level for V_{OUT} compensation. 0.3125mV/LSB (if the VCOMP DAC reference is 320mV). LSB = VCOMP_DAC_REF / 256 / 4.
7:6	R/W	5MV_VO_COMP_STEP	Sets the V_{OUT} compensation COMP adding step by counting the PWM number during SETVID_FAST/SLOW. This value updates every (5MV_VO_COMP_STEP + 1) PWM1.
5	R/W	5MV_VO_COMP_STEP_EN	Enables the device to count PWM1 when adding V_{OUT} compensation. This bit is effective when bit[4] of this command is set to 1. 1b'0: Disabled 1b'1: Enabled
4	R/W	5MV_VO_COMP_EN	Enables the device to add a 5mV V_{OUT} compensation when the VR is in 5mV mode. 1b'0: Disabled 1b'1: Enabled
3:1	R/W	VCOMP_STEP_EXIT_DELAY	Sets the V_{OUT} compensation adding step by counting the PWM number after decay finishes. This value updates every bits[3:1] PWM1.
0	R/W	VCOMP_STEP_EXIT_DECAY_EN	Enables the VR to add V_{OUT} compensation to COMP by counting the PWM after decay finishes. Otherwise, V_{OUT} compensation is added once decay finishes. 1b'0: Add V_{OUT} compensation to COMP once 1b'1: Add V_{OUT} compensation to COMP by counting PWM

MFR_PROTECT_MODE (34h)

Format: Unsigned binary

The MFR_PROTECT_MODE command on Page 0 sets the over-temperature protection (OTP) and V_{IN} over-voltage protection (OVP) modes for all rails. It also sets rail A's modes for under-voltage protection (UVP), over-voltage protection (OVP1 and OVP2), and over-current protection (OCP).

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14	R/W	SS_OC_EN	Enables the phase over-current (OC) turn-off switch during soft start. 1'b0: Disabled 1'b1: Enabled
13	R/W	TEMP_FAULT_EN	Enables TEMP faults. 1'b0: Disabled 1'b1: Enabled
12	R/W	OT_FLAG_EN	Enables over-temperature protection (OTP). 1'b0: Disabled 1'b1: Enabled

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11	R/W	VIN_FLAG_EN	Enables V_{IN} under-voltage protection (UVP) and over-voltage protection (OVP). 1'b0: Disabled 1'b1: Enabled
10	R/W	OTP_LATCH	Sets the OTP mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
9	R/W	VIN_UVLO_LATCH	Sets the V_{IN} UVP mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
8	R/W	VIN_OVP_LATCH	Sets the V_{IN} OVP mode. 1'b0: Hiccup mode 1'b1: Latch-off mode
7:6	R/W	MFR_UVP_SET_MODE	Sets the rail A UVP mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times and then latch off
5:4	R/W	MFR_OVP2_SET_MODE	Sets the rail A OVP_VID mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times and then latch off
3:2	R/W	MFR_OVP1_SET_MODE	Sets the rail A OVP_VMAX mode. Bit[3]: Enables OVP1 Bit[2]: Sets the OVP1 mode, where 1 selects latch-off mode and 0 selects hiccup mode
1:0	R/W	MFR_OCP_SET_MODE	Sets the rail A OCP mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times and then latch off

VIN_ON (35h)

Format: Unsigned binary

The VIN_ON command on Page 0 sets the V_{IN} under-voltage lockout (UVLO) rising threshold.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VIN_ON	Sets the V_{IN} on threshold when V_{IN} is rising. 0.125V/LSB. For example, to set V_{IN} on at 5V, write 28h to bits[7:0] of this command.

VIN_OFF (36h)

Format: Unsigned binary

The VIN_OFF command on Page 0 sets the V_{IN} under-voltage lockout (UVLO) falling threshold.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VIN_OFF	Sets the V_{IN} off threshold when V_{IN} is falling. 0.125V/LSB. For example, to set V_{IN} off at 4V, write 20h to bits[7:0].

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MFR_VCAL_FS_PI (37h)

Format: Unsigned binary

The MFR_VCAL_FS_PI command on Page 0 sets the PI parameters for the rail A frequency loop and DC loop.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:6	R/W	MFR_FS_LOOP_PI	Sets the PI parameter for the frequency loop.
5:0	R/W	MFR_VCAL_PI	Sets the PI parameter for the DC loop.

IOUT_CAL_GAIN_SET (38h)

Format: Unsigned binary

The IOUT_CAL_GAIN_SET command on Page 0 sets rail A's PMBus I_{OUT} report gain.

Bits	Access	Bit Name	Description
15:10	R/W	IOUT_CAL_OFFSET	Sets the constant offset for the PMBus I_{OUT} report. 0.25A/LSB.
9:0	R/W	IOUT_CAL_GAIN	Sets the I_{OUT} report gain, calculated with the following equation: $IOUT_CAL_GAIN = I_{CCMAX} + 5\mu A / (G_{IMON} \times K_{CS})$ Where K_{CS} is the CS gain of the Intelli-Phase™ (in μA/A).

MFR_VR_CONFIG (39h)

Format: Unsigned binary

The MFR_VR_CONFIG command on Page 0 enables some rail A functions, such as DC loop calibration and APS.

Bits	Access	Bit Name	Description
15	R/W	IMVP9_SEL	Sets the two rails to IMVP8 or IMVP9. This only affects the VRRDY assignment. 1'b0: IMVP8 1'b1: IMVP9 and above
14	R/W	MFR_RAIL_EN	Enables rail A's power output. 1'b1: Enabled 1'b0: Disabled
13	R/W	MFR_CYC_OCP_FROM_FW	Determines whether the OCP_PHASE limit is selected by the register or SVID command. 1'b1: The OCP_PHASE limit is set by the register 1'b0: The OCP_PHASE limit is set by the SVID command
12	R/W	MFR_WAIT_SETTLE_SEL	Selects when rail A's VRRDY goes from low to high as DVID rises from 0V (not including VBOOT) if SVID 34h is written to 00. 1b'0: VRRDY turns high when DVID starts rising from 0V (not including V_{BOOT}) 1b'1: VRRDY turns high after DVID rises from 0V (not including V_{BOOT})
11	R/W	MFR_PMBUS_SR_SEL	Selects the VID slew rate for rail A when the PMBus controls V_{OUT}. 1b'0: V_{OUT} changes with a fast slew rate when the PMBus controls V_{OUT} 1b'1: V_{OUT} changes with a slow slew rate when the PMBus controls V_{OUT}
10	R/W	MFR_PMBUS_PS_EN	Enables the PMBus to control rail A's power state in PMBus mode. 1'b0: Disabled 1'b1: Enabled

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9:8	R/W	MFR_PMBUS_PS	Sets rail A's power state when the PMBus controls the power state. 2'b00: PS0 2'b01: PS1 2'b10: PS2 2'b11: PS3
7	R/W	MFR_VID_STEP_SEL	Selects rail A's VID step. 1'b1: 5mV/LSB 1'b0: 10mV/LSB
6	R/W	MFR_FS_LOOP_PS1_EN	Enables the frequency loop in PS1. This function is disabled if the extending t_{ON} function is enabled in PS1 (MFR_APSI_CTRL (30h), bits[12:10] are not set to 3'd1). For this bit to be enabled, disable PS1_CTRL_GTCLK_DIS_R1 (1Ah on Page 0), bit[10] = 1). 1'b1: Enabled 1'b0: Disabled
5	R/W	MFR_FS_LOOP_EN	Enables the frequency loop in PS0/PS1. 1'b1: Enabled 1'b0: Disabled
4	R/W	MFR_DC_LOOP_DCM_EN	Enables the DC loop in DCM. 1'b1: Enabled 1'b0: Disabled
3	R/W	MFR_DC_LOOP_EN	Enables the DC loop in PS0, PS1, PS2, and PS3. 1'b1: Enabled 1'b0: Disabled
2	R/W	MFR_IPHASE_BALANCE_EN	Enables the current balance loop in PS0. 1'b1: Enabled 1'b0: Disabled
1	R/W	MFR_APS_EN	Enables APS in PS0 and PS1 if MFR_PSI_ICC_CTRL (4Ah), bit[7] = 1. 1'b1: Enabled 1'b0: Disabled
0	R/W	MFR_PMBUS_MODE_SEL	Determines whether rail A is controlled by the PMBus or SVID. 1'b0: SVID control 1'b1: PMBus control

MFR_AUDIBLE_REDUCE (3Ah)

Format: Unsigned binary

The MFR_AUDIBLE_REDUCE command on Page 0 configures rail A's audible noise reduction parameters.

Bits	Access	Bit Name	Description
15:10	R/W	RAND_A	Sets the RAND_A parameter for the random number algorithm.
9:8	R/W	AUDIBLE_REDUCE_EN	Selects the mode for audible noise reduction. 2'bx0: Disable PANR 2'b01: Enable PANR and use a fixed delay time when the delayed DVID ramps down, as set by MFR_VID_DOWN_DELAY (3Bh), bits[15:0] 2'b11: Enable PANR and use the random delay time when the delayed DVID ramps down. The random delay time is set by MFR_DC_CB_DYNC_SET (32h), bits[15:13]
7:0	R/W	VID_TARGET_DELTA	Sets the VID delta threshold to delay dynamic VID. If VID_PRESENT - VID_TARGET > MFR_AUDIBLE_REDUCE, bits[7:0], then DVID is delayed for a duration.

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MFR_VID_DOWN_DELAY (3Bh)

Format: Unsigned binary

The MFR_VID_DOWN_DELAY command on Page 0 configures the delay time when the delayed DVID ramps down on rail A.

Bits	Access	Bit Name	Description
15:0	R/W	MFR_VID_DOWN_DELAY	1µs/LSB.

MFR_FILTER_SET (3Ch)

Format: Unsigned binary

The MFR_FILTER_SET command on Page 0 sets the parameters for the VID filter, as well as the slow slew rate for rail A.

Bits	Access	Bit Name	Description
15:12	R/W	MFR_FS_LOOP_HYS_ON_R1	10ns/LSB for the f_{SW} error. If the error exceeds MFR_FS_LOOP_HYS_ON_R1, the f_{SW} loop starts running.
11:9	R/W	MFR_FS_LOOP_HYS_OFF_R1	10ns/LSB for the f_{SW} error. If the error is below MFR_FS_LOOP_HYS_ON_R1, the f_{SW} loop is held.
8	R/W	MFR_FS_HYS_EN_R1	1’b1: Enable the hysteresis function
7	R/W	MFR_DAC_CMP_EN	Enables DAC_CMP_FILTER from the analog of rail A, which filters the VID_DAC output until the filtered VID_DAC output level equals the VID_DAC output when a DVID down command is interrupted by a DVID up command. For this bit to be effective, the DAC_CMP_EN bit must be set to 1’b1. 1’b0: Disabled 1’b1: Enabled
6	R/W	MFR_VID_FILTER_EN	Enables the VID filter for rail A, which is the VID_DAC output filter for SETVID_FAST/SLOW_DOWN transitions. There is no VID filter when VID goes up or VID goes down due to decay or a PS4 command. 1’b0: Disabled 1’b1: Enabled
5:4	R/W	MFR_VID_FILTER	Sets rail A’s VID_DAC output filter. 2’b00: 1µs added filter when VID ramps down or there is a steady VOUT 2’b01: 3µs added filter when VID ramps down or there is a steady VOUT 2’b10: 5µs added filter when VID ramps down or there is a steady VOUT 2’b11: 7µs added filter when VID ramps down or there is a steady VOUT
3:0	R/W	MFR_SLOW_SR_SEL	Selects the slew rate when rail A receives the SETVID_SLOW command. For this function, EN must be off. 4’b1xxx: 1/16 of the fast slew rate 4’b01xx: 1/8 of the fast slew rate 4’b001x: 1/4 of the fast slew rate 4’b0001: 1/2 of the fast slew rate

MFR_TRANS_FAST (3Dh)

Format: Unsigned binary

The MFR_TRANS_FAST command on Page 0 sets the reference fast slew rate when rail A receives the SETVID_FAST_UP command.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13:12	R/W	VID_STEP_DECAY	Sets the rail A reference minus the step during decay. The step = 2 x VID_STEP_DECAY + 1.

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11	R/W	VID_SUBTRACT	Selects the rail A slew rate when the reference removes the additional rising step. 1'b0: 1/4 of the fast slew rate 1'b1: 1/8 of the fast slew rate
10:8	R/W	VID_RISING_STEP	Sets the VID to rise one more step after VID reaches the target. This raises V_{OUT}. In 5mV mode, one more rising step = VID_RISING_STEP x 2 + 1. In 10mV mode, one more rising step = VID_RISING_STEP.
7:6	R/W	VID_STEP_NUM	Sets the rail A reference step in one VID_SR_CNT period when the slew rate rises. The step is equal to DEC(VID_STEP_NUM) + 1.
5:0	R/W	VID_SR_CNT	Sets the time length that V_{REF} changes once for rail A. 100ns/LSB.

MFR_EN_SEQUENCE_CFG (3Eh)

Format: Unsigned binary

The MFR_EN_SEQUENCE_CFG command on Page 0 sets the system behavior when EN changes.

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R/W	MTP_EN_LOW_LPM_EN	Enables low-power mode when EN de-asserts (pulls low). 1'b1: Enabled 1'b0: Disabled
11	R/W	MFR_EN_MTP_COPY	Enables copying to the MTP when EN is pulled up (if the PE pin is pulled high). 1'b1: Enabled 1'b0: Disabled
10:7	R/W	MFR_PRECHECK_TIME	Sets the time length for the synchronized EN pin to remain high for EN start-up or EN restart. 100μs/LSB. This is the first start-up delay.
6:0	R/W	MFR_EN_DLY	Sets the delay for rail A to wait for the output power after bits[10:7] of this command passes, and when there is no V_{IN} or temperature fault. 20μs/LSB. This is the second start-up delay, and it is also the delay for hiccup mode, retry mode, and for the PMBus turning off and then on.

MFR_ALT_SET (3Fh)

Format: Unsigned binary

The MFR_ALT_SET command on Page 0 sets rail A's alert timing.

Bits	Access	Bit Name	Description
15:13	R/W	ALERT_FIRST_STEP	Sets the number of VID changes when the first change for VID_ALERT. The first VID change is equal to the value set by these bits.
12:11	R/W	ALERT_STEP_NUM	Sets the number of VID changes when VID_ALERT changes once. The step is set to DEC(ALERT_STEP_NUM) + 1.
10:6	R/W	ALERT_DELAY_TIME	Sets the delay time to pull the VR_SETTLE signal high after the alert reference reaches the target VID. 100ns/LSB.
5:0	R/W	ALERT_SR_CNT	Sets the time length for the alert reference to change one step. 100ns/LSB.

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MFR_SW_LF_SET (40h)

Format: Unsigned binary

The MFR_SW_LF_SET command on Page 0 defines rail A's low PWM frequency threshold. If the time length between the adjacent PWMs of the same phase is longer than the length set by MFR_SW_LF_LIMIT, then f_{SW} is low.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:10	R/W	MFR_SW_LF_FILT	Filters the low-frequency signal. The signal asserts only when it has been trigged for (MFR_SW_LF_FILT) continuous times. If these bits are set to 0, the signal asserts when it has been triggered once.
9	R/W	MFR_SW_LF_EN	Enables the low-frequency detection function. 1'b1: Enabled 1'b0: Disabled
8:0	R/W	MFR_SW_LF_LIMIT	Sets the low-frequency detection threshold. 10ns/LSB.

MFR_SW_HF_SET (41h)

Format: Unsigned binary

The MFR_SW_HF_SET command on Page 0 defines rail A's high-frequency detection threshold. If the PWM1 period is shorter than the low-level frequency, then f_{SW} is high.

Bits	Access	Bit Name	Description
15:11	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
10:9	R/W	MFR_SW_HF_FILT	Filters the high-frequency signal. The signal only asserts when it has been triggered for (MFR_SW_HF_FILT) continuous times. If these bits are set to 0, the signal asserts when it has been triggered once.
8	R/W	MFR_SW_HF_EN	Enables the high-frequency detection function. 1'b1: Enabled 1'b0: Disabled
7:0	R/W	MFR_SW_HF_LIMIT	Sets the high-frequency detection threshold. 10ns/LSB.

MFR_TON_ADJ_PS1_SW_LF_TH (42h)

Format: Unsigned binary

The MFR_TON_ADJ_PS1_SW_LF_TH command on Page 0 sets rail A's low-frequency threshold when the t_{ON} extend function is enabled in PS1.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_TON_ADJ_PS1_SW_LF_TH	10ns/LSB.

MFR_PS2_OFFSLOPE_TON_TH (43h)

Format: Unsigned binary

The MFR_PS2_OFFSLOPE_TON_TH command on Page 0 sets rail A's t_{ON} threshold width when the slope compensation function in PS2/PS3 is disabled (t_{ON} exceeds the threshold).

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	MFR_PS2_OFFSLOPE_TON_TH	10ns/LSB.

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MFR_TON_ADJ_PS1_SW_HF_TH (44h)

Format: Unsigned binary

The MFR_TON_ADJ_PS1_SW_HF_TH command on Page 0 sets rail A's high-frequency threshold when the t_{ON} extend function is enabled in PS1.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_TON_ADJ_PS1_SW_HF_TH	10ns/LSB.

MFR_TON_ADJ_PS2_SW_HF_TH (45h)

Format: Unsigned binary

The MFR_TON_ADJ_PS2_SW_HF_TH command on Page 0 sets rail A's high-frequency threshold when the t_{ON} extend function is enabled in PS2/PS3.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_TON_ADJ_PS2_SW_HF_TH	10ns/LSB.

MFR_SLOPE_CNT_SETPS1 (46h)

Format: Unsigned binary

The MFR_SLOPE_CNT_SETPS1 command on Page 0 sets the saturation value for slope ramp compensation during 1-phase operation on rail A.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	MFR_SLOPE_CNT_SETPS1	Sets the slope compensation saturation time for 1-phase CCM. Typically, this time is set at 1.3 x (t_S - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_SETPS1 (47h)

Format: Unsigned binary

The MFR_SLOPE_SR_SETPS1 command on Page 0 sets the slope ramp compensation slew rate during 1-phase operation on rail A.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_SETPS1	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_1P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_SETPS1	Sets the current source for slope voltage generation. 0.25μA/LSB.

MFR_CONFIG2 (48h)

Format: Unsigned binary

The MFR_CONFIG2 command on Page 0 sets some functions for rail A.

Bits	Access	Bit Name	Description
15	R/W	MFR_VID_RISE_SATUR_CASE_DIS	1'b0: Sets RISING_STEP to 0 if VID reaches the limit
14	R/W	MFR_I2C_TIMEOUT_DIS	1'b1: Disable PMBus-SCL line low-level detection
13	R/W	VIN_FIL_EN	1'b1: Enable the analog filter for the V_{IN} sense

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12	R/W	MFR_VIN_SNS_ FILT_EN	1’b1: Enables the digital RC filter for the V_{IN} sense
11:10	R/W	MFR_VIN_SNS_ FILT_PARA	Sets the V_{IN} sense digital RC filter. 2’b00: 60µs RC filter 2’b01: 450µs RC filter 2’b10: 1890µs RC filter 2’b11: 7650µs RC filter
9	R/W	MFR_PANR_SLOW_ SLEWRATE_EN_R1	1’b1: The PANR slow down slew rate is 1/8 of the slow slew rate
8:6	R/W	MFR_RISE_STEP_ FOR_FAST_R1	Sets the number of additional rising steps for rail A after the VID reaches the target. This raises V_{OUT} with a fast slew rate. Rising step in 5mV mode = MFR_RISE_STEP_FOR_FAST_R1 x 2 + 1. Rising step in 10mV mode = MFR_RISE_STEP_FOR_FAST_R1.
5	R/W	MFR_SETPS1_ PHASE2_EN_R1	1’b0: Disable 2-phase running in PS1 1’b1: Enable 2-phase running in PS1
4	R/W	MFR_PANR_DECAY_ DELAY_EN	1’b0: Disable the PANR delay with a decay command 1’b1: Enable the PANR delay with a decay command
3	R/W	MFR_PANR_DECAY_ MODE_EN	1’b0: Disable decay behavior in PANR mode 1’b1: Enable decay behavior in PANR mode
2	R/W	MFR_ADDPS_ HIZ2HIGH_EN	1’b1: Enable the Hi-Z to high function when adding phases 1’b0: Disable the Hi-Z to high function when adding phases
1	R/W	MFR_ECOV2_CYC_ STATUS_POS_MODE	1’b1: SVID-0x11h, bit[2] asserts only at the rising edge of CYC mode 1’b0: SVID-0x11h, bit[2] asserts if CYC mode is maintained
0	R/W	MFR_PS4_MTP_ OPR_EN	1’b0: Disable MTP commands in PS4 1’b1: Enable MTP commands in PS4

MFR_CONFIG3 (49h)

Format: Unsigned binary

The MFR_CONFIG3 command on Page 0 sets certain functions.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Reserved. Set to 1 by default.
14	R/W	RESERVED	Reserved. Set to 1 by default.
13	R/W	RESERVED	Reserved. Set to 0 by default.
12	R/W	RESERVED	Reserved. Set to 1 by default.
11	R/W	RESERVED	Reserved. Set to 0 by default.
10:9	R/W	MFR_CYC_ NORMAL_FILT_ CNT	Sets the cycle-by-cycle current limit de-bounce time. If the number of normally generated PWM1 pulse exceeds 2 x MFR_CYC_NORMAL_FILT_CNT +1, then exit CYC limit mode.
8	R/W	MFR_LL_MINUS_ EN_R1	1’b0: Disables LL_MINUS (a function that can decrease LL) when receiving a SETVID_FAST command 1’b1: Enables LL_MINUS when receiving a SETVID_FAST command
7	R/W	MFR_PSCHG_ COMP_EN_R1	1’b0: Disables adding a COMP voltage when the PS changes 1’b1: Enables adding a COMP voltage when the PS changes
6:4	R/W	MFR_PSCHG_ COMP_R1	Adds a COMP voltage when changing the PS. 2.5mV/LSB (10mV / 4).
3:2	R/W	RESERVED	Reserved.

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1:0	R/W	MFR_FAST_SR_ VID_CHG_R1	Sets the hysteresis to enable the fast slew rate function when SETVID_FAST has been received and VID exceeds the set limit. This only affects one more step and LL_MINUS. In 5mV steps: 80mV/LSB, with a maximum of 240mV. In 10mV steps: 160mV/LSB, with a maximum of 480mV.

MFR_PSI_ICC_CTRL (4Ah)

Format: Unsigned binary

The MFR_PSI_ICC_CTRL command on Page 0 sets power-saving behaviors (among others) for rail A.

Bits	Access	Bit Name	Description
15	R/W	MFR_DIS_LOOP_ RST_TON	Resets the t_{ON} width when the frequency loop and current balance loop are held or disabled. This disables the sigma-delta function. 1'b1: Enabled 1'b0: Disabled
14	R/W	MFR_VID_TAB_SEL_ FLY	Enables on-the-fly (online) changes to VID_STEP. 1'b1: Enabled 1'b0: Disabled
13	R/W	MFR_VID_TAB_SEL_ MODE	Determines whether VID_STEP is selected by VID_STEP from the VID_STRAP pin or MFR_VR_CONFIG (39h), bits[7]. 1'b1: VID_STEP is set by the VID_STRAP pin (pull this pin high in 5mV mode; pull it low in 10mV mode) 1'b0: VID_STEP is set by the register
12	R/W	MFR_SVID_ DETECTION_EN	Enables the SVID detection function. 1'b1: Enabled 1'b0: Disabled
11	R/W	MFR_RMS_GAIN1_ EN	Sets the remote-sense gain. 1'b1: The gain is 1:1. Choose this gain when VID_STEP = 1 (5mV step) 1'b0: The gain is 2:1
10	R/W	MFR_SETPS_POS_ FILT_FSW	Shields the frequency detection function for about 3 PWM pulses after receiving a SETPS command. 1'b1: Enabled 1'b0: Disabled
9	R/W	MFR_TON_ADJ_ OFF_FSW	Shields the frequency detection function when t_{ON} is extended or reduced. (MFR_APSI_CTRL (30h), bits[15:10] do not equal 6'b001_001). 1'b1: Enabled 1'b0: Disabled
8	R/W	MFR_CYC_OCP_ EN_FILT	Enables the filter for the cycle-by-cycle current limit (CYCLE_OCP) function by 3µs. If the CYCLE_OCP limit has a delay on OCP-DAC, then the CYC_OCP enable signal comes first and causes a false CYCLE_OCP. 1'b1: Enabled 1'b0: Disabled
7	R/W	MFR_APS_PS1_EN	Enables APS in PS1. Only valid when MFR_VR_CONFIG (39h), bit[1] = 1. For this function to be effective, enable MFR_GATECLK_DIS (1Ah), bits[11:10]. 1'b1: Enabled 1'b0: Disabled
6	R/W	MFR_PS2_OFF_ IMON_BIAS	Enables the device to turn off the IMON bias current (5µA) in PS2 and PS3. 1'b1: Enabled 1'b0: Disabled

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5	R/W	MFR_PS2_OFF_SLOPE	Enables the device to turn off the slope compensation function in PS2 and PS3. Only valid when t_{ON} exceeds the value in MFR_PS2_OFFSLOPE_TON_TH (43h), bits[6:0]. 1'b1: Enabled 1'b0: Disabled
4	R/W	MFR_OCP_CMP_EN_FILT	Enables the device to filter the over-current protection (OCP) signal by 60µs when enabling the OCP comparator circuit when the circuit has been turned off. 1'b1: Enabled 1'b0: Disabled
3	R/W	MFR_PS1_2_OFF_OCP_CMP	Enables the device to turn off the CS comparator and CS buffer while in PS1, PS2, or PS3. 1'b1: Enabled 1'b0: Disabled
2	R/W	MFR_PS2_OFF_DLL	Enables the device to turn off the delay line loop (DLL) function in PS2 and PS3. The DLL clock is only off when all rails have turned off the DLL function. 1'b1: Enabled 1'b0: Disabled
1	R/W	MFR_PS1_STB_LOW_EN	Enables the device to pull the STBA pin low in PS1 to save power if the Intelli-Phase™ supports this mode. 1'b1: Enabled 1'b0: Disabled
0	R/W	MFR_PS2_STB_LOW_EN	Enables the device to pull the STBA pin low in PS2 and PS3 to save power if the Intelli-Phase™ supports this mode. 1'b1: Enabled 1'b0: Disabled

MFR_APS_PHASE_HYS (4Bh)

Format: Unsigned binary

The MFR_APS_PHASE_HYS command on Page 0 sets rail A's hysteresis during APS, as well as the thresholds for DCM and 1-phase CCM.

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
12:9	R/W	MFR_0PHL	Sets the threshold to go into DCM from 1-phase CCM. 1A/LSB.
8:4	R/W	MFR_1PHL	Sets the threshold to go to 1-phase CCM from 2-phase CCM. 1A/LSB.
3:0	R/W	MFR_PHASE_HYS	Sets the current hysteresis for different phases. 1A/LSB.

MFR_VOUT_MAX_9BIT (4Ch)

Format: Unsigned binary

The MFR_VOUT_MAX_9BIT command on Page 0 sets rail A's upper limit for VID + OFFSET. In PMBus mode, if VID + OFFSET exceeds this limit, then the command is acknowledged and the output is clamped at this limit. In SVID mode, if VID + OFFSET exceeds this limit, then this command is rejected and the output remains at the voltage that was set before this command.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	MFR_VOUT_MAX_9BIT	Sets rail A's upper limit for VID + OFFSET.

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MFR_SLOPE_CNT_DCM_SET (4Dh)

Format: Unsigned binary

The MFR_SLOPE_CNT_DCM_SET command on Page 0 sets rail A's slope discharge time and slope compensation saturation value in DCM.

Bits	Access	Bit Name	Description
15	R/W	MFR_SLOPE_ LEAKAGE	Enables the device to turn off the switch in the slope charging loop when the slope is saturated in PS2. 1'b0: Disabled 1'b1: Enabled
14:12	R/W	SLOPE_ DISCHARGE_TIME	Sets the slope discharge time. 10ns/LSB. The discharge time can be calculated with the following equation: Slope Discharge Time = (SLOPE_DISCHARGE_TIME + 1) x 10
11:9	R/W	MFR_OFFSLOPE_ TRIM	Sets V_{COMP} when the slope compensation function is off in PS2 or PS3. It is recommended to make this value 0, but it may need to be trimmed in actual applications. The LSB can be calculated with the following equation: LSB = VCOMP_DAC x 8 / 256 / 4 (V/LSB)
8:0	R/W	MFR_SLOPE_CNT_ DCM	Sets the slope compensation saturation time for 1-phase DCM. Typically, this time is set at 2 x (t_S - t_{BLANK}), where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_DCM (4Eh)

Format: Unsigned binary

The MFR_SLOPE_SR_DCM command on Page 0 sets the VR slope compensation slew rate for rail A in 1-phase DCM.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_ DCM	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_DCM)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_ DCM	Sets the current source for slope voltage generation. 0.25μA/LSB.

MFR_SHUTDOWN_LEVEL (4Fh)

Format: Unsigned binary

The MFR_SHUTDOWN_LEVEL command on Page 0 sets rail A's shutdown level. When V_{REF} is below this level while slewing downward, the VR stops switching and starts to decay. This command also sets the rail A slew rate, alert time, and bit[0] of STATUS1 when SVID sends VID within ±2LSB in 5mV mode.

Bits	Access	Bit Name	Description
15:14	R/W	MFR_IMMED_REF_ STEP	Sets the VID (output reference) step when SVID sends VID within ±2LSB in 5mV mode on rail A.
13:11	R/W	MFR_IMMED_ALT_ TIME	Sets the time length for ALERT signal on the SVID line to slew one step (MFR_ALT_SET (3Fh), bits[12:11] + 1) when SVID sends VID within ±2LSB in 5mV mode on rail A. 100ns/LSB.
10:8	R/W	MFR_IMMED_REF_ TIME	Sets the time length for VID to slew one step (bits[15:14] of this command) when the SVID sends VID within ±2LSB in rail A's 5mV mode. 100ns/LSB.
7	R/W	MFR_IMMEDIATE_ SVID_EN	Enables rail A to force the STATUS1, bit[0] to 1'b1. 1'b0: Disabled. STATUS1, bit[0] remains at 1'b0 until it settles normally 1'b1: Enabled. Forces STATUS1, bit[0] to 1'b1 when the SETVID command is received within ±2LSB

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6	R/W	MFR_IMMEDIATE_REF_EN	Enables rail A using bits[15:8] of this command. 1'b0: Disabled 1'b1: Enabled
5:0	R/W	MFR_SHUTDOWN_LEVEL	This value should exceed one VID step to prevent under-voltage protection (UVP) from accidentally being triggered. 5mV/LSB (in 5mV mode). 10mV/LSB (in 10mV mode).

MFR_SYS_PASSWORD (50h)

Format: Unsigned binary

The MFR_SYS_PASSWORD command on Page 0 stores the system password. This register can be stored in the MTP.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_SYS_PASSWORD	Stores the system password.

MFR_INPUT_PASSWORD (51h)

Format: Unsigned binary

The MFR_INPUT_PASSWORD command on Page 0 is used as an input port. This register cannot be stored in the MTP. Other registers can only be changed through the PMBus if MFR_SYS_PASSWORD (50h), bits[7:0] = MFR_INPUT_PASSWORD (51h), bits[7:0].

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_INPUT_PASSWORD	Inputs the system password.

MFR_ADDR_SVID_CTRL (52h)

Format: Unsigned binary

The MFR_ADDR_SVID_CTRL command on Page 0 sets rail A's SVID address.

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
5:4	R/W	MFR_SVID_ALLCALL_CTRL	Sets the all call address. 2'b 00: No all address 2'b 01: Sets 0Eh to be the all call address 2'b 10: Sets 0Fh to be the all call address 2'b 11: Sets both 0Eh and 0Fh to be all call addresses
3:0	R/W	MFR_ADDR_SVID	Sets the SVID address for rail A. 4'b 0000: The rail A address is 00h 4'b 0001: The rail A address is 01h 4'b 0010: The rail A address is 10h 4'b 0011: The rail A address is 11h

MFR_ICC_MAX_SET (53h)

Format: Unsigned binary

The MFR_ICC_MAX_SET command on Page 0 sets rail A's I_{CCMAX}.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

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9:8	R/W	MFR_ICC_MAX_ HIGH_EXPO	Sets the high exponent for MFR_ICC_MAX. I_{CCMAX} can be calculated with the following equation: I_{CCMAX} = MFR_ICC_MAX x $2^{MFR_ICC_MAX_HIGH_EXPO}$
7:0	R/W	MFR_ICC_MAX	1A/LSB. If MFR_ICC_MAX = 0, the rail does not start up.

MFR_CYC_OCP_FACTOR (54h)

Format: Unsigned binary

The MFR_CYC_OCP_FACTOR command on Page 0 sets the gain and offset for the cycle-by-cycle current limit (CYCLE_OCP) on rail A. The CYCLE_OCP limit is equal to 1.28V + [(CYCLE_OCP_LIMIT / PHASE_NUM - RIPPLE_CURRENT) x MFR_CYC_OCP_GAIN + MFR_CYC_OCP_OFFSET x 0.01V].

Bits	Access	Bit Name	Description
15:9	R/W	MFR_CYC_OCP_ OFFSET	Sets a constant offset for the CYCLE_OCP limit. 10mV/LSB. The default value should be (1.23V - 1.28V) / 0.01V = -5.
8:0	R/W	MFR_CYC_OCP_ GAIN	Sets the gain for the CYCLE_OCP limit. The gain can be calculated with the following equation: Gain = 12800 x R_{CS} x K_{CS} Where K_{CS} is the current-sense gain of the Intelli-Phase™ (in A/A), and R_{CS} is the sample current-sense resistor (in Ω). For example, if K_{CS} = 10μA/A and R_{CS} = 1500Ω, then the ideal gain should be 192.

MFR_PWR_INDUCTOR_GAIN (55h)

Format: Unsigned binary

The MFR_PWR_INDUCTOR_GAIN command on Page 0 sets rail A's ripple current gain, which corresponds to the value of the power inductor.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_PWR_ INDUCTOR_GAIN	Sets the ripple current gain, which can be calculated with the following equation: Gain = 2^{15} / 5 / L Where L is the inductance (in nH). For example, if the inductor is 150nH, then the ideal gain should be 0x2C.

MFR_OCP_OVP_DAC_LIMIT (60h)

Format: Unsigned binary

The MFR_OCP_OVP_DAC_LIMIT command on Page 0 set the DAC limit for over-current protection (OCP) and over-voltage protection (OVP) on rail A.

Bits	Access	Bit Name	Description
15:8	R/W	OCP_DA_LIMIT	Sets the per-phase OCP limit, calculated with the following equation: OCP_DA_LIMIT = per-Phase_OC_Value x (K_{CS} x R_{CS}) x 100 - 5 For example, if R_{CS} = 1kΩ and K_{CS} = 10μA/A, set the per-phase OCP value to 40A, which means that OCP_DA_LIMIT = 35 (0x23h).
7:0	R/W	OVP_DA_LIMIT	Sets the VR threshold for the V_{OUT} limit. Once V_{OUT} exceeds this level, the VR initiates a protection. 10mV/LSB.

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MFR_OVP_UVP_SET (61h)

Format: Unsigned binary

The MFR_OVP_UVP_SET command on Page 0 sets rail A's threshold for under-voltage protection (UVP), as well as the delay time for UVP and over-voltage protection (OVP).

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R/W	UVP_SEL	Sets the UVP threshold. 1'b1: V_{REF} - 150mV 1'b0: V_{REF} - 300mV
11:6	R/W	OVP_DELAY_TIME	Sets the OVP2 delay time for rail A. 200ns/LSB.
5:0	R/W	UVP_DELAY_TIME	Sets the UVP delay time for rail A. 20μs/LSB.

MFR_OCP_SET (62h)

Format: Unsigned binary

The MFR_OCP_SET command on Page 0 sets the rail A IMON over-current protection (OCP) threshold and delay time.

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
12:7	R/W	MFR_OCP_SET_ DELAYTIME	Sets the average OCP delay time for rail A. 20μs/LSB.
6:0	R/W	MFR_OCP_SET_ LEVEL	Sets rail A's over-current (OC) limit value (1A/LSB). The total OCP limit is set by MFR_OCP_SET_LEVEL multiplied by the phase number, which is compared to the value set by READ_IOUT (8Ch) / 4.

READ_VFB_SENSE (70h)

Format: Unsigned binary

The READ_VFB_SENSE command on Page 0 returns the sensed V_{FBA} voltage.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VFB_SENSE	1.5625mV/LSB.

READ_AD_RESULT (71h)

Format: Unsigned binary

The READ_AD_RESULT command on Page 0 returns the ADC result of the channels set by MFR_DBG_ADC_CHANNEL (2Ah).

Bits	Access	Bit Name	Description
15	R	ADC_AVG_TRIM_ RDY	Returns the flag that finishes the 64-average filter of the ADC sample result.
14:0	R	READ_AD_RESULT	Returns the half of the summed value of the 64-average filter ADC sample result. This value is equal to 64 x ADC_RESULT / 2.

SVID_REG_80H_81H (72h)

Format: Unsigned binary

The SVID_REG_80H_81H command on Page 0 stores part of the SVID command (not including GETREG 80h/81h/82h), which is stored in SVID addresses 80h and 81h.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.

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11:0	R	SVID_REG_80H_81H	Bits[11:8]: Store the address of the received SVID command. Bit[7]: Stores the frame error flag. Bit[6]: Stores the parity error flag. Bit[5]: Stores the parity in the command. Bits[4:0]: Store the 5-bit CMD in the SVID command.

SYS_STATE_AND_SVID_REG_82H (73h)

Format: Unsigned binary

The SYS_STATE_AND_SVID_REG_82H command on Page 0 stores the calculation state, chip state, and part of the SVID command (not including GETREG 80h/81h/82h, which is stored in the SVID addresses 82h).

Bits	Access	Bit Name	Description
15:12	R	CALCU_PRES_ STATE	Returns the state of the calculation module.
11:8	R	CHIP_PRES_STATE	Returns the state of the chip's CTRL module.
7:0	R	SVID_REG_82H	Stores the received SVID command payload.

MFR_SLAVE_ADDR (74h)

Format: Unsigned binary

The MFR_SLAVE_ADDR command on Page 0 stores the chip address.

Bits	Access	Bit Name	Description
15:7	R	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R	MFR_SLAVE_ADDR	Stores the final target address of the PMBus.

READ_RAIL_STATE (75h)

Format: Unsigned binary

The READ_RAIL_STATE command on Page 0 stores other rail A states.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R	SYS_CTRL_PRES_ STATE	Stores the SYS_CTRL state for rail A.
5:3	R	TON_CALC_PRES_ STATE	Stores the t_{ON} calculated state for rail A.
2:0	R	REF_OUT_PRES_ STATE	Stores the state of the VID reference generation module for rail A.

READ_VCOMP (76h)

Format: Unsigned binary

The READ_VCOMP command on Page 0 stores the DC compensation value for rail A.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	READ_VCOMP	0.3125mV/LSB.

CHECK_SUM_USER (77h)

Format: Unsigned binary

The CHECK_SUM_USER command on Page 0 stores the CHECK_SUM result of the user codes.

Bits	Access	Bit Name	Description
15:0	R	CHECK_SUM_USER	Stores the CHECK_SUM result of the user codes.

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STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 0 stores rail A's status with 1 byte.

Bits	Access	Bit Name	Description
7	R	MASTER_OR_SLAVE	Indicates the PMBus MASTER_SLAVE_SIG flag. 1b'0: Target mode. The controller acknowledges valid PMBus commands 1b'1: Initiator mode. The controller does not acknowledge any command
6	R	OFF	Indicates the power off flag, when V_{OUT} = 0V.
5	R	VOUT_OV_FAULT	Records the over-voltage protection (OVP) fault.
4	R	IOUT_OC_FAULT	Records the over-current protection (OCP) fault.
3	R	VIN_UV_FAULT	Records the V_{IN} under-voltage lockout (UVLO) fault.
2	R	TEMPERATURE	Records the over-temperature protection (OTP) fault.
1	R	CML	Records the communication error fault.
0	R	VOUT_MAX_ WARNING	Records the V_{OUT} max warning flag.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 0 stores rail A's status with 2 bytes.

Bits	Access	Bit Name	Description
15	R	OVP_OR_UVP	Indicates the over-voltage protection (OVP) or under-voltage protection (UVP) flag.
14	R	OCP_OR_CS_OCP_ OR_UVP	Indicates the over-current protection (OCP) or phase OCP and UVP flag.
13:12	R	RESERVED	Reserved. Set to 2'd0 by default.
11	R	VR_SETTLE	Indicates the VR_SETTLE flag.
10:8	R	RESERVED	Reserved. Set to 3'd0 by default.
7	R	MASTER_OR_SLAVE	Indicates the PMBus MASTER_SLAVE_SIG flag. 1b'0: Target mode. The controller acknowledges valid PMBus commands 1b'1: Initiator mode. The controller does not acknowledge any command
6	R	OFF	Indicates the power off flag, when V_{OUT} = 0V.
5	R	VOUT_OV_FAULT	Records the over-voltage protection (OVP) fault.
4	R	IOUT_OC_FAULT	Records the over-current protection (OCP) fault.
3	R	VIN_UV_FAULT	Records the V_{IN} under-voltage lockout (UVLO) fault.
2	R	TEMPERATURE	Records the over-temperature protection (OTP) fault.
1	R	CML	Records the communication error fault.
0	R	VOUT_MAX_ WARNING	Records the V_{OUT} max warning flag.

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 0 stores rail A's V_{OUT} status.

Bits	Access	Bit Name	Description
7	R	STATUS_OVP	Indicates the over-voltage protection (OVP) flag status.
6	R	STATUS_OV_FLAG	Indicates the over-voltage (OV) comparator flag status.

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5	R	STATUS_UV	Indicates the under-voltage (UV) comparator flag status.
4	R	STATUS_UVP	Indicates the under-voltage protection (UVP) flag status.
3	R	STATUS_VMAX_WARN	Indicates the VOUT_MAX warning flag status.
2:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 0 stores rail A's I_{OUT} status.

Bits	Access	Bit Name	Description
7	R	STATUS_OCP	Indicates the over-current protection (OCP) flag status.
6	R	STATUS_OC_UVP	Indicates the per-phase OCP and under-voltage protection (UVP) flag status.
5	R	STATUS_OC_LIMIT	Indicates the IMON OCP or the per-phase OCP trig flag status.
4:0	R	RESERVED	Reserved.

STATUS_INPUT (7Ch)

Format: Unsigned binary

The STATUS_INPUT command on Page 0 stores rail A's input status.

Bits	Access	Bit Name	Description
7	R	STATUS_VIN_OVP	Indicates the V_{IN} over-voltage protection (OVP) flag status.
6	R	RESERVED	Reserved.
5	R	STATUS_VIN_UVLO	Indicates the V_{IN} under-voltage lockout (UVLO) flag status.
4:0	R	RESERVED	Reserved.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 0 stores rail A's temperature status.

Bits	Access	Bit Name	Description
7	R	STATUS_OTP	Indicates the over-temperature protection (OTP) flag status.
6	R	STATUS_OT_MFLT	Indicates the OTP trigger and Intelli-Phase™ fault flag status.
5:0	R	RESERVED	Reserved.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command on Page 0 stores the communication status.

Bits	Access	Bit Name	Description
15:8	R	ECED_EVENT_CNT	Stores the ECED occurrence counter.
7	R	CML_INVALID_CMD	Indicates the status of the unsupported PMBus command flag.
6	R	CML_INVALID_DATA	Indicates the status of the communication error while transmitting a data flag.
5	R	PMBUS_PEC_ERROR	Indicates the status of the PEC error during PMBus communication flag.
4	R	MTP_CRC_ERROR	Indicates the status of the CRC error during an MTP communication flag.
3	R	MTP_WRFAIL_FLAG	Indicates the status of WRFAIL during an MTP communication flag.
2	R	MTP_ECED_FLAG	Indicates the status of ECED during an MTP communication flag.

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1	R	CML_OTHER_FAULT	Indicates the status if an unexpected start/stop is triggered during a PMBus communication flag.
0	R	MTP_SIGNATURE_ FAULT	Indicates the flag of a signature fault, which indicates whether the data in {000h, 001h} of the MTP is 16'h1234.

READ_VREF_PS (80h)

Format: Unsigned binary

The READ_VREF_PS command on Page 0 stores rail A's PS state and VID reference.

Bits	Access	Bit Name	Description
15:13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R	VID_STEP_SEL_ FINAL	Indicates the value of internal VID_STEP for rail A (5mV/10mV, considering the VID_STRAP pin and the register setting). 1'b1: 5mV 1'b0: 10mV
11:9	R	PS_STATE	Stores rail A's power stage. 3'b1xx:PS4 3'b011: PS3 3'b010: PS2 3'b001: PS1 3'b000: PS0
8:0	R	SVID_VREF	Stores the VID reference for rail A.

READ_VIN (88h)

Format: Unsigned binary

The READ_VIN command on Page 0 stores the V_{IN} report.

Bits	Access	Bit Name	Description
15:11	R	VIN_EXPO	Fixed to 11101 (bin) = -3 (dec).
10:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	READ_VIN	Monitors V_{IN}. 0.125V/LSB.

READ_VOUT (8Bh)

Format: Unsigned binary

The READ_VOUT command on Page 0 stores rail A's V_{OUT} report.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VOUT	If VID_STEP = 10mV, 3.125mV/LSB. If VID_STEP = 5mV and the remote-sense gain = 2:1, then 3.125mV/LSB. If VID_STEP = 5mV and the remote-sense gain = 1:1, then 1.5625mV/LSB.

READ_IOUT (8Ch)

Format: Unsigned binary

The READ_IOUT command on Page 0 stores rail A's I_{OUT} report.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_IOUT	0.25A/LSB.

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READ_TEMPERATURE (8Dh)

Format: Unsigned binary

The READ_TEMPERATURE command on Page 0 stores the temperature report.

Bits	Access	Bit Name	Description
15:11	R	RESERVED	Unused. Writes are ignored and reads are always 0.
10:0	R	READ_ TEMPERATURE	Returns the sensed temperature from TEMP. 1°C/LSB.

PROTOCOL_ID_EN_RDY (90h)

Format: Unsigned binary

The PROTOCOL_ID_EN_RDY command on Page 0 sets the PROTOCOL_ID for rail D (input power domain) and the VR. It also sets the time length from EN's positive edge to when the VR is ready to receive the SVID command, according to Intel specifications. Its format is the same as SVID specifications.

Bits	Access	Bit Name	Description
15:12	R/W	PROTOCOL_ID_VR_ R4	Provides rail D's lower 4 bits of PROTOCOL_ID. Identifies what version of the SVID protocol the controller supports. Input the correct value. 05h: IMVP8 08h: IMVP9 0Eh: IMVP9.1
11:8	R/W	PROTOCOL_ID_VR	Provides VR's lower 4 bits of PROTOCOL_ID. Identifies what version of SVID protocol the controller supports. Input the correct value. 05h: IMVP8 08h: IMVP9 0Eh: IMVP9.1
7:0	R/W	ENABLE_TO_SVID_ RDY_VR	Sets the time length (in μs) from EN's positive edge to the time when the VR is ready to receive the SVID command. The time length is equal to (bits[3:0] of this command) / 16 x 2 ^ (bits[7:4] of this command). Set this value according to the application requirements.

MFR_SVID_CFG (91h)

Format: Unsigned binary

The MFR_SVID_CFG command on Page 0 enables some functions.

Bits	Access	Bit Name	Description
15	R/W	MFR_RAILB_ BELONG_CORE	Selects whether rail B belongs to the Core or GT. 1'b1: Rail B belongs to the Core 1'b0: Rail B belongs to GT
14:12	R/W	DVID_SETPS4_PS0_ EN	Bit[14]: Enables the device to reject SETREG_VOUTMAX when the payload < VID_SETTING command. Bit[13]: Enables ACK SETPS4 CMD during DVID. Bit[12]: Enables ACK SETPS0 CMD during DVID.
11	R/W	MFR_STORE_ MTPSTATE	Enables the device to store the MTP_WR state to the SVID registers for debugging. 1b'0: Disabled 1b'1: Enabled

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10:9	R/W	MFR_DECAY_CFG	Configures the decaying slew rate. 2b'00 or 2b'11: Normal decay, Hi-Z PWM, or output discharge slew rate, depending on the output capacitor and I_{OUT} 2b'01: Decay with a fast slew rate. V_{REF} discharges with a fast slew rate when the decay command is received 2b'10: Decay with a slow slew rate. V_{REF} discharges with a slow slew rate when the decay command is received
8	R/W	PSYS_AST_HOT_EN	Determines whether the PSYS over-critical level asserts VRHOT#. 1'b0: No assertion 1'b1: Assertion
7:0	R/W	MFR_TEMP_MAX	Sets the over-temperature (OT) warning limit. VRHOT# asserts when the sensed temperature reaches this threshold. 1°C/LSB.

VENDOR_ID_PRODUCT_ID (92h)

Format: Unsigned binary

The VENDOR_ID_VR command on Page 0 returns the unique identification for the VR vendor and the unique identification for the VR product. The vendor ID is assigned by Intel. This register is mandatory, and the VR must return the assigned vendor ID. The VR vendor assigns the product ID.

Bits	Access	Bit Name	Description
15:8	R/W	VENDOR_ID_VR	Returns the unique identification for the VR vendor, assigned by Intel.
7:0	R/W	PRODUCT_ID_VR	Returns the unique identification for the VR product, assigned by the VR vendor.

PRODUCT_DATA_CODE (93h)

Format: Unsigned binary

The PRODUCT_DATA_CODE command on Page 0 returns the unique 4-digit hex code identifier for different devices or projects for the VR controller. The vendor assigns this data.

Bits	Access	Bit Name	Description
15:8	R/W	PRODUCT_REV_VR	Returns the unique 2-digit hex code identifier assigned by the vendor for different customers. 80 by default. Do not change this value.
7:0	R/W	PRODUCT_DATA_ CODE_VR	Returns the unique 2-digit hex code identifier assigned by the vendor for different projects.

LOT_CODE_VR (94h)

Format: Unsigned binary

The LOT_CODE_VR command on Page 0 returns the code revision.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	LOT_CODE_VR	Returns the digital code revision assigned by the VR vendor.

PS3_PS4_EXIT_DELAY (95h)

Format: Unsigned binary

The PS3_PS4_EXIT_DELAY command on Page 0 sets the time length for rail A to exit PS3/PS4. The format is the same as SVID specifications.

Bits	Access	Bit Name	Description
15:8	R/W	PS3_EXIT_ LATENCY_VR	Sets the time length (in µs) for rail A to exit PS3. The time length is equal to (bits[11:8] of this command) / 16 x 2 ^ (bits[15:12] of this command).

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7:0	R/W	PS4_EXIT_ LATENCY_VR	Sets the time length (in µs) for rail A to exit PS4. The time length is equal to (bits[3:0] of this command)/ 16 x 2 ^ (bits[7:4] of this command).

MFR_SR_FAST_TOLERANCE (96h)

Format: Unsigned binary

The MFR_SR_FAST_TOLERANCE command on Page 0 sets rail A's output tolerance, the data register containing the rail A fast slew rate capability, and the slew rate that the platform VR can sustain.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_SR_FAST_VR	Indicates the fast slew rate capability that the platform VR can sustain. Binary format in mV/µs (i.e. 0Ah = 10mV/µs). 1mV/µs per LSB.
7:0	R/W	MFR_VR_ TOLERANCE	This data register contains the VR TOB based on the board's parts (e.g. inductor DCR, inductance tolerance, and current-sense errors). Binary format (in mV) (i.e. 13h = ±19mV tolerance budget). 1mV/LSB.

MFR_SVID_06H_34H_VR (97h)

Format: Unsigned binary

The MFR_SVID_06H_34H_VR command on Page 0 sets the MULTI_VR_CONFIG and capabilities for rail A.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	MFR_MULTI_VR_ CONFIG	Sets the initial value of the lower 2 bits of SVID MUTI_VR_CONFIG (34h). The bitmapped data register that configures multiple VRs' behavior on the same bus can be configured to reset the behavior of VR_READY under a 0V VID command.
7:0	R/W	CAPABILITY_VR	This is a bitmapped register that identifies the SVID VR capabilities, and which of the optional telemetry registers are supported. 00h indicates that only required registers are supported. Bit[7]: Set to 1 if (15h) is formatted to FFh = I_{CCMAX} for VR12.5 and beyond Bit[6]: Temperature ADC (17h) Bit[5]: P_{IN} ADC (1Bh) Bit[4]: V_{IN} ADC (1Ah) Bit[3]: I_{IN} ADC (19h) Bit[2]: P_{OUT} ADC (18h) Bit[1]: V_{OUT} ADC (16h) Bit[0]: I_{OUT}/J_{OUT} ADC format (15h)

MFR_SVID_06H_34H_PSYS (98h)

Format: Unsigned binary

The MFR_SVID_06H_34H_PSYS command on Page 0 sets the MULTI_VR_CONFIG and capabilities for rail 4 (input power domain).

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	MFR_MULTI_VR_ CONFIG_PSYS	Returns the initial value of SVID MUTI_VR_CONFIG (34h), bits[3:2] for the input power domain.

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7:0	R/W	CAPABILITY_VR_PSYS	This is a bitmapped register that identifies the SVID VR capabilities, and which of the optional telemetry registers are supported. 00h indicates that only required registers are supported. Bit[7]: Set to 1 if (15h) is formatted to FFh = I_{CCMAX} for VR12.5 and beyond Bit[6]: Temperature ADC (17h) Bit[5]: P_{IN} ADC (1Bh) Bit[4]: V_{IN} ADC (1Ah) Bit[3]: I_{IN} ADC (19h) Bit[2]: P_{OUT} ADC (18h) Bit[1]: V_{OUT} ADC (16h) Bit[0]: I_{OUT}/J_{OUT} ADC format (15h)

MFR_STANDBY_HOT_SET (99h)

Format: Unsigned binary

The MFR_STANDBY_HOT_SET command on Page 0 sets the VRHOT# behaviors.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_SVID_ADDR_MODE	1'b1: Supports a separate address for each rail
12	R/W	MFR_AUXIMON_ALERT_EN	Enables the device to assert #ALT when the AUX_IMON report exceeds the AUXIMON_MAX. 1'b1: Enabled 1'b0: Disabled
11	R/W	MFR_STANDBY_HOT_EN	Enables the standby hot function. When all rails are in PS4 and the core rails exit PS4, the device asserts VRHOT# to save power. 1'b1: Enabled 1'b0: Disabled
10:0	R/W	MFR_STANDBY_HOT_TIME	Sets the VRHOT# assertion time when the standby hot function is enabled. 1ms/LSB. De-asserts VRHOT# when the rail of GT changes its PS state or the rail of the Core goes into PS4 again.

MFR_SVID_OFFSET (9Ah)

Format: Unsigned binary

The MFR_SVID_OFFSET command on Page 0 sets the default value of the offset for SVID-VID and enables the SVID function

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8	R/W	MFR_SVID_RAIL_EN_R1	Enables the SVID function for rail A. 1'b1: Enabled 1'b0: Disabled
7:0	R/W	MFR_SVID_OFFSET_INIT_R1	Sets the default value of the SVID-VID offset.

MFR_MIN_ON_TIME (A0h)

Format: Unsigned binary

The MFR_MIN_ON_TIME command on Page 0 sets the minimum PWM on time.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
2:0	R/W	MFR_MIN_ON_TIME	10ns/LSB.

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MFR_MIN_OFF_TIME (A1h)

Format: Unsigned binary

The MFR_MIN_OFF_TIME command on Page 0 sets the minimum PWM off time.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	MFR_MIN_OFF_TIME	10ns/LSB.

MFR_MIN_HIZ_TIME (A2h)

Format: Unsigned binary

The MFR_MIN_HIZ_TIME command on Page 0 sets the minimum off time when exiting Hi-Z to low, as well as the minimum Hi-Z time.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:7	R/W	MFR_MIN_LOW_EXIT_HIZ	Sets the minimum off time when exiting Hi-Z to low. 20ns/LSB.
6:0	R/W	MFR_MIN_HIZ_TIME	Sets the minimum PWM Hi-Z time. 10ns/LSB.

MFR_BLANK_TIME (A3h)

Format: Unsigned binary

The MFR_BLANK_TIME command on Page 0 sets the minimum time for PWM phases on rail A.

Bits	Access	Bit Name	Description
15:5	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
4:0	R/W	MFR_BLANK_TIME	Sets the blanking time, calculated with the following equation: (MFR_BLANK_TIME + 3) x 10ns

MFR_PSI_TRIM4 (B0h)

Format: Unsigned binary

The MFR_PSI_TRIM4 command on Page 0 sets rail A's slope compensation value for DCM, PS1, PS2, and PS3.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	MFR_TRIM_SETPS2_3	Sets the slope output compensation in PS2 and PS3. 2.5mV/LSB.
9:5	R/W	MFR_TRIM_SETPS1	Sets the slope output compensation in PS1. 2.5mV/LSB.
4:0	R/W	MFR_TRIM_DCM	Sets the slope output compensation in DCM. 2.5mV/LSB.

MFR_PSI_TRIM1 (B1h)

Format: Unsigned binary

The MFR_PSI_TRIM1 command on Page 0 sets rail A's slope output compensation in 1-phase, 2-phase, and 3-phase CCM.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	MFR_TRIM_3	Sets rail A's slope output compensation during 3-phase CCM. 2.5mV/LSB.
9:5	R/W	MFR_TRIM_2	Sets rail A's slope output compensation during 2-phase CCM. 2.5mV/LSB.
4:0	R/W	MFR_TRIM_1	Sets rail A's slope output compensation during 1-phase CCM. 2.5mV/LSB.

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MFR_PSI_TRIM2 (B2h)

Format: Unsigned binary

The MFR_PSI_TRIM2 command on Page 0 sets rail A's slope output compensation during 4-phase CCM.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	RESERVED	Reserved.
9:5	R/W	RESERVED	Reserved.
4:0	R/W	MFR_TRIM_4	Sets rail A's slope output compensation during 4-phase operation. 2.5mV/LSB.

MFR_PSI_TRIM3 (B3h)

Format: Unsigned binary

The MFR_PSI_TRIM3 command on Page 0 sets rail B's slope output compensation in 2-phase, and 1-phase CCM.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	MFR_TRIM_6	Sets rail B's slope output compensation during 1-phase CCM. 2.5mV/LSB.
9:5	R/W	MFR_TRIM_5	Sets rail B's slope output compensation during 2-phase CCM. 2.5mV/LSB.
4:0	R/W	RESERVED	Reserved.

MFR_CS_READ1 (B4h)

Format: Unsigned binary

The MFR_CS_READ1 command on Page 0 stores the ADC sample result of CS1 (I_{CS1}).

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	MFR_CS1	I_{CS1} = (MFR_CS1 x 8 x 1.6V / 1024 - 1.23V) / R_{CS} / K_{CS}

MFR_CS_READ2 (B5h)

Format: Unsigned binary

The MFR_CS_READ2 command on Page 0 stores the ADC sample results of CS2 and CS3 (I_{CS2} and I_{CS3}, respectively).

Bits	Access	Bit Name	Description
15:8	R	MFR_CS3	I_{CS3} = (MFR_CS3 x 8 x 1.6V / 1024 - 1.23V) / R_{CS} / K_{CS}
7:0	R	MFR_CS2	I_{CS2} = (MFR_CS2 x 8 x 1.6V / 1024 - 1.23V) / R_{CS} / K_{CS}

MFR_CS_READ3 (B6h)

Format: Unsigned binary

The MFR_CS_READ3 command on Page 0 stores the ADC sample result of CS4 (I_{CS4}).

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Internal use only.
7:0	R	MFR_CS4	I_{CS4} = (MFR_CS4 x 8 x 1.6V / 1024 - 1.23V) / R_{CS} / K_{CS}

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RESERVED (B7h)

Format: Unsigned binary

The RESERVED command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Internal use only.
7:0	R	RESERVED	Internal use only.

MFR_CS_READ5 (B8h)

Format: Unsigned binary

The MFR_CS_READ5 command on Page 0 stores the ADC sample results of CS5 and CS6 (I_{CS5} and I_{CS6}, respectively).

Bits	Access	Bit Name	Description
15:8	R	MFR_CS6	I_{CS6} = (MFR_CS6 x 8 x 1.6V / 1024 - 1.23V) / R_{CS} / K_{CS}
7:0	R	MFR_CS5	I_{CS5} = (MFR_CS5 x 8 x 1.6V / 1024 - 1.23V) /R_{CS} / K_{CS}

READ_AUXIMON (B9h)

Format: Unsigned binary

The READ_AUXIMON command on Page 0 stores the AUXIMON report. This value is monitored by sensing the voltage on the AUX_IMON pin.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R	READ_AUXIMON_ EXPO	Sets the exponent value to calculate AUXIMON.
7:0	R	READ_AUXIMON	AUXIMON can be calculated with the following equation: AUXIMON = READ_AUXIMON x 2 ^ (READ_AUXIMON_EXPO x I_AUX_MAX / (256 x 8 / 11)

READ_PIN (BAh)

Format: Unsigned binary

The READ_PIN command on Page 0 stores the total system input power (P_{IN}). P_{IN} is monitored by sensing the voltage on the PSYS pin.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	READ_PIN	Returns the monitored total system P_{IN}. 1W/LSB.

MFR_VIN_HYS_OFFS_SET (BBh)

Format: Unsigned binary

The MFR_VIN_HYS command on Page 0 sets the V_{IN} sense hysteresis and V_{IN} sense offset. The V_{IN} sample result is equal to the ADC result, plus MFR_VIN_SENSE_OFFSET. MFR_VIN_HYS is the threshold for the V_{IN} sample result variation to trigger an on-time calculation.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:4	R/W	MFR_VIN_HYS	Sets the threshold for V_{IN} sample result variation to trigger an on-time calculation. The on time is refreshed when the V_{IN} sample variation exceeds MFR_VIN_HYS. 0.1V/LSB.

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3:0	R/W	MFR_VIN_SENSE_ OFFSET	Sets the V_{IN} sample offset. Bit[3] is the signed bit. 25mV/LSB.

MFR_PIN_MAX (BCh)

Format: Unsigned binary

The MFR_PIN_MAX command on Page 0 is the P_{IN} sensor scale, which is configured by the platform designer to the rating of the P_{IN} sensor (2W/LSB). The SVID PIN_MAX register (2Eh) is half of P_{IN_MAX}. P_{IN_MAX} = 2 x MFR_PIN_MAX x 2 ^ MFR_PIN_MAX_EXPO.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	MFR_PIN_MAX_ EXPO	Sets the high exponent to calculate P_{IN_MAX}.
7:0	R/W	MFR_PIN_MAX	Sets the base number of the system P_{IN} senor scale. 2W/LSB. P_{IN_MAX} can be calculated with the following equation: P_{IN_MAX} = 2 x MFR_PIN_MAX x 2 ^ MFR_PIN_MAX_EXPO

MFR_AUXIMON_MAX_SET (BDh)

Format: Unsigned binary

The MFR_AUXIMON_MAX_SET command on Page 0 sets the AUX_IMON sensor scale for the SVID register 15h (P_{IN} domain). This value is configured by the platform designer to the rating of the AUX_IMON sensor (1A/LSB).

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	MFR_AUXIMON_ MAX_HIGH_EXPO	Sets the high exponent to calculate MFR_AUXIMON_MAX.
7:0	R/W	MFR_AUXIMON_ MAX	Sets the base number of AUX_IMON MAX, which can be calculated with the following equation: AUX_IMON_MAX = MFR_AUXIMON_MAX x 2 ^ MFR_AUXIMON_MAX_HIGH_EXPO

MFR_ADDR_PMBUS (C0h)

Format: Unsigned binary

The MFR_ADDR_PMBUS command on Page 0 configures the device's PMBus address.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7	R/W	PMBUS_ADDR_ MODE	Determines how the PMBus address is set and read. 1'b1: The 7-bit PMBus address is set via the registers 1'b0: The 4MSB are set by the register. The 3LSB of the PMBus address are determined by the ADDR pin voltage, and bits[2:0] of this command are read-only. Any values written to bits[2:0] are ignored
6:0	R/W	PMBUS_ADDR_ VALUE	Determines the set value for the PMBus address if bit[7] of this command is set to 1'b1. The address is determined by the ADDR pin voltage and bits[6:3] of this command if bit[7] is set to1'b0.

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MFR_VIN_OV_UV_LIMIT (C1h)

Format: Unsigned binary

The MFR_VIN_OV_UV_LIMIT command on Page 0 sets the V_{IN} under-voltage (UV) warning threshold. If the sensed V_{IN} drops below this limit, the system indicates that V_{IN} is too low. This command also sets the V_{IN} over-voltage protection (OVP) threshold. If the sensed V_{IN} exceeds this limit, the system takes action according to the V_{IN} OVP mode.

Bits	Access	Bit Name	Description
15:8	R/W	VIN_UV_WARNING_LIMIT	Sets the V_{IN} under-voltage (UV) warning level. 0.125V/LSB.
7:0	R/W	VIN_OV_FAULT_LIMIT	Sets the V_{IN} over-voltage protection (OVP) level. 0.125V/LSB.

MFR_OTP_SET (C2h)

Format: Unsigned binary

The MFR_OTP_SET command on Page 0 sets the VR's over-temperature protection (OTP) threshold.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:7	R/W	MFR_OTP_LIMIT	Sets the over-temperature protection (OTP) limit. When the junction temperature monitored on the TEMP pin exceeds OTP_LIMIT, the VR shuts off and disables the output. 1°C/LSB.
6:0	R/W	MFR_OTP_HYS	Sets the temperature hysteresis for OTP if this protection is set to non-latch mode. When the junction temperature monitored on TEMP drops below MFR_OTP_LIMIT - MFR_OTP_HYS, the PWM initiates a soft start as it would during a normal start-up sequence. 1°C/LSB.

MFR_SLOPE_CNT_1P (D2h)

Format: Unsigned binary

The MFR_SLOPE_CNT_1P command on Page 0 sets the slope voltage ramping time for the VR in 1-phase CCM. It is for rail A only.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_SLOPE_CNT_1P	Sets the slope compensation saturation time for 1-phase CCM. Typically, this time is set at 1.3 x (t_S - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_1P (D3h)

Format: Unsigned binary

The MFR_SLOPE_SR_1P command on Page 0 sets the VR slope compensation slew rate in 1-phase CCM. It is for rail A only. Sets the final slope voltage amplitude between 20mV and 30mV to stabilize the system.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_1P	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_1P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_1P	Sets the current source for slope voltage generation. 0.25μA/LSB.

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MFR_SLOPE_CNT_2P (D4h)

Format: Unsigned binary

The MFR_SLOPE_CNT_2P Page 0 sets the slope voltage ramping time for the VR in 2-phase CCM. It is for rail A only.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_SLOPE_CNT_2P	Sets the slope compensation saturation time for 2-phase CCM. Typically, this time is set at 1.3 x (t_S / 2 - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_2P (D5h)

Format: Unsigned binary

The MFR_SLOPE_SR_2P command on Page 0 sets the VR slope compensation slew rate in 2-phase CCM. It is for rail A only. Sets the final slope voltage amplitude between 20mV and 30mV to stabilize the system.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_2P	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_2P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_2P	Sets the current source for slope voltage generation. 0.25μA/LSB.

MFR_SLOPE_CNT_3P (D6h)

Format: Unsigned binary

The MFR_SLOPE_CNT_3P command on Page 0 sets the slope voltage ramping time for the VR in 3-phase CCM. It is for rail A only.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_SLOPE_CNT_3P	Sets the slope compensation saturation time for 3-phase CCM. Typically, this time is set at 1.3 x (t_S / 3 - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_3P (D7h)

Format: Unsigned binary

The MFR_SLOPE_SR_3P command on Page 0 sets the VR slope compensation slew rate in 3-phase CCM. It is for rail A only. Sets the final slope voltage amplitude between 20mV and 30mV to stabilize the system.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_3P	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_3P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_3P	Sets the current source for slope voltage generation. 0.25μA/LSB.

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MFR_SLOPE_CNT_4P (D8h)

Format: Unsigned binary

The MFR_SLOPE_CNT_4P command on Page 0 sets the slope voltage ramping time for the VR in 4-phase CCM. It is for rail A only.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_SLOPE_CNT_4P	Sets the slope compensation saturation time for 4-phase CCM. Typically, this time is set at 1.3 x (t_S / 4 - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_4P (D9h)

Format: Unsigned binary

The MFR_SLOPE_SR_4P command on Page 0 sets the VR slope compensation slew rate in 4-phase CCM. It is for rail A only.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_4P	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_4P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_4P	Sets the current source for slope voltage generation. 0.25μA/LSB.

RESERVED1 (DAh)

Format: Unsigned binary

The RESERVED1 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	INTERNAL_USE	Reserved.

RESERVED2 (DBh)

Format: Unsigned binary

The RESERVED2 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	INTERNAL_USE	Reserved.
5:0	R/W	INTERNAL_USE	Reserved.

RESERVED3 (DCh)

Format: Unsigned binary

The RESERVED3 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	INTERNAL_USE	Reserved.

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RESERVED4 (DDh)

Format: Unsigned binary

The RESERVED4 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	INTERNAL_USE	Reserved.
5:0	R/W	INTERNAL_USE	Reserved.

RESERVED5 (DEh)

Format: Unsigned binary

The RESERVED5 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	INTERNAL_USE	Reserved.

RESERVED6 (DFh)

Format: Unsigned binary

The RESERVED6 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	INTERNAL_USE	Reserved.
5:0	R/W	INTERNAL_USE	Reserved.

MFR_SLOPE_CNT_5P (E0h)

Format: Unsigned binary

The MFR_SLOPE_CNT_5P command on Page 0 sets the slope voltage ramping time for the VR in 2-phase CCM. It is for rail B only.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_SLOPE_CNT_5P	Sets the slope compensation saturation time for 2-phase CCM for rail B. Typically, this time is set at 1.3 x (t_S / (phase number) - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_5P (E1h)

Format: Unsigned binary

The MFR_SLOPE_SR_5P command on Page 0 sets the VR slope compensation slew rate in 2-phase CCM. It is for rail B only.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_5P	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_5P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_5P	Sets the current source for slope voltage generation. 0.25μA/LSB.

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MFR_SLOPE_CNT_6P (E2h)

Format: Unsigned binary

The MFR_SLOPE_CNT_6P command on Page 0 sets the slope voltage ramping time for the VR in 1-phase CCM. It is for rail B only.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_SLOPE_CNT_6P	Sets the slope compensation saturation time for 1-phase CCM for rail B. Typically, this time is set at 1.3 x (t_S / 1 - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_6P (E3h)

Format: Unsigned binary

The MFR_SLOPE_SR_6P command on Page 0 sets the VR slope compensation slew rate in 1-phase CCM. It is for rail B only.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_6P	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_6P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_6P	Sets the current source for slope voltage generation. 0.25μA/LSB.

MFR_CS_OFFSET2_3 (E4h)

Format: Unsigned binary

The MFR_CS_OFFSET2_3 command on Page 0 sets the current bias for the thermal offset. It is for 2-phase and 3-phase operation.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_CS_OFFSET3	Sets the CS3 offset in the current balance loop. LSB = 3.2V / K_{CS} / R_{CS} / 1023. Where K_{CS} is the current-sense gain (in μA/A), and R_{CS} is the current-sense sample resistor (in Ω).
7:0	R/W	MFR_CS_OFFSET2	Sets the CS2 offset in the current balance loop. LSB = 3.2V / K_{CS} / R_{CS} / 1023. Where K_{CS} is the current-sense gain (in μA/A), and R_{CS} is the current-sense sample resistor (in Ω).

MFR_CS_OFFSET4 (E5h)

Format: Unsigned binary

The MFR_CS_OFFSET4 command on Page 0 sets the current bias for the thermal offset. It is for 4-phase operation.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Internal use only.
7:0	R/W	MFR_CS_OFFSET4	Sets the CS4 offset in the current balance loop. LSB = 3.2V / K_{CS} / R_{CS} / 1023. Where K_{CS} is the current-sense gain (in μA/A), and R_{CS} is the current-sense sample resistor (in Ω).

RESERVED7 (E6h)

Format: Unsigned binary

The RESERVED7 command on Page 0 are reserved.

Bits	Access	Bit Name	Description
15:8	R/W	INTERNAL_USE	Reserved.

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7:0	R/W	INTERNAL_USE	Reserved.

MFR_CS_OFFSET5_6 (E7h)

Format: Unsigned binary

The MFR_CS_OFFSET5_6 command on Page 0 sets the current bias for the thermal offset. It is for 5-phase and 6-phase operation.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_CS_OFFSET6	Sets the CS6 offset in the current balance loop. LSB = 3.2V / K_{CS} / R_{CS} / 1023. Where K_{CS} is the current-sense gain (in μA/A), and R_{CS} is the current-sense sample resistor (in Ω).
7:0	R/W	MFR_CS_OFFSET5	Sets the CS5 offset in the current balance loop. LSB = 3.2V / K_{CS} / R_{CS} / 1023. Where K_{CS} is the current-sense gain (in μA/A), and R_{CS} is the current-sense sample resistor (in Ω).

MFR_IMON_SVID1 (E8h)

Format: Unsigned binary

The MFR_IMON_SVID1 command on Page 0 sets the gain and offset for the I_{OUT} report from the VR to the SVID processor for 1-phase operation on rail A. R_{IMON} can be calculated with Equation (11):

$$R_{IMON} = 1.6V \times (8 / 11) \times [1 / (I_{CC_MAX} \times K_{CS} / 32 + 5\mu A)] \quad (11)$$

Where K_{CS} is the current-sense gain (in μA/A), and I_{CC_MAX} is the maximum current set by MFR_ICC_MAX_SET (53h) (Page 0 for rail A, and Page 1 for rail B).

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_IMON_SVID_ OFFSET1	Sets the constant offset for the IMON report (SVID - 15h) for the SVID initiator. Bit[14] is the signed bit. LSB = 1 / 255 x I_{CC_MAX}.
7:0	R/W	MFR_IMON_SVID_ GAIN1	Sets the gain for the IMON report (SVID - 15h) for the SVID initiator, calculated with the following equation: Gain = (I_{CCMAX} x K_{CS} x K_{IMON} + I_{BIAS}) / (I_{CC_MAX} x K_{CS} x K_{IMON}) x 128 Where K_{CS} is the current-sense gain (in μA/A), and I_{CC_MAX} is the maximum current set by MFR_ICC_MAX_SET (53h).

MFR_IMON_SVID2 (E9h)

Format: Unsigned binary

The MFR_IMON_SVID2 command on Page 0 sets the gain and offset for the I_{OUT} report from the VR to the SVID processor for 2-phase operation on rail A.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_IMON_SVID_ OFFSET2	Sets the constant offset for the IMON report (SVID - 15h) for the SVID initiator. Bit[14] is the signed bit. LSB = 1 / 255 x I_{CC_MAX}.
7:0	R/W	MFR_IMON_SVID_ GAIN2	Sets the gain for the IMON report (SVID - 15h) for the SVID initiator, calculated with the following equation: Gain = (I_{CC_MAX} x K_{CS} x K_{IMON} + I_{BIAS}) / (I_{CC_MAX} x K_{CS} x K_{IMON}) x 128 Where K_{CS} is the current-sense gain (in μA/A), and I_{CC_MAX} is the maximum current set by MFR_ICC_MAX_SET (53h).

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MFR_IMON_SVID3 (EAh)

Format: Unsigned binary

The MFR_IMON_SVID3 command on Page 0 sets the gain and offset for the I_{OUT} report from the VR to the SVID processor for 3-phase operation on rail A.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_IMON_SVID_ OFFSET3	Sets the constant offset for the IMON report (SVID - 15h) for the SVID initiator. Bit[14] is the signed bit. LSB = 1 / 255 x I_{CC_MAX}.
7:0	R/W	MFR_IMON_SVID_ GAIN3	Sets the gain for the IMON report (SVID - 15h) for the SVID initiator, calculated with the following equation: $Gain = (I_{CC_MAX} \times K_{CS} \times K_{IMON} + I_{BIAS}) / (I_{CC_MAX} \times K_{CS} \times K_{IMON}) \times 128$ Where K_{CS} is the current-sense gain (in μA/A), and I_{CC_MAX} is the maximum current set by MFR_ICC_MAX_SET (53h).

MFR_IMON_SVID4 (EBh)

Format: Unsigned binary

The MFR_IMON_SVID4 command on Page 0 sets the gain and offset for the I_{OUT} report from the VR to the SVID processor for 4-phase operation on rail A.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_IMON_SVID_ OFFSET4	Sets the constant offset for the IMON report (SVID - 15h) for the SVID initiator. Bit[14] is the signed bit. LSB = 1 / 255 x I_{CC_MAX}.
7:0	R/W	MFR_IMON_SVID_ GAIN4	Sets the gain for the IMON report (SVID - 15h) for the SVID initiator, calculated with the following equation: $Gain = (I_{CC_MAX} \times K_{CS} \times K_{IMON} + I_{BIAS}) / (I_{CC_MAX} \times K_{CS} \times K_{IMON}) \times 128$ Where K_{CS} is the current-sense gain (in μA/A), and I_{CC_MAX} is the maximum current set by MFR_ICC_MAX_SET (53h).

RESERVED8 (ECh)

Format: Unsigned binary

The RESERVED8 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	INTERNAL_USE	Reserved.
7:0	R/W	INTERNAL_USE	Reserved.

RESERVED9 (EDh)

Format: Unsigned binary

The RESERVED9 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	INTERNAL_USE	Reserved.
7:0	R/W	INTERNAL_USE	Reserved.

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RESERVED10 (EEh)

Format: Unsigned binary

The RESERVED10 command on Page 0 is reserved.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	INTERNAL_USE	Reserved.
7:0	R/W	INTERNAL_USE	Reserved.

MFR_IMON_SVID5 (EFh)

Format: Unsigned binary

The MFR_IMON_SVID5 command on Page 0 sets the gain and offset for the I_{OUT} report from the VR to the SVID processor for 2-phase operation on rail B.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_IMON_SVID_ OFFSET5	Sets the constant offset for the IMON report (SVID - 15h) for the SVID initiator. Bit[14] is the signed bit. LSB = 1 / 255 x I_{CC_MAX}.
7:0	R/W	MFR_IMON_SVID_ GAIN5	Sets the gain for the IMON report (SVID - 15h) for the SVID initiator, calculated with the following equation: $Gain = (I_{CC_MAX} \times K_{CS} \times K_{IMON} + I_{BIAS}) / (I_{CC_MAX} \times K_{CS} \times K_{IMON}) \times 128$ Where K_{CS} is the current-sense gain (in μA/A), and I_{CC_MAX} is the maximum current set by MFR_ICC_MAX_SET (53h on Page 1).

MFR_IMON_SVID6 (F0h)

Format: Unsigned binary

The MFR_IMON_SVID6 command on Page 0 sets the gain and offset for the I_{OUT} report from the VR to the SVID processor for 1-phase operation on rail B.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_IMON_SVID_ OFFSET6	Sets the constant offset for the IMON report (SVID - 15h) for the SVID initiator. Bit[14] is the signed bit. LSB = 1 / 255 x I_{CC_MAX}.
7:0	R/W	MFR_IMON_SVID_ GAIN6	Sets the gain for the IMON report (SVID - 15h) for the SVID initiator, calculated with the following equation: $Gain = (I_{CC_MAX} \times K_{CS} \times K_{IMON} + I_{BIAS}) / (I_{CC_MAX} \times K_{CS} \times K_{IMON}) \times 128$ Where K_{CS} is the current-sense gain (in μA/A), and I_{CC_MAX} is the maximum current set by MFR_ICC_MAX_SET (53h on Page 1).

MFR_CB_PI_SET (F1h)

Format: Unsigned binary

The MFR_CB_PI_SET command on Page 0 defines the negative and positive saturation level of the current balance loop and frequency loops. It also sets the proportion integrate (PI) value for the current balance loop.

Bits	Access	Bit Name	Description
15:12	R/W	MFR_TUNE_NSATU	Defines the negative saturation level of the current balance loop and frequency loop. 10ns/LSB, ranging between -80ns and 0ns. Bit[15] is the signed bit. For example, to set the negative saturation level to -50ns, set these bits to 4'hB.

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11:8	R/W	MFR_TUNE_PSATU	Defines the positive saturation level of the current balance loop and frequency loop. 10ns/LSB, ranging between 0ns and 70ns. For example, to set the positive saturation level to 50ns, set these bits to 4'h5.
7:6	R/W	RESERVED	Reserved.
5:0	R/W	MFR_CB_PI	Sets the PI parameter value for the current balance loop.

MFR_VIN_GAIN_SET (F2h)

Format: Unsigned binary

The MFR_VIN_GAIN_SET command on Page 0 sets the gain and constant offset for the V_{IN} report.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_VIN_OFFSET	Sets the constant offset for the V_{IN} report. 0.125V/LSB.
7:0	R/W	MFR_VIN_GAIN	Sets the gain for the V_{IN} report, calculated with the following equation: Gain = 2 x 4096 x 16 x 1.6 / 1023 = 205 (set 205 as the default)

MFR_AUXIMON_SVID (F3h)

Format: Unsigned binary

The MFR_AUXIMON_SVID command on Page 0 sets the gain and constant offset for the AUX_IMON report (SVID - 15h of the 0xD input power domain). R_{AUX_IMON} can be estimated with Equation (12):

$$R_{AUX_IMON} = 1.16 / (AUX_IMON_MAX \times K_{AUX} \times AUX_IMON_GAIN) \quad (12)$$

Where K_{AUX} is the AUX_IMON current gain (in μA/A), AUX_IMON_GAIN is the divider gain (1:1), and AUX_IMON_MAX is the maximum AUX_IMON current as set by MFR_AUXIMON_MAX_SET (BDh).

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_AUXIMON_ SVID_OFFSET	Sets the constant offset of the AUX_IMON report (SVID - 15h of the 0xD domain) for the SVID initiator. Bit[14] is the signed bit. LSB = 1 / 255 x AUX_IMON_MAX.
7:0	R/W	MFR_AUXIMON_ SVID_GAIN	Sets the gain of the AUX_IMON report (SVID - 15h of the 0xD domain) for the SVID initiator. The default value is 128.

MFR_PSYS_SVID (F4h)

Format: Unsigned binary

The MFR_PSYS_SVID command on Page 0 sets the gain and constant offset for the PSYS report (SVID - 1Bh of the 0xD input power domain). R_{PSYS} can be calculated with Equation (13):

$$R_{PSYS} = V_{PSYS_MAX} / (PSYS_MAX \times I_{SYS}) \quad (13)$$

Where I_{SYS} is the input power gain (in μA/W), V_{PSYS_MAX} is related to PSYS_GAIN, which is the divider gain set by MFR_PSYS_GAIN_SEL (F6h), and PSYS_MAX is the maximum input power (in W) set by MFR_PIN_MAX (BCh).

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:8	R/W	MFR_PSYS_SVID_ OFFSET	Sets the constant offset of the PSYS report (SVID - 1Bh of the 0xD domain) for the SVID initiator. LSB = 1 / 255 x PSYS_MAX.
7:0	R/W	MFR_PSYS_SVID_ GAIN	Sets the PSYS report gain (SVID - 1Bh of the 0xD domain) for the SVID initiator. The default value is 128.

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MFR_TEMPERATURE_GAIN_SET (F5h)

Format: Unsigned binary

The MFR_TEMPERATURE_GAIN_SET command on Page 0 sets the temperature-sense gain and offset.

Bits	Access	Bit Name	Description
15:8	R/W	TEMPERATURE_ OFFSET	Sets the temperature-sense offset. Signed value, 1°C/LSB. For example, to set MFR_TEMP_OFFSET to -2°C, set MFR_TEMP_OFFSET to 8'hFE. The default value is 10.
7:0	R/W	TEMPERATURE_ GAIN	Sets the relationship between the temperature (T(°C)) and temperature-sense voltage (VTEMP_SENSE). The default value is 160, but it can be calculated with the following equation: T (°C) = A x 1/2 x VTEMP_SENSE + B Where A is TEMPERATURE_GAIN / 0.8, and B is TEMPERATURE_OFFSET.

MFR_PSYS_GAIN_SEL (F6h)

Format: Unsigned binary

The MFR_PSYS_GAIN_SEL command on Page 0 sets the PSYS divider gain inside the chip.

Bits	Access	Bit Name	Description
15:2	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
1:0	R/W	MFR_PSYS_GAIN_ SEL	2'b01: Selects a 5:8 gain. PSYS_SENSE = (V_{PSYS} x 5/8) x 1023 / 1.6; V_{PSYS_MAX} = 2.56V 2'b1x: Selects a 1:1 gain. PSYS_SENSE = V_{PSYS} x 1023 / 1.6; V_{PSYS_MAX} = 1.6V

CLEAR_EEPROM_FAULTS (FEh)

Format: Unsigned binary

The CLEAR_EEPROM_FAULTS command on Page 0 clears the EEPROM fault bits. If no other protection remains after this command is sent, the VR starts ramping and outputs power.

This command is write-only. There is no data byte for this command.

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PAGE 1 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 1 selects the register page. The MPQ29164 has three register pages: Page 0, Page 1, and Page 3. Page 0 and Page 1 are the common commands that are used in application; these values are stored in the multiple-time programmable (MTP) memory. Page 3 is the debugging register that is used for ATE testing; debugging information is not stored in the MTP. Do not write to Page 3's registers.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
1:0	R/W	PAGE	Selects the Page register. 2'b11: Page 3 (debugging page) 2'b10: None 2'b01: Page 1 (rail B and trim registers) 2'b00: Page 0 (rail A registers and some registers for rail B)

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 1 configures the converter's operational state.

Bits	Access	Bit Name	Description
7	R/W	ON_OFF_STATE	Controls whether the PMBus device output is on or off. 2'b0x: The output is off 2'b1x: The output is on
6	R/W	RESERVED	Reserved.
5:4	R/W	VOLT_CMD_ SOURCE	Controls the basic source of the V_{OUT} command when the PMBus device output is on (bit[7] of this command = 1). 2'b00: The nominal V_{OUT} is set by the PMBus VOUT_COMMAND data 2'b01: The nominal V_{OUT} is set by the PMBus VOUT_MARGIN_LOW data 2'b10: The nominal V_{OUT} is set by the PMBus VOUT_MARGIN_HIGH data 2'b11: Not supported
3:2	R/W	MARGIN_FAULT_ RESPONSE	Reserved.
1:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

Format: Unsigned binary

The CLEAR_FAULTS command on Page 1 clears any fault bits that have been set on the rails. This command clears all bits in all status registers simultaneously.

This command is write-only. There is no data byte for this command.

CLEAR_LAST_FAULT (08h)

Format: Unsigned binary

The CLEAR_LAST_FAULT command on Page 1 clears the faults in LAST_FAULT_BLOCK (07h on Page 0).

This command is write-only. There is no data byte for this command.

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SINGLE_READ_TRIG (09h)

Format: Unsigned binary

The SINGLE_READ_TRIG command on Page 1 commands the device to read the data from the MTP via MFR_SINGLE_RW_ADDR (0Ah on Page 0), bits[7:0].

This command is write-only. There is no data byte for this command.

SINGLE_WRITE_TRIG (0Ch)

Format: Unsigned binary

The SINGLE_WRITE_TRIG command on Page 1 writes the data from MFR_SINGLE_WR_DATA (0Bh on Page 0) to the MTP via MFR_SINGLE_RW_ADDR (0Ah on Page 0), bits[15:8].

This command is write-only. There is no data byte for this command.

STORE_USER_ALL (15h)

Format: Unsigned binary

The STORE_USER_ALL command on Page 1 instructs the PMBus device to copy the Page 0 to Page 1 contents (not including the read-only registers) from the operating memory to the matching locations in the MTP, regardless of the current PMBus register page. This command can be used while the device is outputting power.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

Format: Unsigned binary

The RESTORE_USER_ALL command on Page 1 instructs the PMBus device to copy the Page 0 to Page 1 contents from the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have matching locations in the operating memory are ignored. This command cannot be used while the device is outputting power unless MFR_EEPROM_COPY_EN (1Dh on Page 0), bit[1] is set to 1.

This command is write-only. There is no data byte for this command.

TM_MTP_WRITE_TRIG (19h)

Format: Unsigned binary

The TM_MTP_WRITE_TRIG command on Page 1 is used for the MTP auto-test function.

This command is write-only. There is no data byte for this command.

MFR_IDROOP_CTRL (1Bh)

Format: Unsigned binary

The MFR_IDROOP_CTRL command on Page 1 sets the I_{DROOP} function.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:7	R/W	AC_DROOP_COMP	Selects the bandwidth and bias current for the AC droop.
6	R/W	DAC_CMP_EN	Enables the DAC_CMP function (compared with VREF_FILTER with VREF_DAC). For this bit to be effective, the MFR_DAC_CMP_EN bit must be set to 1'b1. 1'b1: Enabled 1'b0: Disabled
5	R/W	IDROOP_BW_SET	Selects the I_{DROOP} bandwidth. 1'b0: Low bandwidth 1'b1: High bandwidth

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4	R/W	IDROOP_EN	Enables the DC I_{DROOP} or the AC I_{DROOP}. 1'b0: Enables DC I_{DROOP} 1'b1: Enables AC I_{DROOP}
3:0	R/W	IDROOP_SET	Sets the I_{DROOP} DC gain to set the digital load-line gain. 4'h0: 0 4'h1: 4/8 x 1/8 4'h2: 5/8 x 1/8 4'h3: 6/8 x 1/8 4'h4: 7/8 x 1/8 4'h5: 8/8 x 1/8 4'h6: 9/8 x 1/8 4'h7: 10/8 x 1/8 4'h8: 11/8 x 1/8 4'h9: 12/8 x 1/8 4'hA: 13/8 x 1/8 4'hB: 14/8 x 1/8 4'hC: 15/8 x 1/8 4'hD: 16/8 x 1/8 4'hE: 17/8 x 1/8 4'hF: 18/8 x 1/8

MFR_LOW_VOUT_TRIM (1Fh)

Format: Unsigned binary

The MFR_LOW_VOUT_TRIM command on Page 1 applies a fixed offset voltage to the V_{OUT} command value for different power states when V_{OUT} undergoes DVID to a lower value. Typically, this command is used by the end user to trim V_{OUT} when the PMBus device is assembled into the end user's system.

Bits	Access	Bit Name	Description
15:12	R/W	LOW_VOUT_TRIM_TH	Sets the level to apply LOW_VOUT_TRIM. If the V_{OUT} gain = 2:1, then 0.1V/LSB. If the V_{OUT} gain = 1:1, then 0.05V/LSB.
11:8	R/W	LOW_VOUT_TRIM_2_CCM	Applies a fixed offset voltage to V_{OUT} in multi-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
7:4	R/W	LOW_VOUT_TRIM_1_CCM	Applies a fixed offset voltage to V_{OUT} in 1-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
3:0	R/W	LOW_VOUT_TRIM_DCM	Applies a fixed offset voltage to V_{OUT} in 1-phase DCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 1 sets the rail B V_{OUT} when the PMBus controls the output.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

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7:0	R/W	VOUT_COMMAND	Sets the rail reference voltage (VID_DAC output voltage) in PMBus mode. In 5mV VID step mode: if RMS_GAIN = 2:1 (4Ah, bit[11] = 0), V_{REF} = (VID + 49) / 2 x 5mV if RMS_GAIN = 1:1 (4Ah, bit[11] = 1), V_{REF} = (VID + 49) / 2 x 10mV In 10mV VID step mode: V_{REF} = (VID + 19) / 2 x 10mV

MFR_VOUT_TRIM (22h)

Format: Unsigned binary

This MFR_VOUT_TRIM command on Page 1 applies a fixed offset voltage to the commanded V_{OUT} for different power states when V_{OUT} exceeds the value set by MFR_LOW_VOUT_TRIM (1Fh on Page 1), bits[15:12]. Typically, this command is used by the end user to trim V_{OUT} when the PMBus device is assembled into the end user's system.

Bits	Access	Bit Name	Description
15:12	R/W	VOUT_TRIM_3_CCM	Applies a fixed offset voltage to V_{OUT} in ≥3-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
11:8	R/W	VOUT_TRIM_2_CCM	Applies a fixed offset voltage to V_{OUT} in 2-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
7:4	R/W	VOUT_TRIM_1_CCM	Applies a fixed offset voltage to V_{OUT} in 1-phase CCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.
3:0	R/W	VOUT_TRIM_DCM	Applies a fixed offset voltage to V_{OUT} in 1-phase DCM. If the V_{OUT} gain = 2:1, then 3.125mV/LSB. If the V_{OUT} gain = 1:1, then 1.5625mV/LSB.

VOUT_CAL_OFFSET (23h)

Format: Unsigned binary

The VOUT_CAL_OFFSET command on Page 1 offers an offset VID for the rail B target determined by VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW. This command is the initial value of the SVID offset.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_CAL_OFFSET	Sets the VID offset in PMBus mode. It is also the initial value for the SVID offset register (SVID - 33h). 5mV/LSB or 10mV/LSB according to MFR_VR_CONFIG (39h), bit[7]. -80h ~ +7Fh.

MFR_VOUT_MAX (24h)

Format: Unsigned binary

The MFR_VOUT_MAX command on Page 1 sets the initial value of SVID VOUT_MAX (SVID - 30h) for rail B, which sets an upper limit on the VID target (not including the offset) of SVID to prevent V_{OUT} from being set to a possibly dangerous level. If an attempt is made to set the VID target above VOUT_MAX, the command is rejected. The PMBus VID target is not constrained by MFR_VOUT_MAX.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_CAL_OFFSET	Sets an upper limit on the rail B VID target (not including the offset) of SVID.

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VOUT_MARGIN_HIGH (25h)

Format: Unsigned binary

The VOUT_MARGIN_HIGH command on Page 1 sets the rail B reference voltage (VID_DAC V_{OUT}) at the command margin high state.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_MARGIN_HIGH	Sets the reference voltage (VID_DAC V_{OUT}) at the command margin high state.

VOUT_MARGIN_LOW (26h)

Format: Unsigned binary

The VOUT_MARGIN_LOW command on Page 1 sets the rail B reference voltage (VID_DAC V_{OUT}) at the command margin low state.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	VOUT_MARGIN_LOW	Sets the reference voltage (VID_DAC V_{OUT}) at the command margin low state.

MFR_VBOOT (27h)

Format: Unsigned binary

The MFR_VBOOT command on Page 1 sets the boot-up voltage (V_{BOOT}) for rail B.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_VBOOT	Sets V_{BOOT} for rail B (following the VID table). For example, to set V_{BOOT} to 0.9V using the 5mV VID table, set these bits to 0x83h.

MFR_FS (28h)

Format: Unsigned binary

The MFR_FS command on Page 1 sets the rail B frequency.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	MFR_FS	Sets the rail B operation frequency. 50kHz/LSB.

MFR_PHASE_NUM (29h)

Format: Unsigned binary

The MFR_PHASE_NUM command on Page 1 sets the rail B phase number.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
2:0	R/W	MFR_PHASE_NUM	Sets the phase number for rail B.

MFR_CONFIG1 (2Bh)

Format: Unsigned binary

The MFR_CONFIG1 command on Page 1 sets certain functions.

Bits	Access	Bit Name	Description
15	R/W	MFR_OFF_IMON_BIAS_R2	1’b1: Disable the IMON biased current

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14:13	R/W	MFR_CYC_MODE_R2	Keep both of these bits set to 1.
12	R/W	MFR_ADAP_CLK_EN_R2	Enables switching to low clock running in PS2/PS1 (if DLL is enabled off in PS2/PS1). 1'b1: Enabled 1'b0: Disabled
11	R/W	MFR_PS1_OFF_DLL_EN_R2	Enables DLL to turn off in PS1. 1'b1: Enabled 1'b0: Disabled
10	R/W	MFR_ECOV2_DYNAMIC_FLT_OC_R2	Enables the OC pre-phase signal to hold the current balance (CB) loop. This function must be enabled if the CB loop is enabled. 1'b0: Disabled 1'b1: Enabled
9:8	R/W	MFR_LL_MINUS_R2	Sets the fast slew rate function when receiving a SETVID_FAST command. Reduces I_{DROOP} when VID_Fast occurs at a large LL. I_{DROOP} gain-X cannot be set bellow 0. MFR_CONFIG3 (49h), bit[8] enables this function. 2'b00: I_{DROOP} gain (1Bh (on Page 0), bits[3:0]) - 4 2'b01: I_{DROOP} gain (1Bh (on Page 0), bits[3:0]) - 3 2'b10: I_{DROOP} gain (1Bh (on Page 0), bits[3:0]) - 2 2'b11: I_{DROOP} gain (1Bh (on Page 0),, bits[3:0]) - 1
7	R/W	MFR_BLK_SET_EN_R2	1'b0: Disables the shield PWM_SET signal when the slope saturates and enables the slope leakage reduction function 1'b1: Enables the shield PWM_SET signal when the slope saturates and enables the slope leakage reduction function
6:4	R/W	MFR_BLK_SET_POS_RANGE_R2	Sets the shield time for PWM_SET after the slope saturates. The shield time can be calculated with the following equation: Shield time = MFR_BLK_SET_POS_RANGE_R2 x 20 + 10ns
3	R/W	MFR_BLK_SET_PRE_RANGE_EN_R2	1'b0: Disable the shield PWM_SET signal before the slope saturates 1'b1: Enable the shield PWM_SET signal before the slope saturates; the shield time can be set by bits[2:0] of this command
2:0	R/W	MFR_BLK_SET_PRE_RANGE_R2	If bit[2] = 0, then bits[1:0] have the following options: 2'b00: 280ns 2'b01: 200ns 2'b10: 120ns 2'b11: 40ns If bit[2] = 1: then bits[1:0] have the following options: 2'b00: 140ns 2'b01: 100ns 2'b10: 60ns 2'b11: 20ns

MFR_IMON_SNS_OFFS (2Ch)

Format: Unsigned binary

The MFR_IMON_SNS_OFFS command on Page 1 applies a constant offset on the IMONB ADC sample result due to a 5µA IMON bias current.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_IMON_SNS_OFFS	The value should be -(5µA x R_{IMON} x 1023 / 1.6). Convert this value to a two's complement number.

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MFR_PLATFORM_TIME_SET (2Eh)

Format: Unsigned binary

The MFR_PLATFORM_TIME_SET command on Page 1 sets the rail B period after VID_PRES has added the rising step, and before VID_PRES starts to subtract the rising step. It also sets the time delay for one rail to exit PS4 while another rail is not in PS4.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:6	R/W	MFR_SGL_PS4_DLY	Sets the time delay when rail B exits PS4 while rail A is not in PS4. 1µs/LSB.
5:0	R/W	MFR_PLATFORM_ TIME	Sets the V_{REF} hold time from when V_{REF} rises to the target VID plus an additional step x VID step, when DVID ramps up. 1µs/LSB.

MFR_APSI_CTRL (30h)

Format: Unsigned binary

The MFR_APSI_CTRL command on Page 1 controls the APS behaviors and t_{ON} extension for rail B.

Bits	Access	Bit Name	Description
15:13	R/W	MFR_PS23_TON_ FACTOR	Sets the t_{ON} extended factor in PS2 and PS3 (not in APS). 3'd0: 75% 3'd1: 100% 3'd2: 125% 3'd3: 150% 3'd4: 175% 3'd5: 200% 3'd6: 225% 3'd7: 250%
12:10	R/W	MFR_PS1_TON_ FACTOR	Sets the t_{ON} extended factor in PS1 (not in APS). 3'd0: 75% 3'd1: 100% 3'd2: 125% 3'd3: 150% 3'd4: 175% 3'd5: 200% 3'd6: 225% 3'd7: 250%
9	R/W	MFR_ADP_PSI_ BYPASS	Disables the SETPS command when APS is enabled. Active high.
8	R/W	MFR_ADP_OC_ EXIT_EN	Enables the 1-phase CCM/DCM rail to exit to full-phase running when there is a per-phase over-current (OC) condition in APS mode. Active high.
7:5	R/W	PHASE_DROP_ DELAY	Sets the delay time to drop phases after detecting that the total current is smaller than the phase-shedding threshold. About 120µs/LSB.
4	R/W	APS_VID_CHANGE	Holds APS for a set time after DVID decays.
3	R/W	LOAD_STEP_FSW_ DET	Enables the VR to enter full-phase when f_{SW} is high at APS 1'b0: Disabled 1'b1: Enabled
2:0	R/W	APS_DELAY_TIME	Sets the delay time to enable APS after high/low frequency detection or DVID.

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MFR_FS_LOOP_CYC_RIPPLE_SET (31h)

Format: Unsigned binary

The MFR_FS_LOOP_CYC_RIPPLE_SET command on Page 1 sets rail B's ripple parameters for Fast-V mode in SVID mode, as well as the frequency loop parameters.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8	R/W	MFR_CYC_RIPPLE_FILT	Enables the device to hold the phase current ripple when DVID or the cycle over-current protection (OCP) limit is updated. 1'b1: Enabled 1'b0: Disabled
7:6	R/W	MFR_CYC_RIPPLE_GAIN	Sets the ripple current gain, which can be used to reduce the cycle current limit. 2'b00: 0%. No ripple current offset 2'b01: 25% ripple current offset 2'b10: 50% ripple current offset 2'b11: 100% ripple current offset
5:3	R/W	MFR_FS_LOOP_CNT	Sets the delay time to hold the frequency loop. ADC sample period/LSB.
2:0	R/W	MFR_FS_LOOP_CTRL	Enables the device to hold the frequency loop when there are changes due to DVID, high or low frequencies (HF/LF), or the power state (PS). Bit[2]: DVID Bit[1]: PS changes Bit[0]: HF/LF detection

MFR_DC_CB_DYNC_SET (32h)

Format: Unsigned binary

The MFR_DC_CB_DYNC_SET command on Page 1 controls rail B's dynamic behavior for the DC loop and current balance loop.

Bits	Access	Bit Name	Description
15:13	R/W	MFR_PANR_RAND_BW	Selects a range of random numbers. It is valid when PANR is enabled (set by MFR_AUDIBLE_REDUCE (3Ah on Page 1), bit[8]) and the random delay is enabled (set by MFR_AUDIBLE_REDUCE (3Ah on Page 1), bit[9]). RAND_A = MFR_AUDIBLE_REDUCE (3Ah on Page 1), bits[15:10] RAND_C = MFR_VID_DOWN_DELAY (3Bh on Page 1), bits[15:0] RAND_x0 = {2'd0, MFR_TRANS_FAST (3Dh on Page 1), bits[13:0] RAND_DELAY = rem(RAND_A x RAND_x0 + RAND_C, 65536)} Where rem is used to take the remainder, and USED_RAND_DELAY is the actual delay time for PANR. 3'b000: USED_RAND_DELAY = {10'd0, RAND_DELAY bits[5:0]} 3'b001: USED_RAND_DELAY = {8'd0, RAND_DELAY, bits[7:0]} 3'b010: USED_RAND_DELAY = {6'd0, RAND_DELAY, bits[9:0]} 3'b011: USED_RAND_DELAY = {4'd0, RAND_DELAY, bits[11:0]} 3'b100: USED_RAND_DELAY = {2'd0, RAND_DELAY, bits[13:0]} 3'b101: USED_RAND_DELAY = {4'd0, RAND_DELAY, bits[15:4]} 3'b110: USED_RAND_DELAY = {2'd0, RAND_DELAY, bits[15:2]} 3'b111: USED_RAND_DELAY = {RAND_DELAY, bits[15:0]}
12:10	R/W	MFR_DC_CAL_CNT	Sets the delay time to hold the DC loop. ADC sample period/LSB.
9	R/W	MFR_PFM_CTRL	Disables the low-frequency signal when the optimal t_{ON} is shorter than MIN_ON_TIME. Effective low. 1'b1: Enabled 1'b0: Disabled

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8:6	R/W	MFR_DC_CAL_CTRL	Enables the device to hold the DC loop when there are changes due to DVID, high or low frequencies (HF/LF), and the power state (PS). Bit[8]: DVID Bit[7]: PS changes Bit[6]: HF/LF detection
5:3	R/W	MFR_CB_CAL_CTRL	Enables the device to hold the current balance loop when there are changes due to DVID, high or low frequencies (HF/LF), and the power state (PS). Bit[5]: DVID Bit[4]: PS changes Bit[3]: HF/LF detection
2:0	R/W	MFR_CB_CAL_CNT	Sets the delay time to hold the current balance loop. ADC sample period/LSB.

MFR_VOUT_CMPS_SET (33h)

Format: Unsigned binary

The MFR_VOUT_CMPS_SET command on Page 1 sets V_{OUT} compensation behaviors for rail B.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_VOUT_CMPS_MAX	Sets the rails' maximum level for V_{OUT} compensation. 0.3125mV/LSB (if the VCOMP DAC reference is 320mV). LSB = VCOMP_DAC_REF / 256 / 4.
7:6	R/W	5MV_VO_COMP_STEP	Sets the V_{OUT} compensation COMP adding step by counting the PWM number during SETVID_FAST/SLOW. This value updates every (5MV_VO_COMP_STEP + 1) PWM1.
5	R/W	5MV_VO_COMP_STEP_EN	Enables the device to count PWM1 when adding V_{OUT} compensation. This bit is effective when bit[4] of this command is set to 1. 1b'0: Disabled 1b'1: Enabled
4	R/W	5MV_VO_COMP_EN	Enables the device to add a 5mV V_{OUT} compensation when the VR is under 5mV mode. 1b'0: Disabled 1b'1: Enabled
3:1	R/W	VCOMP_STEP_EXIT_DELAY	Sets the V_{OUT} compensation adding step by counting the PWM number after decay finishes. This value updates every (VOMP_STEP_EXIT_DELAY) PWM1.
0	R/W	VCOMP_STEP_EXIT_DECAY_EN	Enables the VR to add V_{OUT} compensation by counting the PWM after decay finishes. Otherwise, V_{OUT} compensation is added once decay finishes. 1b'0: Add V_{OUT} compensation to COMP once 1b'1: Add V_{OUT} compensation to COMP by counting PWM

MFR_PROTECT_MODE (34h)

Format: Unsigned binary

The MFR_PROTECT_MODE command on Page 1 sets rail B's modes for under-voltage protection (UVP), over-voltage protection (OVP1 and OVP2), and over-current protection (OCP).

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:6	R/W	MFR_UVP_SET_MODE	Sets rail B's UVP mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times and then latch off

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5:4	R/W	MFR_OVP2_SET_MODE	Sets rail B's OVP_VID mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times and then latch off
3:2	R/W	MFR_OVP1_SET_MODE	Sets rail B's OVP_VMAX mode. Bit[3]: Enables OVP1 Bit[2]: Sets the OVP1 mode, where 1 selects latch-off mode and 0 selects hiccup mode
1:0	R/W	MFR_OCP_SET_MODE	Sets rail B's OCP mode. 2'b00: No action 2'b01: Latch-off mode 2'b10: Hiccup mode 2'b11: Retry 6 times and then latch off

MFR_VCAL_FS_PI (37h)

Format: Unsigned binary

The MFR_VCAL_FS_PI command on Page 1 sets the PI parameters for the rail B frequency loop and DC loop.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:6	R/W	MFR_FS_LOOP_PI	Sets the PI parameter for the frequency loop.
5:0	R/W	MFR_VCAL_PI	Sets the PI parameter for the DC loop.

IOUT_CAL_GAIN_SET (38h)

Format: Unsigned binary

The IOUT_CAL_GAIN command on Page 1 sets rail B's PMBus I_{OUT} report gain.

Bits	Access	Bit Name	Description
15:10	R/W	IOUT_CAL_OFFSET	Sets the constant offset for the PMBus I_{OUT} report. 0.25A/LSB.
9:0	R/W	IOUT_CAL_GAIN	Sets the I_{OUT} report gain, calculated with the following equation: $IOUT_CAL_GAIN = I_{CCMAX} + 5\mu A / (G_{IMON} \times K_{CS})$ Where K_{CS} is the CS gain of the Intelli-Phase™ (in A/A).

MFR_VR_CONFIG (39h)

Format: Unsigned binary

The MFR_VR_CONFIG command on Page 1 enables some rail B functions, such as DC loop calibration and APS.

Bits	Access	Bit Name	Description
15	R/W	IMVP9_SEL	Sets the two rails to IMVP8 or IMVP9. This only affects the VRRDY assignment. 1b'0: IMVP8 1b'1: IMVP9 and above
14	R/W	MFR_RAIL_EN	Enables rail B's power output. 1'b1: Enabled 1'b0: Disabled

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13	R/W	MFR_CYC_OCP_FROM_FW	Determines whether the OCP_PHASE limit is selected by the register or SVID command. 1'b1: The OCP_PHASE limit is set by the register 1'b0: The OCP_PHASE limit is set by the SVID command
12	R/W	MFR_WAIT_SETTLE_SEL	Selects when rail B's VRRDY goes low to high as DVID rises from 0V (not including V_{BOOT}) if SVID 34h is written to 00. 1b'0: VRRDY turns high when DVID starts rising from 0V (not including V_{BOOT}) 1b'1: VRRDY turns high after DVID rises from 0V (not including V_{BOOT})
11	R/W	MFR_PMBUS_SR_SEL	Selects the VID slew rate for rail B when the PMBus controls V_{OUT}. 1b'0: V_{OUT} changes with a fast slew rate when the PMBus controls V_{OUT} 1b'1: V_{OUT} changes with a slow slew rate when the PMBus controls V_{OUT}
10	R/W	MFR_PMBUS_PS_EN	Enables the PMBus to control rail B's power state in PMBus mode. 1'b0: Disabled 1'b1: Enabled
9:8	R/W	MFR_PMBUS_PS	Sets rail B's power state when the PMBus controls the power state. 2'b00: PS0 2'b01: PS1 2'b10: PS2 2'b11: PS3
7	R/W	MFR_VID_STEP_SEL	Selects rail B's VID step. 1'b1: 5mV/LSB 1'b0: 10mV/LSB
6	R/W	MFR_FS_LOOP_PS1_EN	Enables the frequency loop in PS1. This function is disabled if the extending t_{ON} function is enabled in PS1 (MFR_APSI_CTRL (30h on Page 1), bits[12:10] are not set to 3'd1). For this bit to be enabled, disable PS1_CTRL_GTCLK_DIS_R2 by setting 1Ah (on Page 1), bit[11] = 1. 1'b1: Enabled 1'b0: Disabled
5	R/W	MFR_FS_LOOP_EN	Enables the frequency loop in PS0/PS1. 1'b1: Enabled 1'b0: Disabled
4	R/W	MFR_DC_LOOP_DCM_EN	Enables the DC loop in DCM. 1'b1: Enabled 1'b0: Disabled
3	R/W	MFR_DC_LOOP_EN	Enables the DC loop in PS0, PS1, PS2, and PS3. 1'b1: Enabled 1'b0: Disabled
2	R/W	MFR_IPHASE_BALANCE_EN	Enables the current balance loop in PS0. 1'b1: Enabled 1'b0: Disabled
1	R/W	MFR_APS_EN	Enables APS in PS0 and PS1 if MFR_PSI_ICC_CTRL (4Ah on Page 1), bit[7] = 1. 1'b1: Enabled 1'b0: Disabled
0	R/W	MFR_PMBUS_MODE_SEL	Determines whether rail B is controlled by the PMBus or SVID. 1'b0: SVID control 1'b1: PMBus control

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MFR_AUDIBLE_REDUCE (3Ah)

Format: Unsigned binary

The MFR_AUDIBLE_REDUCE command on Page 1 configures rail B's audible noise reduction parameters.

Bits	Access	Bit Name	Description
15:10	R/W	RAND_A	Sets the RAND_A parameter for the random number algorithm.
9:8	R/W	AUDIBLE_REDUCE_EN	Selects the audible noise reduction mode. 2'bx0: Disable PANR 2'b01: Enable PANR and use a fixed delay time when the delayed DVID ramps down 2'b11: Enable PANR and use the random delay time when the delayed DVID ramps down. The random delay time is set by MFR_DC_CB_DYNC_SET (32h), bits[15:13]
7:0	R/W	VID_TARGET_DELTA	Sets the VID delta threshold to delay dynamic VID. If VID_PRESENT - VID_TARGET > MFR_AUDIBLE_REDUCE, bits[7:0], DVID is delayed for a duration. Follow the VID step selection (5mV/LSB or 10mV/LSB).

MFR_VID_DOWN_DELAY (3Bh)

Format: Unsigned binary

This MFR_VID_DOWN_DELAY command on Page 1 configures the delay time when the delayed DVID ramps down on rail B.

Bits	Access	Bit Name	Description
15:0	R/W	MFR_VID_DOWN_DELAY	1μs/LSB.

MFR_FILTER_SET (3Ch)

Format: Unsigned binary

The MFR_FILTER_SET command on Page 1 sets the parameters for the VID filter, as well as the slow slew rate for rail B.

Bits	Access	Bit Name	Description
15:12	R/W	MFR_FS_LOOP_HYS_ON_R2	10ns/LSB for the f_{SW} error. If the error exceeds MFR_FS_LOOP_HYS_ON, the f_{SW} loop starts running.
11:9	R/W	MFR_FS_LOOP_HYS_OFF_R2	10ns/LSB for the f_{SW} error. If the error is below MFR_FS_LOOP_HYS_ON, the f_{SW} loop is held.
8	R/W	MFR_FS_HYS_EN_R2	Enables the frequency loop hysteresis function 1'b0: Disabled 1'b1: Enabled
7	R/W	MFR_DAC_CMP_EN	Enables DAC_CMP_FILTER from the analog of rail B, which filters the VID_DAC output until the filtered VID_DAC output level equals the VID_DAC output when SETVID_DOWN is interrupted by SETVID_UP. For this bit to be effective, the DAC_CMP_EN bit must be set to 1'b1. 1'b0: Disabled 1'b1: Enabled
6	R/W	MFR_VID_FILTER_EN	Enables the VID filter for rail B, which is the VID_DAC output filter for SETVID_FAST/SLOW_DOWN transitions. There is no VID filter when VID goes up or VID goes down due to decay or a PS4 command. 1'b0: Disabled 1'b1: Enabled

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5:4	R/W	MFR_VID_FILTER	Sets rail B's VID_DAC output filter. 2'b00: 1μs added filter when VID ramps down or there is a steady V_{OUT} 2'b01: 3μs added filter when VID ramps down or there is a steady V_{OUT} 2'b10: 5μs added filter when VID ramps down or there is a steady V_{OUT} 2'b11: 7μs added filter when VID ramps down or there is a steady V_{OUT}
3:0	R/W	MFR_SLOW_SR_SEL	Selects the slew rate when rail B receives the SETVID_SLOW command. 4'b1xxx: 1/16 of the fast slew rate 4'b01xx: 1/8 of the fast slew rate 4'b001x: 1/4 of the fast slew rate 4'b0001: 1/2 of the fast slew rate

MFR_TRANS_FAST (3Dh)

Format: Unsigned binary

The MFR_TRANS_FAST command on Page 1 sets the reference fast slew rate when rail B receives the SETVID_FAST_UP command.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13:12	R/W	VID_STEP_DECAY	Sets the rail B reference minus the step during decay. The step = 2 x VID_STEP_DECAY + 1.
11	R/W	VID_SUBTRACT	Selects the rail B slew rate when the reference removes the additional rising step. 1'b0: 1/4 of the fast slew rate 1'b1: 1/8 of the fast slew rate
10:8	R/W	VID_RISING_STEP	Sets the VID to rise one more step after VID reaches the target. This raises V_{OUT}. In 5mV mode, one more rising step = VID_RISING_STEP x 2 + 1. In 10mV mode, one more rising step = VID_RISING_STEP.
7:6	R/W	VID_STEP_NUM	Sets the rail B reference step in one VID_SR_CNT period when the slew rate rises. The step is equal to DEC(VID_STEP_NUM) + 1.
5:0	R/W	VID_SR_CNT	Sets the time length that V_{REF} changes once for rail B. 100ns/LSB.

MFR_EN_DLY (3Eh)

Format: Unsigned binary

The MFR_EN_DLY command on Page 1 sets the rail B output power delay when EN asserts.

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	MFR_EN_DLY	Sets the delay for rail B to wait for the output power after MFR_EN_SEQUENCE_CFG (3Eh on Page 0), bits[10:7] passes, and when there is no V_{IN} or temperature fault. 20μs/LSB. This is the second start-up delay, and it is also the delay for hiccup mode, retry mode, and the PMBus turning off then on.

MFR_ALT_SET (3Fh)

Format: Unsigned binary

The MFR_ALT_SET command on Page 1 sets rail B's alert timing.

Bits	Access	Bit Name	Description
15:13	R/W	ALERT_FIRST_STEP	Sets the number of VID changes when the first change for VID_ALERT. The first VID change is equal to the value set by these bits.

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12:11	R/W	ALERT_STEP_NUM	Sets the number of VID changes when VID_ALERT changes once. The step is set to DEC (ALERT_STEP_NUM) + 1.
10:6	R/W	ALERT_DELAY_TIME	Sets the delay time to pull the VR_SETTLE signal high after the alert reference reaches the target VID. 100ns/LSB.
5:0	R/W	ALERT_SR_CNT	Sets the time length for the alert reference to change one step. 100ns/LSB.

MFR_SW_LF_SET (40h)

Format: Unsigned binary

The MFR_SW_LF_SET command on Page 1 defines rail B's PWM low-frequency threshold. If the time length between the adjacent PWM of the same phase is longer than the time length set by MFR_SW_LF_LIMIT, then f_{SW} is low.

Bits	Access	Bit Name	Description
15:12	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
11:10	R/W	MFR_SW_LF_FILT	Filters the low-frequency signal. The signal only asserts when it has been triggered for (MFR_SW_LF_FILT) continuous times. If these bits are set to 0, the signal asserts when it has been triggered once.
9	R/W	MFR_SW_LF_EN	Enables the low-frequency detection function. 1'b1: Enabled 1'b0: Disabled
8:0	R/W	MFR_SW_LF_LIMIT	Sets the low-frequency detection threshold. 10ns/LSB.

MFR_SW_HF_SET (41h)

Format: Unsigned binary

The MFR_SW_HF_SET command on Page 1 defines rail B's high-frequency detection threshold. If the PWM1 period is shorter than the low-level frequency, then f_{SW} is high.

Bits	Access	Bit Name	Description
15:11	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
10:9	R/W	MFR_SW_HF_FILT	Filters the high-frequency signal. The signal only asserts when it has been triggered for (MFR_SW_HF_FILT) continuous times. If these bits are set to 0, the signal asserts when it has been triggered once.
8	R/W	MFR_SW_HF_EN	Enables the high-frequency detection function. 1'b1: Enabled 1'b0: Disabled
7:0	R/W	MFR_SW_HF_LIMIT	Sets the high-frequency detection threshold. 10ns/LSB.

MFR_TON_ADJ_PS1_SW_LF_TH (42h)

Format: Unsigned binary

The MFR_TON_ADJ_PS1_SW_LF_TH command on Page 1 sets rail B's low-frequency threshold when the t_{ON} extend function is enabled in PS1.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_TON_ADJ_PS1_SW_LF_TH	10ns/LSB.

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MFR_PS2_OFFSLOPE_TON_TH (43h)

Format: Unsigned binary

The MFR_PS2_OFFSLOPE_TON_TH command on Page 1 sets rail B's t_{ON} threshold width when the slope compensation function is disabled in PS2 and PS3 (t_{ON} exceeds the threshold).

Bits	Access	Bit Name	Description
15:7	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
6:0	R/W	MFR_PS2_ OFFSLOPE_TON_TH	10ns/LSB.

MFR_TON_ADJ_PS1_SW_HF_TH (44h)

Format: Unsigned binary

The MFR_TON_ADJ_PS1_SW_HF_TH command on Page 1 sets rail B's high-frequency threshold when the t_{ON} extend function is enabled in PS1.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_TON_ADJ_ PS1_SW_HF_TH	10ns/LSB.

MFR_TON_ADJ_PS2_SW_HF_TH (45h)

Format: Unsigned binary

The MFR_TON_ADJ_PS2_SW_HF_TH command on Page 1 sets rail B's high-frequency threshold when the t_{ON} extend function is enabled in PS2 and PS3.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R/W	MFR_TON_ADJ_ PS2_SW_HF_TH	10ns/LSB.

MFR_SLOPE_CNT_SETPS1 (46h)

Format: Unsigned binary

The MFR_SLOPE_CNT_SETPS1 command on Page 1 sets the saturation value for slope ramp compensation during 1-phase operation on rail B.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	MFR_SLOPE_CNT_ SETPS1	Sets the slope compensation saturation time for 1-phase CCM. Typically, this time is set at 1.3 x (t_S - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_SETPS1 (47h)

Format: Unsigned binary

The MFR_SLOPE_SR_SETPS1 command on Page 1 sets the slope ramp compensation slew rate during 1-phase operation on rail B.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_ SETPS1	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_1P)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_ SETPS1	Sets the current source for slope voltage generation. 0.25μA/LSB.

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MFR_CONFIG2 (48h)

Format: Unsigned binary

The MFR_CONFIG2 command on Page 1 sets some functions.

Bits	Access	Bit Name	Description
15:14	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
13	R/W	MFR_VIDDOWN_ DEASSERT_FVM_ FAST	1'b1: Enable de-asserting VRHOT# if the VID down command is received, even if there is a cycle-by-cycle current limit function (CYC case) 1'b0: De-assert VRHOT# if a VID down command is received and there is no CYC case
12	R/W	MFR_SETTLE_ DEASSERT_FVM_ FAST	1'b1: Enable de-assertion of VRHOT# if V_{OUT} settles when there is still a CYC case 1'b0: De-assert VRHOT# if V_{OUT} settles and there is no CYC case
11	R/W	MFR_FVM_ VRHOT_FAST_EN	Sets the delay time for VRHOT# fast assertion. 1'b1: 30ns delay 1'b0: 150ns delay
10	R/W	MFR_CYC_OC_ ONLINE_BLANK	Enables the CYC function for several microseconds, until a new CYC limit is stable. 1'b1: Enabled 1'b0: Disabled
9	R/W	MFR_PANR_SLOW_ SLEWRATE_EN_ R2	Enables reducing the PANR slow down slew rate to 1/8 of the slow slew rate. 1'b1: Enabled 1'b0: Disabled
8:6	R/W	MFR_RISE_STEP_ FOR_FAST_R2	Sets the number of additional rising steps for rail B after the VID reaches the target to increase V_{OUT} for the fast slew rate. Rising step in 5mV mode = MFR_RISE_STEP_FOR_FAST_R2 x 2 + 1 Rising step in 10mV mode = MFR_RISE_STEP_FOR_FAST_R2
5	R/W	MFR_SETPS1_ PHASE2_EN_R2	Enables 2-phase running in a PS1 state. 1'b1: Enabled 1'b0: Disabled
4	R/W	MFR_PWM_SHIELD	Shields PWM when the slope saturates. 1'b0: Disabled 1'b1: Enabled
3	R/W	MFR_SLOPE_ LEAKAGE_ALL_PS	Selects the condition to enable the leakage off function. 1'b0: All PS state 1'b1: DCM
2	R/W	MFR_PANR_SLOW	After the PANR delay, the DVID down slew rate stays slow. 1'b0: Disabled 1'b1: Enabled
1	R/W	MFR_ECOV2_CYC_ LIMIT_VREF_EN	1'b1: Enables holding the DVID function during Fast_V mode. Alert assertion is delayed until V_{OUT} ramps to the target
0	R/W	MFR_ECOV2_FVM_ VRHOT	1'b1: Enable the FVM-VRHOT# assertion function

MFR_CONFIG3 (49h)

Format: Unsigned binary

The MFR_CONFIG3 command on Page 1 sets some functions for rail B.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

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8	R/W	MFR_LL_MINUS_EN_R2	1'b0: Disables LL_MINUS when receiving SETVID_FAST 1'b1: Enables LL_MINUS when receiving SETVID_FAST
7	R/W	MFR_PSCHG_COMP_EN_R2	1'b0: Disables adding a comp voltage when the PS changes 1'b1: Enables to add comp voltage when the PS changes
6:4	R/W	MFR_PSCHG_COMP_R2	Adds a COMP voltage when changing the power stage. 2.5mV/LSB (10mV / 4).
3:2	R/W	RESERVED	Reserved.
1:0	R/W	MFR_FAST_SR_VID_CHG_R2	Sets the hysteresis to enable the fast slew function when SETVID_FAST has been received and VID changes over the set limit. This only affects one more step and LL_MINUS. In 5mV steps: 80mV / LSB, with a maximum of 240mV In 10mV steps: 160mV / LSB, with a maximum of 480mV

MFR_PSI_ICC_CTRL (4Ah)

Format: Unsigned binary

The MFR_PSI_ICC_CTRL command on Page 1 sets power-saving behaviors (among others) for rail B.

Bits	Access	Bit Name	Description
15	R/W	MFR_DIS_LOOP_RST_TON	Resets the t_{ON} width when the frequency loop and current balance loop are held or disabled. This disables the sigma-delta function. 1'b1: Enabled 1'b0: Disabled
14	R/W	MFR_VID_TAB_SEL_FLY	Enables on-the-fly (online) changes for VID_STEP. 1'b1: Enabled 1'b0: Disabled
13	R/W	MFR_VID_TAB_SEL_MODE	Determines if VID_STEP is selected by VID_STEP from the VID_STRAP pin or MFR_VR_CONFIG (39h on Page 1), bits[7]. 1'b1: VID_STEP is set by the VID_STRAP pin (pull this pin high in 5mV mode; pull it low in 10mV mode) 1'b0: VID_STEP is set by the register
12	R/W	MFR_PS2_DLL_EN_FILT	Reserved.
11	R/W	MFR_RMS_GAIN1_EN	Sets the remote-sense gain. 1'b1: The gain is 1:1. Select this gain when VID_STEP = 5mV 1'b0: The gain is 2:1
10	R/W	MFR_SETPS_POS_FILT_FSW	Shields the frequency detection function for about 3 PWM pulses after receiving a SETPS command. 1'b1: Enabled 1'b0: Disabled
9	R/W	MFR_TON_ADJ_OFF_FSW	Shields the frequency detection function when t_{ON} is extended or reduced. (MFR_APSI_CTRL (30h on Page 1), bits[15:10] do not equal 6'b001_001). 1'b1: Enabled 1'b0: Disabled
8	R/W	MFR_CYC_OCP_EN_FILT	Enables the filter for the CYCLE_OCP function by 3μs. If the CYCLE_OCP limit has a delay on OCP-DAC, the CYC_OCP enable signal comes first and causes a false CYCLE_OCP. 1'b1: Enabled 1'b0: Disabled

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7	R/W	MFR_APS_PS1_EN	Enables APS in PS1. Only valid when MFR_VR_CONFIG (39h), bit[1] = 1. For this function to be effective, enable MFR_GATECLK_DIS (1Ah), bits[11:10]. 1'b1: Enabled 1'b0: Disabled
6	R/W	MFR_PS2_OFF_ IMON_BIAS	Enables the device to turn off the IMON bias current (5μA) in PS2 and PS3. 1'b1: Enabled 1'b0: Disabled
5	R/W	MFR_PS2_OFF_ SLOPE	Turns off the slope compensation function in PS2/PS3. Only valid when t_{ON} exceeds the value in MFR_PS2_OFFSLOPE_TON_TH (43h), bits[6:0]. 1'b1: Enabled 1'b0: Disabled
4	R/W	MFR_OCP_CMP_ EN_FILT	Enables the device to filter the OCP signal by 60μs when enabling the OCP comparator circuit when it has been turned off. 1'b1: Enabled 1'b0: Disabled
3	R/W	MFR_PS1_2_OFF_ OCP_CMP	Enables the device to turn off the CS comparator and CS buffer while in PS1, PS2, and PS3. 1'b1: Enabled 1'b0: Disabled
2	R/W	MFR_PS2_OFF_DLL	Enables the device to turn off the delay line loop (DLL) function in PS2 and PS3. The DLL clock is only off when all rails have turned off the DLL function. 1'b1: Enabled 1'b0: Disabled
1	R/W	MFR_PS1_STB_ LOW_EN	Enables the device to pull the STBB pin low in PS1 to save power if the Intelli-Phase™ supports this mode. 1'b1: Enabled 1'b0: Disabled
0	R/W	MFR_PS2_STB_ LOW_EN	Enables the device to pull the STBB pin low in PS2/PS3 to save power if the Intelli-Phase™ supports this mode. 1'b1: Enabled 1'b0: Disabled

MFR_APS_PHASE_HYS (4Bh)

Format: Unsigned binary

The MFR_APS_PHASE_HYS command on Page 1 sets rail B's hysteresis during APS, as well as the thresholds for DCM and 1-phase CCM.

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
12:9	R/W	MFR_0PHL	Sets the threshold to go from DCM to 1-phase CCM. 1A/LSB.
8:4	R/W	MFR_1PHL	Sets the threshold to go from 1-phase CCM to 2-phase CCM. 1A/LSB.
3:0	R/W	MFR_PHASE_HYS	Sets the current hysteresis for different phases. 1A/LSB.

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MFR_VOUT_MAX_9BIT (4Ch)

Format: Unsigned binary

The MFR_VOUT_MAX_9BIT command on Page 1 sets rail B's upper limit for VID + OFFSET. In PMBus mode, if VID + OFFSET exceeds this limit, the command is acknowledged, and the output is clamped at this limit. In SVID mode, if VID + OFFSET exceeds this limit, this command is rejected, and the output remains at the voltage that was set before this command.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:0	R/W	MFR_VOUT_MAX_9BIT	Sets rail B's upper limit for VID + OFFSET.

MFR_SLOPE_CNT_DCM_SET (4Dh)

Format: Unsigned binary

The MFR_SLOPE_CNT_DCM_SET command on Page 1 sets rail B's slope discharge time and slope compensation saturation value in DCM.

Bits	Access	Bit Name	Description
15	R/W	MFR_SLOPE_LEAKAGE	Enables the device to turn off the switch in the slope charging loop when the slope is saturated in PS2. 1'b0: Disabled 1'b1: Enabled
14:12	R/W	SLOPE_DISCHARGE_TIME	Sets the slope discharge time. 10ns/LSB. The discharge time can be calculated with the following equation: Slope discharge time = (SLOPE_DISCHARGE_TIME + 1) x 10
11:9	R/W	MFR_OFFSLOPE_TRIM	Sets V_{COMP} when the slope compensation function is off in PS2 and PS3. It is recommended to make this value 0, but it may need to be trimmed in actual applications. The LSB can be calculated with the following equation: LSB = VCOMP_DAC x 8 / 256 / 4 (V/LSB)
8:0	R/W	MFR_SLOPE_CNT_DCM	Sets the slope compensation saturation time for 1-phase DCM. Typically, this time is set at 2 x (t_S - t_{BLANK}) time, where t_S the switching period, and t_{BLANK} is the PWM blanking time. 10ns/LSB.

MFR_SLOPE_SR_DCM (4Eh)

Format: Unsigned binary

The MFR_SLOPE_SR_DCM command on Page 1 sets the VR slope compensation slew rate for rail B in 1-phase DCM.

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R/W	MFR_SLOPE_CAP_DCM	Sets the capacitor number for slope voltage generation. The capacitance is equal to (8 - DEC(CAP_DCM)) x 3.7pF.
5:0	R/W	MFR_SLOPE_SR_DCM	Sets the current source for slope voltage generation. 0.25μA/LSB.

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MFR_SHUTDOWN_LEVEL (4Fh)

Format: Unsigned binary

The MFR_SHUTDOWN_LEVEL command on Page 1 sets the rail B shutdown level. When V_{REF} is below this level while slewing downward, the VR stops switching and starts to decay.

Bits	Access	Bit Name	Description
15:14	R/W	MFR_IMMED_REF_STEP	Sets the VID (output reference) step when SVID sends VID within ±2LSB in 5mV mode on rail B.
13:11	R/W	MFR_IMMED_ALT_TIME	Sets the time length for ALERT signal on the SVID line to slew one step (MFR_ALT_SET (3Fh), bits[12:11] + 1) when SVID sends VID within ±2LSB in 5mV mode on rail B. 100ns/LSB.
10:8	R/W	MFR_IMMED_REF_TIME	Sets the time length for VID to slew one step (bits[15:14] of this command) when the SVID sends VID within ±2LSB in rail B's 5mV mode. 100ns/LSB.
7	R/W	MFR_IMMEDIATE_SVID_EN	Enables rail B to force the STATUS bit[0] to 1'b1. 1'b0: Disabled. STATUS bit[0] remains at 1'b0 until it settles normally 1'b1: Enabled. Forces STATUS bit[0] to 1'b1 when the SETVID command is received within ±2LSB
6	R/W	MFR_IMMEDIATE_REF_EN	Enables rail B using bits[15:8] of this command. 1'b0: Disabled 1'b1: Enabled
5:0	R/W	MFR_SHUTDOWN_LEVEL	This value should exceed one VID step to prevent under-voltage protection (UVP) from accidentally being triggered. 5mV/LSB (in 5mV mode). 10mV/LSB (in 10mV mode).

MFR_ADDR_SVID_CTRL (52h)

Format: Unsigned binary

The MFR_ADDR_SVID_CTRL command on Page 1 sets the SVID address for rail B.

Bits	Access	Bit Name	Description
15:4	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
3:0	R/W	MFR_ADDR_SVID	Sets the SVID address for rail B. 4'b 0000: The rail B address is 00h 4'b 0001: The rail B address is 01h 4'b 0010: The rail B address is 10h 4'b 0011: The rail B address is 11h

MFR_ICC_MAX_SET (53h)

Format: Unsigned binary

The MFR_ICC_MAX_SET command on Page 1 sets rail B's I_{CCMAX}.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	MFR_ICC_MAX_HIGH_EXPO	Sets the high exponent for MFR_ICC_MAX. I_{CCMAX} can be calculated with the following equation: I_{CCMAX} = MFR_ICC_MAX x 2 ^ (MFR_ICC_MAX_HIGH_EXPO)
7:0	R/W	MFR_ICC_MAX	1A/LSB. If MFR_ICC_MAX = 0, the rail does not start up.

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MFR_CYC_OCP_FACTOR (54h)

Format: Unsigned binary

The MFR_CYC_OCP_FACTOR command on Page 1 sets the gain and offset for the cycle-by-cycle current limit (CYCLE_OCP) on rail B. The CYCLE_OCP limit is equal to 1.28V + [(CYCLE_OCP_LIMIT / PHASE_NUM - RIPPLE_CURRENT) x MFR_CYC_OCP_GAIN + MFR_CYC_OCP_OFFSET x 0.01V].

Bits	Access	Bit Name	Description
15:9	R/W	MFR_CYC_OCP_ OFFSET	Sets a constant offset for the CYCLE_OCP limit. 10mV/LSB. The default value should be (1.23V - 1.28V) / 0.01V = -5.
8:0	R/W	MFR_CYC_OCP_ GAIN	Sets the gain for the CYCLE_OCP limit. The gain can be calculated with the following equation: $Gain = 12800 \times R_{CS} \times K_{CS}$ Where K_{CS} is the current-sense gain of the Intelli-Phase™ (in A/A), and R_{CS} is the sample current-sense resistor (in Ω). For example, if K_{CS} = 10μA/A and R_{CS} = 1500Ω, then the ideal gain should be 192.

MFR_PWR_INDUCTOR_GAIN (55h)

Format: Unsigned binary

The MFR_PWR_INDUCTOR_GAIN command on Page 1 sets rail B's ripple current gain, which corresponds to the value of the power inductor.

Bits	Access	Bit Name	Description
15:8	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R/W	MFR_PWR_ INDUCTOR_GAIN	Sets the ripple current gain, which can be calculated with the following equation: $Gain = 2^{15} / 5 / L$ Where L is the inductance (in nH). For example, if the inductor is 150nH, then the ideal gain should be 0x2C.

MFR_OCP_OVP_DAC_LIMIT (60h)

Format: Unsigned binary

The MFR_OCP_OVP_DAC_LIMIT command on Page 1 sets the DAC limit for over-current protection (OCP) and over-voltage protection (OVP) on rail B.

Bits	Access	Bit Name	Description
15:8	R/W	OCP_DA_LIMIT	Sets the per-phase OCP limit, calculated with the following equation: OCP_DA_LIMIT = per-phase OCP value x (KCS x RCS) x 100 - 5 For example, if R_{CS} = 1kΩ, K_{CS} = 10μA/A, set the per-phase OCP limit to 40A, meaning OCP_DA_LIMIT = 35 (0x23h).
7:0	R/W	OVP_DA_LIMIT	Sets the VR threshold for the V_{OUT} limit. Once V_{OUT} exceeds this level, the VR initiates a protection. 10mV/LSB.

MFR_OVP_UVP_SET (61h)

Format: Unsigned binary

The MFR_OVP_UVP_SET command on Page 1 sets the rail B threshold for under-voltage protection (UVP), as well as the delay time for UVP and over-voltage protection (OVP).

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.

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12	R/W	UVP_SEL	Sets the UVP threshold. 1'b1: V_{REF} - 150mV 1'b0: V_{REF} - 300mV
11:6	R/W	OVP_DELAY_TIME	Sets the OVP2 delay time for rail B. 200ns/LSB.
5:0	R/W	UVP_DELAY_TIME	Sets the UVP delay time for rail B. 20μs/LSB.

MFR_OCP_SET (62h)

Format: Unsigned binary

The MFR_OCP_SET command on Page 1 sets the rail B IMON over-current protection (OCP) threshold and delay time.

Bits	Access	Bit Name	Description
15:13	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
12:7	R/W	MFR_OCP_SET_DELAYTIME	Sets the average OCP delay time for rail B. 20μs/LSB.
6:0	R/W	MFR_OCP_SET_LEVEL	Sets rail B's over-current (OC) limit value (1A/LSB). The total OCP limit is set by MFR_OCP_SET_LEVEL multiplied by the phase number, which is compared to the value set by READ_IOUT (8Ch) / 4.

READ_VFB_SENSE (70h)

Format: Unsigned binary

The READ_VFB_SENSE command on Page 1 returns the sensed V_{FBB} voltage.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VFB_SENSE	Returns the sensed V_{FBB} voltage. 1.5625mV/LSB.

READ_AD_RESULT (71h)

Format: Unsigned binary

The READ_AD_RESULT command on Page 1 returns the ADC result of the channels set by MFR_DBG_ADC_CHANNEL (2Ah on Page 0).

Bits	Access	Bit Name	Description
15	R	ADC_AVG_TRIM_RDY	Returns the flag that finishes the 64-average filter of the ADC sample result.
14:0	R	READ_AD_RESULT	Returns half of the summed value of the 64-average filter ADC sample result. This value is equal to 64 x ADC_RESULT / 2.

READ_RAIL_STATE (75h)

Format: Unsigned binary

The READ_RAIL_STATE command on Page 1 stores other rail B states.

Bits	Access	Bit Name	Description
15:9	R	RESERVED	Unused. Writes are ignored and reads are always 0.
8:6	R	SYS_CTRL_PRES_STATE	Stores the SYS_CTRL state for rail B.
5:3	R	TON_CALC_PRES_STATE	Stores the t_{ON} calculation module for rail B.
2:0	R	REF_OUT_PRES_STATE	Stores the state of the VID reference generation module for rail B.

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READ_VCOMP (76h)

Format: Unsigned binary

The READ_VCOMP command on Page 1 stores the DC compensation value for rail B.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Unused. Writes are ignored and reads are always 0.
7:0	R	READ_VCOMP	0.3125mV/LSB.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 1 stores the state of rail B with 1 byte.

Bits	Access	Bit Name	Description
7	R	MASTER_OR_SLAVE	Indicates the PMBus MASTER_SLAVE_SIG flag. 1b'0: Target mode. The controller acknowledges valid PMBus commands 1b'1: Initiator mode. The controller does not acknowledge any command
6	R	OFF	Indicates the power off flag, when V_{OUT} = 0V.
5	R	VOUT_OV_FAULT	Records the over-voltage protection (OVP) fault.
4	R	IOUT_OC_FAULT	Records the over-current protection (OCP) fault.
3	R	VIN_UV_FAULT	Records the V_{IN} under-voltage lockout (UVLO) fault.
2	R	TEMPERATURE	Records the over-temperature protection (OTP) fault.
1	R	CML	Records the communication error fault.
0	R	VOUT_MAX_ WARNING	Records the V_{OUT} max warning flag.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 1 stores status of rail B with 2 bytes.

Bits	Access	Bit Name	Description
15	R	OVP_OR_UVP	Indicates the over-voltage protection (OVP) or under-voltage protection (UVP) flag.
14	R	OCP_OR_CS_OCP_ OR_UVP	Indicates the over-current protection (OCP) or phase OCP and UVP flag.
13:12	R	RESERVED	Fixed to 2'd0.
11	R	VR_SETTLE	Indicates the VR_SETTLE flag.
10:8	R	RESERVED	Fixed to 3'd0.
7	R	MASTER_OR_SLAVE	Indicates the PMBus MASTER_SLAVE_SIG flag. 1b'0: Target mode. The controller acknowledges valid PMBus commands 1b'1: Initiator mode. The controller does not acknowledge any command
6	R	OFF	Indicates the power off flag, when V_{OUT} = 0V.
5	R	VOUT_OV_FAULT	Records the over-voltage protection (OVP) fault.
4	R	IOUT_OC_FAULT	Records the over-current protection (OCP) fault.
3	R	VIN_UV_FAULT	Records the V_{IN} under-voltage lockout (UVLO) fault.
2	R	TEMPERATURE	Records the over-temperature protection (OTP) fault.
1	R	CML	Records the communication error fault.
0	R	VOUT_MAX_ WARNING	Records the V_{OUT} max warning flag.

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STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 1 stores rail B's V_{OUT} status.

Bits	Access	Bit Name	Description
7	R	STATUS_OVP	Indicates the over-voltage protection (OVP) flag status.
6	R	STATUS_OV_FLAG	Indicates the over-voltage (OV) comparator flag status.
5	R	STATUS_UV	Indicates the under-voltage (UV) comparator flag status.
4	R	STATUS_UVP	Indicates the under-voltage protection (UVP) flag status.
3	R	STATUS_VMAX_ WARN	Indicates the VOUT_MAX warning flag status.
2:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 1 stores rail B's I_{OUT} status.

Bits	Access	Bit Name	Description
7	R	STATUS_OCP	Indicates the over-current protection (OCP) flag status.
6	R	STATUS_OC_UVP	Indicates the per-phase OCP and under-voltage protection (UVP) flag status.
5	R	STATUS_OC_LIMIT	Indicates the IMON OCP or the per-phase OCP trig flag status.
4:0	R	RESERVED	Reserved.

READ_VREF_PS (80h)

Format: Unsigned binary

The READ_VREF_PS command on Page 1 stores the PS state and VID reference for rail B.

Bits	Access	Bit Name	Description
15:13	R	RESERVED	Unused. Writes are ignored and reads are always 0.
12	R	VID_STEP_SEL_ FINAL	Indicates the value of internal VID_STEP for rail B (5mV/10mV, considering the VID_STRAP pin and the register setting). 1'b1: 5mV 1'b0: 10mV
11:9	R	PS_STATE	Stores rail B's power stage. 3'b1xx: PS4 3'b011: PS3 3'b010: PS2 3'b001: PS1 3'b000: PS0
8:0	R	SVID_VREF	Stores the VID reference for rail B.

READ_VOUT (8Bh)

Format: Unsigned binary

The READ_VOUT command on Page 1 stores the V_{OUT} report for rail B.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Unused. Writes are ignored and reads are always 0.
9:0	R	READ_VOUT	If VID_STEP = 10mV, 3.125mV/LSB. If VID_STEP = 5mV and the remote-sense gain = 2:1, then 3.125mV/LSB. If VID_STEP = 5mV and the remote-sense gain = 1:1, then 1.5625mV/LSB.

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READ_IOUT (8Ch)

Format: Unsigned binary

The READ_IOUT command on Page 1 stores rail B's I_{OUT} report.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Unused. Writes are ignored and reads are always 0.
11:0	R	READ_IOUT	0.25A/LSB.

PS3_PS4_EXIT_DELAY (95h)

Format: Unsigned binary

The PS3_PS4_EXIT_DELAY command on Page 1 sets the time length for rail B to exit PS3 and PS4. The format is the same as the SVID specifications.

Bits	Access	Bit Name	Description
15:8	R/W	PS3_EXIT_ LATENCY_VR	Sets the time length (in µs) for rail B to exit PS3. The time length is equal to (bits[11:8] of this command) / 16 x 2 ^ (bits[15:12] of this command).
7:0	R/W	PS4_EXIT_ LATENCY_VR	Sets the time length (in µs) for rail B to exit PS4. The time length is equal to (bits[3:0] of this command)/ 16 x 2 ^ (bits[7:4] of this command).

MFR_SR_FAST_TOLERANCE (96h)

Format: Unsigned binary

The MFR_VR_TOLERANCE command on Page 1 sets rail B's output tolerance, the data register containing the rail B fast slew rate capability, and the slew rate that the platform VR can sustain.

Bits	Access	Bit Name	Description
15:8	R/W	MFR_SR_FAST_VR	Returns the fast slew rate that the platform VR supports in binary format. 1mV/µs per LSB.
7:0	R/W	MFR_VR_ TOLERANCE	This data register contains the VR TOB based on the board's parts (e.g. inductor DCR, inductance tolerance, and current-sense errors). 1mV/LSB. (e.g. 13h = ±19mV tolerance budget).

MFR_SVID_06H_34H_VR (97h)

Format: Unsigned binary

The MFR_SVID_06H_34H_VR command on Page 1 sets the MULTI_VR_CONFIG and capability of rail B.

Bits	Access	Bit Name	Description
15:10	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
9:8	R/W	MFR_MULTI_VR_ CONFIG	Sets the initial value of the lower 2 bits of SVID MUTI_VR_CONFIG (34h). The bitmapped data register that configures multiple VRs behavior on the same bus can be configured to reset the behavior of VR_READY under a 0V VID command.
7:0	R/W	CAPABILITY_VR	This is a bitmapped register that identifies the SVID VR capabilities, and which of the optional telemetry registers are supported. 00h indicates that only required registers are supported. Bit[7]: Set to 1 if (15h) is formatted FFh = I_{CCMAX} for VR12.5 and beyond Bit[6]: Temperature ADC (17h) Bit[5]: P_{IN} ADC (1Bh) Bit[4]: V_{IN} ADC (1Ah) Bit[3]: I_{IN} ADC (19h) Bit[2]: P_{OUT} ADC (18h) Bit[1]: V_{OUT} ADC (16h) Bit[0]: I_{OUT}/J_{OUT} ADC format (15h)

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MFR_SVID_OFFSET (9Ah)

Format: Unsigned binary

The MFR_SVID_OFFSET command on Page 1 sets the default value of offset of SVID-VID and enables the SVID function

Bits	Access	Bit Name	Description
15:9	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
8	R/W	MFR_SVID_ OFFSET_INIT_R2	Enables the SVID function for rail B. 1'b1: Enabled 1'b0: Disabled
7:0	R/W	MFR_SVID_RAIL_ EN_R2	Sets the default value of the SVID-VID offset.

MFR_BLANK_TIME (A3h)

Format: Unsigned binary

The MFR_BLANK_TIME command on Page 1 sets the minimum PWM phase time for rail B.

Bits	Access	Bit Name	Description
15:5	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
4:0	R/W	MFR_BLANK_TIME	Sets the blanking time, calculated with the following equation: (MFR_BLANK_TIME + 3) x 10ns

MFR_PSI_TRIM4 (B0h)

Format: Unsigned binary

The MFR_PSI_TRIM4 command on Page 1 sets rail B's slope compensation value of in DCM, PS1, PS2, and PS3.

Bits	Access	Bit Name	Description
15	R/W	RESERVED	Unused. Writes are ignored and reads are always 0.
14:10	R/W	MFR_TRIM_ SETPS2_3	Sets the slope output compensation in PS2 and PS3. 2.5mV/LSB.
9:5	R/W	MFR_TRIM_SETPS1	Sets the slope output compensation in PS1. 2.5mV/LSB.
4:0	R/W	MFR_TRIM_DCM	Sets the slope output compensation in DCM. 2.5mV/LSB.

CLEAR_EEPROM_FAULTS (FEh)

Format: Unsigned binary

The CLEAR_EEPROM_FAULTS command on Page 1 clears the EEPROM fault bits. If no protection remains after this command is sent, the VR starts ramping and outputs power.

This command is write-only. There is no data byte for this command.

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TYPICAL APPLICATION CIRCUIT

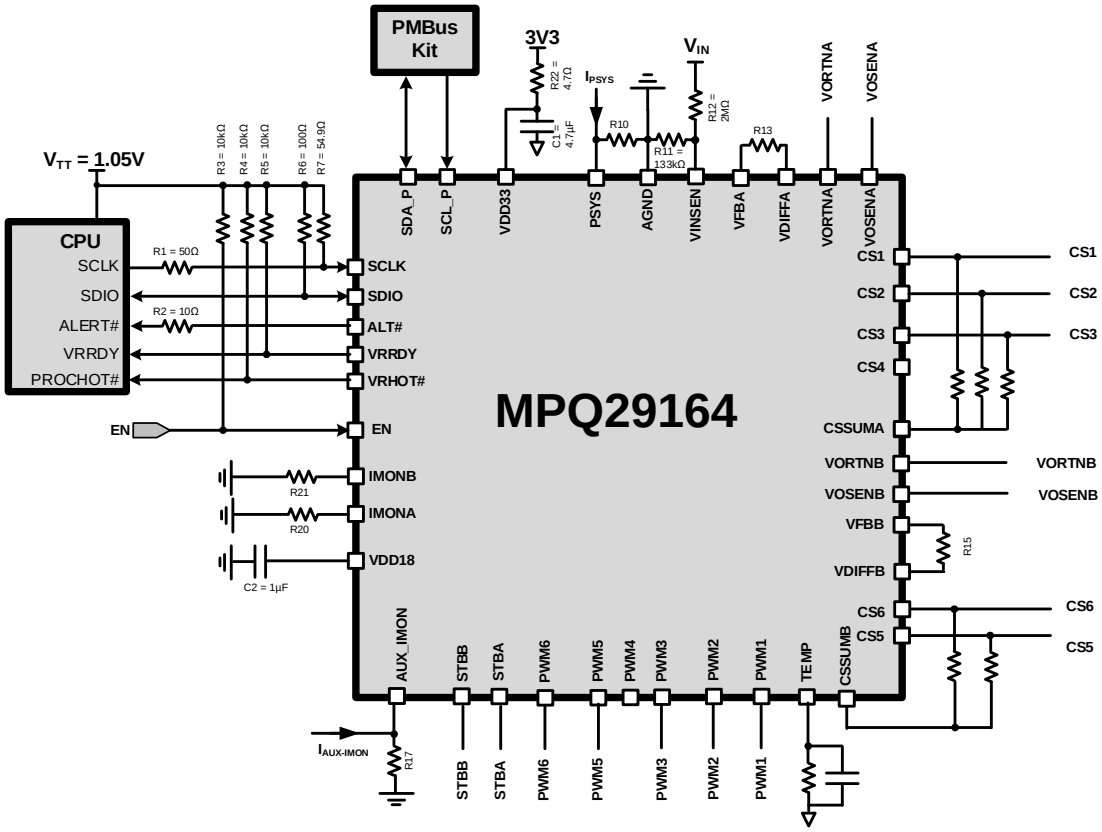

Figure 21: Typical Application Circuit

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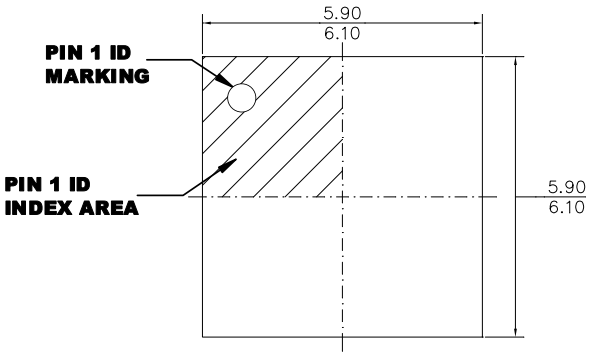
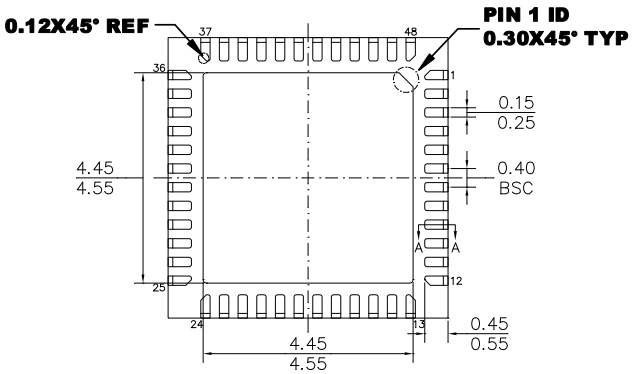
PACKAGE INFORMATION

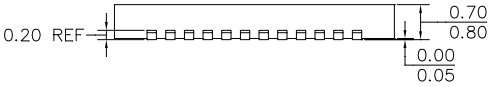
TQFN-48 (6mmx6mm)
Wettable Flank



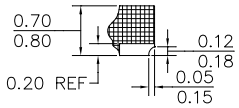
TOP VIEW



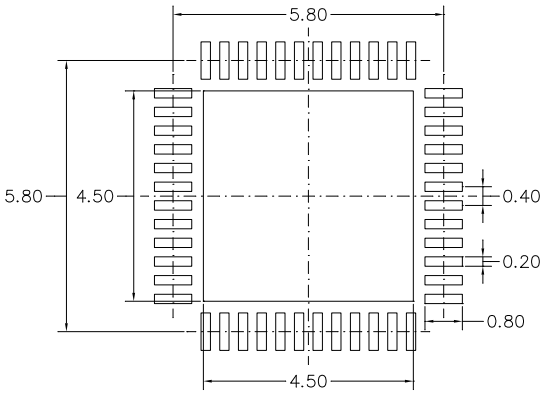
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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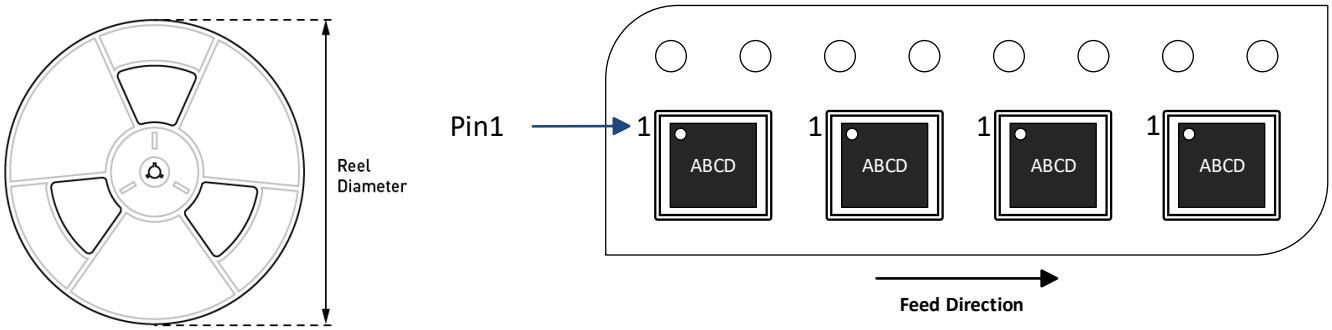
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ29164GQKTE-xxxx-AEC1-Z	TQFN-48 (6mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/23/2025	Initial Release	-

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