MPQ2420-AEC1

75V, 0.3A, Synchronous Step-Down Converter with Watchdog AEC-Q100 Qualified

DESCRIPTION

The MPQ2420 is a step-down switching regulator with integrated high- and low-side, high-voltage power MOSFETs. It provides a highly efficient output of up to 0.3A. The integrated watchdog adds additional security redundancy to the system.

The wide 4.5V to 75V input range accommodates a variety of step-down applications in an automotive environment. A 5µA shutdown mode quiescent current in a full temperature range is ideal for battery-powered applications. It allows for high-power conversion efficiency over a wide load range by scaling down the switching frequency under a light-load condition to reduce switching and gate driver losses. The start-up switching frequency and short circuit can also be scaled down to prevent inductor current runaway.

Full protection features include under-voltage lockout (UVLO) and thermal shutdown. Thermal shutdown provides reliable, fault-tolerant operation.

The MPQ2420 is available in a TSSOP-16 EP package.

FEATURES

- 20µA Quiescent Current for Buck Only
- Wide 4.5V to 75V Operating Input Range (80V ABS MAX)
- 1.2Ω/0.45Ω Internal Power MOSFETs
- Programmable Soft Start
- FB Tolerance: 1% at Room Temperature, 2% at Full Temperature
- Adjustable Output Voltage
- Integrated Window Watchdog
- Power-On Reset during Power-Up
- Under-Voltage Lockout and Thermal Shutdown
- Programmable Short Window Mode or Long Window Mode
- Low Shutdown Mode Current of 5µA
- TSSOP-16 EP Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery-Powered Systems

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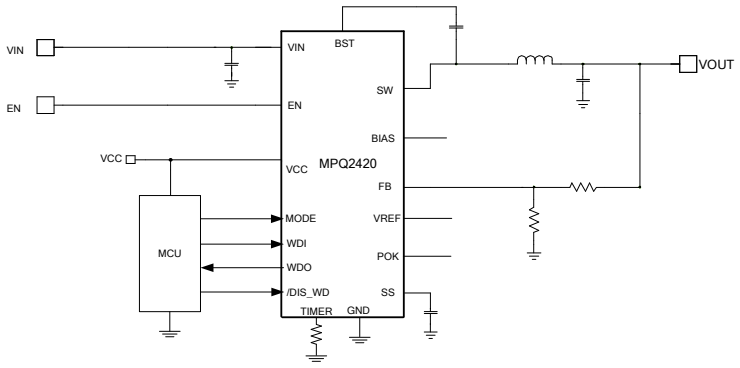
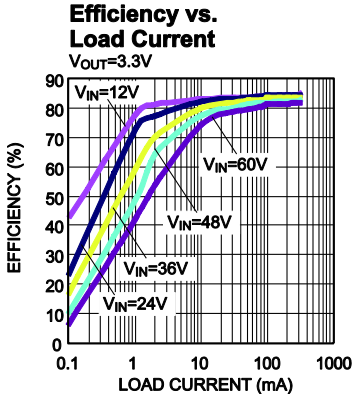
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ2420GF	TSSOP-16 EP	*See Below*
MPQ2420GF-AEC1		

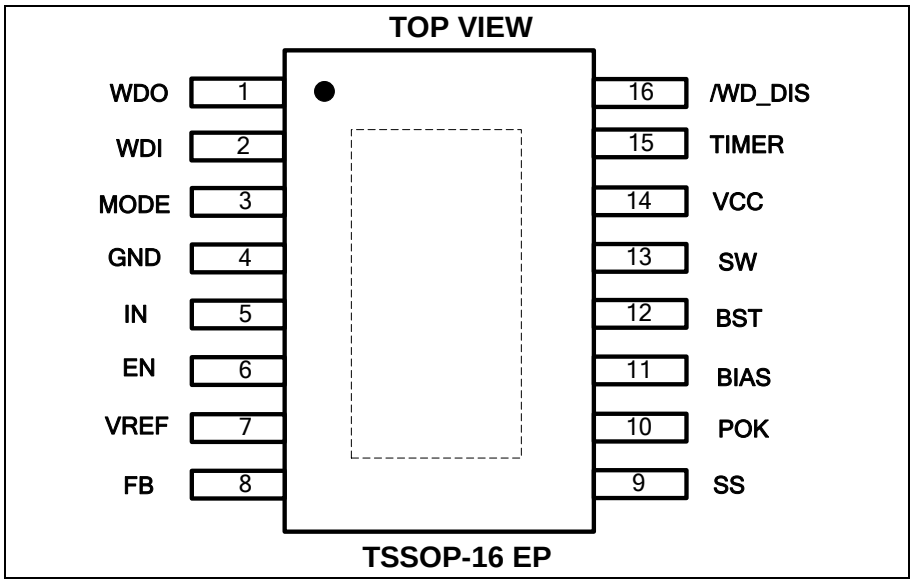
* For Tape & Reel, add suffix –Z (e.g. MPQ2420GF–Z)

TOP MARKING

MPSYYWW
MP2420
LLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2420: Part code of MPQ2420GF
LLLLLL: Lot number

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) …… ..... -0.3V to +80V
Switch voltage (V_{SW}) …… …….-0.3V to V_{IN} + 1V
BST to SW…… ……-0.3 to +6.0V
All other pins…….. ……-0.3V to +6.0V
EN sink current…… .....……150μA
Continuous power dissipation (T_A = +25°C) (2)
TSSOP-16 EP……...….2.7W
Junction temperature……..……150°C
Lead temperature …… .....……260°C
Storage temperature…….-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN})…… ..... 4.5V to 75V
Output voltage (V_{OUT})……1V to 0.9×V_{IN}
Operating junction temp. (T_J) ..... -40°C to 125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP-16 EP ……..……..45…….10…°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{EN} = 2V, V_{CC} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
DC/DC Converter					
Supply quiescent current	No load, V_{FB} = 1.2V		20	30	µA
Shutdown supply current	V_{EN} < 0.3V		2.2	5	µA
V_{IN} UVLO rising threshold		3.9	4.2	4.4	V
V_{IN} UVLO falling threshold		3.45	3.75	3.95	
V_{IN} UVLO hysteresis			0.45		V
Feedback voltage	V_{IN} = 4.5V to 75V, T_J = 25°C	0.99	1.0	1.01	V
	V_{IN} = 4.5V to 75V	0.98		1.02	V
Feedback current	V_{FB} = 1.2V	-50	2	50	nA
V_{REF} voltage	V_{IN} = 4.5V to 75V, I_{REF} = 100µA	0.965	1	1.035	V
Upper switch-on resistance	V_{BST} - V_{SW} = 5V, T_J = 25°C	0.9	1.2	1.5	Ω
	V_{BST} - V_{SW} = 5V	0.7		2.5	Ω
Lower switch-on resistance	V_{BIAS} = 5V, T_J = 25°C	0.275	0.45	0.625	Ω
	V_{BIAS} = 5V	0.2		0.9	Ω
Lower switch leakage	V_{EN} = 0V, V_{SW} = 75V			1	µA
Peak current limit		630	720	810	mA
Minimum switch-on time(5)			120		ns
Enable rising threshold		1.25	1.55	1.85	V
Enable falling threshold		1.152	1.2	1.248	V
Enable threshold hysteresis			0.35		V
Enable current	V_{EN} = 2.4V		0.8		µA
Soft-start current		4	5.5	7	µA
POK upper trip threshold	FB respect to the nominal value	86	90	94	%
POK lower trip threshold	FB respect to the nominal value	81	85	89	%
POK threshold hysteresis	FB respect to the nominal value		5		%
POK deglitch timer			40		µs
POK output voltage low	I_{SINK} = 1mA			0.4	V
FB OVP rising threshold			1.05	1.1	V
FB OVP hysteresis			50		mV
Thermal shutdown(5)			175		°C
Thermal shutdown hysteresis(5)			20		°C

NOTE:

5) Derived from bench characterization. Not tested in production.

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 2V, V_{CC} = 5V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Watchdog Power Supply						
Timer voltage		R_{TIMER} = 51k		0.3		V
Quiescent current	I_Q	R_{TIMER} = 100k		16	19	µA
		R_{TIMER} = 51k		25	32	µA
Power-on reset threshold	$V_{POR-HIGH}$	WDO goes high with rising V_{CC}	4.4	4.6	4.8	V
	$V_{POR-LOW}$	WDO goes low with falling V_{CC}	4.3	4.5	4.7	V
Watchdog Timing						
Single period	T	R_{TIMER} = 51k	-10%	880	+10%	µs
Power-on delay(6)	t_0	R_{TIMER} = 51k		10		cycle
Sync signal monitoring time(6)	t_1	R_{TIMER} = 51k		450		cycle
Watchdog window close time (short mode) (6)	t_2	R_{TIMER} = 51k, mode = low		15		cycle
Watchdog window open time (short mode) (6)	t_3	R_{TIMER} = 51k, mode = low		10		cycle
Watchdog window close time (long mode) (6)	t_4	R_{TIMER} = 51k, mode = high		1500		cycle
Watchdog window open time (long mode) (6)	t_5	R_{TIMER} = 51k, mode = high		1000		cycle
WDO reset pulse width(6)	t_6	R_{TIMER} = 51k		4		cycle
WDI_OK pulse width			10		5000	µs
Watchdog Input and Output						
WDI logic high			3.2			V
WDI logic low					0.8	V
MODE logic high			3.2			V
MODE logic low					0.8	V
MODE input current		MODE = 5V		0.1	1	µA
		MODE = 0V		5	8	µA
/WD_DIS logic high			3.2			V
/WD_DIS logic low					0.8	V
/WD_DIS input current		WD_DIS = 5V		0.1	1	µA
		WD_DIS = 0V		5	8	µA
WDO high		VCC = 5V, I_{WDO} = 1mA	V_{CC}-0.2			V
WDO low		VCC = 5V, I_{WDO} = 1mA			0.2	V
		VCC = 1V, I_{WDO} = 300µA			0.1	V

NOTE:

6) Guaranteed by design.

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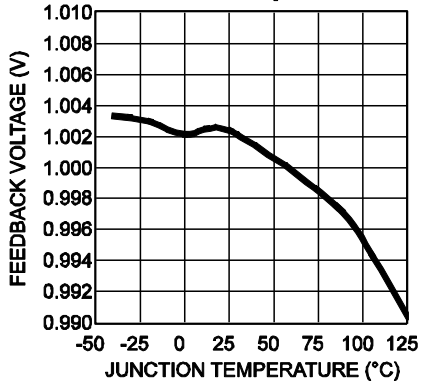
TYPICAL CHARACTERISTICS

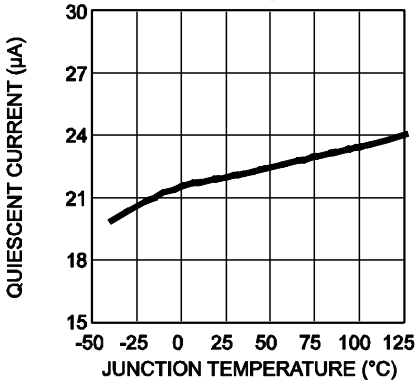
DC/DC Converter

V_{IN} = 12V, unless otherwise noted.

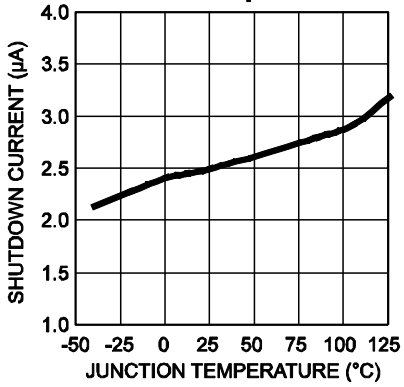
Feedback Voltage vs. Junction Temperature



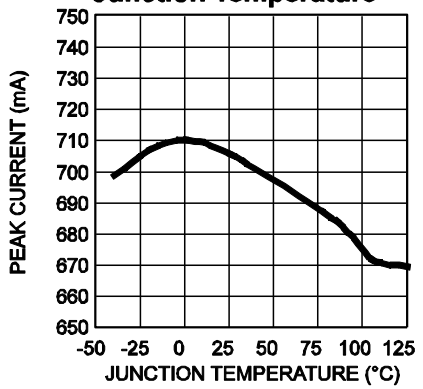
Quiescent Current vs. Junction Temperature



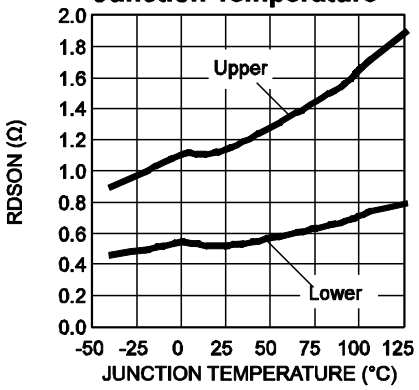
Shutdown Current vs. Junction Temperature



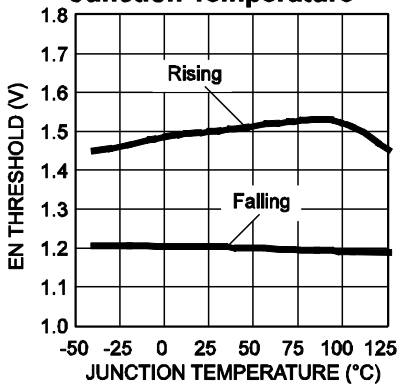
Current Limit vs. Junction Temperature



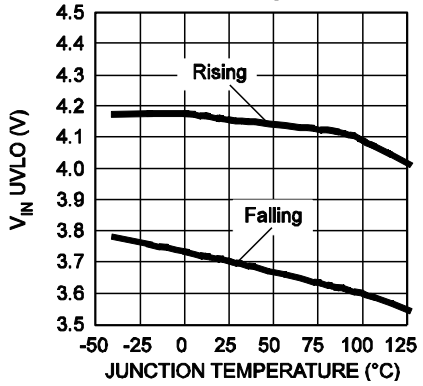
Switch On Resistance vs. Junction Temperature



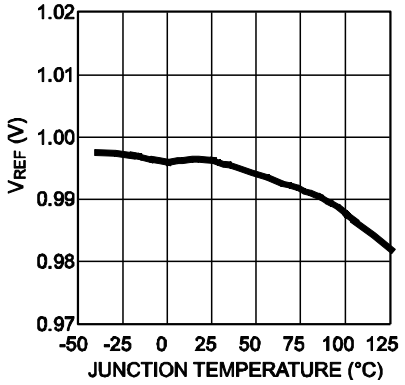
EN Threshold vs. Junction Temperature



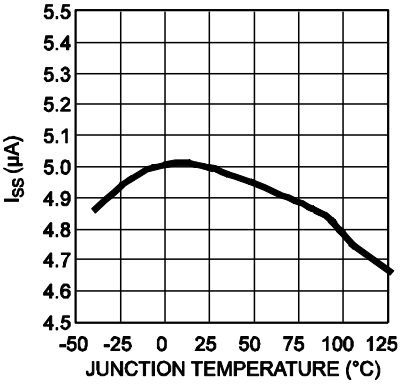
V_{IN} UVLO vs. Junction Temperature



V_{REF} vs. Junction Temperature



I_{SS} vs. Junction Temperature



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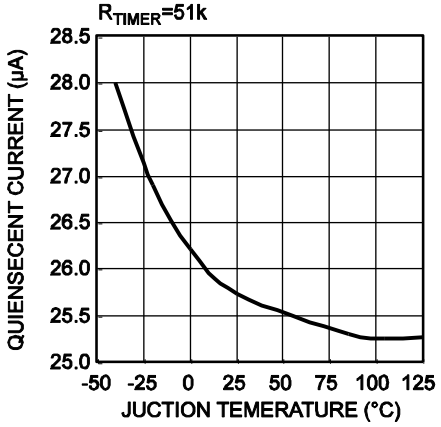
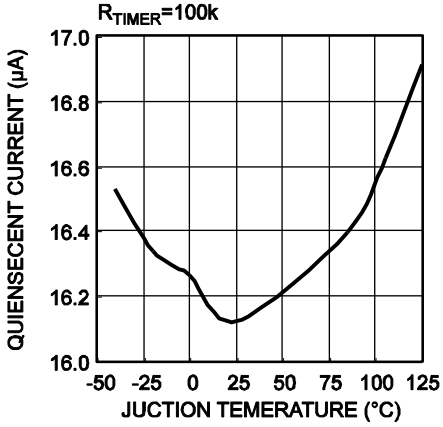
TYPICAL CHARACTERISTICS *(continued)*

Watchdog

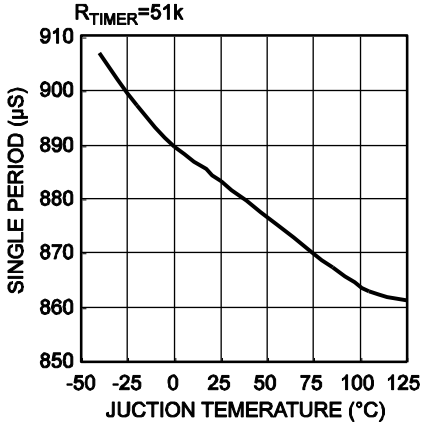
Quiescent Current vs. Junction Temerature



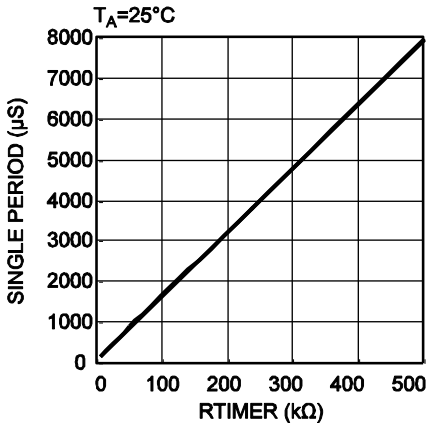
Quiescent Current vs. Junction Temerature



Single Period vs. Junction Temerature



Single Period vs. RTIMER



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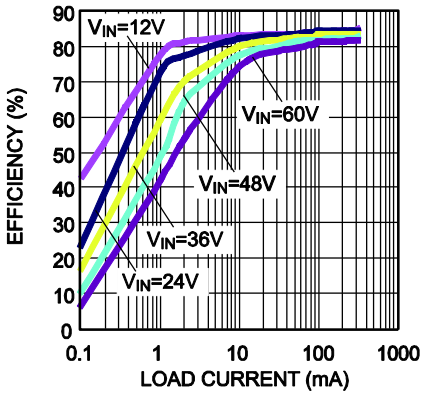
TYPICAL PERFORMANCE CHARACTERISTICS

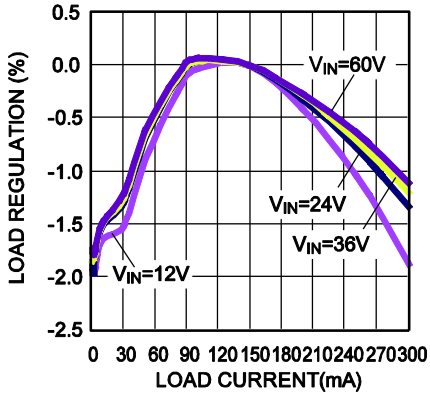
DC/DC Converter

V_{IN} = 12V, V_{OUT} = 3.3V, L = 33µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

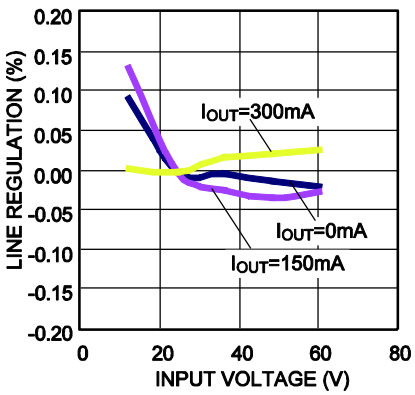
Efficiency vs. Load Current



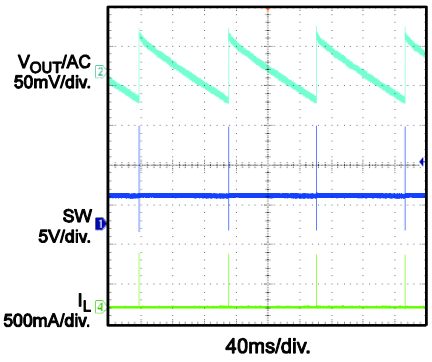
Load Regulation



Line Regulation



Steady State
I_{OUT}=0A



Steady State
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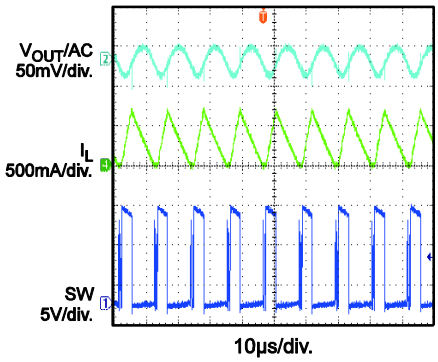
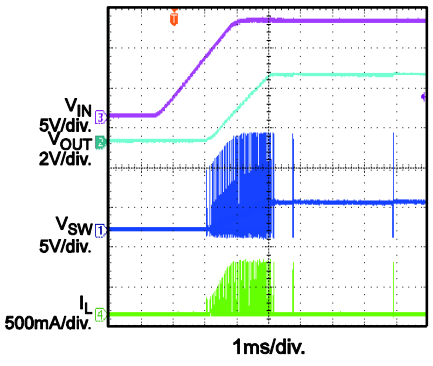
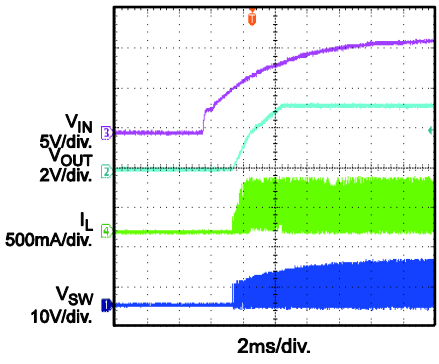


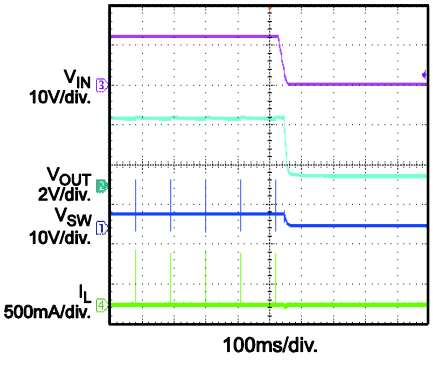
Start-Up through V_{IN}
I_{OUT} = 0A



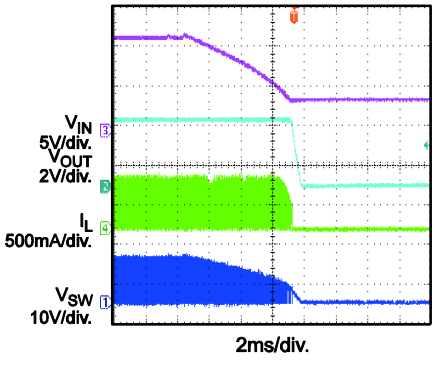
Start-Up through V_{IN}
I_{OUT} = 0.3A



Shutdown through V_{IN}
I_{OUT} = 0A



Shutdown through V_{IN}
I_{OUT} = 0.3A



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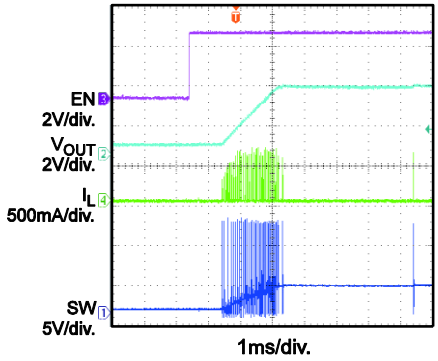
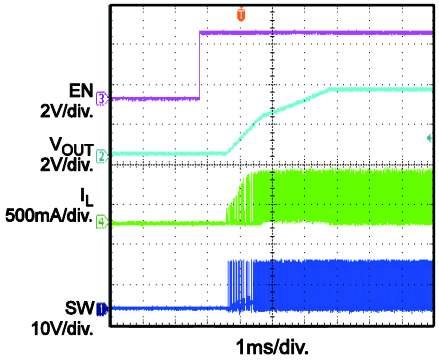
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 33µH, C_{OUT} = 2x22µF, T_A = 25°C, unless otherwise noted.

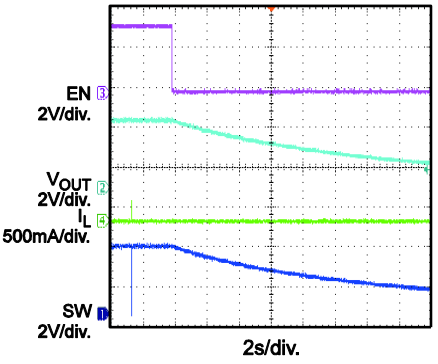
Start-Up through EN
I_{OUT} = 0A



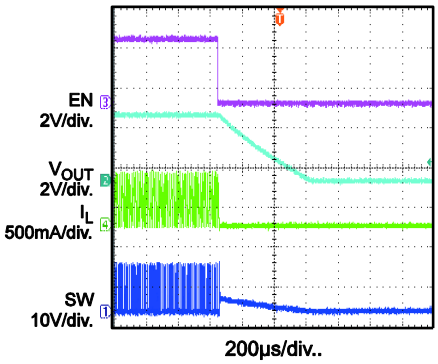
Start-Up through EN
I_{OUT} = 0.3A



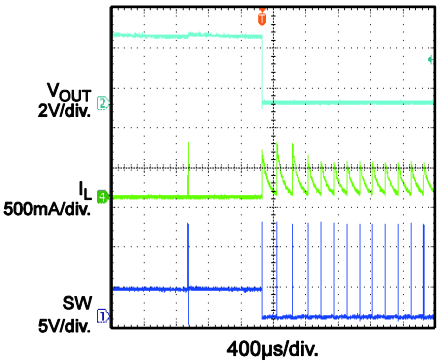
Shutdown through EN
I_{OUT}=0A



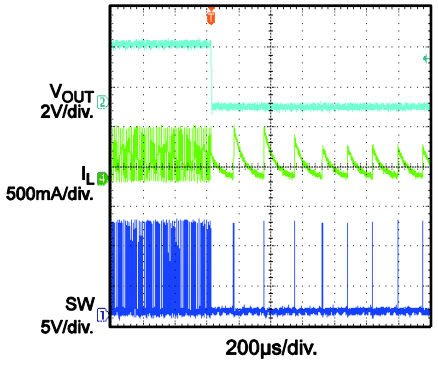
Shutdown through EN
I_{OUT}=0.3A



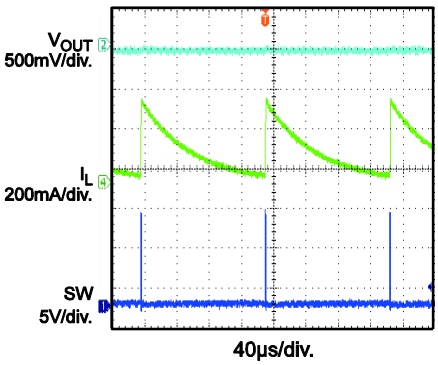
SCP Entry
I_{OUT}=0A to Short Circuit



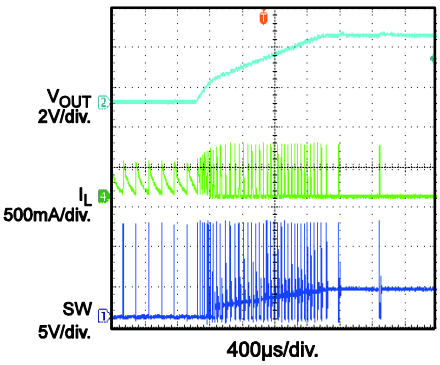
SCP Entry
I_{OUT}=0.3A to Short Circuit



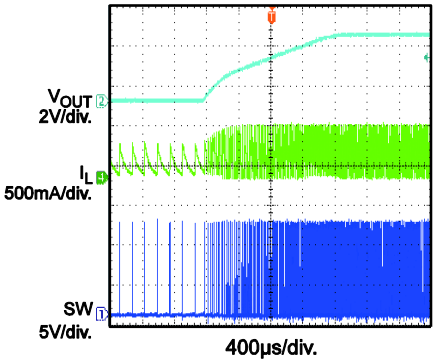
SCP Steady State



SCP Recovery
Short Circuit to I_{OUT}=0A



SCP Recovery
Short Circuit to I_{OUT}=0.3A



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PIN FUNCTIONS

Pin #	Name	Description
Watchdog		
1	WDO	**Watchdog output.** WDO outputs the reset signal to MCU.
2	WDI	**Watchdog input.** WDI receives the trigger signal from MCU.
3	MODE	**Mode switching.** Pull MODE high to make the watchdog work in a long window mode. Pull MODE low to make the watchdog work in a short window mode. MODE has a weak internal pull-up.
4	GND	**Ground.** Connect GND as close as possible to the output capacitor to avoid high-current switch paths.
14	VCC	**Power input.**
15	TIMER	**Watchdog timer.** Set the time out with an external resistor
16	/WD_DIS	**Watchdog disable.** Pull /WD_DIS low to disable the watchdog. Pull /WD_DIS high to enable the watchdog. /WD_DIS has a weak internal pull-up.
DC/DC		
4	GND	**Ground.** Same as GND in Watchdog.
5	IN	**Input supply.** IN requires a decoupling capacitor connected to ground to reduce switching spikes.
6	EN	**Enable input.** Pull EN below the low threshold to shut the chip down. Pull EN above the high threshold to enable the chip. Float EN to disable the chip.
7	VREF	**Reference voltage output.**
8	FB	**Feedback input to the error amplifier (QFN-10 3mmx3mm package only).** Connect FB to the tap of an external resistive divider between the output and GND. FB sets the regulation voltage when compared to the internal 1V reference.
9	SS	**Soft-start control input.** Connect a capacitor from SS to GND to set the soft-start period.
10	POK	**Open-drain power-good output.** A high output indicates that V_{OUT} is higher than 90% of the reference. POK is pulled down during shutdown.
11	BIAS	**Controller bias input.** BIAS supplies current to the internal circuit when V_{BIAS} > 2.9V and provides a feedback input for the SOIC8E package, which has a fixed output only.
12	BST	**Bootstrap.** BST provides a positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between BST and SW.
13	SW	**Switch node.**
	Exposed Pad	**Connect exposed pad to GND plane for optimal thermal performance.**

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FUNCTIONAL BLOCK DIAGRAM

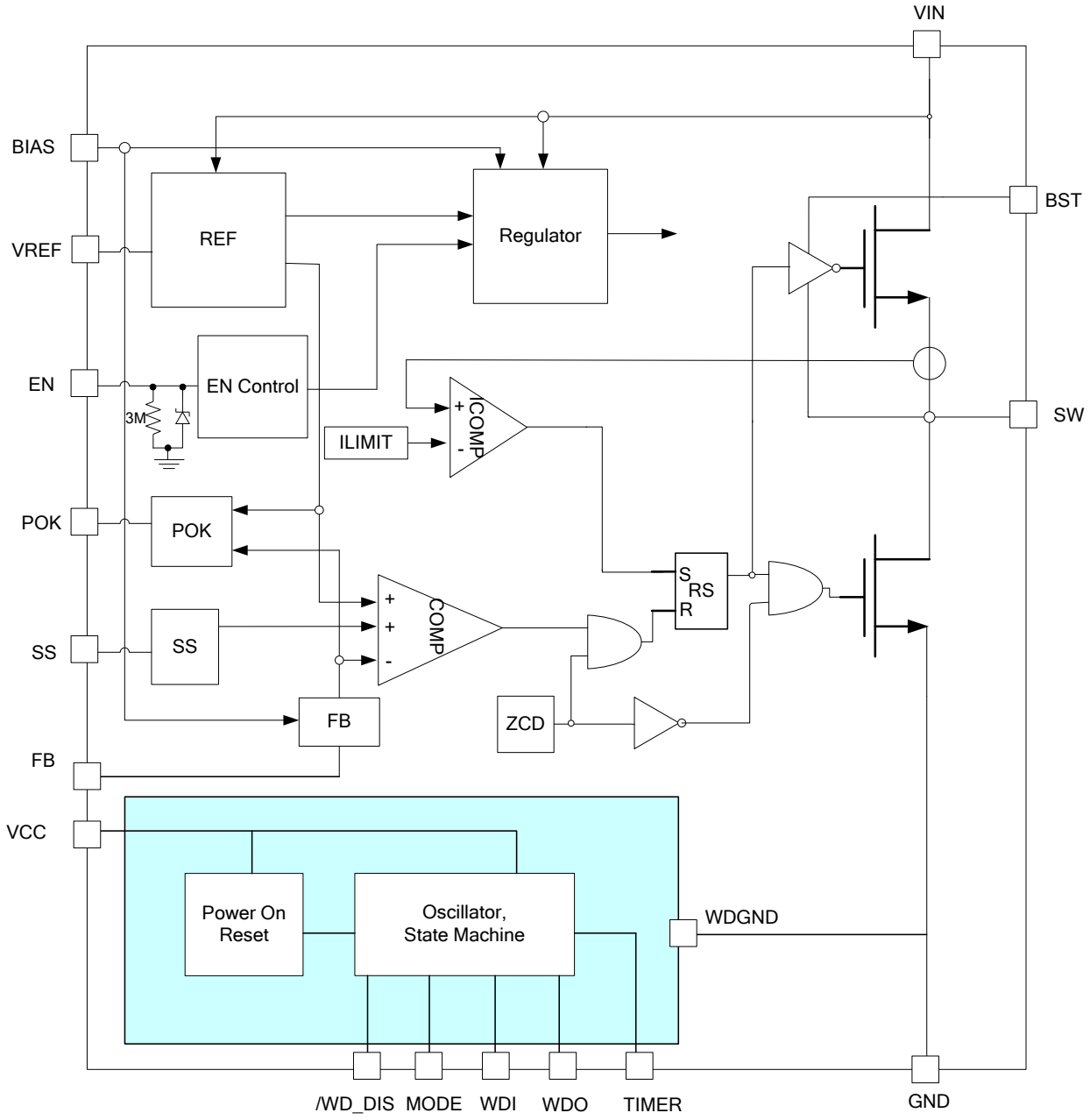

Figure 1: Functional Block Diagram

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DC/DC OPERATION

The MPQ2420 is a 75V, 0.3A, synchronous, step-down, switching regulator with integrated high-side and low-side, high-voltage power MOSFETs (HS-FET and LS-FET, respectively). It provides a highly efficient 0.3A output and features a wide input voltage range, external soft-start control, and precision current limit. It has a very low operational quiescent current, making it suitable for battery-powered applications.

Control Scheme

The ILIM comparator, FB comparator, and zero current detector (ZCD) block control of the PWM (see Figure 2). If V_{FB} is below the 1V reference and the inductor current drops to zero, the HS-FET turns on, and the ILIM comparator begins sensing the HS-FET current. When the HS-FET current reaches its limit, the HS-FET turns off, and the LS-FET and the ZCD block turn on. The ILIM comparator turns off to reduce the quiescent current. The LS-FET and the ZCD block turn off after the inductor current drops to zero. If V_{FB} is below the 1V reference, the HS-FET turns on and begins another cycle. If V_{FB} remains higher than the 1V reference, the HS-FET remains off until V_{FB} drops below 1V.

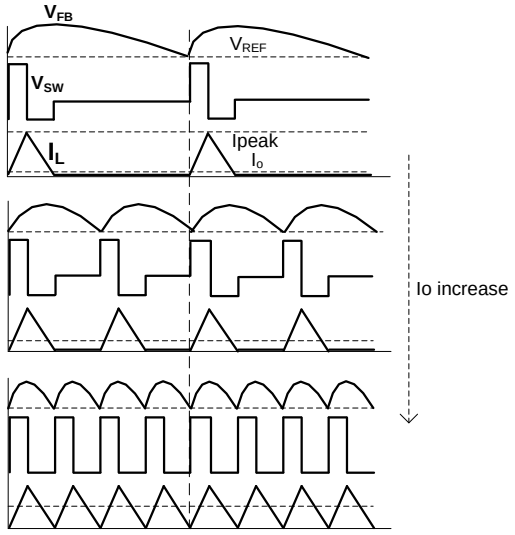

Figure 2: Control Scheme

Internal Regulator and BIAS

The 2.6V internal regulator powers most of the internal circuitry. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} is greater than 3.0V, the output of the regulator is in full regulation. Lower values of V_{IN} result in lower output voltages. When V_{BIAS} > 2.9V, the BIAS supply overrides the input voltage and supplies power to the internal regulator. When V_{BIAS} > 4.5V, BIAS powers the LS-FET driver. Using BIAS to power the internal regulators improves efficiency. It is recommended to connect BIAS to the regulated output voltage when it is in the 2.9V to 5.5V range. When the output voltage is out of this range, BIAS can be powered using an external supply of >2.9V to >4.5V.

Enable Control (EN)

The MPQ2420 has a dedicated enable control (EN). When V_{IN} goes high, EN enables and disables the chip (high logic). Its falling threshold is a consistent 1.2V, and its rising threshold is about 350mV. When floating, EN is pulled down internally to GND to disable the chip.

When EN = 0V, the chip enters the lowest shutdown current mode. When EN is higher than zero, but lower than its rising threshold, the chip remains in shutdown mode with a slightly larger shutdown current.

A Zener diode is connected internally from EN to GND. The typical clamping voltage of the Zener diode is 6.5V. V_{IN} can be connected to EN through a high ohm (Ω) resistor if the system does not have another logic input acting as an EN signal. The resistor must be designed to limit the EN sink current to less than 150μA. Since there is an internal 3M resistor from EN to GND, the external pull-up resistor should be smaller than $\frac{[V_{IN(MIN)} - 1.55V] \times 3M}{1.55V}$ to ensure that EN can turn on at the lowest operational V_{IN}.

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Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating below the operational supply voltage range. The UVLO rising threshold is about 4.2V while its falling threshold is about 3.75V.

Soft Start (SS)

The MPQ2420 employs a soft-start (SS) mechanism to prevent the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a constant current to charge an external soft-start capacitor. The SS voltage ramps up slowly from 0V at a slow pace set by the SS time. When V_{SS} is less than V_{REF}, V_{SS} overrides V_{REF}, and the FB comparator uses V_{SS} as the reference instead of V_{REF}. When V_{SS} is higher than V_{REF}, V_{REF} resumes control.

V_{SS} can be much smaller than $V_{FB,}$ but it can only barely exceed V_{FB}. If V_{FB} drops, V_{SS} tracks V_{FB}. This function prevents an output voltage overshoot during short-circuit recovery. When the short circuit is removed, a new SS process ramps up.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed its upper threshold, the entire chip shuts down. When the temperature falls below its lower threshold, the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating HS-FET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is about 2.4V with a hysteresis of about 300mV. During the UVLO, the SS voltage resets to zero. When the UVLO is disabled, the regulator follows the soft-start process.

The dedicated internal bootstrap regulator charges and regulates the bootstrap capacitor to about 5V. When the voltage difference between BST and SW falls below its working parameters, a PMOS pass transistor connected from V_{IN} to BST turns on to charge the bootstrap capacitor. The current path runs from V_{IN} to BST to SW. The external circuit must have enough voltage headroom to accommodate charging.

If V_{IN} is sufficiently higher than SW, the bootstrap capacitor charges. When the HS-FET is on, V_{IN} is about equal to SW, and the bootstrap capacitor cannot charge. The optimal charging period occurs when the LS-FET is on and V_{IN} - V_{SW} is at its largest. V_{SW} is equal to V_{OUT} when there is no current in the inductor. The difference between V_{IN} and V_{OUT} charges the bootstrap capacitor.

If the internal circuit does not have sufficient voltage and time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage operates in its normal region.

Start-Up and Shutdown

If both V_{IN} and V_{EN} are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

If the internal supply rail is high, an internal timer keeps the power MOSFET off for about 50µs to clear any start-up glitches. When the soft-start block is enabled, the SS output is held low and ramps up slowly.

Three events can shut down the chip: V_{EN} low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The internal supply rail is then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power OK (POK)

POK is an open-drain power good output. A high output indicates that V_{OUT} is higher than 90% of its nominal value. POK is pulled down in shutdown mode.

Reference Voltage Output (V_{REF})

V_{REF} has an output reference voltage of 1V. It has up to 500µA of source current capability.

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WATCHDOG OPERATION

Supply Voltage

A supply voltage of V_{CC} = 5V +/-10% is recommended for normal operation. WDO is pulled low when V_{CC} rises to 1V or higher. When V_{CC} rises to 4.65V, WDO remains at a low level for t_0 to reset the MCU.

Timer

Calculate Period T (μs) with Equation (1):

$$T(\mu s) = 15.75 \times R_{TIMER}(k\Omega) + 73.5 \quad (1)$$

Calculate R_{TIMER} (kΩ) with Equation (2):

$$R_{TIMER}(k\Omega) = 0.063 \times T(\mu s) - 4.67 \quad (2)$$

For example, if R_{TIMER}=51kΩ, then T≈0.88ms.

Monitor MCU Synchronization Signal

When the watchdog is in a sync signal monitoring state, the watchdog IC receives a WDI_OK signal from the MCU within t_1, the timer resets and the watchdog enters normal operation (WDI remains low for 10μs to 5ms). If the watchdog does not receive the WDI_OK signal from the MCU during t_1, it generates a reset signal and enters the sync signal monitoring state again.

Short Window Mode

When the MCU and watchdog are synchronized correctly and MODE is low, the watchdog operates in short window mode if WDI_OK is received in a window close state (t_2). The watchdog then outputs a reset signal and enters the sync signal monitoring state.

If WDI_OK is received in a window open state (t_3), the watchdog enters a window close state. The MCU is in normal operation in this situation.

If WDI_OK is not received in t_2+t_3, the watchdog outputs a reset signal and enters the sync signal monitoring state.

MODE is pulled high during the short window mode, and the watchdog enters a long window mode.

Long Window Mode

When the MCU and watchdog are synchronized correctly and MODE is high, the watchdog works in a long window mode if WDI_OK is received in a window close state (t_4). The watchdog then outputs a reset signal and enters the sync signal monitoring state.

If WDI_OK is received in a window open state (t_5), the watchdog enters a window close state. The MCU is in normal operation in this situation.

If WDI_OK is not received in t_4+t_5, the watchdog then outputs a reset signal and enters the sync signal monitoring state.

MODE is pulled low during a long window mode, and the watchdog then enters a short window mode.

Watchdog Disable

Pull /WD_DIS low to disable the watchdog. Pull /WD_DIS high to enable the watchdog. It has a weak internal pull-up so leaving /WD_DIS open enables the watchdog.

WDI Error

The WDI signal remaining at a low level for longer than the max WDI_OK pulse width is regarded as an error. When this error occurs, WDO is pulled down until WDI rises to a high level again.

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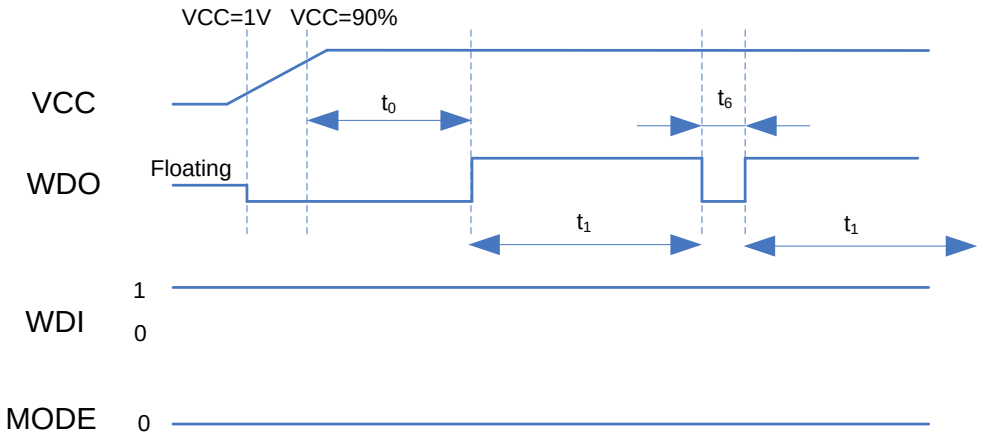
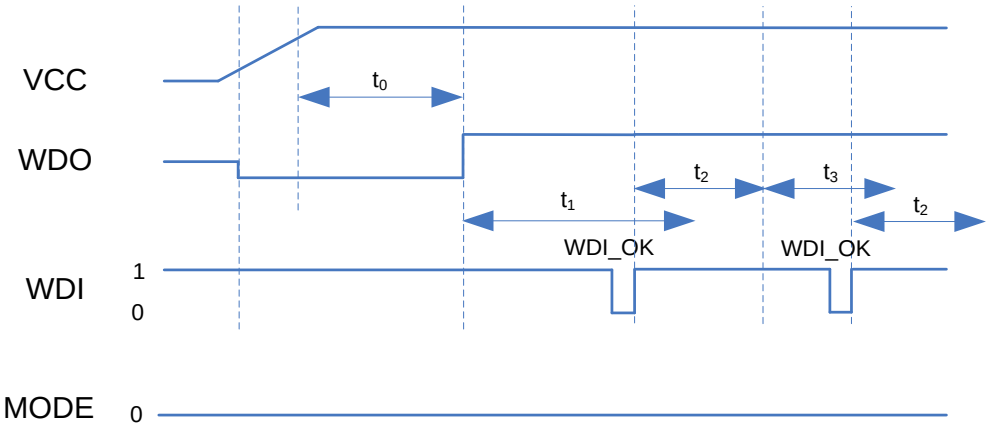
TIMING DIAGRAM

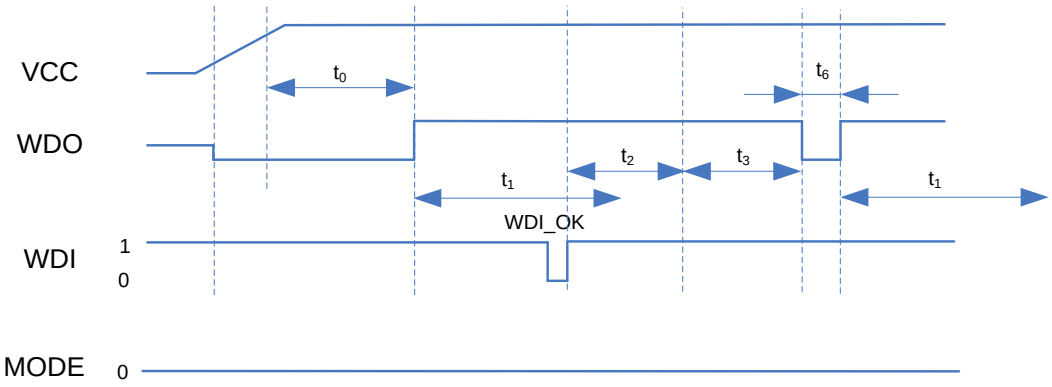
Power-On Reset and No-Sync Signal



Synchronized by WDI and Triggered in Open Window (MODE=0, Short Window Mode)



Synchronized by WDI and No-Trigger Signal (MODE=0, Short Window Mode)



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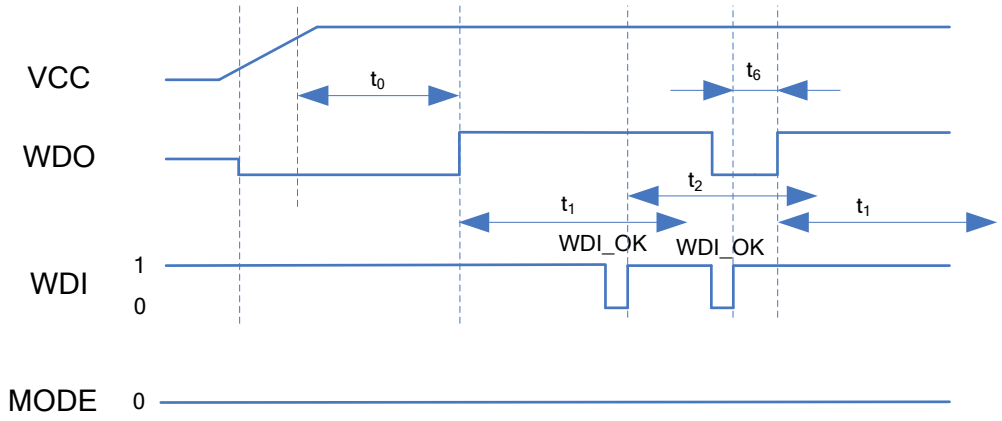
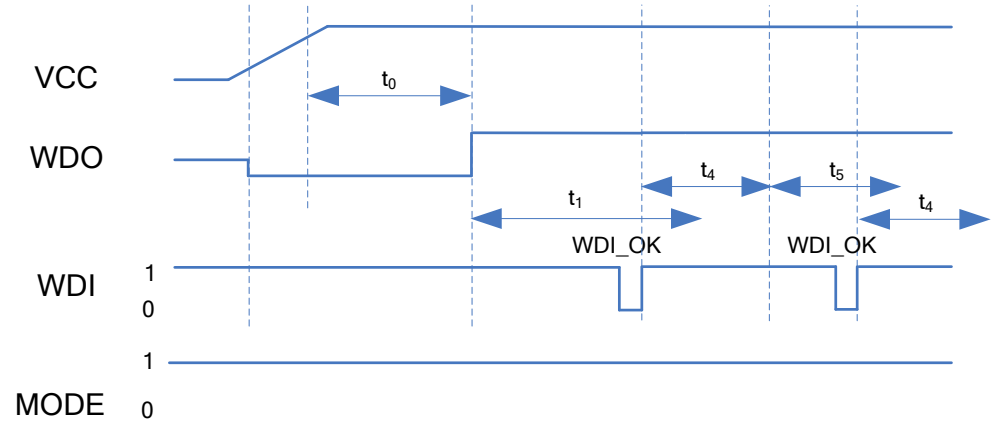
Synchronized by WDI and Triggered in Closed Window (MODE=0, Short Window Mode)

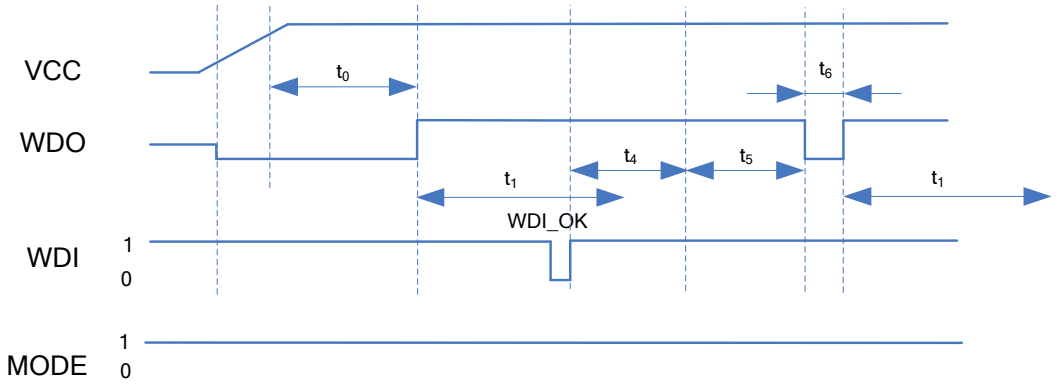


NOTE: When the WDI_OK rising edge approaches WDO when it is low, the t_6 timer resets. In the above situation, the WDO reset signal keeps a t_6+WDI_OK time.

Synchronized by WDI and Triggered in Open Window (MODE=1, Long Window Mode)



Synchronized by WDI and No-Trigger Signal (MODE=1, Long Window Mode)



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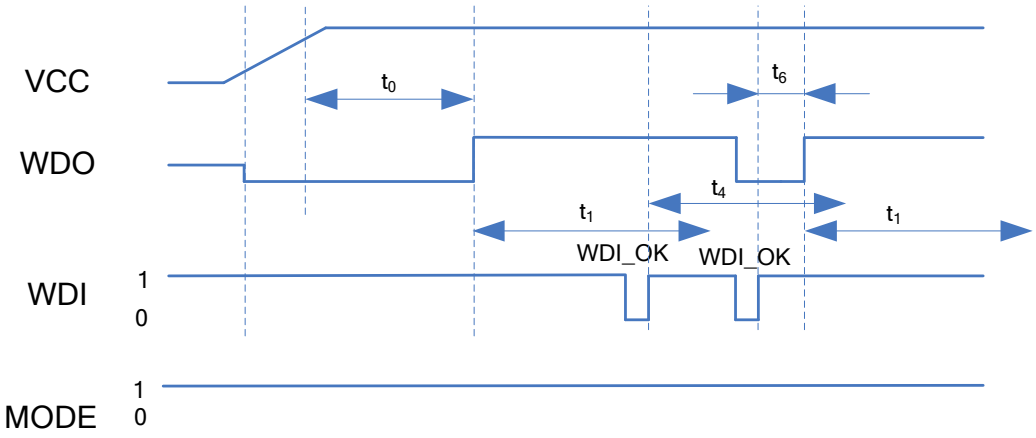
Synchronized by WDI and Triggered in Closed Window (MODE=1, Long Window Mode)



NOTE: When the WDI_OK rising edge approaches WDO when it is low, the t_6 timer resets. In the above situation, the WDO reset signal keeps a t_6+WDI_OK time.

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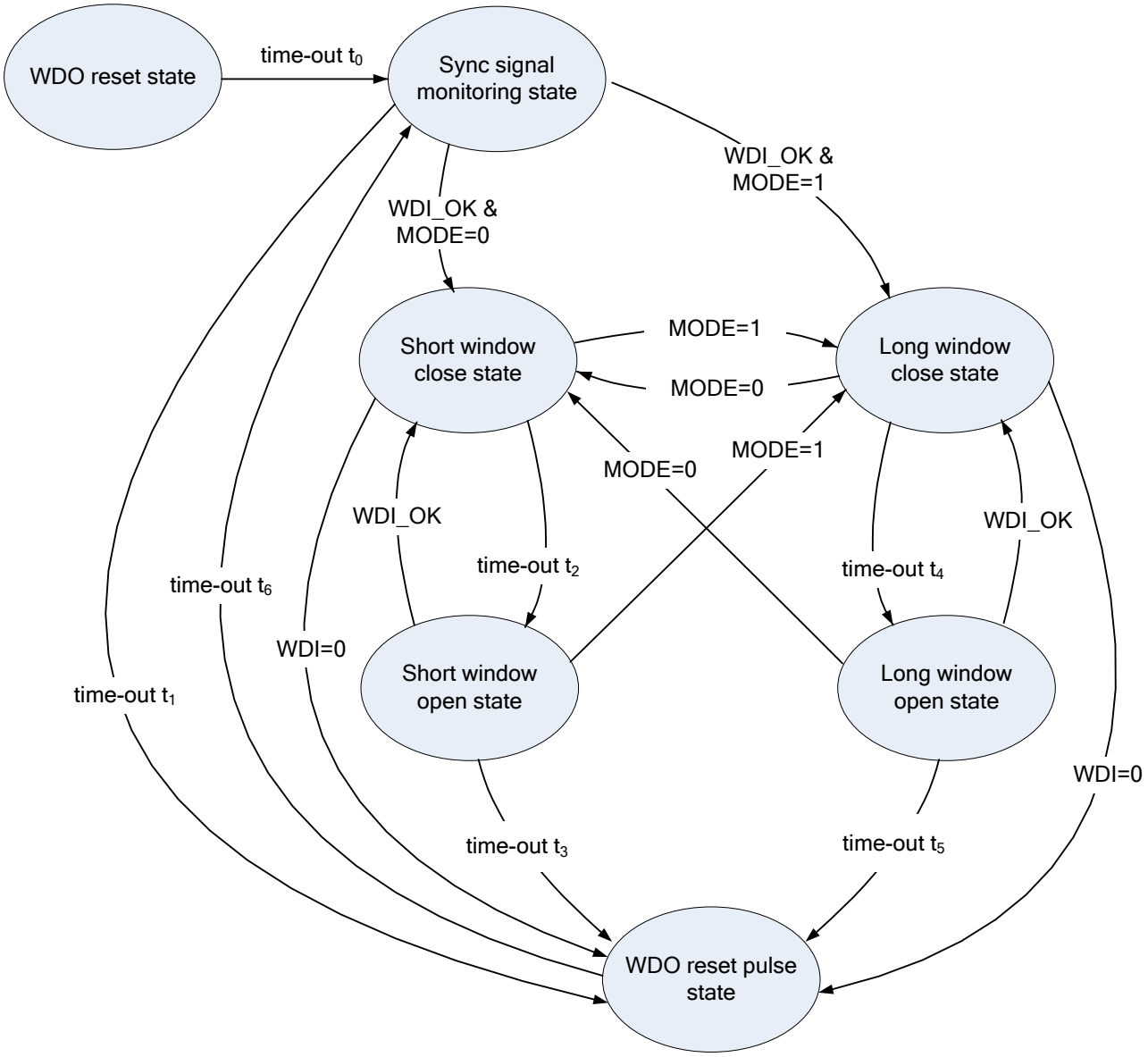
STATE DIAGRAM



NOTE: The above state diagram does not show a WDI error situation.

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APPLICATION INFORMATION

Selecting the Inductor

The I_{peak} is fixed, and the inductor value can be determined with Equation (3):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times I_{peak} \times f_s} \quad (3)$$

Where f_S is the switching frequency at the maximum output current.

A larger inductor value results in a lower switching frequency and higher efficiency. However, the larger value inductor has a larger physical size, a higher series resistance, a lower saturation current, and/or a slow load transient dynamic performance. The inductor value has a lower limit, which is determined by the minimum on time. To keep the inductor functioning properly, choose an inductor value that is higher than L_{MIN}, which is derived from Equation (4):

$$L_{MIN} = \frac{V_{IN(MAX)} \times t_{ON(MIN)}}{I_{peak}} \quad (4)$$

Where $V_{IN(MAX)}$ is the maximum value of the input voltage, and $t_{ON(MIN)}$ is the 115ns minimum switch on time.

Switching Frequency

The switching frequency can be estimated with Equation (5):

$$f_s = \frac{2 \times Io \times V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak}^2 \times V_{IN} \times L} \quad (5)$$

A larger inductor can produce a lower f_S. f_S increases as Io increases. When Io increases to its maximum value $I_{peak}/2$, f_S also reaches its highest value. The maximum f_S value can be estimated with Equation (6):

$$f_{s(max)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{I_{peak} \times V_{IN} \times L} \quad (6)$$

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB. To achieve the desired output voltage, select a resistor divider using Equation (7):

$$\frac{R1}{R2} = \frac{V_{OUT}}{V_{REF}} - 1 \quad (7)$$

Where V_{REF} is the FB reference voltage 1V.

The current flowing into the resistor divider increases the supply current, especially at no-load and light-load conditions. The V_{IN} supply current caused by the feedback resistors can be calculated with Equation (8):

$$I_{IN_FB} = \frac{V_{OUT}}{R1 + R2} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta} \quad (8)$$

Where η is the efficiency of the regulator.

To reduce this current, resistors in the MΩ range are recommended. The recommended value of the feedback resistors are shown in Table 1.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	1200	523
5	1200	300

Under-Voltage Lockout Point Setting

The MPQ2420 has an internal fixed under-voltage lockout (UVLO) threshold. The rising threshold is about 4.2V while the falling threshold is about 3.75V. An external resistor divider between EN and V_{IN} can be used to obtain a higher equivalent UVLO threshold (see Figure 3).

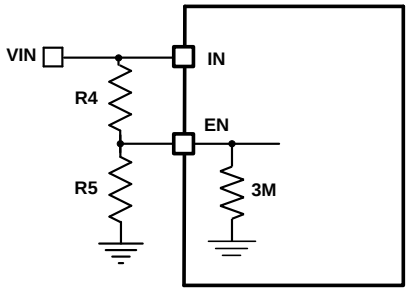

Figure 3: Adjustable UVLO Using EN

The UVLO threshold can be calculated with Equation (9) and Equation (10):

$$UVLO_{TH_Rising} = (1 + \frac{R4}{3M // R5}) \times EN_{TH_Rising} \quad (9)$$

$$UVLO_{TH_Falling} = (1 + \frac{R4}{3M // R5}) \times EN_{TH_Falling} \quad (10)$$

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Soft-Start Capacitor

The soft-start time is the duration of an internal 5μA current source charging the SS capacitor from 0 to the FB reference voltage (1V). The SS capacitor value can be determined with Equation (11):

$$C_{SS} = 5 \times t_{SS}(\mu F) \quad (11)$$

Feed-Forward Capacitor

The HS-FET turns on when FB drops below the reference voltage, producing good load transient performance. However, this also causes the HS-FET to be sensitive to the FB voltage during turn-on. The HS-FET is easily affected by FB noise at turn-on, which can trigger a Fsw jitter. Fsw jitter occurs most often when the Vo ripple is very small. To improve jitter performance, it is recommended to use a small feed-forward capacitor of about 39pF between Vo and FB.

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TYPICAL APPLICATION CIRCUITS

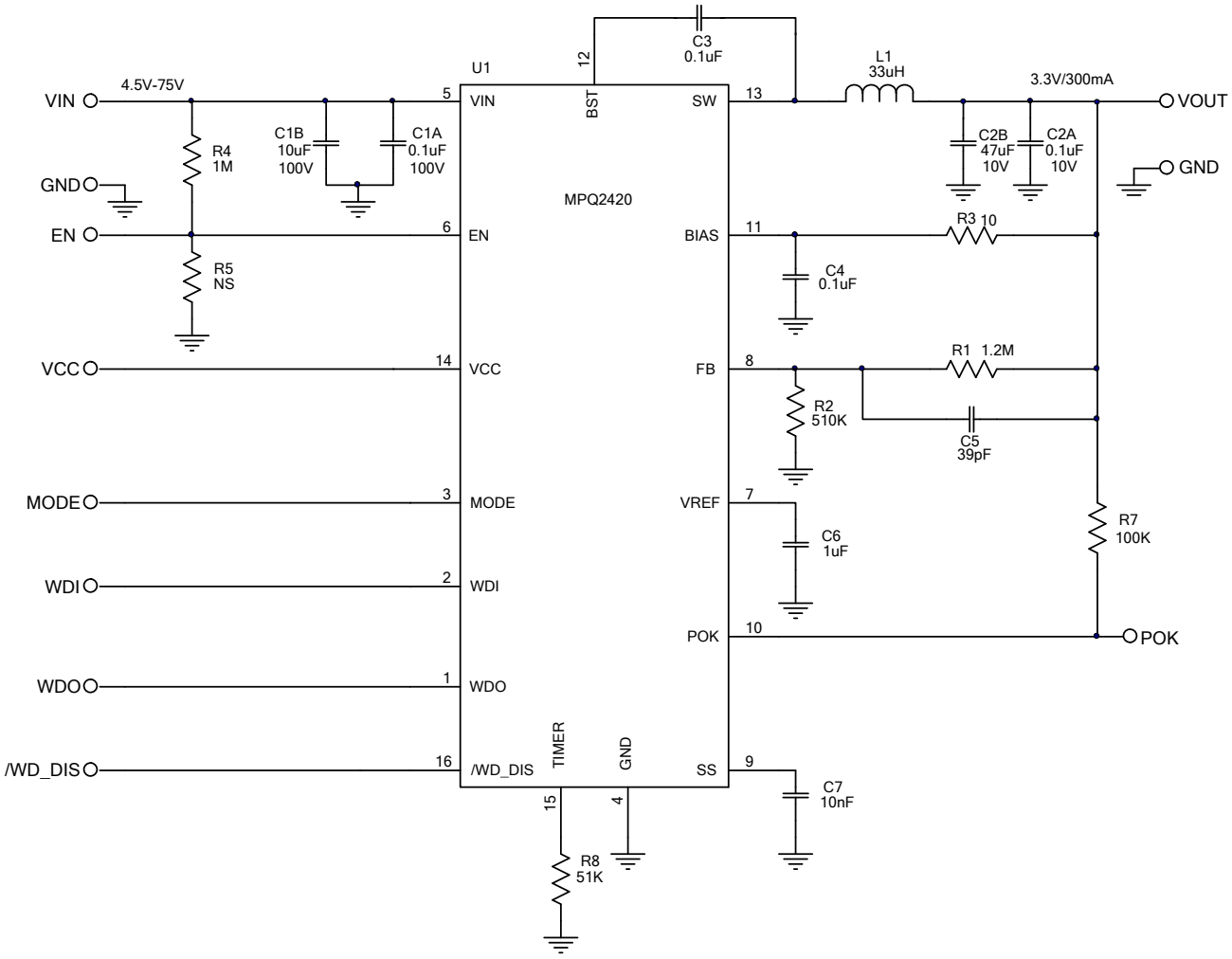

Figure 4: 3.3V Output Typical Application Circuit

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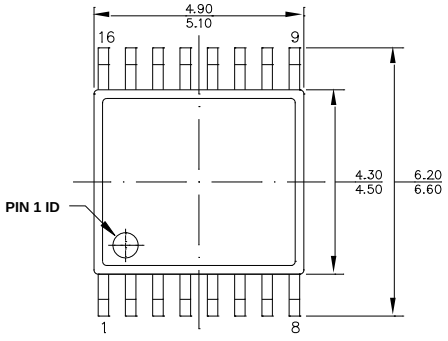
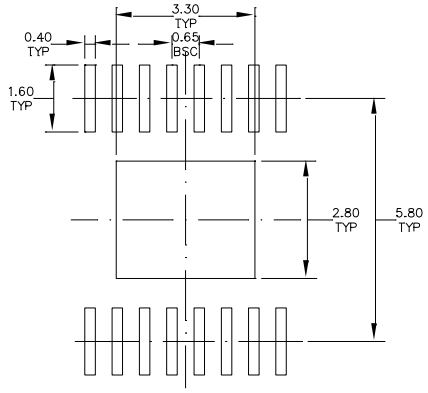
PACKAGE INFORMATION

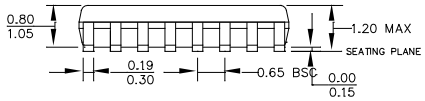
TSSOP-16 EP



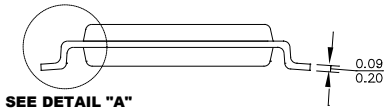
TOP VIEW



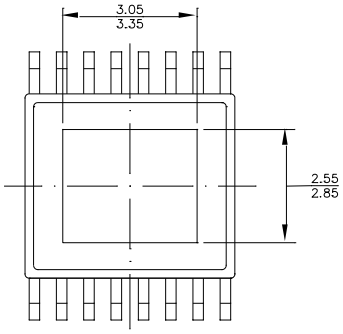
RECOMMENDED LAND PATTERN



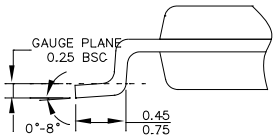
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6) DRAWING IS NOT TO SCALE.

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