MPQ2362-AEC1

Dual 2A, 23V, 380kHz Step-Down Converter with Frequency Synchronization with AEC-Q100 Qualified

DESCRIPTION

The MPQ2362 is a dual monolithic step-down switch mode converter with built-in internal power MOSFETs. It achieves 2A continuous output current for each output over a wide input supply range with excellent load and line regulation. Each channel can be independently synchronized to a frequency up to 1.2MHz.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. In shutdown mode the regulator draws 40µA of supply current.

The MPQ2362 requires a minimum number of readily available standard external components.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EVQ2362DF-00A	2.2”X x 1.6”Y x 0.4”Z

FEATURES

- Guaranteed Industrial/Automotive Temp Range Limits
- 2A Current for Each Output
- 0.18Ω Internal Power MOSFET Switch
- Stable with Low ESR Ceramic Capacitors
- Up to 90% Efficiency
- 40µA Shutdown Mode
- Fixed 380kHz Frequency
- Thermal Shutdown
- Wide 4.75V to 23V Operating Input Range
- Each Output Adjustable from 1.22V to 16V
- Configurable for Single Output with Double the Current
- Programmable Under Voltage Lockout
- Frequency Synchronization Input
- Available in TSSOP20 with Exposed Pad Package
- Available in AEC-Q100 Qualified Grade 1

APPLICATIONS

- Automotive and Industrial Power Systems
- Distributed Power Systems
- I/O and Core supplies
- Set top boxes
- Cable Modems

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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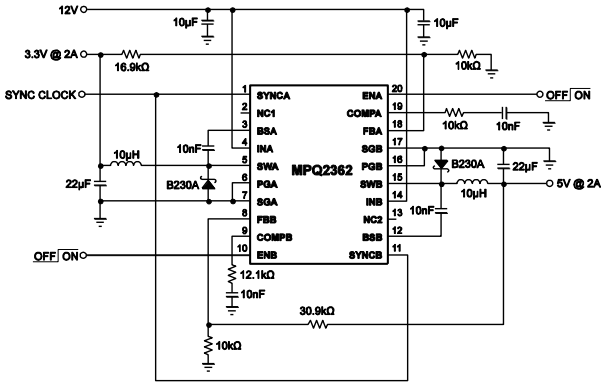
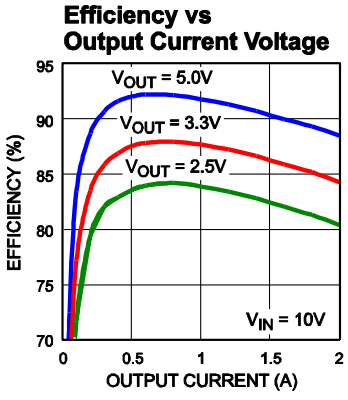
TYPICAL APPLICATION





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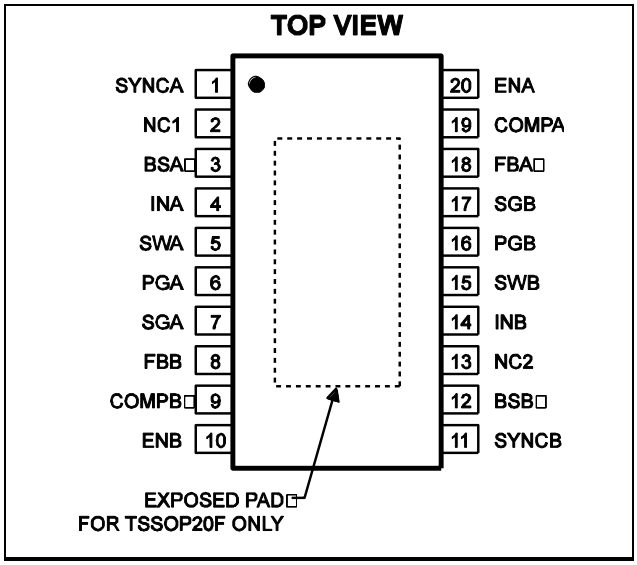
ORDERING INFORMATION

Part Number	Package	Top Marking
MPQ2362DF-AEC1*	TSSOP20F	MP2362DF
MPQ2362DF**		

* For Tape & Reel, add suffix -Z (e.g. MPQ2362DF-AEC1-Z).
For RoHS Compliant Packaging, add suffix -LF (e.g. MPQ2362DF-AEC1-LF-Z)
* * For Tape & Reel, add suffix -Z (e.g. MPQ2362DF-Z).
For RoHS Compliant Packaging, add suffix -LF (e.g. MPQ2362DF-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage ($V_{INA, INB}$) 25V
Switch Voltage ($V_{SWA, SWB}$) 26V
Bootstrap Voltage ($V_{BSA, BSB}$) ..... V_{SW} + 6V
Feedback Voltage ($V_{FBA, FBB}$) ..... –0.3V to +6V
Enable/UVLO Voltage ($V_{ENA, ENB}$) ..... –0.3V to +6V
Comp Voltage ($V_{COMPA, COMPB}$) ..... –0.3V to +6V
SYNC Voltage ($V_{SYNCA, SYNCB}$) ..... –0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2) 3.1W
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage (V_{IN}) ..... 4.75V to 23V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP20F ..... 40 ..... 6 ....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C Typical values are at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 23V	T_J=25°C	1.198	1.222	1.246	V
			T_J=-40°C to +125°C	1.185	1.222	1.259	V
Upper Switch-On Resistance(6)	$R_{DS(ON)1}$				0.18		Ω
Lower Switch-On Resistance	$R_{DS(ON)2}$				10	20	Ω
Upper Switch Leakage		V_{EN} = 0V, V_{SW} = 0V				10	μA
Current Limit (5)		T_J=25°C		2.4	3.4	4	A
Current Limit Gain Output Current to Comp Pin Voltage	G_{CS}				2	3.5	A/V
Error Amplifier Voltage Gain	A_{VEA}				400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10 μA	T_J=25°C	500	770	1100	μA/V
			T_J=-40°C to +125°C	300		1200	
Oscillator Frequency	f_{OSC}			260	380	500	kHz
Short Circuit Frequency	f_{SC}	V_{FB} = 0V		10	35	54	kHz
SYNC Frequency		SYNC Drive = 0V to 2.7V	T_J=25°C	0.5		1.2	MHz
			T_J=-40°C to +125°C	0.5		1.0	
EN Shutdown Threshold Voltage	V_{EN}	I_{IN} > 100μA		0.7	1.0	1.3	V
Enable Pull-Up Current	I_{EN}				1.0		μA
EN UVLO Threshold Rising	V_{UVLO}	V_{EN} Rising		2.37	2.50	2.62	V
Supply Current (Shutdown)	I_{OFF}	V_{EN} ≤ 0.4V			40	70	μA
Supply Current (Quiescent)	I_{ON}	V_{EN} ≥ 3V			2.0	2.8	mA
Thermal Shutdown(6)	T_S				160		°C
Maximum Duty Cycle		V_{FB} = 1.0V, f_{SW} = 380kHz			90	98	%
Minimum On Time(6)	t_{ON}				100		ns

Note:

5) Equivalent output current = 1.5A ≥ 50% Duty Cycle
2.0A ≤ 50% Duty Cycle
Assumes ripple current = 30% of load current.
Slope compensation changes current limit above 40% duty cycle.

6) Design guarantee, no production test.

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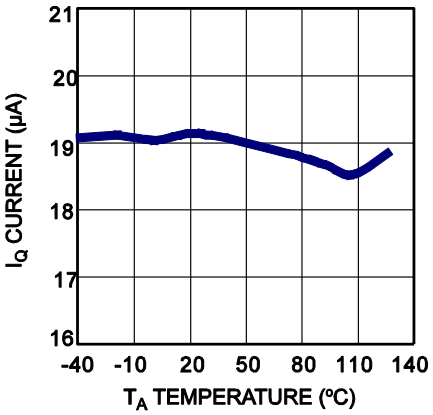
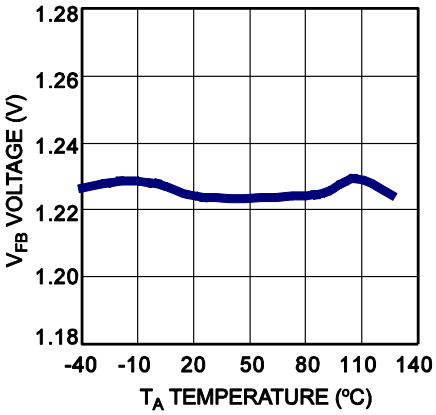
TYPICAL CHARACTERISTICS

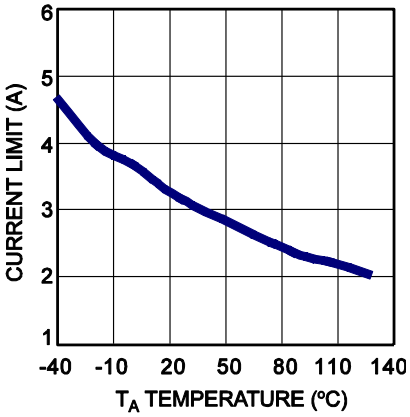
I_Q Current vs. T_A



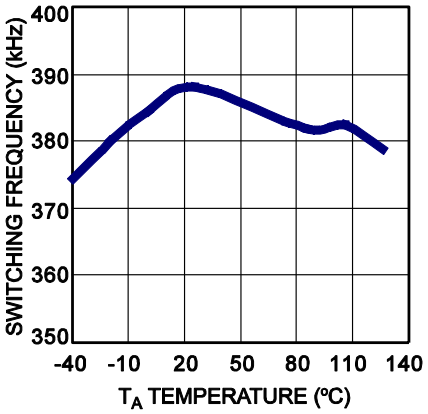
V_{FB} Voltage vs. T_A



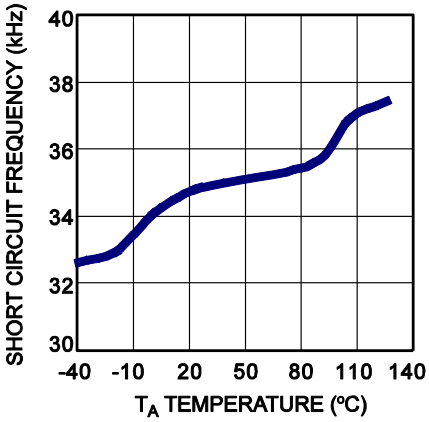
Current Limit vs. T_A



Switching Frequency vs. T_A



Short Circuit Frequency vs. T_A



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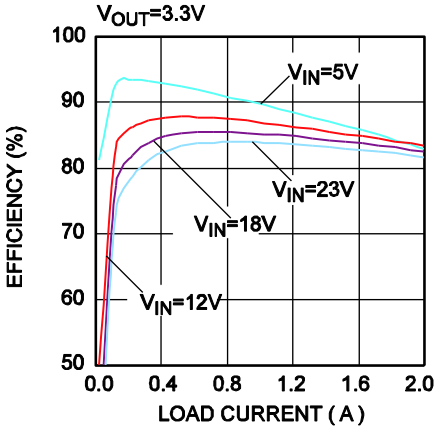
TYPICAL CHARACTERISTICS

Load Efficiency



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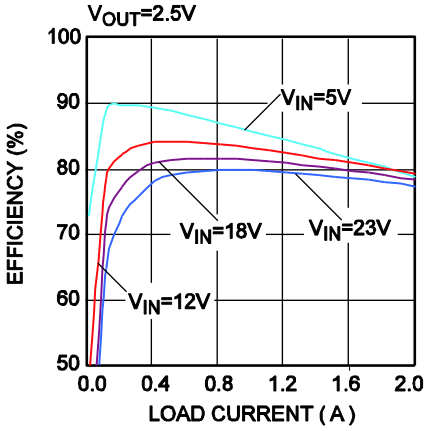
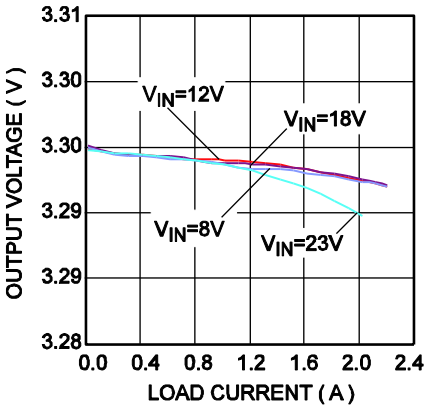
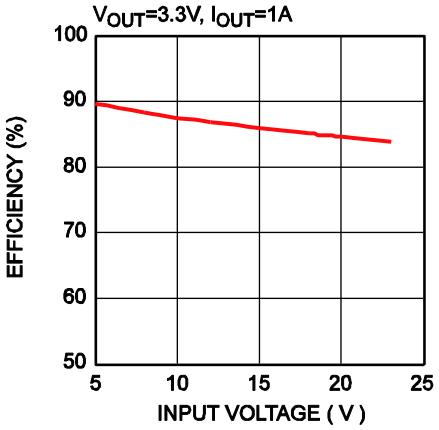


Load Regulation



Line Efficiency



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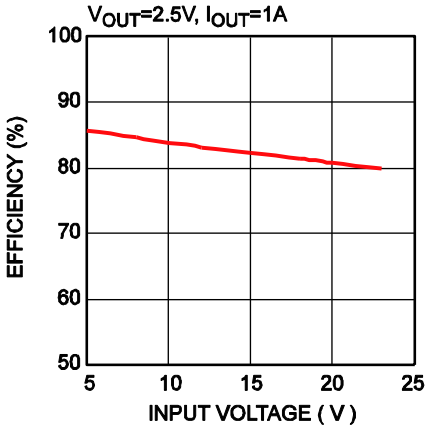

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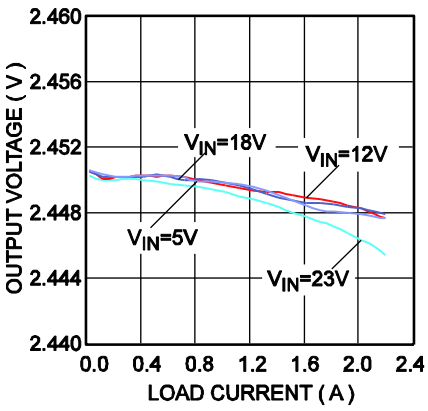
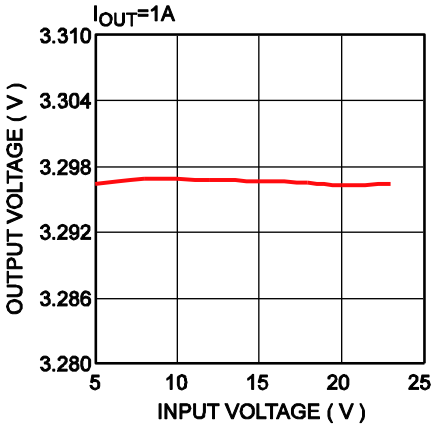
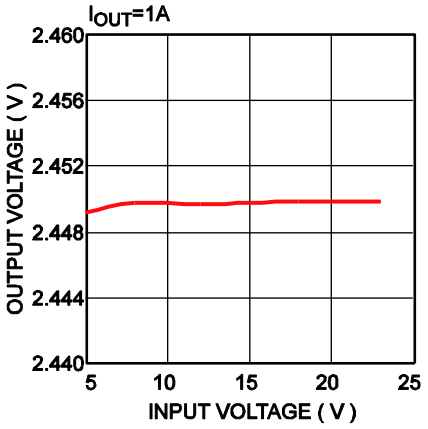


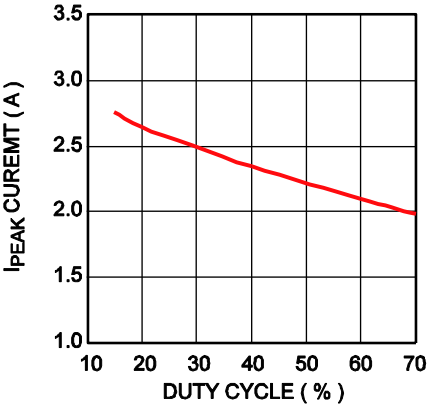
Line Regulation



Line Regulation



I_{PEAK} vs. Duty Cycle



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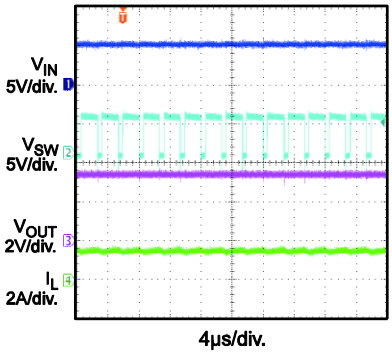
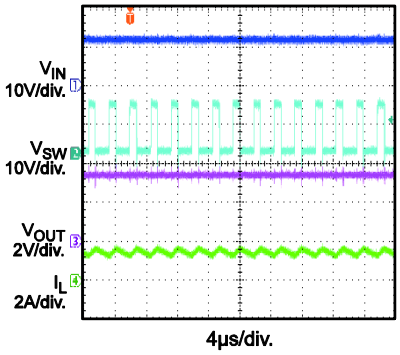
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, C1A=C1B=4.7µF, C2A=C2B=C4A=C4B=22µF, L1A=6.8µH, L1B=4.7µH and T_A=25°C, unless otherwise noted.

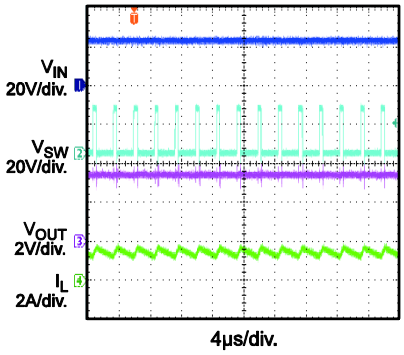
Steady State
V_{IN} =5V, V_{OUT}=3.3V, I_{OUT}=1.5A



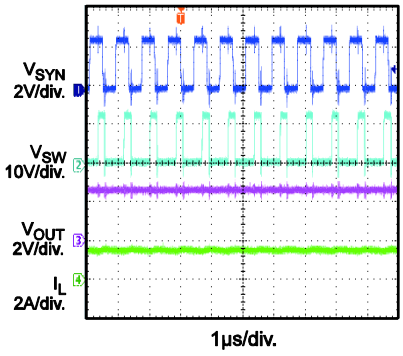
Steady State
V_{OUT}=3.3V, I_{OUT}=1.5A



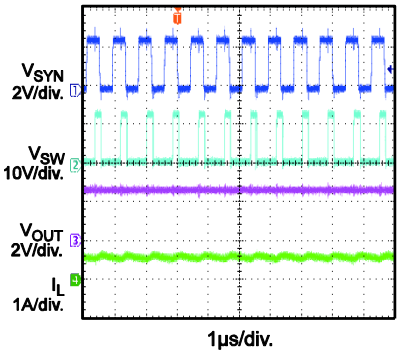
Steady State
V_{IN}=23V, V_{OUT}=3.3V, I_{OUT}=1.5A



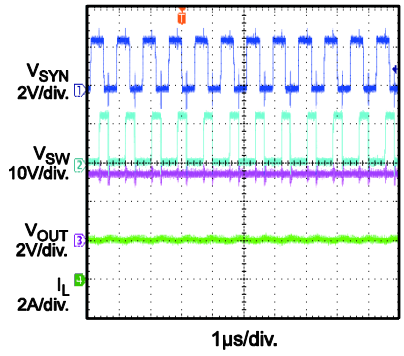
Sync Input
V_{OUT}=2.5V, I_{OUT}=1.5A



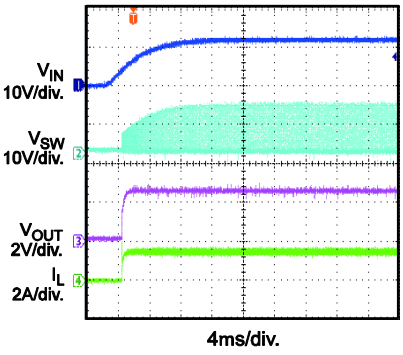
Sync Input
V_{OUT}=2.5V, I_{OUT}=0.5A



Sync Input
V_{OUT}=3.3V, I_{OUT}=2A



Start Up
V_{OUT}=2.5V, I_{OUT}=1.5A



Start Down
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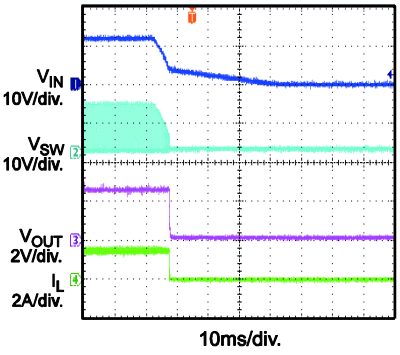
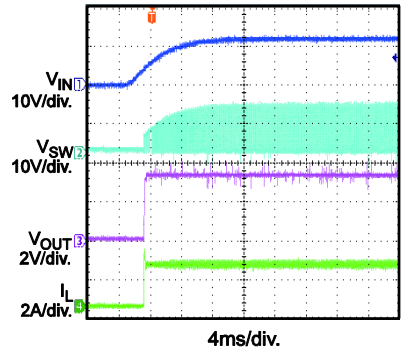


Start Up
V_{OUT}=3.3V, I_{OUT}=2A



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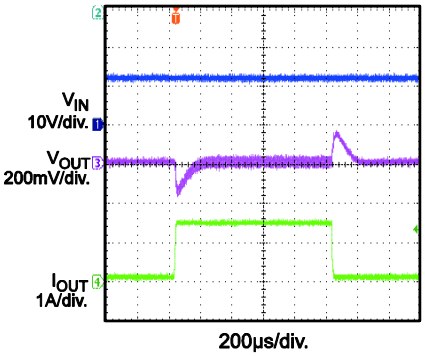
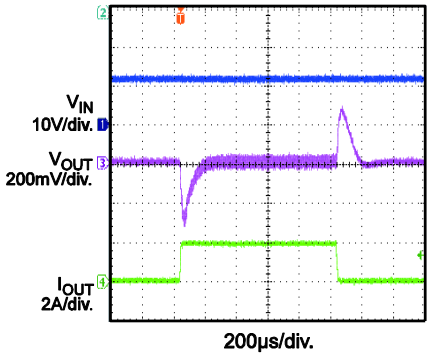
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, C1A=C1B=4.7µF, C2A=C2B=C4A=C4B=22µF, L1A=6.8µH, L1B=4.7µH and T_A=25°C, unless otherwise noted.

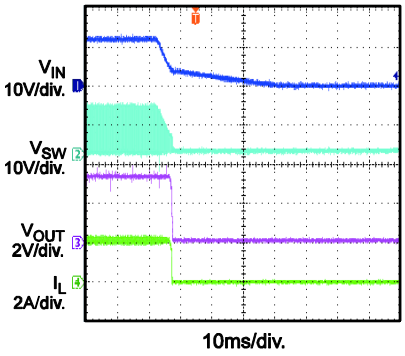
Transient
V_{OUT}=2.5V, I_{OUT}=0.1A - 1.5A



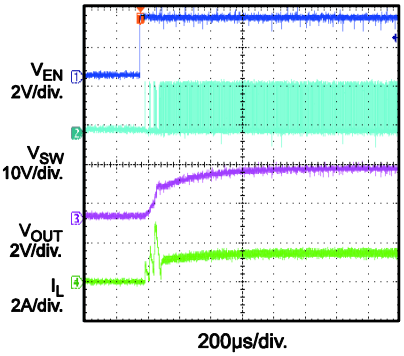
Transient
V_{OUT}=3.3V, I_{OUT}=0.1A -2A



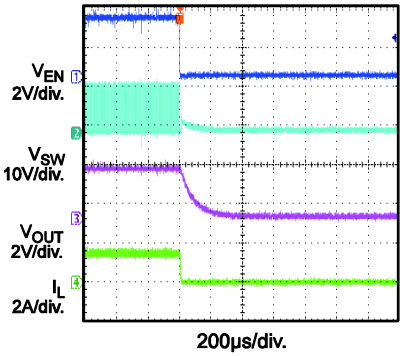
Start Down
V_{OUT}=3.3V, I_{OUT}=2A



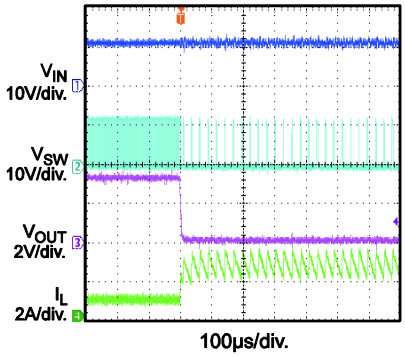
Enable Up
V_{OUT}=2.5V, I_{OUT}=1.5A



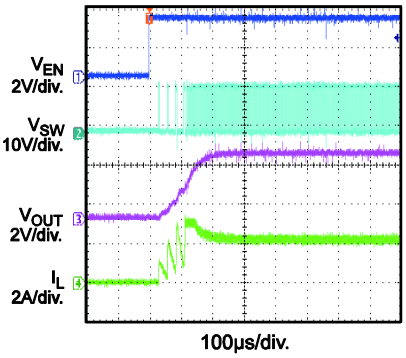
Enable Down
V_{OUT}=2.5V, I_{OUT}=1.5A



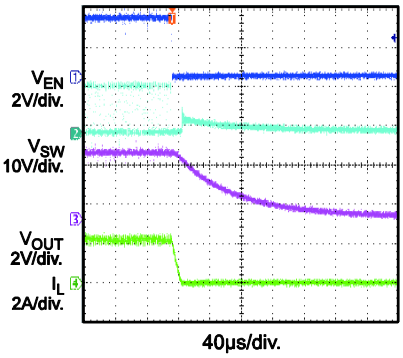
Short Output
V_{OUT}=3.3V, I_{OUT}=1A



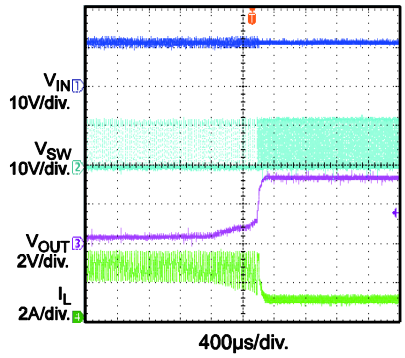
Enable Up
V_{OUT}=3.3V, I_{OUT}=2A



Enable Down
V_{OUT}=3.3V, I_{OUT}=2A



Short Output Recovery
V_{OUT}=3.3V, I_{OUT}=1A



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PIN FUNCTIONS

Pin #	Name	Description
1	SYNCA	Synchronization Input for Channel A. It is internally pulled down to ground with an 11kΩ resistor. Leave it open if unused.
2	NC	No Connect
3	BSA	High-Side Driver Boost Pin. Connect a 10nF capacitor from this pin to SWA.
4	INA	Supply Voltage Channel A. The MPQ2362 operates from a +4.75V to +23V unregulated input. Input Ceramic Capacitors should be close to this pin.
5	SWA	Switch Channel A. This connects the inductor to either INA through M1A or to PGA through M2A.
6	PGA	Power Ground Channel A. This is the Power Ground Connection to the input capacitor ground.
7	SGA	Signal Ground Channel A. This pin is the signal ground reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
8	FBB	Feedback Voltage for Channel B. This pin is the feedback voltage. The output voltage is ratio scaled through a voltage divider, and the center point of the divider is connected to this pin. The voltage is compared to the on board 1.22V reference.
9	COMPB	Compensation Channel B. This is the output of the transconductance error amplifier. A series RC is placed on this pin for proper control loop compensation. Please refer to more in the datasheet.
10	ENB	Enable/UVLO Channel B. A voltage greater than 2.62V enables operation. Leave ENB unconnected for automatic startup. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from V_{IN} to GND. For complete low current shutdown the ENB pin voltage needs to be less than 700mV.
11	SYNCB	Synchronization Input for Channel B. It is internally pulled down to ground with a 11kΩ resistor. Leave it open if unused.
12	BSB	High-Side Driver Boost Pin. Connect a 10nF capacitor from this pin to SWB.
13	NC	No Connect.
14	INB	Supply Voltage Channel B. The MPQ2362 operates from a +4.75V to +23V unregulated input. Input Ceramic Capacitors should be close to this pin.
15	SWB	Switch Channel B. This connects the inductor to either INB through M1B or to PGB through M2B.
16	PGB	Power Ground Channel B. This is the Power Ground Connection to the input capacitor ground.
17	SGB	Signal Ground Channel B. This pin is the signal ground reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
18	FBA	Feedback Voltage for Channel A. This pin is the feedback voltage. The output voltage is ratio scaled through a voltage divider, and the center point of the divider is connected to this pin. The voltage is compared to the on board 1.22V reference.
19	COMPA	Compensation Channel A. This is the output of the transconductance error amplifier. A series RC is placed on this pin for proper control loop compensation. Please refer to more in the datasheet.
20	ENA	Enable/UVLO Channel A. A voltage greater than 2.62V enables operation. Leave ENA unconnected for automatic startup. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from V_{IN} to GND. For complete low current shutdown the ENA pin voltage needs to be less than 700mV.

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OPERATION

The MPQ2362 is a dual channel current mode regulator. The COMP pin voltage is proportional to the peak inductor current. At the beginning of a cycle, the upper transistor M1 is off, and the lower transistor M2 is on (see Figure 1). The COMP pin voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 380KHz CLK signal sets the RS Flip-Flop. Its output turns off M2 and turns on M1 thus connecting the SW pin and inductor to the input supply. The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the Current Comparator.

When the sum of the Current Sense Amplifier output and the Slope Compensation signal exceeds the COMP pin voltage, the RS Flip-Flop is reset and the MPQ2362 reverts to its initial M1 off, M2 on state.

If the sum of the Current Sense Amplifier output and the Slope Compensation signal does not exceed the COMP voltage, the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 1.22V bandgap reference. The polarity is such that a voltage at the FB pin lower than 1.22V increases the COMP pin voltage. Since the COMP pin voltage is proportional to the peak inductor current, an increase in its voltage increases current delivered to the output. The lower 10Ω switch ensures that the bootstrap capacitor voltage is charged during light load conditions. External Schottky Diode D1 carries the inductor current when M1 is off (see Figure 1).

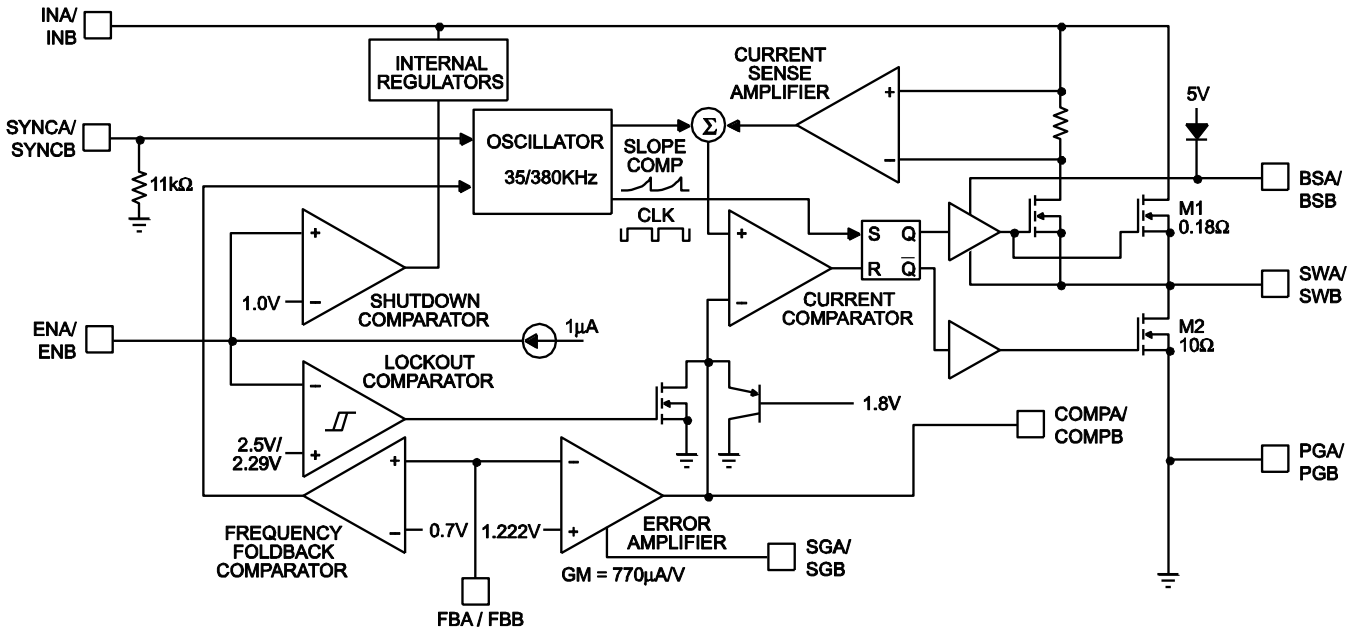

Figure 1—Functional Block Diagram

(Diagram portrays ½ of the MPQ2362)

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APPLICATION INFORMATION

COMPONENT SELECTION

The MPQ2362 has two channels: A and B. The following formulas are used for component selection of both channels. Refer to components with reference “A” for channel A, and components with reference “B” for channel B, respectively, as indicated in Figure 3 (i.e. – R1A for Channel A and R1B for Channel B).

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2}$$

Thus the output voltage is:

$$V_{OUT} = 1.22V \times \frac{R1+R2}{R2}$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage

A typical value for R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using that value, R1 is determined by:

$$R1 = R2 \times (\frac{V_{OUT}}{1.22V} - 1)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 17.0kΩ. Choose a 16.9kΩ, 1% resistor.

Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L1 = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current.

The peak inductor current can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current.

Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high-side switch is off. To reduce losses due to the diode forward voltage and recovery times, use a Schottky diode.

Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

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For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible.

When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L1 is the inductor value, C2 is the output capacitance value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ2362 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

The MPQ2362 employs current mode control on each channel for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{VEA} \times \frac{V_{FB}}{V_{OUT}}$$

Where A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

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$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case (as shown in Figure 2), a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important.

Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system unstable. A good rule of thumb is to set the crossover frequency to below one-tenth of the switching frequency. To optimize the compensation components for conditions not listed in Table 2, the following procedure can be used:

1. Choose the compensation resistor (R3) to set the desired crossover frequency. Determine the R3 value by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency, which is typically less than one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero, f_{Z1}, to below one forth of the crossover frequency provides sufficient phase margin. Determine the C3 value by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

Where R3 is the compensation resistor value.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole f_{P3} at the location of the ESR zero. Determine the C6 value by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

Frequency Synchronization

Each channel of the MPQ2362 can be driven with an external clock of up to 1.2MHz, high frequency synchronization and low VIN can not be achieved the same switching time. The rising edge of the external clock resets the internal clock, and the amplitude of the external clock must be greater than 2.7V.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: D=$\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure2

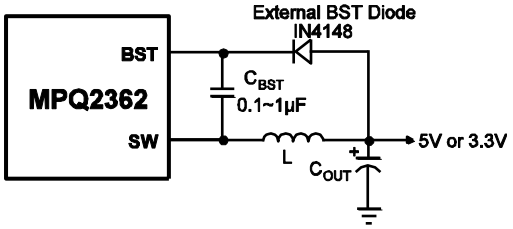

Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

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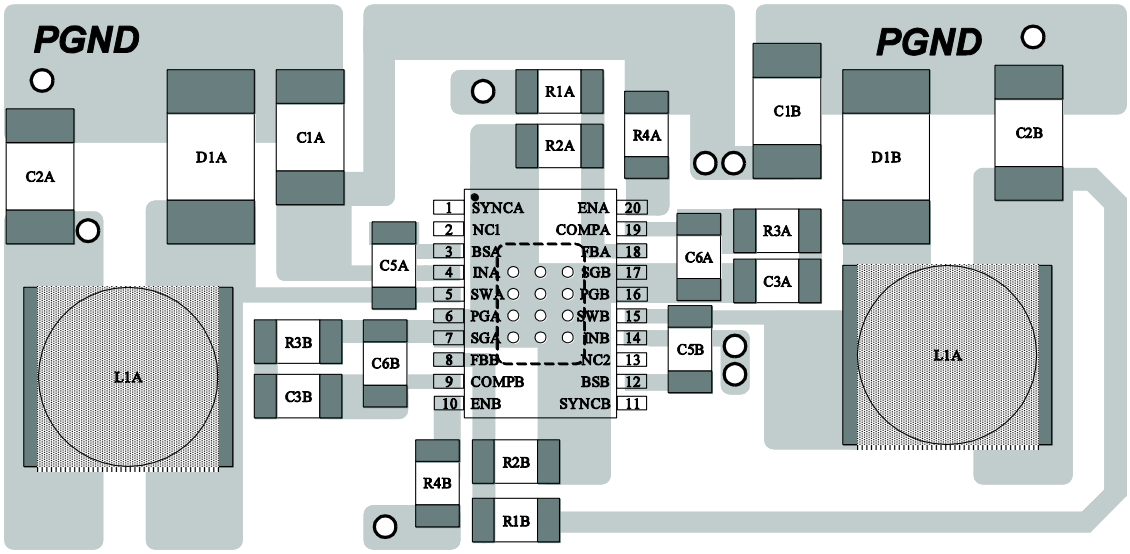
PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure3 for references.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and schottky diode.
2) Keep the connection of schottky diode between SW pin and input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



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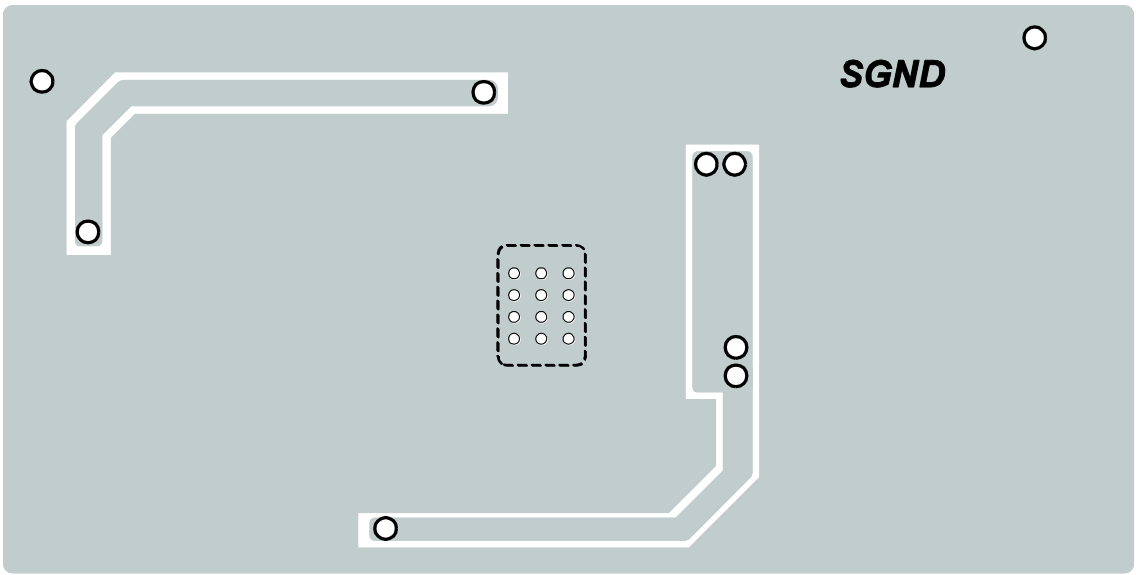

Bottom Layer

Figure3—PCB Layout

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TYPICAL APPLICATION CIRCUITS

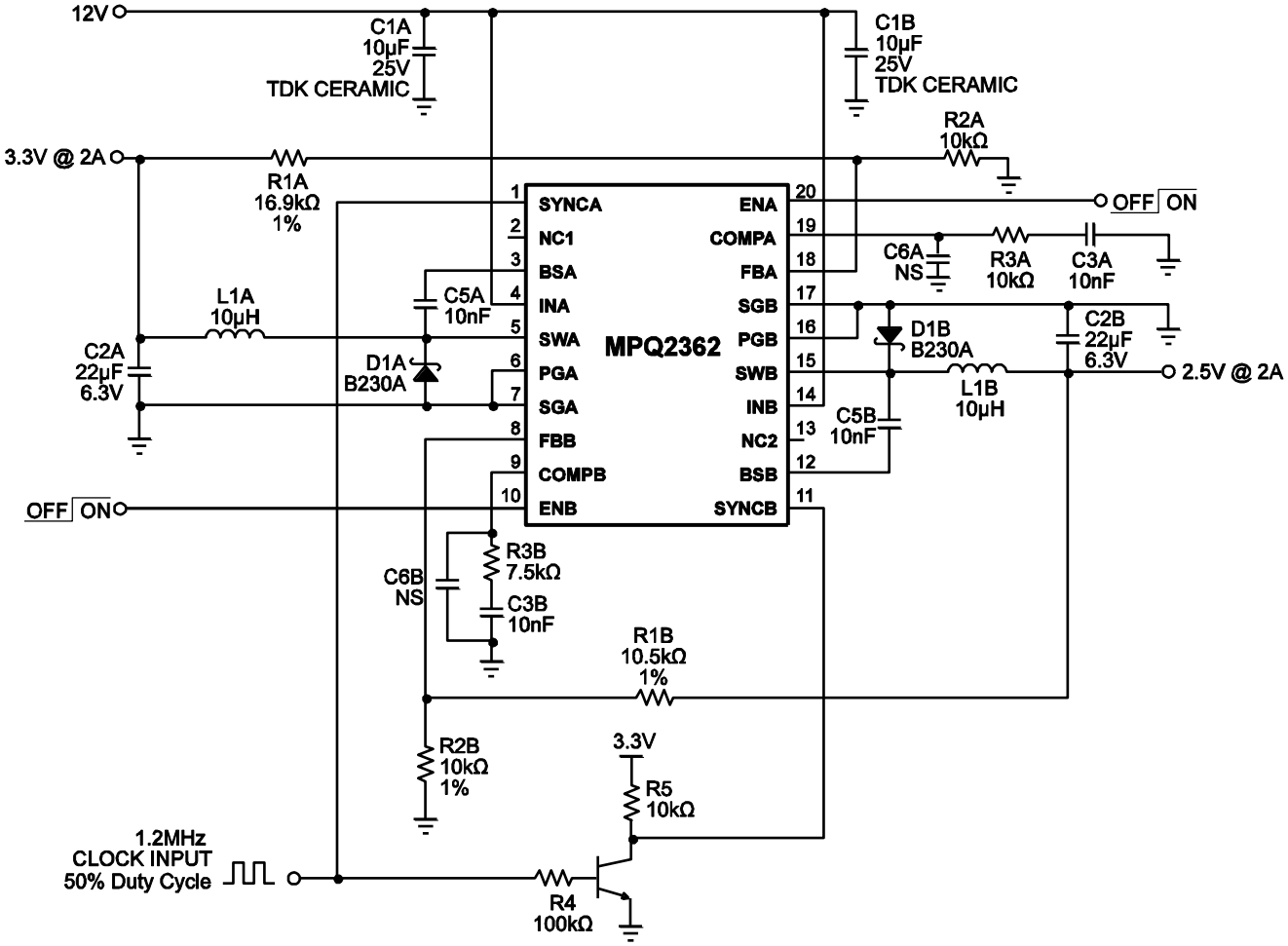

Figure 4—Dual Phase 1.2MHz, 2.5V @ 2A and 3.3V @ 2A Step-down Converter from 12V Input

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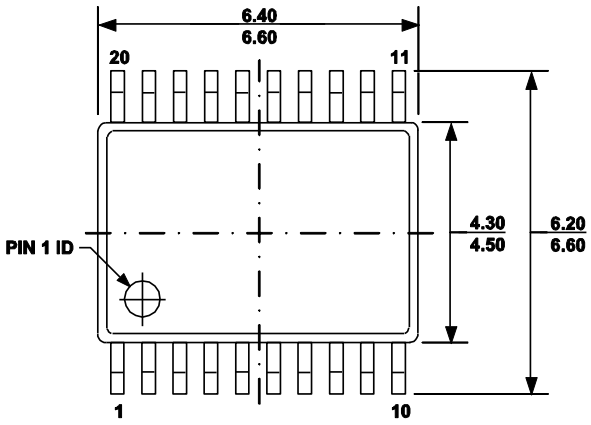
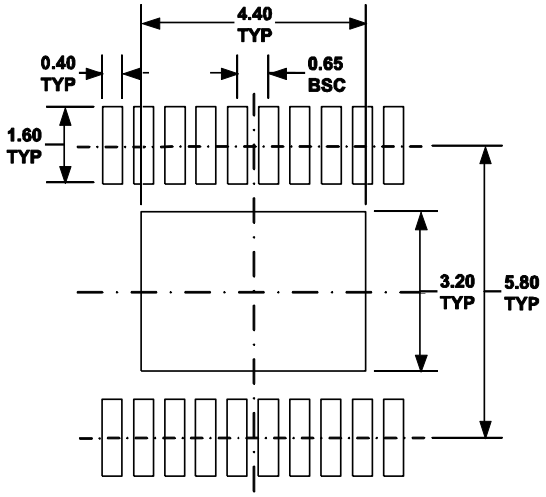
PACKAGE INFORMATION

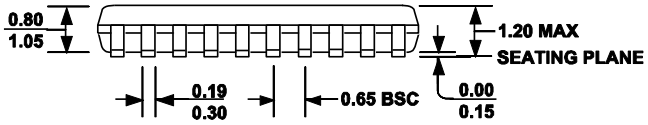
TSSOP20F



TOP VIEW



RECOMMENDED LAND PATTERN



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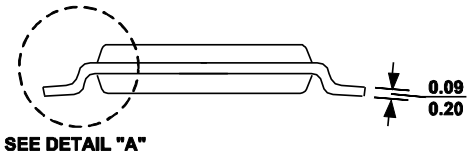
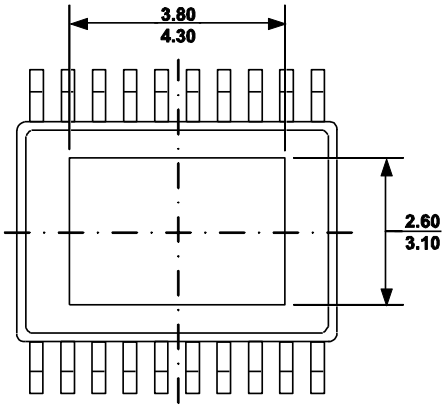
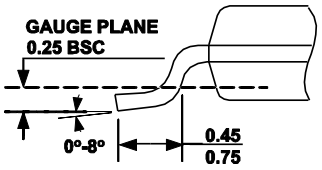


SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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