MPQ2242

6V, 2A, Configurable-Frequency Synchronous Buck Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ2242 is a configurable-frequency (300kHz to 2.2MHz), synchronous, step-down converter. It can achieve up to 2A of continuous output current (I_{OUT}) with peak current control for excellent transient response and efficiency performance. The MPQ2242 operates from a 2.7V to 6V input voltage (V_{IN}) range and generates an output voltage (V_{OUT}) as low as 0.606V. It is ideal for a wide range of applications, including automotive infotainment, clusters, and telematics, as well as portable instruments.

The MPQ2242 integrates a 35mΩ high-side MOSFET (HS-FET) and a 25mΩ synchronous rectifier for high efficiency without an external Schottky diode.

The MPQ2242 can be configured for either advanced asynchronous modulation (AAM) mode or forced continuous conduction mode (FCCM) at light loads. AAM mode provides high efficiency by reducing switching losses at light loads, while FCCM has a controllable frequency and a lower output ripple.

The MPQ2242 offers standard features, including soft start (SS), enable (EN) control, and a power good (PG) indicator. In addition, the MPQ2242 provides over-current protection (OCP) with valley current detection to avoid current runaway, short-circuit protection (SCP), reliable over-voltage protection (OVP), and auto-recovery thermal protection.

With internal compensation, the MPQ2242 requires a minimal number of readily available, standard external components. It is available in a QFN-9 (2mmx3mm) package, and is AEC-Q100 qualified.

FEATURES

- **Cool Thermals**
  - Low-Ohmic MPS BCD FET Technology
- **Reduces Board Size and BOM**
  - Integrated Compensation Network
  - Available in a Small QFN-9 (2mmx3mm) Package
- **Additional Features**
  - Adjustable Output Voltage (V_{OUT}) from 0.606V
  - High-Efficiency Synchronous Mode Control
  - Configurable Frequency Up to 2.2MHz
  - Low Current in Shutdown Mode
  - 100% Duty Cycle Operation
  - Selectable AAM Mode or FCCM Operation
  - External Soft Start
  - Remote EN Control
  - Cycle-by-Cycle Over-Current Protection (OCP)
  - Short-Circuit Protection (SCP)
  - V_{IN} Under-Voltage Lockout (UVLO)
  - V_{OUT} Over-Voltage Protection (OVP)
  - Thermal Shutdown
  - Available in a Wettable Flank Package
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Portable Instruments
- Industrial Supplies
- Battery-Powered Devices

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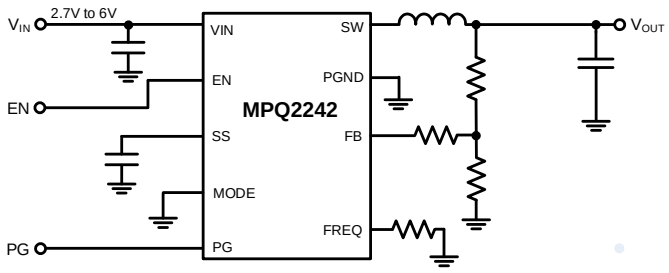
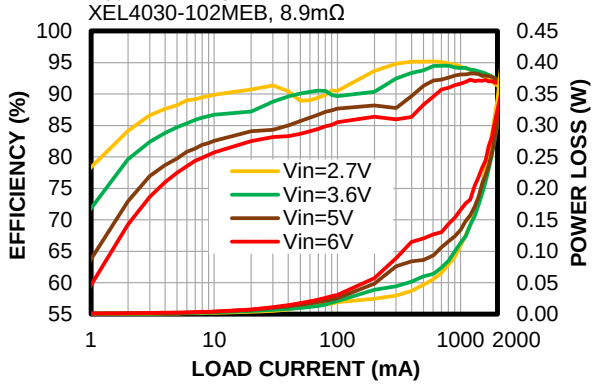
TYPICAL APPLICATION



Efficiency vs. Load Current vs. Power Loss

V_{OUT} = 1.8V, f_{SW} = 2.1MHz, AAM mode, XEL4030-102MEB, 8.9mΩ



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ2242GDE-AEC1***	QFN-9 (2mmx3mm)	*See Below*	1

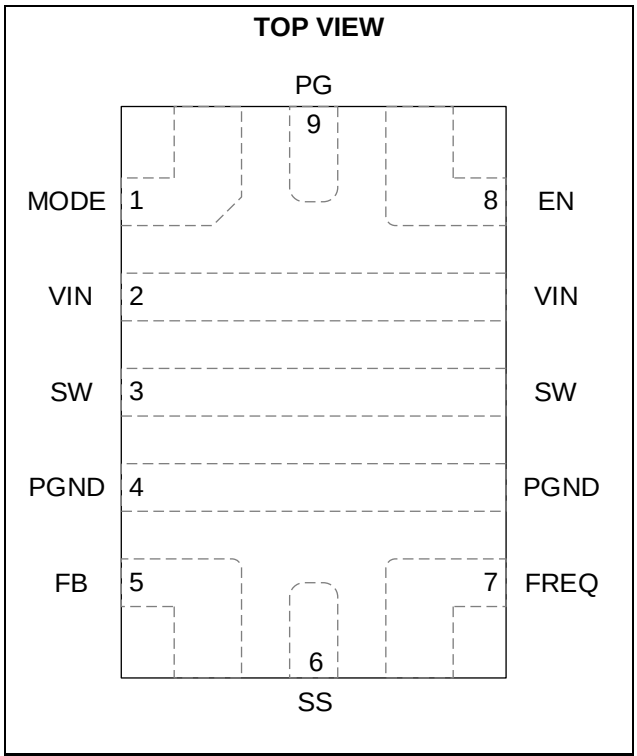
* For Tape & Reel, add suffix -Z (e.g. MPQ2242GDE-AEC1-Z).
** Moisture Sensitivity Level Rating
*** Wettable Flank

TOP MARKING

$\overline{\text{BZL}}$
YWW
LLLL

BZL: Product code of MPQ2242GDE-AEC1
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE



QFN-9 (2mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**Mode selection.** Pull MODE below 0.4V to select advanced asynchronous modulation (AAM) mode. Pull MODE above 1.2V to select forced continuous conduction mode (FCCM). Do not leave this pin floating.
2	VIN	**Input supply.** VIN supplies all power to the converter. To reduce switching spikes, connect a decoupling capacitor to ground, placed as close as possible to the IC.
3	SW	**Switch output.** Connect SW internally to the high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). Connect SW externally to the output inductor.
4	PGND	**Ground.** Connect PGND to larger copper areas on the negative terminals of the input and output capacitors.
5	FB	**Feedback point.** Negative input of the error amplifier (EA). To set the regulation voltage, connect FB to the tap of an external resistor divider between the output and GND. The power good (PG) and under-voltage lockout (UVLO) circuits also use FB to monitor the output voltage (V_{OUT}).
6	SS	**Soft start.** To set the soft-start time (t_{SS}) externally, place a capacitor from SS to GND. Float this pin to activate the internal default 1ms t_{SS}.
7	FREQ	**Configurable switching.** Connect a resistor to GND to set the switching frequency (f_{SW}). See the f_{SW} vs. R_{FREQ} curve on page 12 for more details.
8	EN	**Enable input.** Pull EN below the 0.4V falling threshold to shut down the chip. Pull EN above the 1.2V rising threshold to enable the chip. There is an internal 1MΩ resistor connected from EN to ground.
9	PG	**Power good indicator.** The PG output is an open drain that connects to VIN via an internal pull-up resistor. If the FB voltage (V_{FB}) is within 85% to 115 % of the reference voltage (V_{REF}), PG goes high. If V_{FB} is out of the regulation range, PG goes low. Float this pin if it is not used.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}.....6.5V
V_{SW}.....-0.3V (-3V for < 10ns)
.....to +6.5V (7V for < 10ns)
All other pins .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) (7)
..... 2.8W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (3)
Charged device model (CDM).....Class 2b (4)

Recommended Operating Conditions

Continuous supply voltage (V_{IN}).....2.7V to 6V
Output voltage (V_{OUT}).....0.606V to V_{IN}
Load current range .....0A to 2A
Operating junction temp (T_J).....
.....-40°C to +125°C (5)

Thermal Resistance θ_{JA} θ_{JC}

QFN-9 (2mmx3mm)
JESD51-7.....64.4.....5.7..°C/W (6)
EVQ2242-D-00A.....53.7.....5.1..°C/W (7)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002
4) Per AEC-Q100-011
5) Operating devices at junction temperatures greater than 125°C is possible, please contact MPS for details.
6) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from junction-to-case bottom.
7) Measured on MPS MPQ2242 standard EVB, 6.35cmx6.35cm, 2oz. thick copper, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and Under-Voltage Lockout (UVLO)						
Quiescent supply current	I_Q	Mode = AAM, V_{EN} = 2V, no load, R_{FREQ} = 125kΩ, T_J = 25°C		42	50	μA
		T_J = -40°C to +125°C			120	
Shutdown current	I_{SD}	Mode = AAM, V_{EN} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			20	
V_{IN} UVLO rising threshold	$V_{IN_UVLO_VTH-R}$		2.3	2.5	2.7	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_VTH-F}$		2	2.15	2.3	V
V_{IN} UVLO hysteresis threshold	$V_{IN_UVLO_HYS}$			350		mV
Output and Regulation						
Regulated FB voltage	V_{FB}	T_J = 25°C	0.596	0.606	0.616	V
		T_J = -40°C to +125°C	0.594		0.618	V
FB input current	I_{FB}	V_{FB} = 0.63V		10	100	nA
Output discharge resistor	$R_{DISCHARGE}$		50	100	150	Ω
Switches and Frequency						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_H}$	V_{IN} = 5V, I_{OUT} = 200mA		35	70	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_L}$	V_{IN} = 5V, I_{OUT} = 200mA		25	70	mΩ
HS-FET leakage current	I_{HSW_LKG}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 6V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			30	
LS-FET leakage current	I_{LSW_LKG}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V, T_J = 25°C		0	1	μA
		T_J = -40°C to +125°C			10	
Switching frequency	f_{SW}	R_{FREQ} = 65kΩ	380	450	520	kHz
		R_{FREQ} = 9.31kΩ	1800	2100	2400	
Maximum duty cycle	D_{MAX}			100		%
Minimum on time (8)	t_{ON_MIN}			50		ns
Minimum off time (8)	t_{OFF_MIN}			95		ns
Power Good (PG)						
PG sink current capacity	V_{PG_SINK}	Sink 0.5mA			300	mV
PG logic high voltage	V_{PG_HIGH}	V_{IN} = 5V	4.5			V
PG deglitch	$t_{PG_DEGLITH}$	V_{OUT} rising edge	40	100	180	μs
		V_{OUT} falling edge	10	25	40	μs
PG upper rising threshold	PG_{UP_R}	As a percentage of V_{FB}	108	115	122	%
PG upper hysteresis	PG_{UP_HYS}	As a percentage of V_{FB}		5		%
PG lower rising threshold	PG_{LOW_R}	As a percentage of V_{FB}	80	85	90	%
PG lower hysteresis	PG_{LOW_HYS}	As a percentage of V_{FB}		5		%
Enable (EN)						
EN input rising threshold	V_{EN_RISING}		1.2			V
EN input falling threshold	$V_{EN_FALLING}$				0.4	V
EN input current	I_{EN}	V_{EN} = 2V		2	5	μA
		V_{EN} = 0V		0	0.5	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.6V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
MODE and Soft Start (SS)						
MODE pin rising threshold	V_{MODE_FCCM}	Into FCCM	1.2			V
MODE pin falling threshold	V_{MODE_AAM}	Into AAM mode			0.4	V
Mode input leakage current	I_{MODE}	Pulled up to 6V			1	µA
Soft-start charging current	I_{SS}	V_{SS} = 0V	2	4	6	µA
Default soft-start time	$t_{SS_DEFAULT}$			1		ms
Protections						
Peak current limit	I_{PEAK_LIMIT}	Sourcing, duty cycle = 40%	2.3	3.5	4.7	A
Valley current limit	I_{VALLEY_LIMIT}			2.5		A
Over-current protection (OCP) timer (8)	t_{OCP}			100		µs
Zero-current detection (ZCD) threshold	I_{ZCD}			100		mA
Output over-voltage (OV) limit	OV_{LIMIT}	As a percentage of V_{FB}		115		%
Thermal shutdown (8)	T_{SD}	Temperature rising		170		°C
Thermal shutdown hysteresis (8)	T_{SD_SYS}			25		°C

Note:

8) Not tested in production. Guaranteed by design and characterization.

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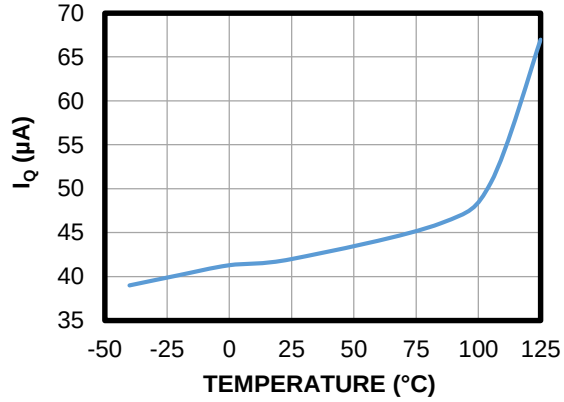
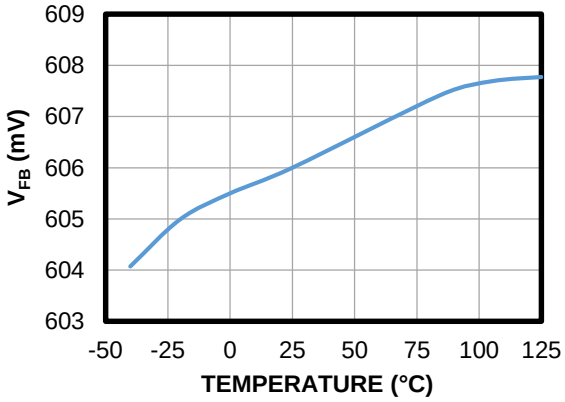
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

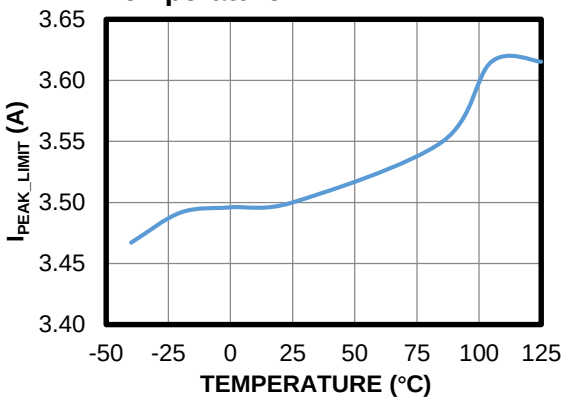
Quiescent Current vs. Temperature



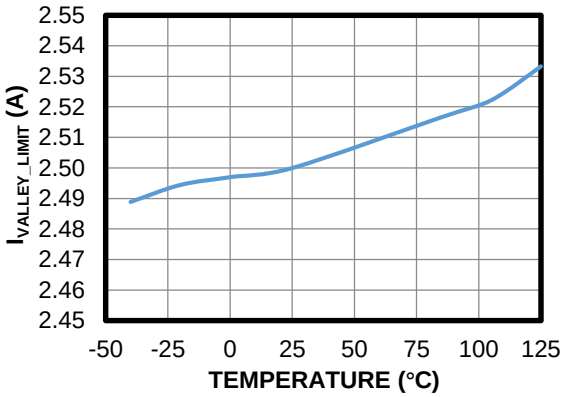
Feedback Voltage vs. Temperature



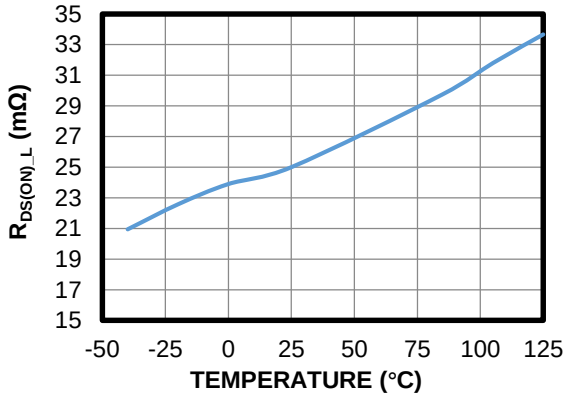
Peak Current Limit vs. Temperature



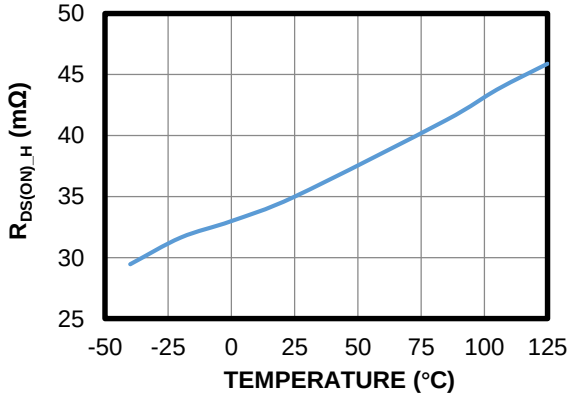
Valley Current Limit vs. Temperature



LS-FET On Resistance vs. Temperature (9)



HS-FET On Resistance vs. Temperature (9)



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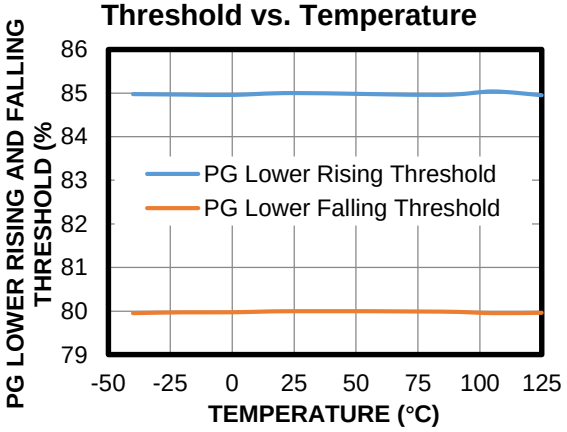
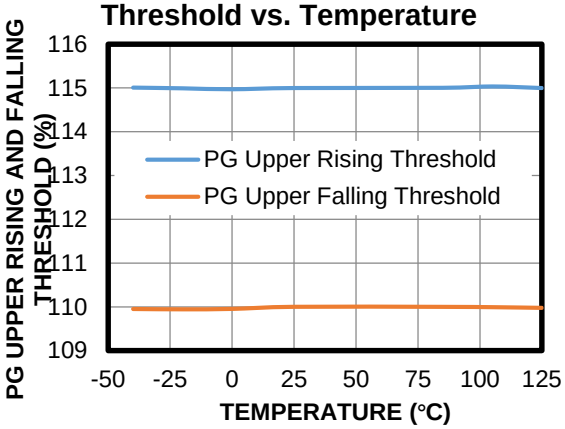
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = 25°C, unless otherwise noted.

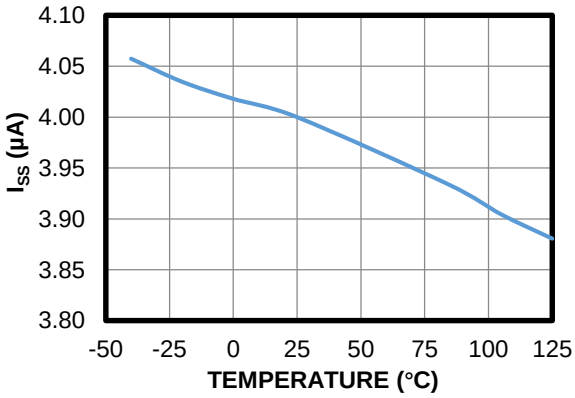
PG Lower Rising and Falling Threshold vs. Temperature



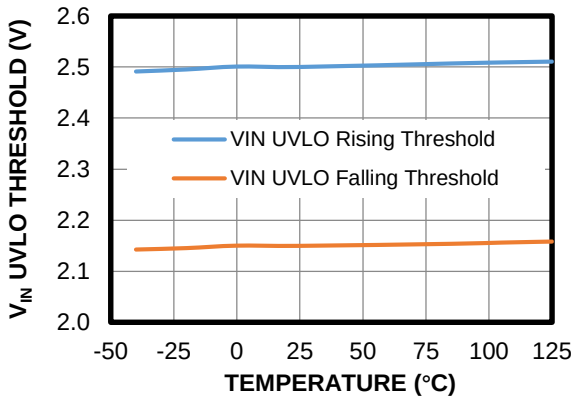
PG Upper Rising and Falling Threshold vs. Temperature



Soft-Start Current vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



Note:

9) This test item is evaluated under V_{IN} = 5V.

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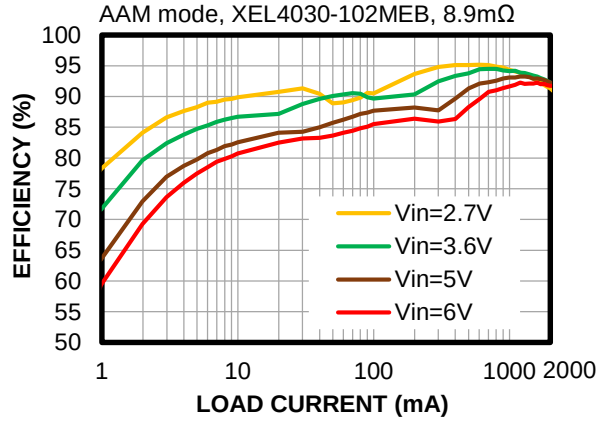
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

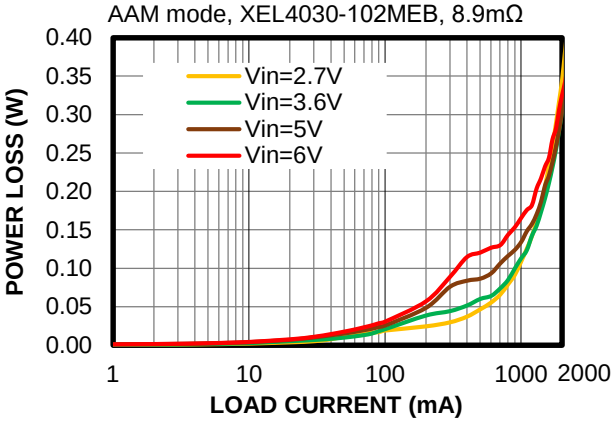
Efficiency vs. Load Current

AAM mode, XEL4030-102MEB, 8.9mΩ



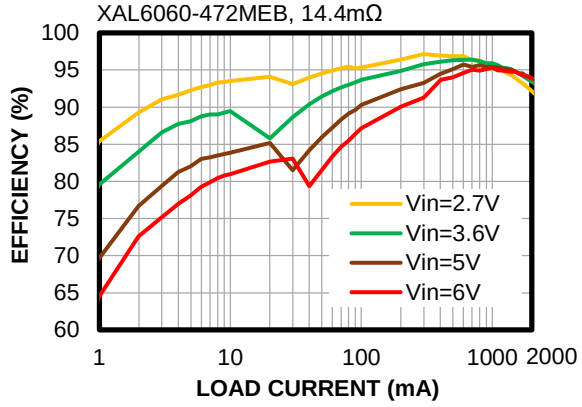
Power Loss vs. Load Current

AAM mode, XEL4030-102MEB, 8.9mΩ



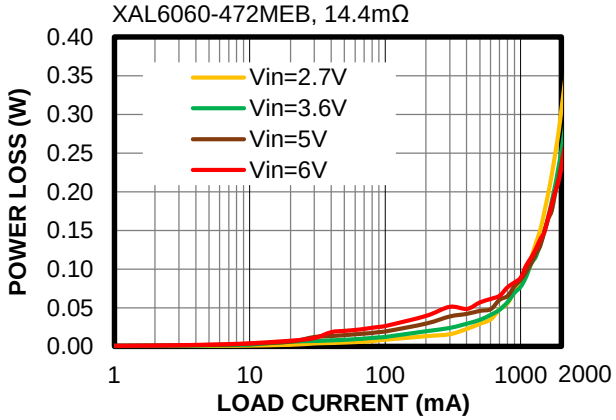
Efficiency vs. Load Current

AAM mode, f_{SW} = 450kHz,
XAL6060-472MEB, 14.4mΩ



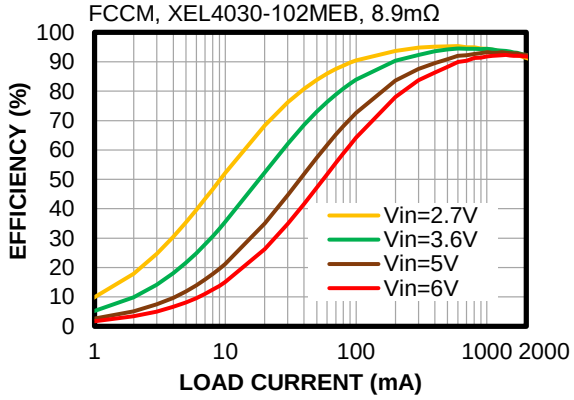
Power Loss vs. Load Current

AAM mode, f_{SW} = 450kHz,
XAL6060-472MEB, 14.4mΩ



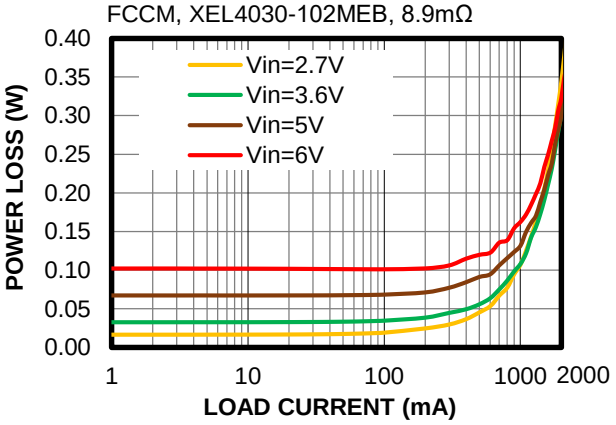
Efficiency vs. Load Current

FCCM, XEL4030-102MEB, 8.9mΩ



Power Loss vs. Load Current

FCCM, XEL4030-102MEB, 8.9mΩ



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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

FCCM, f_{SW} = 450kHz,
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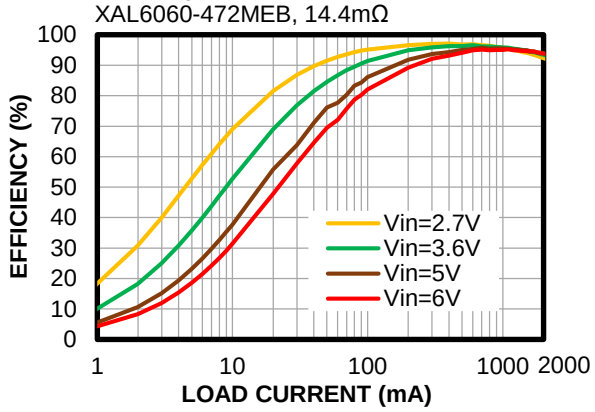
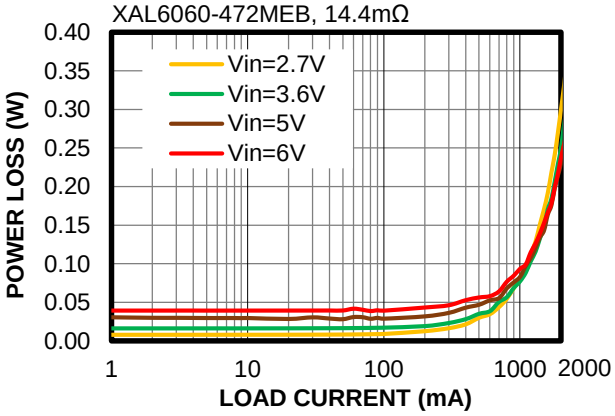


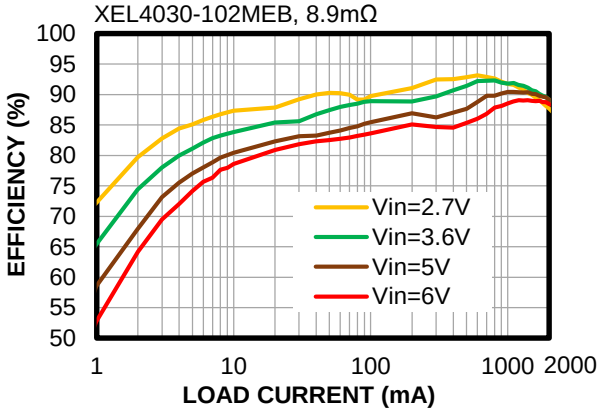
Power Loss vs. Load Current

FCCM, f_{SW} = 450kHz,
XAL6060-472MEB, 14.4mΩ



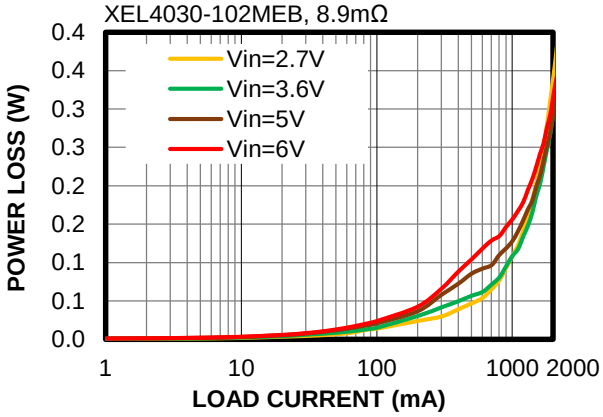
Efficiency vs. Load Current

V_{OUT} = 1.2V, AAM mode,
XEL4030-102MEB, 8.9mΩ



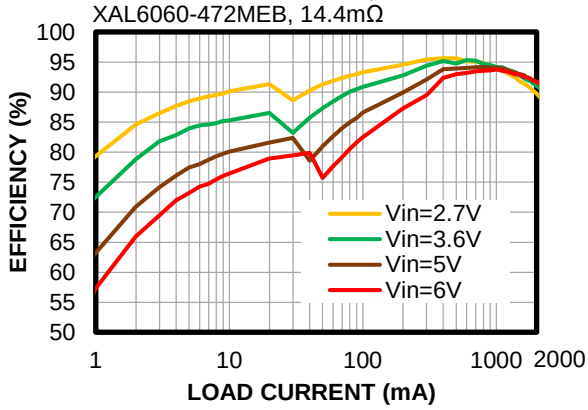
Power Loss vs. Load Current

V_{OUT} = 1.2V, AAM mode,
XEL4030-102MEB, 8.9mΩ



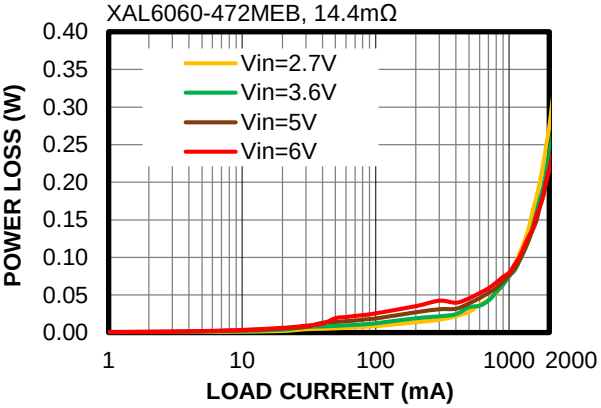
Efficiency vs. Load Current

V_{OUT} = 1.2V, AAM mode, f_{SW} = 450kHz,
XAL6060-472MEB, 14.4mΩ



Power Loss vs. Load Current

V_{OUT} = 1.2V, AAM mode, f_{SW} = 450kHz,
XAL6060-472MEB, 14.4mΩ



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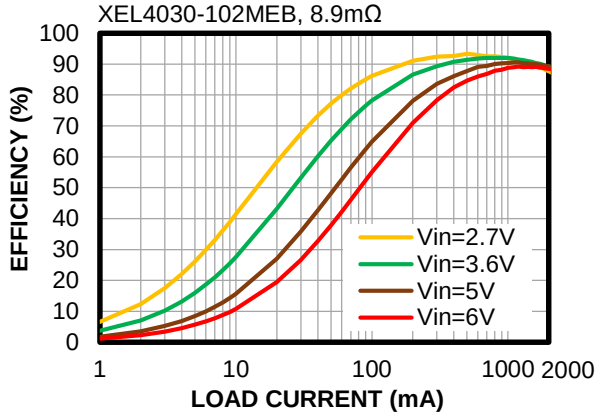
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

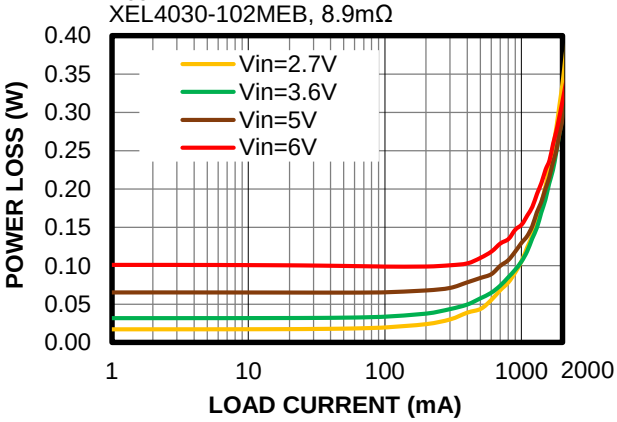
Efficiency vs. Load Current

V_{OUT} = 1.2V, FCCM,
XEL4030-102MEB, 8.9mΩ



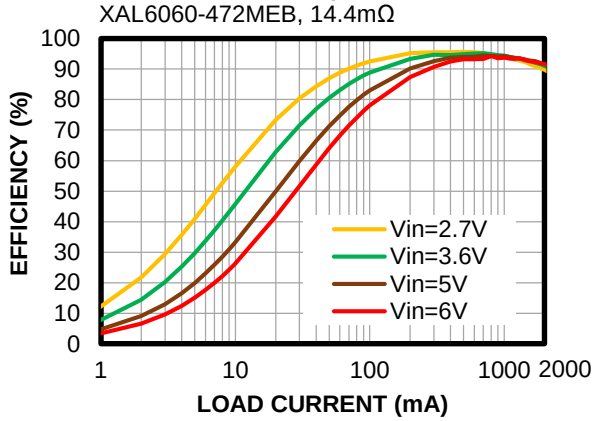
Power Loss vs. Load Current

V_{OUT} = 1.2V, FCCM,
XEL4030-102MEB, 8.9mΩ



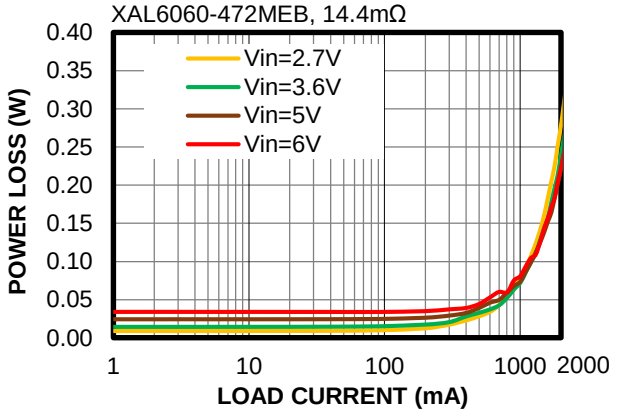
Efficiency vs. Load Current

V_{OUT} = 1.2V, FCCM, f_{SW} = 450kHz,
XAL6060-472MEB, 14.4mΩ



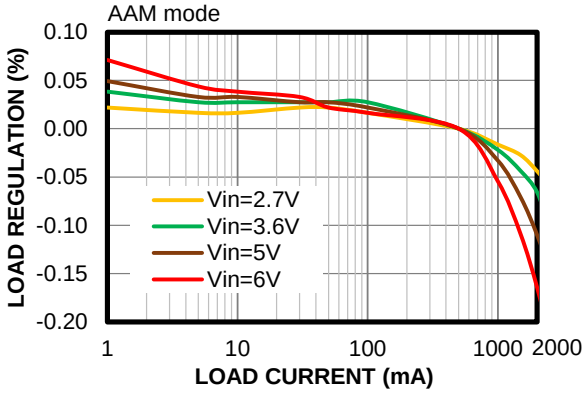
Power Loss vs. Load Current

V_{OUT} = 1.2V, FCCM, f_{SW} = 450kHz,
XAL6060-472MEB, 14.4mΩ



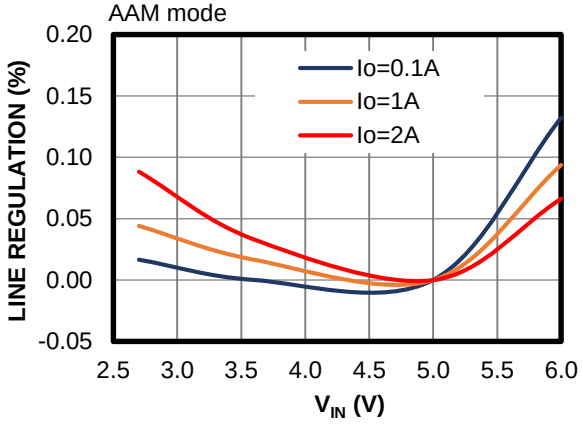
Load Regulation

AAM mode



Line Regulation

AAM mode



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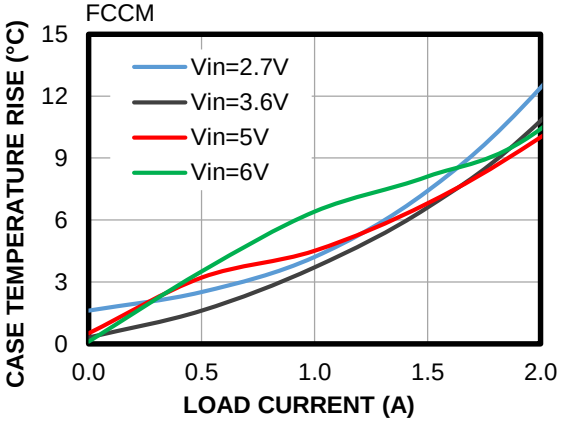
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

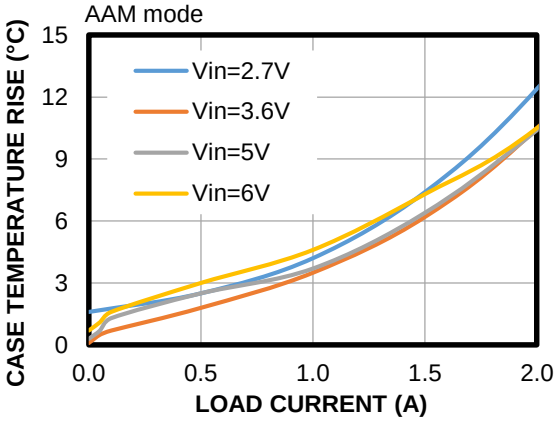
Case Temperature Rise

FCCM

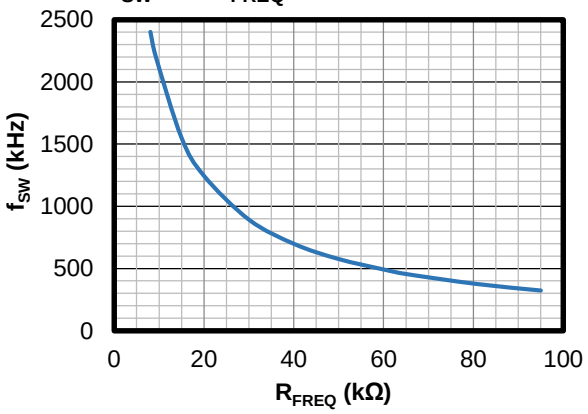


Case Temperature Rise

AAM mode



f_{SW} vs. R_{FREQ}



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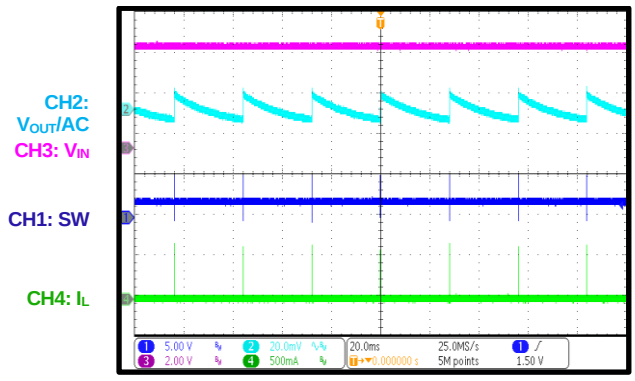
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

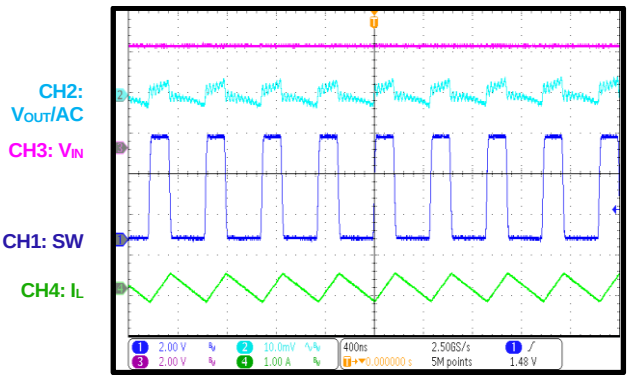
Steady State

I_{OUT} = 0A, AAM mode



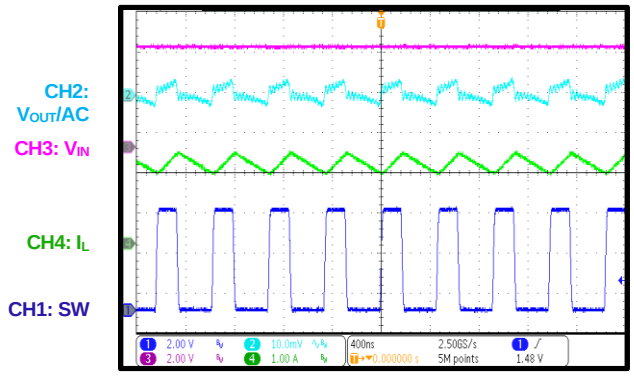
Steady State

I_{OUT} = 0A, FCCM



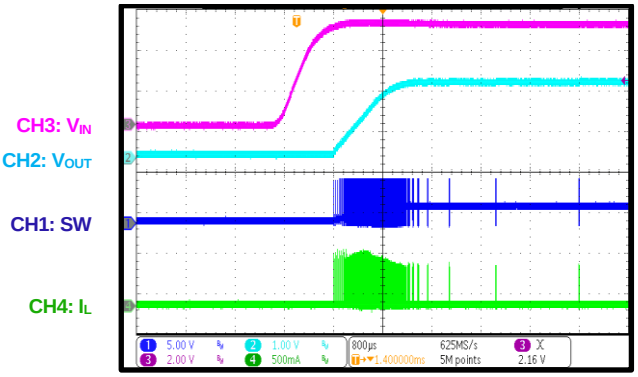
Steady State

I_{OUT} = 2A



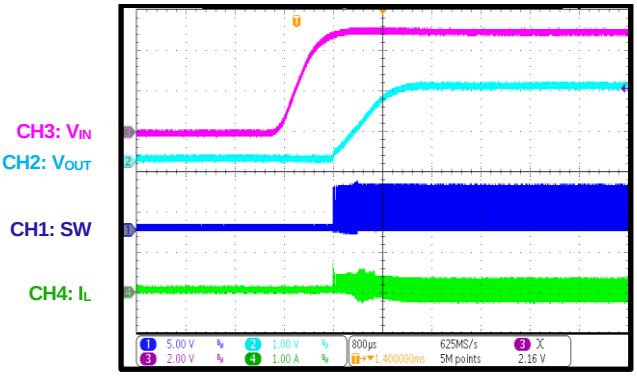
Start-Up through VIN

I_{OUT} = 0A, AAM mode



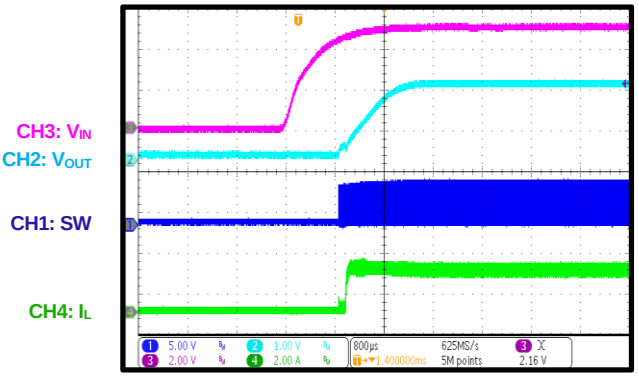
Start-Up through VIN

I_{OUT} = 0A, FCCM



Start-Up through VIN

I_{OUT} = 2A



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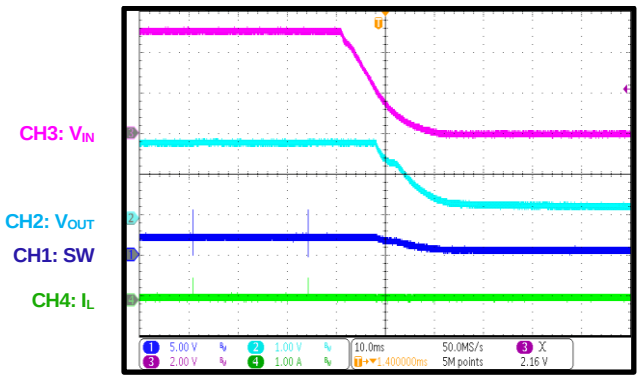
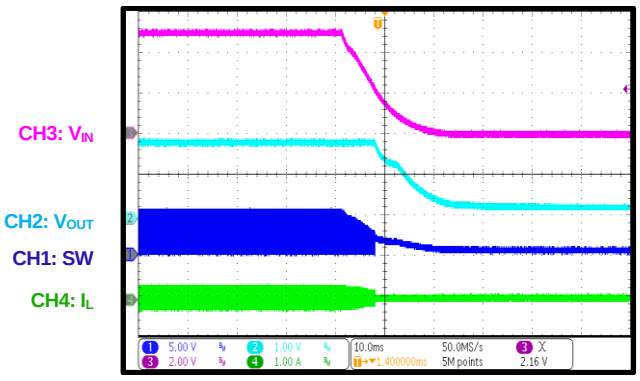
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

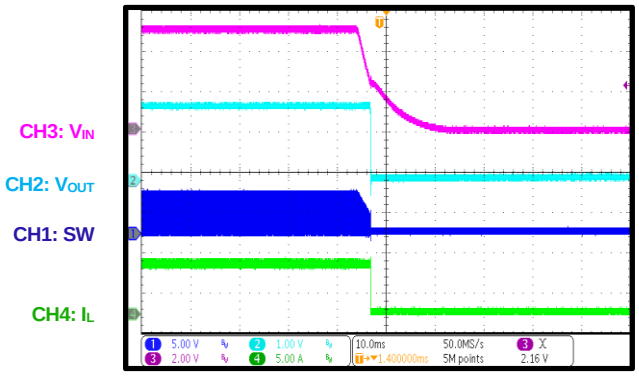
Shutdown through VIN
I_{OUT} = 0A, AAM mode



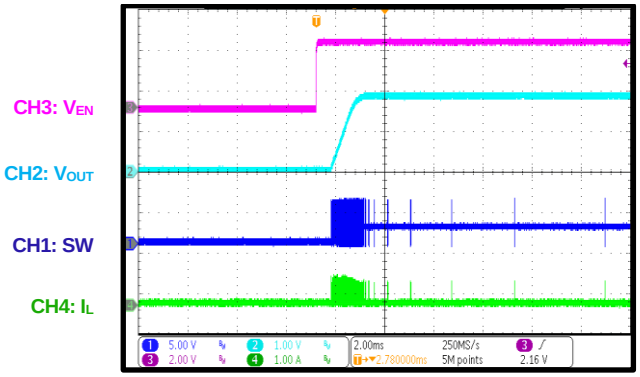
Shutdown through VIN
I_{OUT} = 0A, FCCM



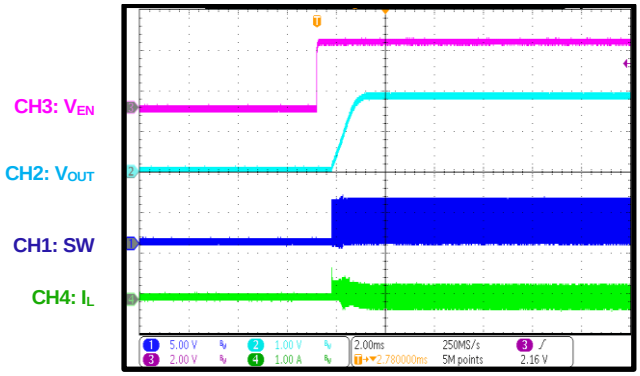
Shutdown through VIN
I_{OUT} = 2A



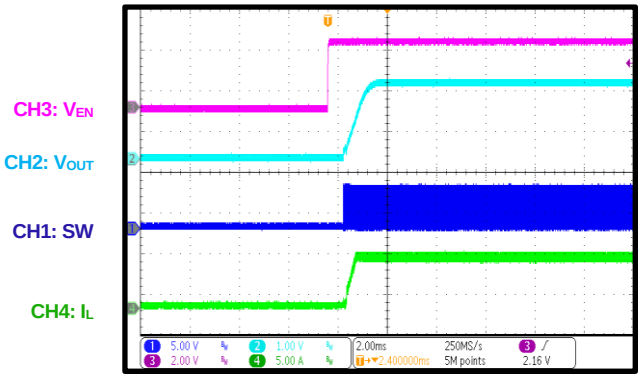
Start-Up through EN
I_{OUT} = 0A, AAM mode



Start-Up through EN
I_{OUT} = 0A, FCCM



Start-Up through EN
I_{OUT} = 2A



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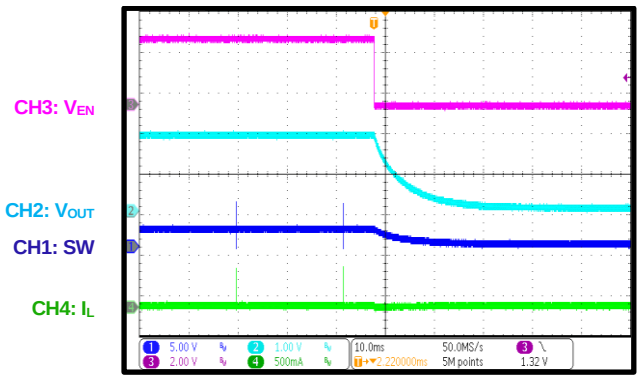
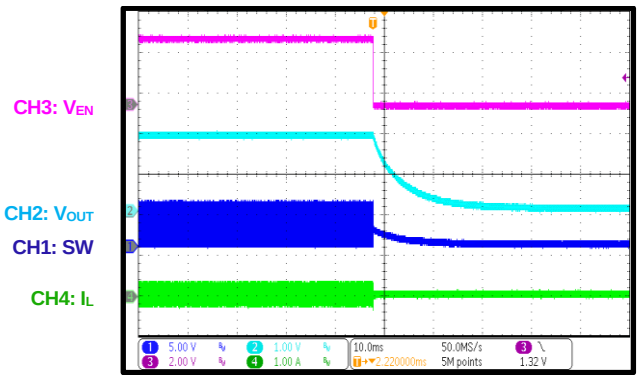
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

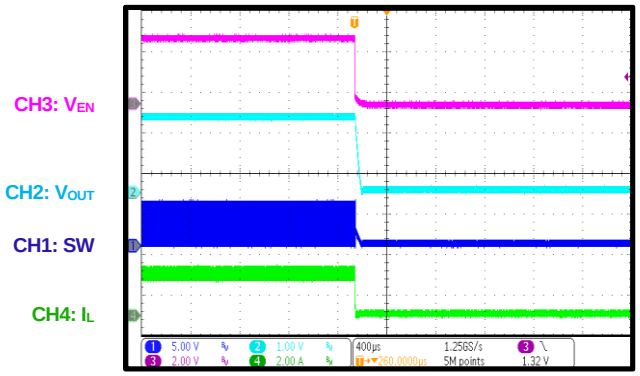
Shutdown through EN
I_{OUT} = 0A, AAM mode



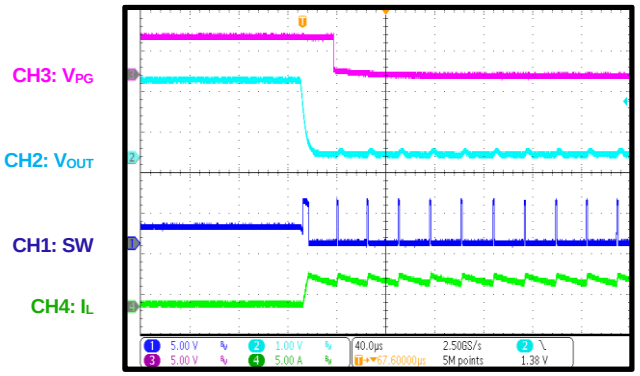
Shutdown through EN
I_{OUT} = 0A, FCCM



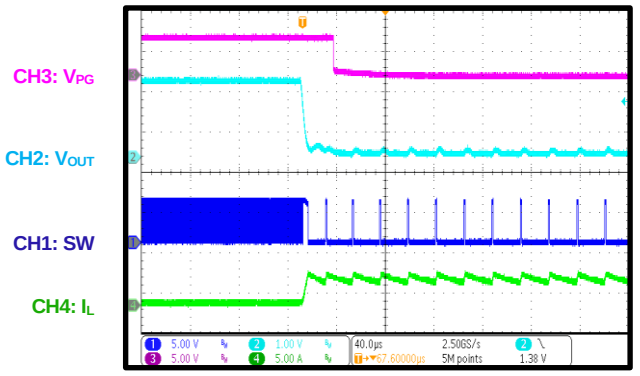
Shutdown through EN
I_{OUT} = 2A



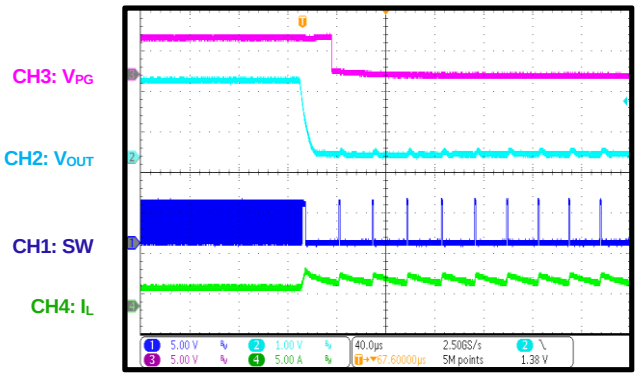
SCP Entry
I_{OUT} = 0A, AAM mode



SCP Entry
I_{OUT} = 0A, FCCM



SCP Entry
I_{OUT} = 2A



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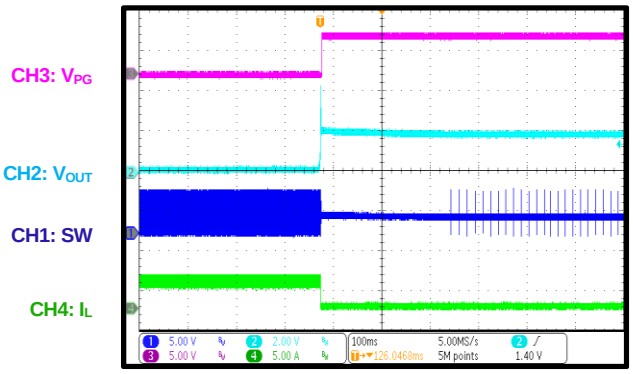
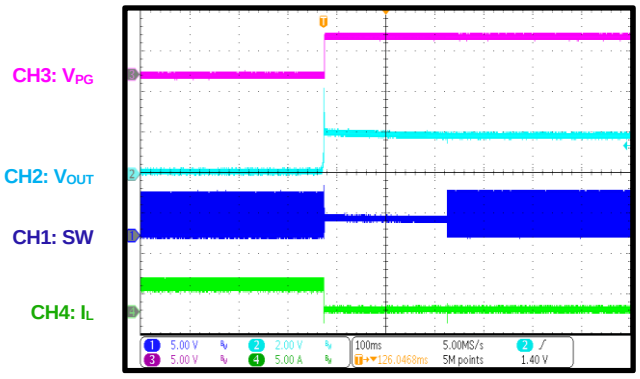
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

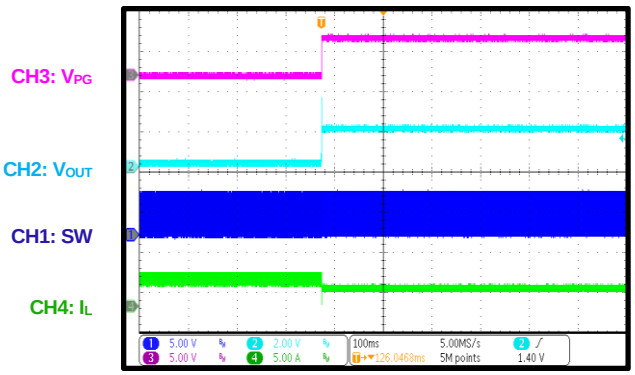
SCP Recovery
I_{OUT} = 0A, AAM mode



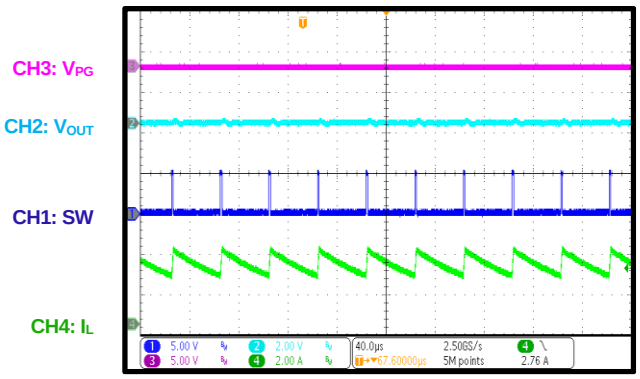
SCP Recovery
I_{OUT} = 0A, FCCM



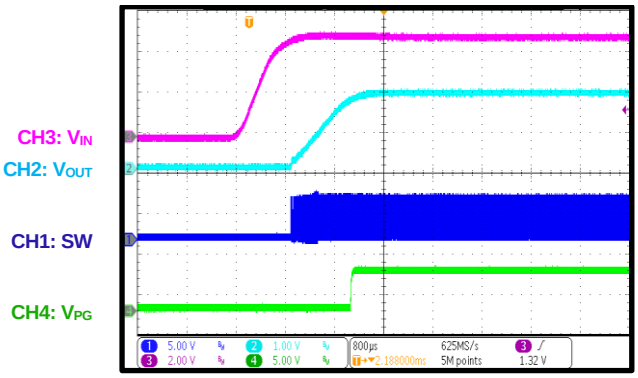
SCP Recovery
I_{OUT} = 2A



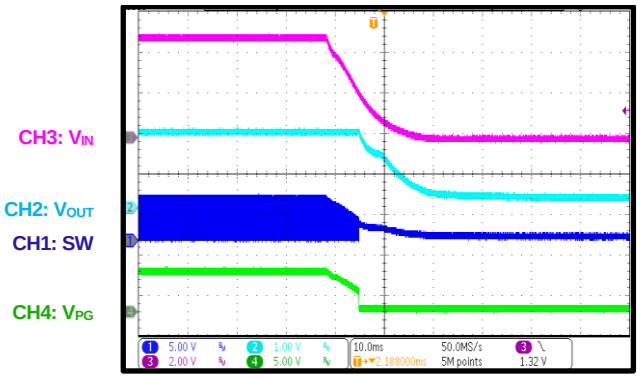
Short-Circuit Protection



PG Start-Up through VIN
I_{OUT} = 0A, FCCM



PG Shutdown through VIN
I_{OUT} = 0A, FCCM



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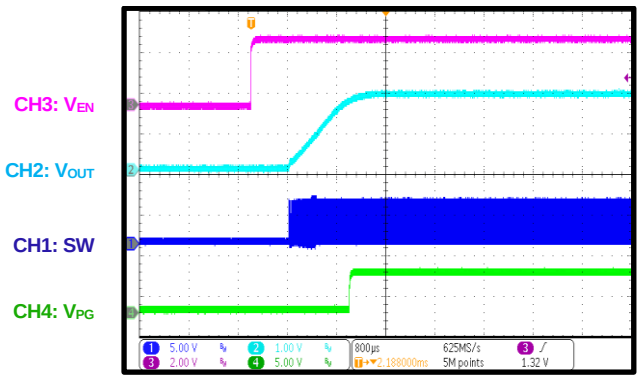
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 22µF, f_{SW} = 2.1MHz, T_A = 25°C, unless otherwise noted.

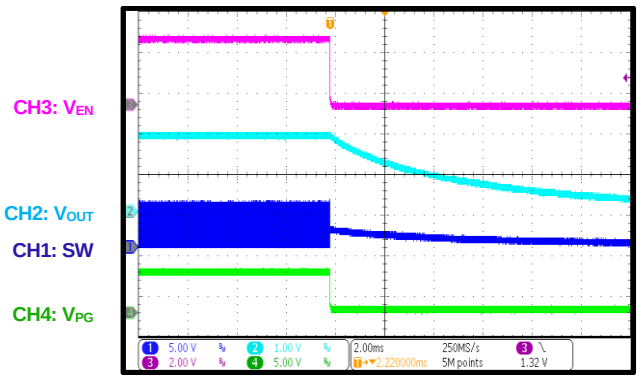
PG Start-Up through EN

I_{OUT} = 0A, FCCM



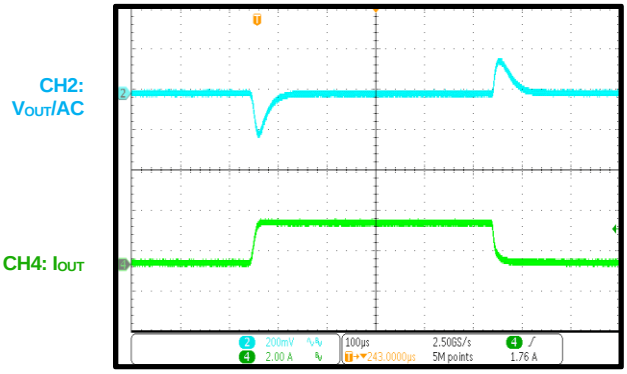
PG Shutdown through EN

I_{OUT} = 0A, FCCM



Load Transient

I_{OUT} = 0A to 2A, 1.6A/µs, AAM



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FUNCTIONAL BLOCK DIAGRAM

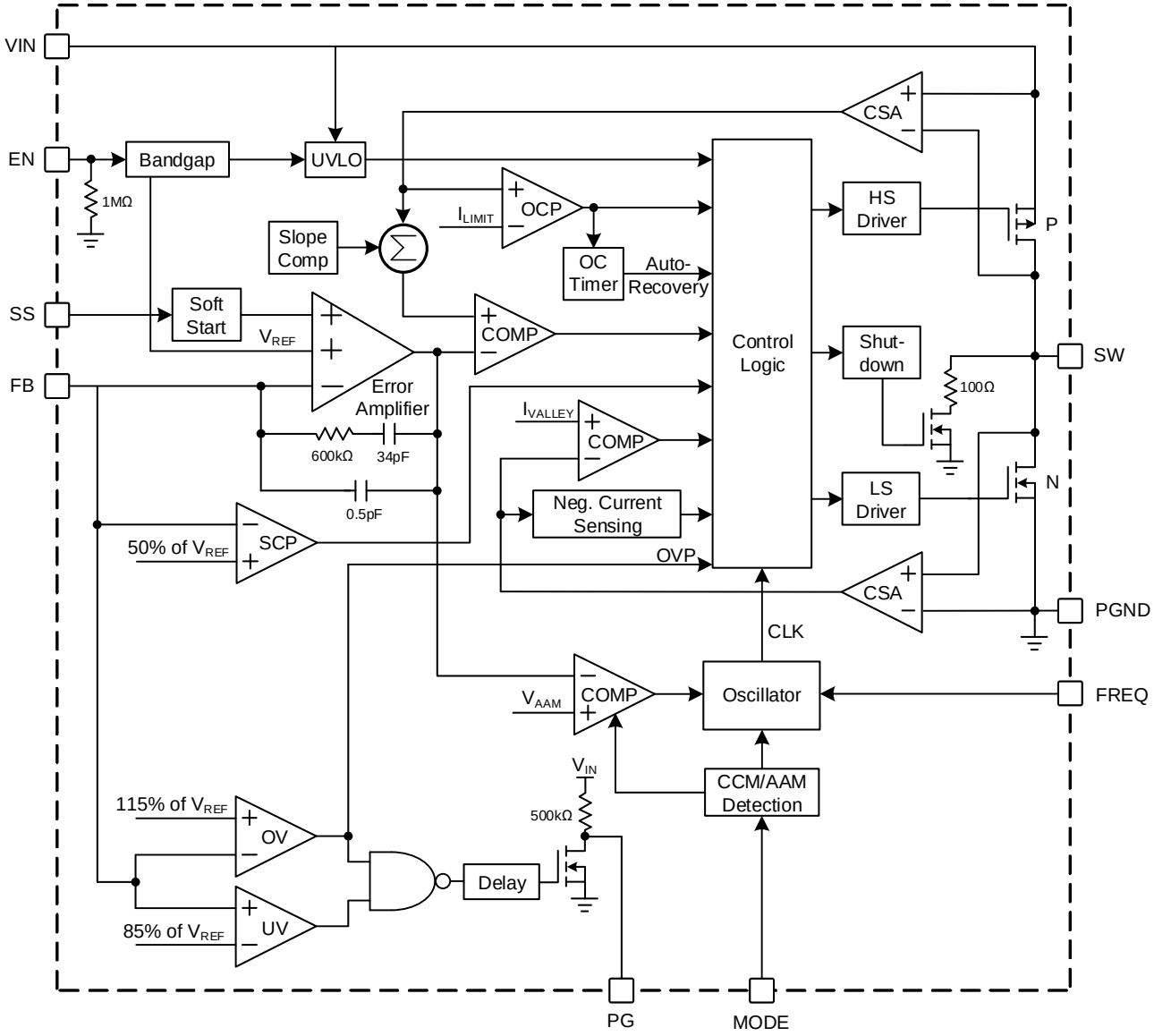

Figure 1: Functional Block Diagram

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OPERATION

The MPQ2242 is a fully integrated, synchronous, rectified, step-down, non-isolated switch-mode converter. It uses peak current mode control with internal compensation for faster transient response and cycle-by-cycle current limiting.

Figure 1 on page 18 shows the block diagram of the device. The MPQ2242 is available with a 2.7V to 6V input voltage (V_{IN}) supply range, and can achieve up to 2A of continuous output current (I_{OUT}), with excellent load and line regulation across an ambient temperature range of -40°C to +125°C. The output voltage (V_{OUT}) can be regulated as low as 0.606V.

The MPQ2242 is optimized for low-voltage portable applications where efficiency and small size are critical. It can operate with up to a 2.2MHz switching frequency (f_{SW}), which enables the use of a smaller inductor while still providing excellent efficiency. It also allows for high power conversion efficiency under light-load conditions with advanced asynchronous modulation (AAM) mode.

Forced Continuous Conduction Mode (FCCM)

Pull MODE high (>1.2V) to force the converter into forced continuous conduction mode (FCCM). In FCCM, the MPQ2242 operates in fixed-frequency, peak current control mode to regulate V_{OUT}, regardless of I_{OUT}.

An internal clock initiates an FCCM cycle. At the rising edge of the clock, the high-side MOSFET (HS-FET) turns on, and the inductor current (I_L) rises linearly to provide energy to the load. The HS-FET remains on until its current reaches the COMP voltage (V_{COMP}), which is the output of the internal error amplifier (EA). V_{COMP} is the difference between the output feedback (FB) voltage (V_{FB}) and the internal high-precision reference (V_{REF}). V_{COMP} determines how much energy should be transferred to the load; a higher load current results in a higher V_{COMP}.

When the HS-FET is off, the low-side MOSFET (LS-FET) turns on immediately and remains on until the next clock starts. During this time, I_L flows through the LS-FET. To avoid shoot-through, a dead time (DT) is inserted to avoid the HS-FET and LS-FET turning on simultaneously. For each turn-on/off period in a switching cycle, the HS-FET remains on or off for a set time limit.

Advanced Asynchronous Modulation (AAM) Mode

Pull MODE low (<0.4V) to force the converter into light-load AAM mode. There is an internally fixed AAM threshold voltage (V_{AAM}). Under light-load conditions, the value of V_{COMP} is low. If V_{COMP} exceeds V_{AAM}, the MPQ2242 first enters discontinuous conduction mode (DCM) with a fixed frequency, as long as I_L approaches 0A.

If the load decreases further, or there is no load and V_{COMP} drops below V_{AAM}, then the internal clock is blocked, and the MPQ2242 skips some pulses. During this time, V_{FB} is below V_{REF}, so V_{COMP} ramps up until it exceeds V_{AAM}. Then the internal clock is reset, and the crossover time is used as a benchmark for the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses.

As I_{OUT} increases from a light-load condition, V_{COMP} and f_{SW} both increase. If I_{OUT} exceeds the critical level while V_{COMP} is above V_{AAM}, the MPQ2242 resumes fixed-frequency control, which is the same as FCCM (see Figure 2).

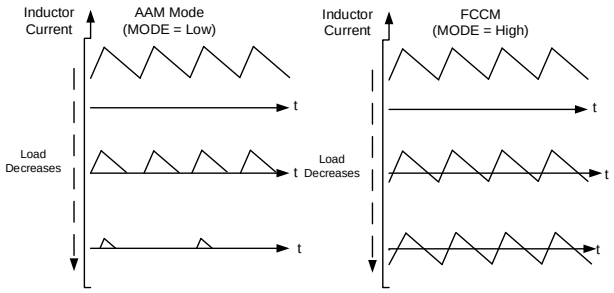

Figure 2 : AAM and FCCM Operation

Enable (EN)

The MPQ2242 can be enabled or disabled via a remote EN signal referenced to ground. The remote EN control operates with positive logic that is compatible with popular logic devices. Positive logic implies that when V_{IN} exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the converter is enabled by pulling EN above 1.2V. Float or ground the EN pin to disable the MPQ2242. There is an internal 1MΩ resistor placed from EN to ground.

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Oscillator

The oscillating frequency of the MPQ2242 can be configured via an external frequency resistor. The frequency resistor should be placed between FREQ and GND, as close to the device as possible. Select the R_{FREQ} value following the f_{SW} vs. R_{FREQ} curve on page 12.

Soft Start (SS) and Output Discharge

The MPQ2242 has soft start (SS). To avoid overshoot at start-up, SS ramps up V_{OUT} at a controlled slew rate when EN goes high.

When SS begins, an internal current source charges the external soft-start capacitor (C_{SS}). When the SS voltage (V_{SS}) falls below V_{REF}, V_{SS} overrides V_{REF} as the EA reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. After SS finishes, the MPQ2242 enters steady state. SS can be used for tracking and sequencing.

The soft-start time (t_{SS}) set by the external C_{SS} can be calculated with Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (1)$$

Where C_{SS} is the external soft-start capacitor, V_{REF} is the internal reference voltage (0.606V), and I_{SS} is the internal 4μA SS charge current.

When SS is floating, t_{SS} is 1ms after the internal setting. The final t_{SS} is either 1ms or the external C_{SS} setting time, whichever is longer. If the MPQ2242 is disabled or experiencing an input shutdown, the device discharges V_{OUT} to GND through an internal 100Ω resistor placed in parallel with the LS-FET.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} (which means the output has a pre-biased voltage) at start-up, then the HS-FET and LS-FET remain off until V_{SS} exceeds V_{FB}.

100% Duty Cycle

The MPQ2242 can operate with 100% duty cycle, which can extend the battery life. When V_{IN} is too low to regulate the output, the device turns the HS-FET completely on to achieve the maximum V_{OUT}.

Power Good (PG) Indicator

The MPQ2242 has power good (PG) indication. PG is the open drain of the MOSFET. When V_{IN} is present, the MOSFET turns on and PG is pulled to GND before SS is ready. If V_{OUT} is within a ±15% window of the rated voltage set by FB, then PG is pulled up to V_{IN} by an internal resistor after a set delay time. If V_{FB} moves outside the ±15% range with a hysteresis, the device pulls PG low to indicate an output failure status.

Over-Current Protection (OCP)

The MPQ2242 has 3.5A cycle-by-cycle peak current limit control. I_L is monitored while the HS-FET is on. Once I_L reaches the peak current limit (I_{PEAK_LIMIT}), the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and I_L decreases. The HS-FET does not turn on again until I_L falls below the valley current limit (I_{VALLEY_LIMIT}), which prevents I_L from running away and possibly damaging the components.

When I_{VALLEY_LIMIT} is triggered, the over-current protection (OCP) timer starts immediately. The OCP timer is set to 100μs. If I_{VALLEY_LIMIT} is reached within this 100μs timeframe during each cycle, short-circuit protection (SCP) is triggered.

Short-Circuit Protection (SCP)

When a short circuit occurs, the MPQ2242 immediately reaches its current limit. Meanwhile, V_{OUT} drops until V_{FB} is below 50% of V_{REF} (0.606V). The device considers this an output dead short, and triggers SCP immediately.

In SCP, I_L is monitored while the HS-FET is on. Once I_L reaches I_{PEAK_LIMIT}, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and I_L drops. The HS-FET does not turn on again until I_L drops below I_{VALLEY_LIMIT}. The device repeats this operation until the short circuit disappears and the output returns to the regulation level. This protection mode prevents I_L from running away and possibly damaging the components.

Over-Voltage Protection (OVP)

The MPQ2242 monitors V_{OUT} through the FB pin to detect over-voltage (OV) conditions. If V_{FB} exceeds 115% of V_{REF} (0.606V), over-voltage protection (OVP) is triggered, and the LS-FET turns on to discharge V_{OUT} until I_L drops to 0A.

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Meanwhile, the HS-FET remains off. Then the LS-FET shuts off, and V_{OUT} is discharged through the internal 100Ω resistor placed in parallel with the LS-FET. The controller does not begin to switch until V_{OUT} is within regulation.

Under-Voltage Lockout Protection (UVLO)

The MPQ2242 has input UVLO protection to ensure reliable output power. Assuming EN is active, the MPQ2242 starts up once V_{IN} exceeds the UVLO rising threshold. Once V_{IN} drops below the UVLO falling threshold, the device shuts down. This function prevents the device from operating at an insufficient supply voltage. This is a non-latch protection.

Thermal Shutdown

The MPQ2242 employs thermal protection by internally monitoring the IC temperature. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature (T_J) exceeds the threshold value (typically 170°C), the entire chip shuts down. This is a non-latch protection. There is a 25°C hysteresis. Once T_J drops to about 145°C, the device initiates a soft start resumes normal operation.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank start-up errors. If the soft-start block is enabled, it first holds its SS output low to ensure the rest of the circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} UVLO, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggers. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to FB sets V_{OUT} (see Figure 3). The feedback resistor (R4) must account for both stability and dynamic response, so it cannot be too large or too small. R5 is estimated to be 100kΩ. R6 can be calculated using Equation (2):

$$R6 = \frac{R5}{\frac{V_{OUT}}{0.606} - 1} \quad (2)$$

Using a T-type feedback network is highly recommended (see Figure 3).

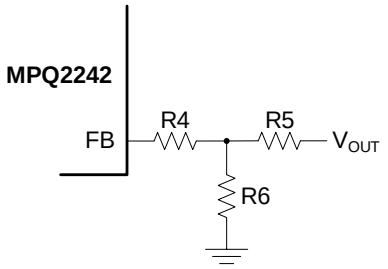

Figure 3: Feedback Network

The R5 and R4 values set the loop bandwidth. Generally, a higher R5 + R4 value results in lower bandwidth. To ensure loop stability, it is strongly recommended to limit the bandwidth at about 10% of f_{SW}.

Table 1 lists the recommended feedback divider resistor values for common output voltages. Check the loop analysis before using in application. Change the resistance of R_T for loop stability if necessary.

Table 1: Resistances for Typical V_{OUT}

V_{OUT} (V)	R4 (kΩ)	R5 (kΩ)	R6 (kΩ)
1.2	100	100 (1%)	100 (1%)
1.5	100	100 (1%)	66.5 (1%)
1.8	100	100 (1%)	49.9 (1%)
2.5	100	100 (1%)	31.6 (1%)
3.3	100	100 (1%)	22.1 (1%)

Selecting the Inductor

The inductor must supply constant current to the output load while being driven by the switching V_{IN}. For a default 2.1MHz application, a 0.47µH to 1.5µH inductor is recommended. For the highest efficiency, chose an inductor with a DC resistance below 15mΩ. A larger-value inductor results in less ripple current and a lower output ripple voltage. However, larger-value inductors are physically larger, and have a higher series resistance and/or lower saturation current.

A good rule to determine the inductance (L) is to make the inductor ripple current approximately 30% of the maximum load current. Ensure that the peak inductor current is below the device peak current limit. L can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum peak inductor current (I_{LP}). I_{LP} can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Do not use other capacitor types, such as Y5V and Z5U, because they lose too much capacitance with frequency, temperature, and bias voltage.

Place the input capacitors (C_{IN}) as close to VIN as possible. For most applications, a 22µF capacitor is sufficient. For applications with higher V_{OUT}, use a 47µF capacitor to improve system stability. To get a small solution size, it is recommended to choose a proper package size capacitor that has a rating voltage compliant with the input specifications.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The rating should exceed the converter's maximum input ripple current.

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The input ripple current (I_{CIN}) can be calculated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, estimated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose C_{IN} with an RMS current rating that is greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (0.1µF) placed as close to the IC as possible. The input capacitance determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system design, choose C_{IN} to meet the relevant specifications.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Low-ESR ceramic capacitors are recommended for their small size and ability to keep the output voltage ripple low. Electrolytic and polymer capacitors may also be used.

The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

Where R_{ESR} is the C_{OUT} equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{\ 2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

When choosing the output capacitance, consider the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, the energy stored in the inductor is transferred to C_{OUT}, which causes its voltage to rise. To achieve a proper overshoot relative to the regulated voltage, C_{OUT} can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^{\ 2} \times L}{V_{OUT}^{\ 2} \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUTMAX} / V_{OUT} is the maximum allowable overshoot.

After calculating the capacitance required for both the ripple and overshoot, choose the larger of the calculated values. The C_{OUT} characteristics also affect the stability of the regulation system. The MPQ2242 can be optimized for a wide range of capacitances and ESR values.

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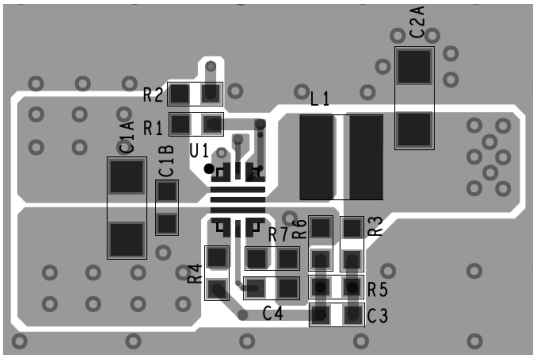
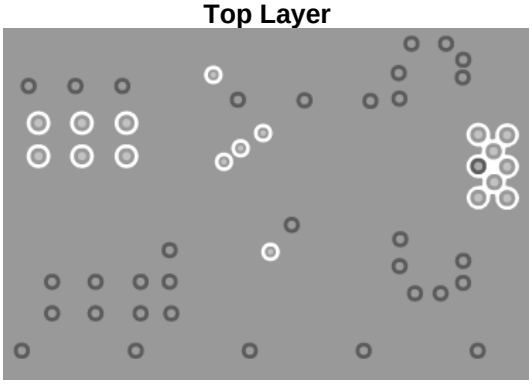
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 4 and follow the guidelines below:

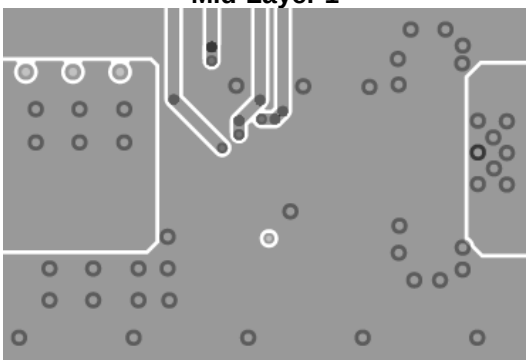
1. Place high-current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place C_{IN} as close to VIN as possible to minimize high-frequency noise.
3. Place the feedback resistor divider as close as possible to FB.
4. Route the FB trace away from the switching (SW) node.
5. Connect the bottom VIN and SW pads to a large copper area to improve thermal performance.
6. Use large copper areas for power planes (VIN, SW, OUT, and GND) to minimize conduction loss and thermal stress.
7. Use multiple vias to connect the power planes to the internal layers.



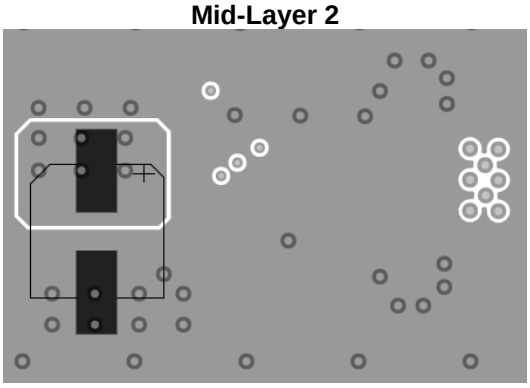
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 4: Recommended PCB Layout (10)

Note:

10) The recommended PCB layout is based on the circuit in Figure 5 on page 25.

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TYPICAL APPLICATION CIRCUITS

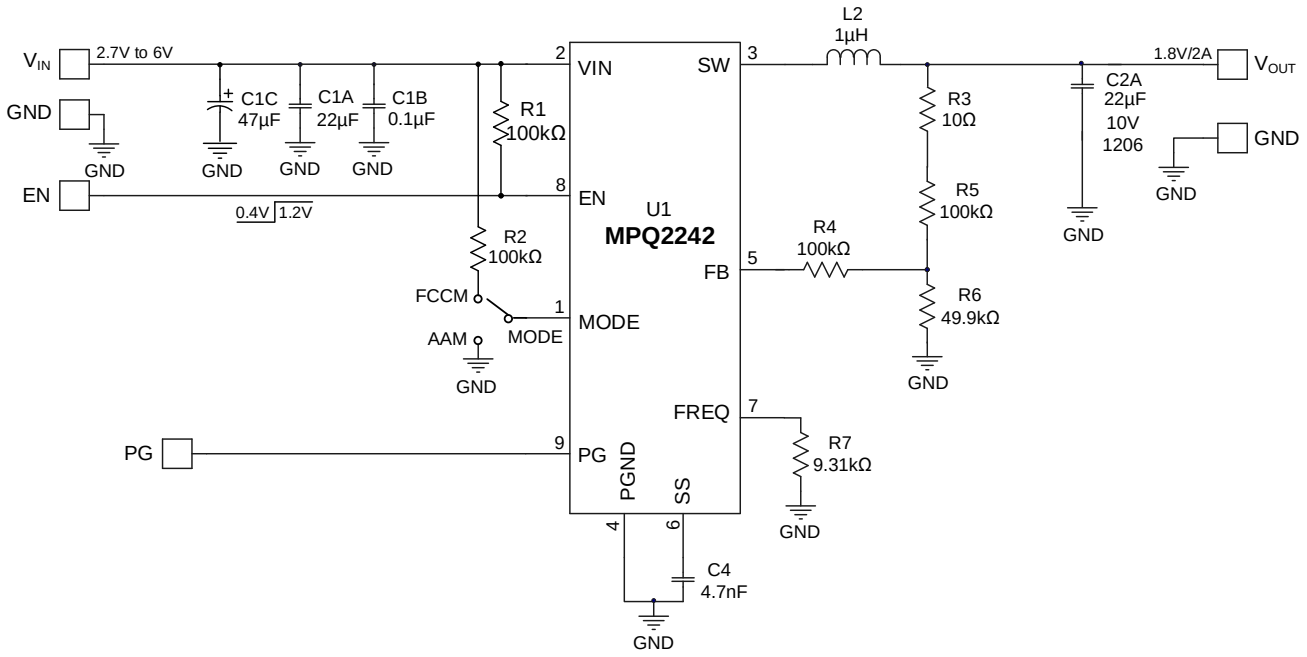

Figure 5: Typical Application Circuit (V_{OUT} = 1.8V, I_{OUT} = 2A)

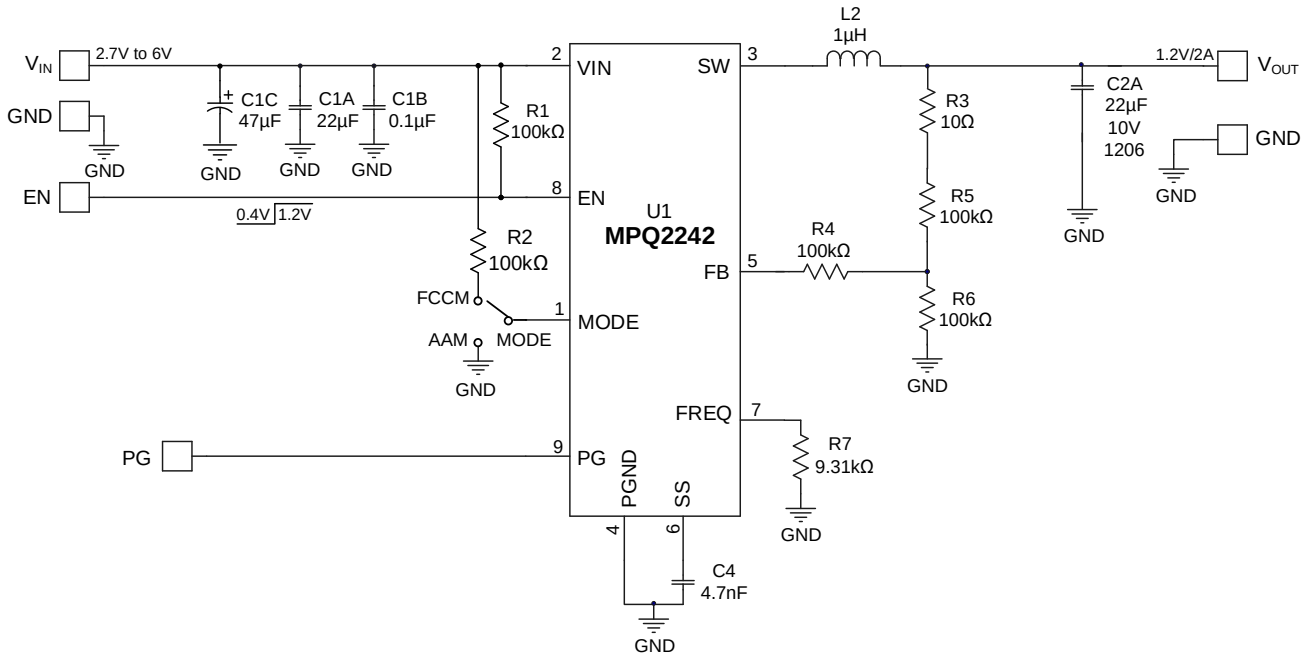

Figure 6: Typical Application Circuit (V_{OUT} = 1.2V, I_{OUT} = 2A)

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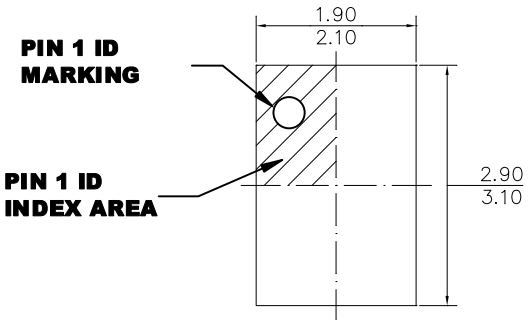
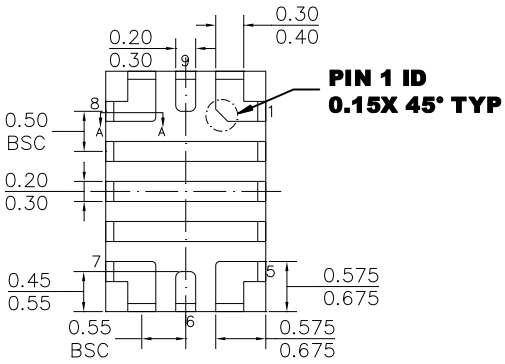
PACKAGE INFORMATION

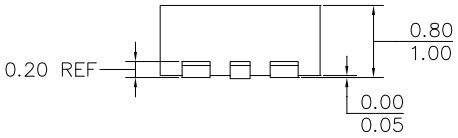
QFN-9 (2mmx3mm)



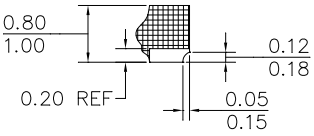
TOP VIEW



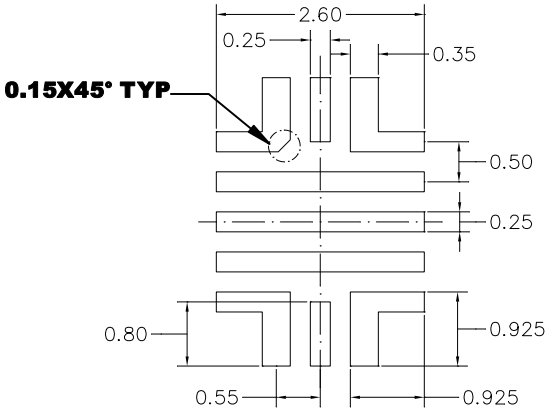
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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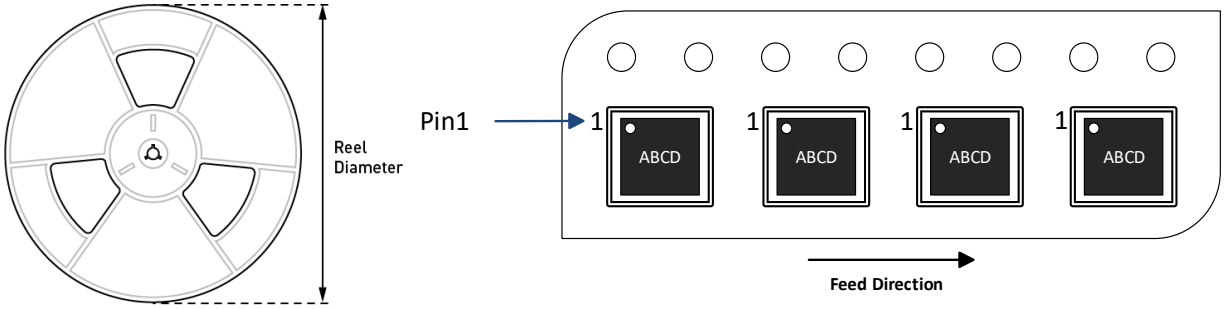
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ2242GDE-AEC1-Z	QFN-9 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/16/2022	Initial Release	-

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