MPM54322

16V, 3A, Dual-Output Power Module with I²C Interface

DESCRIPTION

The MPM54322 is a dual 3A power module that integrates two high-efficiency, step-down DC/DC converter ICs, two inductors, and selected passive components onto a single over-molded package.

The two outputs of the MPM54322 can be paralleled for up to 6A of current. The power module offers an active current balancing function that allows equal current sharing for the outputs in parallel operation.

The MPM54322 offers a dedicated, configurable low-dropout (LDO) regulator with up to 500mA of output current (I_{OUT}) to provide ultra-low noise output.

The MPM54322 adopts constant-on-time (COT) control to provide fast transient response and minimize the required output capacitance.

The MPM54322 provides on-chip non-volatile memory (NVM) to store and restore device configurations. Operation parameters, timing, and protection thresholds are fully configurable via the I²C bus. The MPM54322 offers on-chip current and voltage sensing that allows accurate input voltage (V_{IN}), output voltage (V_{OUT}), I_{OUT}, and temperature telemetry via the I²C bus.

The MPM54322 is available in an ultra-thin ECLGA (5mmx5.5mmx1.85) package.

FEATURES

- Wide 3V to 16V Input Voltage (V_{INx}, where x = 1 or 2) Range
- Dual 3A and up to 6A for Parallel Operation
- MODE Pin to Select Output Voltage (V_{OUTx}, where x = 1 or 2), Parallel Mode, and Timing via Pin-Strapping
- Remote Sense for Both Output Channels
- Configurable 500mA-Rated Low-Dropout (LDO) Regulator with V_{IN} up to 3.6V
- Configurable Soft Start, Soft Shutdown, and Delay with MPS-Patented FLEX-Timer Sequence Control
- Configurable Reference Voltage (V_{REF}) and Slew Rate
- Configurable Switching Frequency (f_{SW}): 500kHz, 750kHz, 1MHz, and 1.25MHz
- Accurate V_{OUT}, Output Current (I_{OUT}), and Junction Temperature (T_J) Telemetry
- Open-Drain Power Good (PG) Indication and General Status Interrupt
- Available in an Ultra-Thin ECLGA (5mmx5.5mmx1.85mm) Package

APPLICATIONS

- Storage and Networking
- FPGA and ASIC Power Supplies
- Computing and Telecommunication

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION

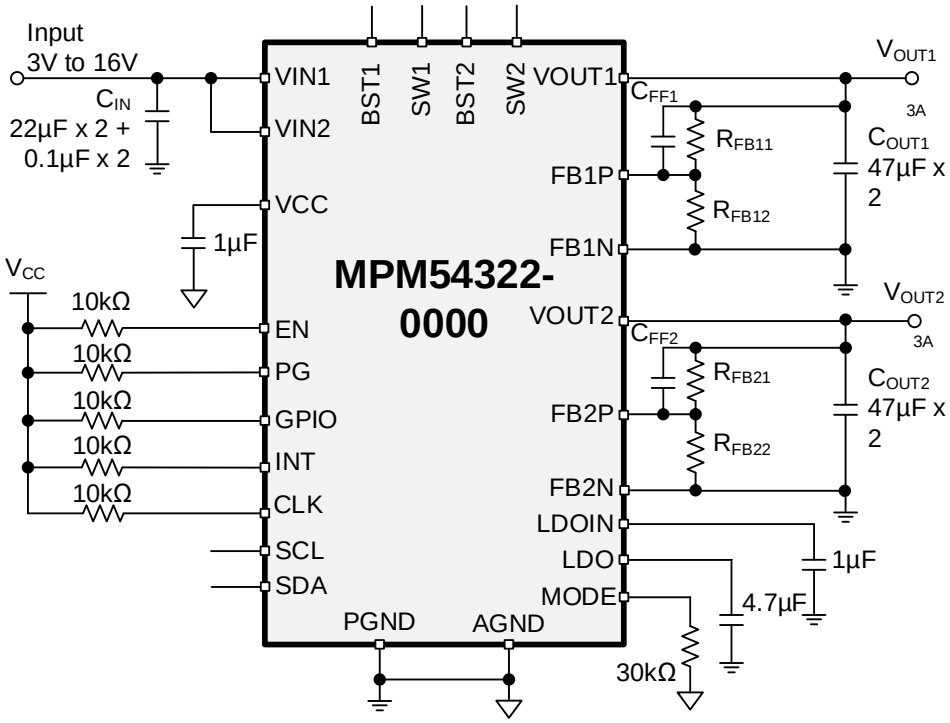


Figure 1: Dual-Output Operation with External Divider

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number *, **	Package	Top Marking	MSL Rating
MPM54322GPB-xxxx***	ECLGA (5mmx5.5mmx1.85mm)	*See Below*	3
MPM54322GPB-0000***			

* For Tray, add suffix -T (e.g. MPM54322GPB-xxxx-T).

** For Tape & Reel, add suffix -Z (e.g. MPM54322GPB-xxxx-Z).

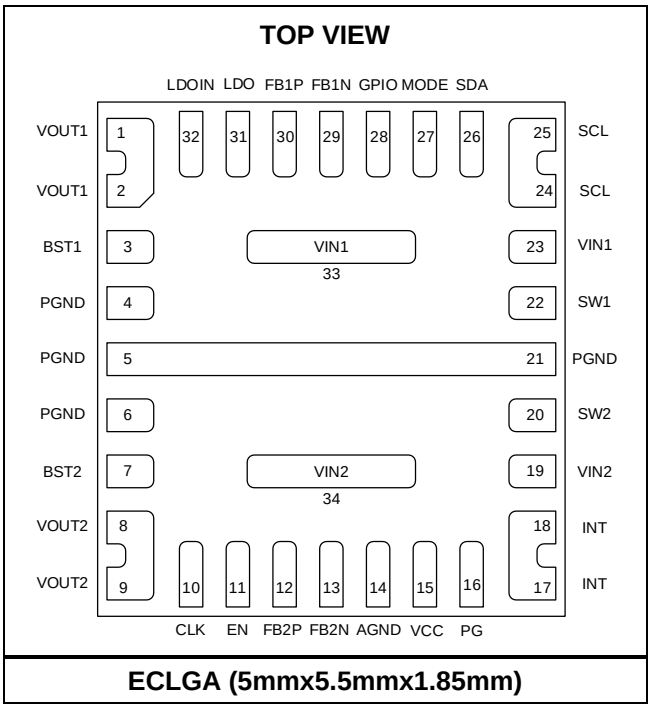
*** “xxxx” is the configuration code identifier for the register setting stored in the NVM. The default number is “0000”. Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code. The MPM54322GPB-0000 is the default version.

TOP MARKING

MPSYYWW
MP54322
LLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP54322: Part number
LLLLLLL: Lot number
M: Module

PACKAGE REFERENCE



ECLGA (5mmx5.5mmx1.85mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 2	VOUT1	**Output of buck converter 1 (buck 1).** Make the VOUT1 connection with a wide PCB trace.
8, 9	VOUT2	**Output of buck converter 2 (buck 2).** Make the VOUT2 connection with a wide PCB trace.
3	BST1	**Bootstrap of buck 1.** Float the BST1 pin.
22	SW1	**switching node of buck 1.** Float the SW1 pin.
4, 5, 6, 21	PGND	**Power ground.** Connect PGND with wide copper traces, and place sufficient vias on the ground plane for improved thermal performance.
20	SW2	**Switching node of buck 2.** Float the SW2 pin.
7	BST2	**Bootstrap of buck 2.** Float the BST2 pin.
10	CLK	**Clock pin for FLEX-time control.**
11	EN	**Enable pin of buck 1, buck 2, and low-dropout (LDO) regulator.** Pull the EN pin high to enable the power module.
12	FB2P	**Positive feedback for buck 2's remote sense.** Connect the FB2P pin to PGND for dual-phase operation.
13	FB2N	**Negative feedback for buck 2's remote sense.** Connect the FB2N pin to PGND for dual-phase operation.
14	AGND	**Analog ground.** Connect AGND to PGND via a single-point connection.
15	VCC	**Internal 3.6V LDO output.** Decouple the VCC pin with a 1μF ceramic capacitor. Place the decoupling capacitor as close to the VCC pin as possible.
16	PG	**Power good output, open drain.** The PG pin pulls low when any enabled regulator falls below the under-voltage (UV) threshold and/or all regulators are disabled.
17, 18	INT	**General status interrupt.** The INT pin is an open-drain output. The power module asserts INT low to communicate any one (or more) critical event(s) to the host. INT remains asserted until the appropriate registers are explicitly cleared, or the power module is reset. Float this pin if it is not used.
19,34	VIN2	**Supply voltage of buck 2.** Ceramic capacitors are required to decouple the input rail. Connect VIN2 using a wide PCB trace. VIN1 and VIN2 must be connected to the same bus voltage.
23, 33	VIN1	**Supply voltage of buck 1.** Ceramic capacitors are required to decouple the input rail. Connect VIN1 using a wide PCB trace. VIN1 and VIN2 must be connected to the same bus voltage.
24, 25	SCL	**I²C bus clock.** The SCL pin supports a 1.8V/3.3V bus voltage. If this pin is not used, SCL should be pulled up to VCC.
26	SDA	**I²C bus data.** The SDA pin supports a 1.8V/3.3V bus voltage. If this pin is not used, SDA should be pulled up to VCC.
27	MODE	**Mode selection pin.** Connect a resistor to this pin to select internal non-volatile memory (NVM) configurations. See the MODE-Determined MTP Configuration section on page 17 for more details.
28	GPIO	**GPIO pin.** The GPIO pin can be configured into the start-up sequence with the regulators or an analog input for the analog-to-digital converter (ADC) circuit. Float this pin if it is not used.
29	FB1N	**Negative feedback for buck 1's remote sense.**
30	FB1P	**Positive feedback for buck 1's remote sense.**
31	LDO	**Output of the LDO.** This LDO is rated for 500mA of output current. Float this pin if the LDO is not used.
32	LDOIN	**Input of the LDO.** The LDOIN pin's voltage should be below 3.6V. Float this pin if the LDO is not used.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{SW1}, V_{SW2} ..... -0.3V to V_{IN} + 0.3V
V_{BST1}, V_{BST2} ..... $V_{SW1/2}$ + 4V
V_{OUT1}, V_{OUT2} 6V
All other pins ..... -0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2)
ECLGA (5mmx5.5mm)..... ..... 6.28W
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN1}, V_{IN2}) ..... 3V to 16V
Output voltage (V_{OUT1}, V_{OUT2})..... 0.3V to 5.5V (4)
Input and output voltage (LDO)..... 3.6V max
Output current (LDO)..... 500mA
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) (6) (7) (8)

ECLGA (5mmx5.5mmx1.86mm)

θ_{JA} .... 19.9°C/W
θ_{JC_TOP} .... 0.97°C/W
θ_{JB} .... 14.8°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) When V_{OUT} is below 3.8V, V_{OUT} can be set by the internal divider via the I²C. When V_{OUT} exceeds 3.8V, V_{OUT} must be set by the external divider.
5) θ_{JA} is the junction-to-ambient thermal resistance. θ_{JC_TOP} is the junction-to-case top thermal characterization parameter. θ_{JB} is the junction-to-board thermal characterization parameter.
6) The thermal parameter is based on tests conducted on the MPS evaluation board (EVM54322-PB-00A) under no airflow cooling conditions in a standard enclosure. The board size is 8cmx8cm, 4-layer; the top and bottom layer copper thickness is 2oz.
7) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on equation $T_J = \theta_{JC_TOP} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of module at real application, and T_{CASE_TOP} is the case top temperature.
8) The junction-to-board thermal characterization parameter, θ_{JB}, is the estimation of the junction temperature in the real system, based on equation $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the entire loss of a module in real applications, and T_{BOARD} is the board temperature.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{INUVLO_R}	Register 0x56, bits D[1:0] configurable	2.6	2.75	2.9	V
V_{IN} UVLO falling threshold	V_{INUVLO_F}			2.6		V
V_{IN} over-voltage (OV) rising threshold	V_{INOVLO_R}		17	18	19	V
VIN quiescent current	I_{Q_PFM}	PFM, no load		2.8	5	mA
Buck Converter 1 (Buck 1), Buck Converter 2 (Buck 2)						
Switch leakage	SW_{ILK1}	T_J = 25°C		0	1	µA
Minimum on time (10)	t_{ON_MIN1}			30		ns
Minimum off time (10)	t_{OFF_MIN1}			130		ns
Output voltage accuracy	V_{FB1P}	Default output of buck 1	-1.5%	0.6	+1.5%	V
			-1.5%	0.8	+1.5%	
			-1.5%	1.2	+1.5%	
			-1.5%	1.8	+1.5%	
Output voltage accuracy	V_{FB2P}	Default output of buck 2	-1.5%	0.6	+1.5%	V
			-1.5%	0.8	+1.5%	
			-1.5%	1.2	+1.5%	
			-1.5%	1.8	+1.5%	
Low-side (LS) current limit (source)	I_{LS_VALLEY}	Registers 0x04, bits D[4:2], and 0x09, bits D[4:2] configurable		4		A
Negative current limit	I_{NOCP}	Forced PWM/OVP discharge	4.1	5.6	7.1	A
Output discharge resistor	$R_{DISCHARGE}$			27		Ω
UV/OV						
Output under-voltage (UV) threshold	V_{UVP_SW1}	Registers 0x05, bits D[3:2], and 0x0A, bits D[3:2] configurable	86%	90%	94%	V_{REF}
Output over-voltage protection (OVP) rising threshold	V_{OVP1_H}	Registers 0x05, bits D[1:0], and 0x0A, bits D[1:0] configurable	109%	113%	117%	V_{REF}
Output OVP recovery threshold	V_{OVP1_L}			110%		V_{REF}
Soft-Start Time						
Soft-start time	t_{START}	Registers 0x41, bits D[6:4], and 0x48, bits D[6:4] configurable	1.6	2	2.4	ms
Soft-stop time	t_{STOP}	Registers 0x41, bits D[3:2], and 0x48, bits D[3:2] configurable		0.5		ms
Switching Frequency (f_{SW})						
Default switching frequency	f_{SW}	Registers 0x02 bits D[5:4], and 0x07 bits D[5:4] configurable	800	1000	1200	kHz
Low-Dropout (LDO) Regulator						
LDOIN UVLO rising threshold	V_{LDOIN_R}		2.4	2.6	2.8	V
LDOIN UVLO hysteresis	V_{LDOIN_HYS}			200		mV

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output voltage	V_{LDO}	Register 0x0C configurable	-3%	1.8	3%	V
LDO load capability	I_{LIM_LDO}		500			mA
LDO voltage regulation (10)	V_{LDO_RG}	LDOIN = 3.3V, LDO = 1.8V, load = 0mA to 500mA		1		%
EN						
EN rising threshold	V_{EN_R}		1	1.2	1.4	V
EN hysteresis	V_{EN_HYS}			200		mV
MODE Detection						
MODE sourcing current	I_{MODE}		11.5	12.8	14.1	uA
MODE detection voltage upper threshold	V_{MODE_DT0}	MODE0 is detected if 0V < V_{MODE} < V_{MODE_DT0}			40	mV
	V_{MODE_DT1}	MODE1 is detected if V_{MODE_DT0} < V_{MODE} < V_{MODE_DT1}	80		120	mV
	V_{MODE_DT2}	MODE2 is detected if V_{MODE_DT1} < V_{MODE} < V_{MODE_DT2}	180		240	mV
	V_{MODE_DT3}	MODE3 is detected if V_{MODE_DT2} < V_{MODE} < V_{MODE_DT3}	320		460	mV
	V_{MODE_DT4}	MODE4 is detected if V_{MODE_DT3} < V_{MODE} < V_{MODE_DT4}	560		760	mV
	V_{MODE_DT5}	MODE5 is detected if V_{MODE_DT4} < V_{MODE} < V_{MODE_DT5}	860		1080	mV
	V_{MODE_DT6}	MODE6 is detected if V_{MODE_DT5} < V_{MODE} < V_{MODE_DT6}	1180		1400	mV
	V_{MODE_DT7}	MODE7 is detected if V_{MODE_DT6} < V_{MODE} < V_{CC}	1660		V_{CC}	mV
PG and INT						
PG (output port sink current capability)	V_{PG_SINK}	Sink 3mA			0.3	V
INT (output port sink current capability)	V_{INT_SINK}	Sink 3mA			0.3	V
PG UV rising	$V_{PG_UV_R}$			95%		V_{REF}
PG UV falling	$V_{PG_UV_F}$	Registers 0x05, bit D[5], and 0x0A, bit D[5] configurable		92.5%		V_{REF}
PG OV rising	$V_{PG_OV_R}$	Registers 0x05, bits D[7:6], and 0x0A, bits D[7:6] configurable		107.5%		V_{REF}
PG OV falling	$V_{PG_OV_F}$			105%		V_{REF}
VCC Regulator						
VCC voltage	V_{CC}	I_{CC} = 25mA	3.4	3.6	3.8	V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0mA to 25mA		1		%
Temperature Protection						
Thermal shutdown (10)	T_{OTP_R}	Register 0x0F, bits D[7:5] configurable		150		°C
Thermal hysteresis (10)	T_{HYS}			20		°C

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CLK						
CLK logic high	V_{CLK_IH}		1.4			V
CLK logic low	V_{CLK_IL}				0.4	V
CLK (output port sink current capability)	V_{CLK_SINK}	Sink 3mA			0.3	V
GPIO						
GPIO (output port sink current capability)	V_{GPIO_SINK}	Sink 3mA			0.3	V
I²C Interface Specifications (9)						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.6	V
Output voltage logic low	V_{OUT_L}	Sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				3.4	MHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		200			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			70		ns
Set-up time for repeated start	t_{SU_STA}		160			ns
Hold time for repeated start	t_{HD_STA}		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop command	t_{SU_STO}		160			ns
SCL and SDA rising time	t_R		10		300	ns
SCL and SDA falling time	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

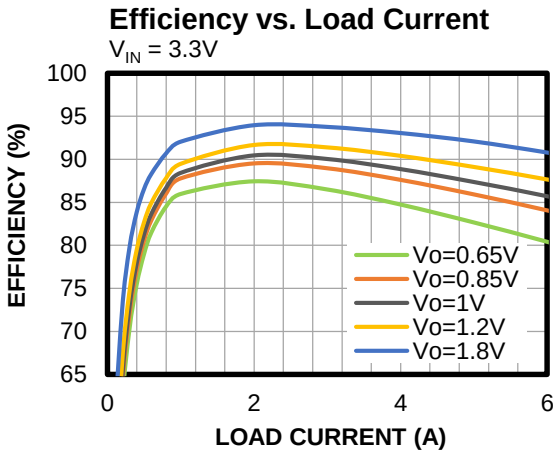
Notes:

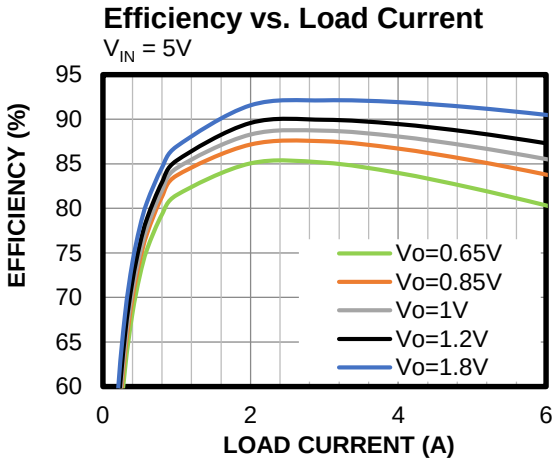
9) Not tested in production. Guaranteed by over-temperature correlation.
10) Guarantee by engineering sample characterization.

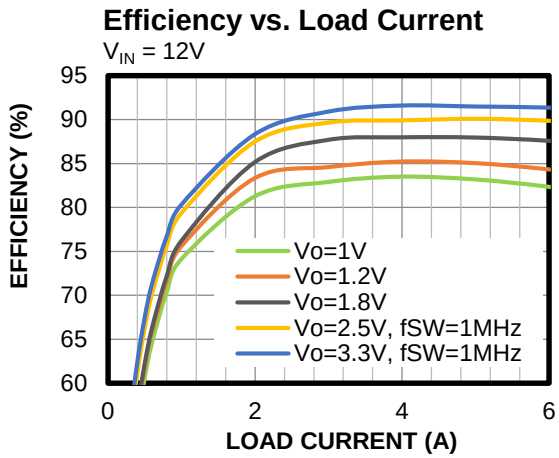
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

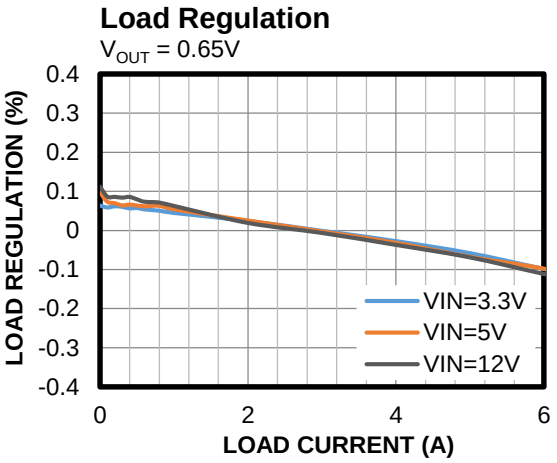
TYPICAL CHARACTERISTICS

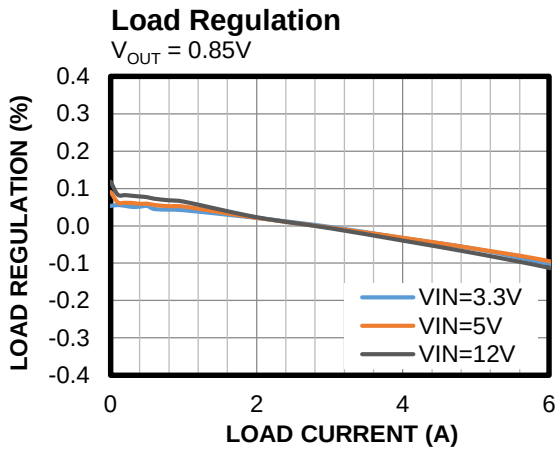
Performance curves are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1.2V, C_{IN} = 2 x 22µF, C_{OUT} = 4 x 22µF, f_{SW} = 750kHz, T_A = 25°C, unless otherwise noted.

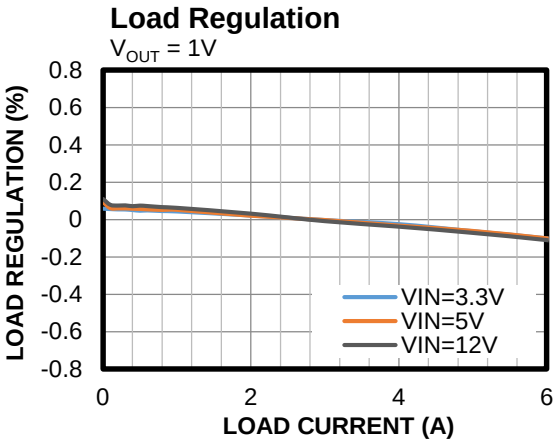












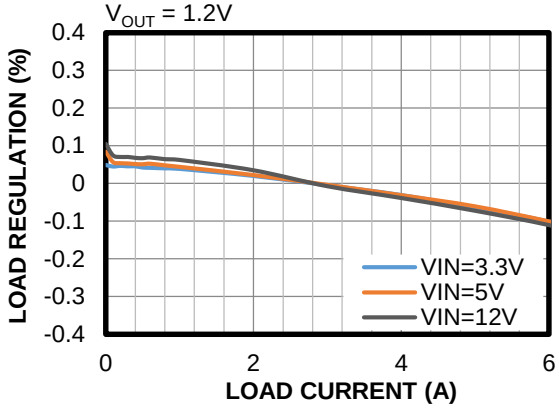
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1.2V, C_{IN} = 2 x 22µF, C_{OUT} = 4 x 22µF, f_{SW} = 750kHz, T_A = 25°C, unless otherwise noted.

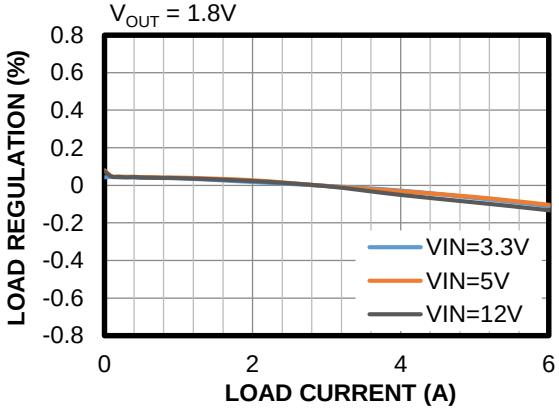
Load Regulation

V_{OUT} = 1.2V



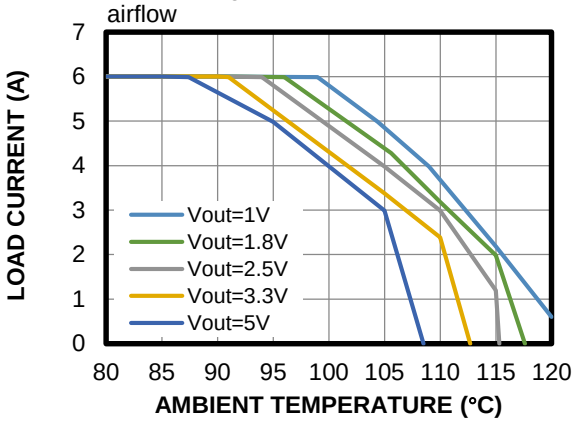
Load Regulation

V_{OUT} = 1.8V



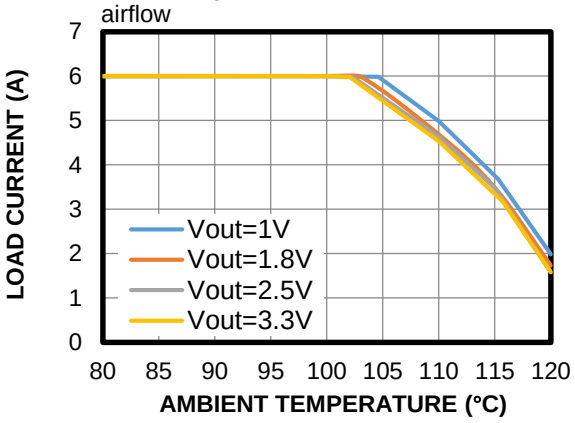
Load Current vs. Ambient Temperature

V_{IN} = 12V, f_{SW} = 1MHz, FCCM, with no airflow



Load Current vs. Ambient Temperature

V_{IN} = 5V, f_{SW} = 1MHz, FCCM, with no airflow



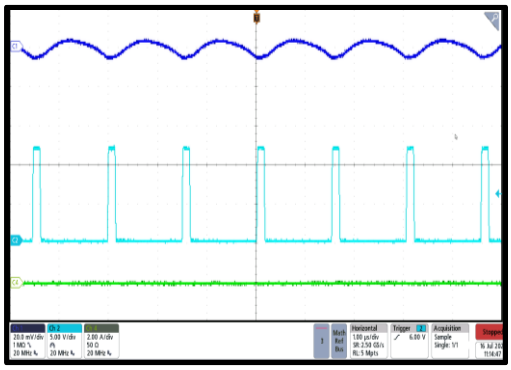
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance curves are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1.2V, C_{IN} = 4 x 22µF, C_{OUT1} = C_{OUT2} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

Steady State

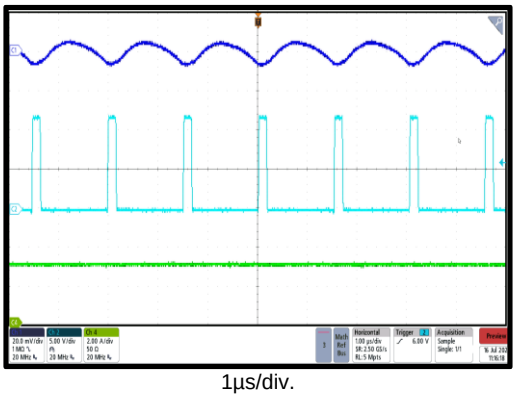
I_{OUT} = 0A, f_{SW} = 750kHz, independent mode, $V_{OUT/AC}$ = 10.4mV



1µs/div.

Steady State

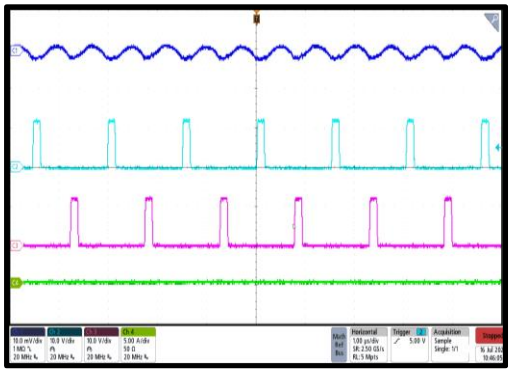
I_{OUT} = 3A, f_{SW} = 750kHz, independent mode, $V_{OUT/AC}$ = 13.6mV



1µs/div.

Steady State

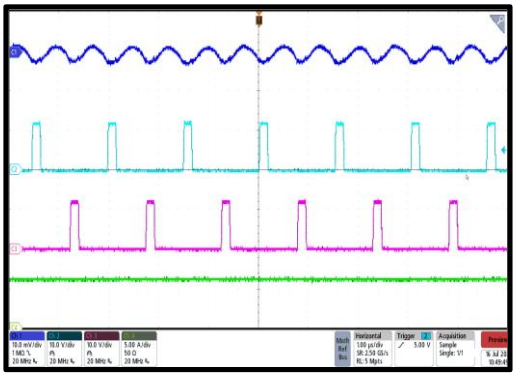
I_{OUT} = 0A, f_{SW} = 750kHz, paralleled mode, $V_{OUT/AC}$ = 3.8mV



1µs/div.

Steady State

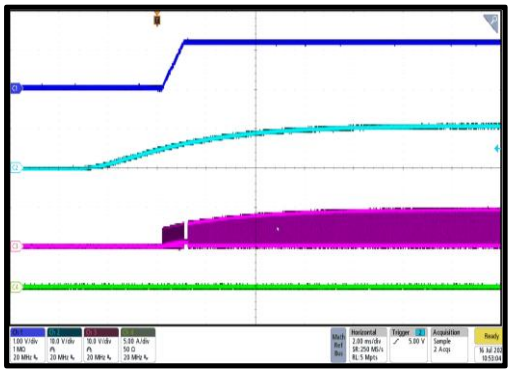
I_{OUT} = 6A, f_{SW} = 750kHz, paralleled mode, $V_{OUT/AC}$ = 4.6mV



1µs/div.

Start-Up through VIN

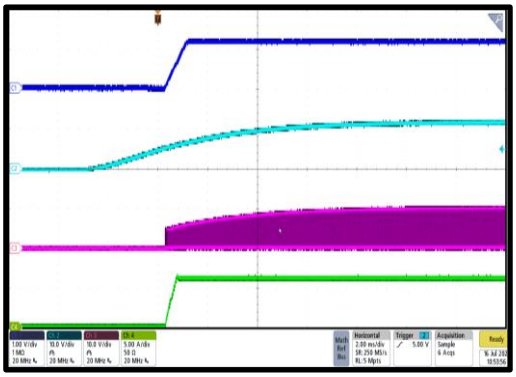
I_{OUT} = 0A, paralleled mode



2ms/div.

Start-Up through VIN

I_{OUT} = 6A, paralleled mode



2ms/div.

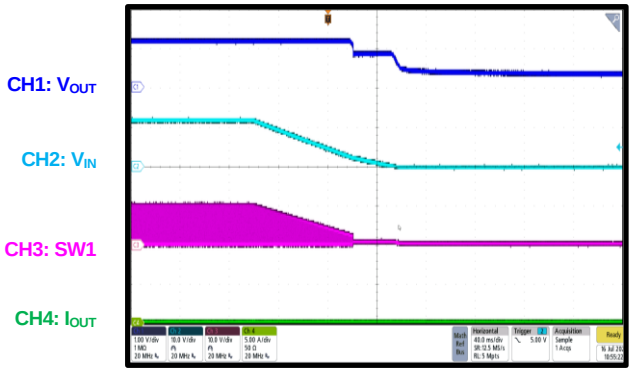
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1.2V, C_{IN} = 4 x 22µF, C_{OUT1} = C_{OUT2} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

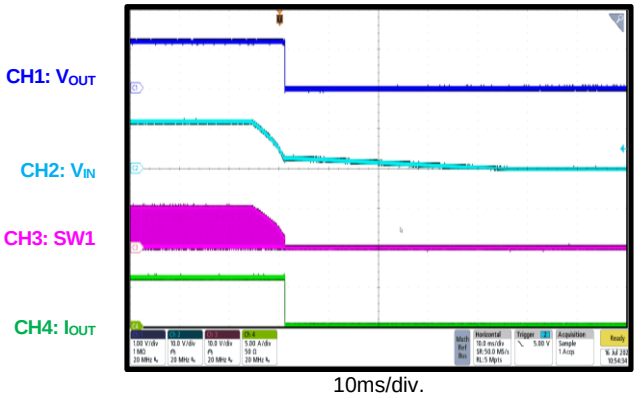
I_{OUT} = 0A, paralleled mode



40ms/div.

Shutdown through VIN

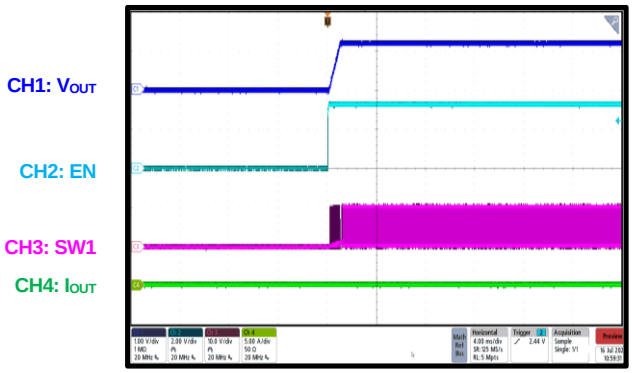
I_{OUT} = 6A, paralleled mode



10ms/div.

Start-Up through EN

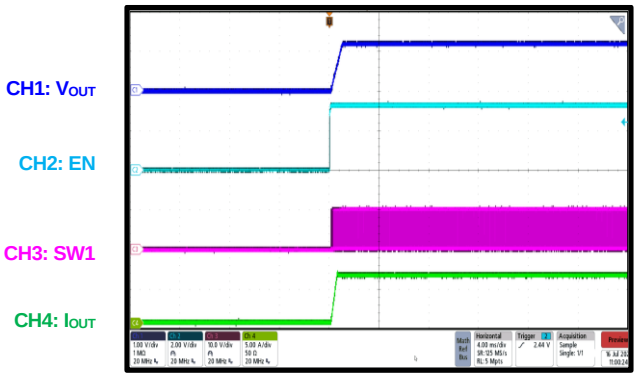
I_{OUT} = 0A, paralleled mode



4ms/div.

Start-Up through EN

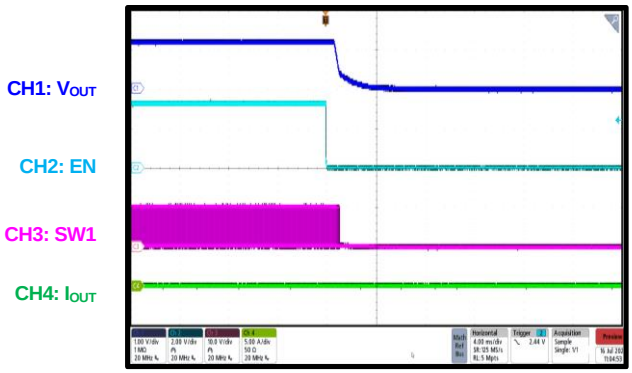
I_{OUT} = 6A, paralleled mode



4ms/div.

Shutdown through EN

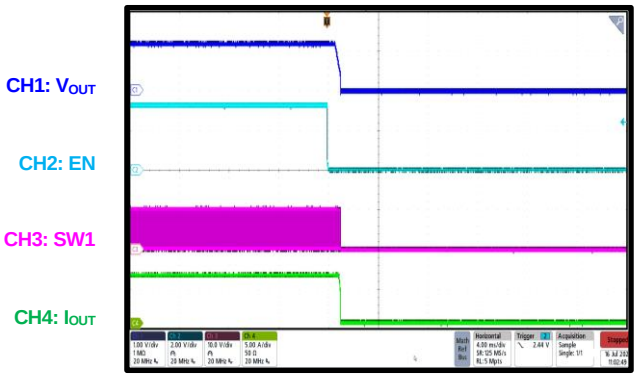
I_{OUT} = 0A, paralleled mode



4ms/div.

Shutdown through EN

I_{OUT} = 6A, paralleled mode



4ms/div.

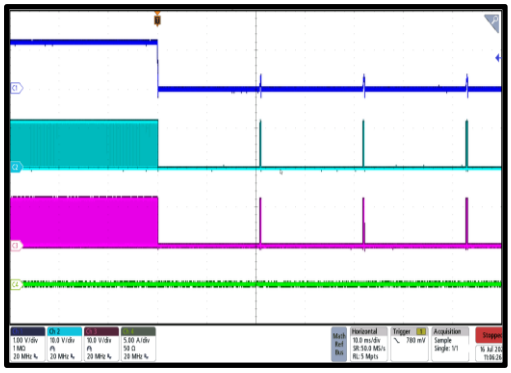
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 12V, V_{OUT} = 1.2V, C_{IN} = 4 x 22µF, C_{OUT1} = C_{OUT2} = 2 x 22µF, T_A = 25°C, unless otherwise noted.

SCP Entry

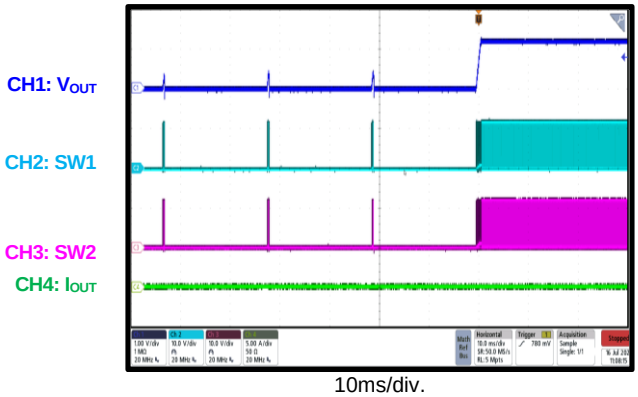
Paralleled mode



10ms/div.

SCP Recovery

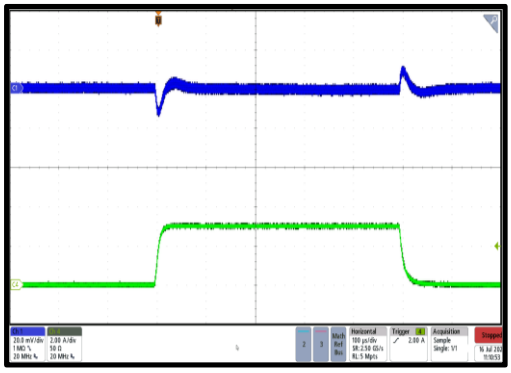
Paralleled mode



10ms/div.

Load Transient Response

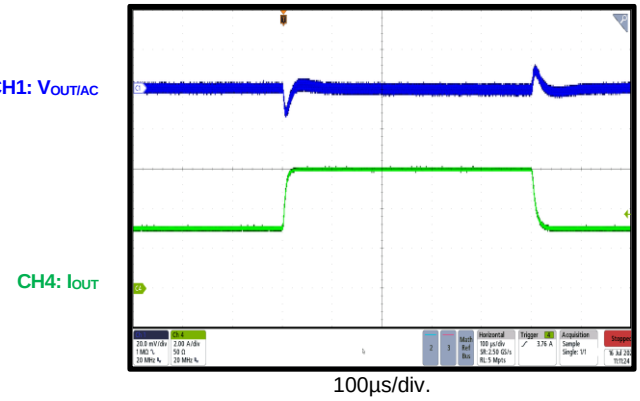
I_{OUT} = 0A to 3A, slew rate = 2.5A/µs e-load, paralleled mode, $V_{OUT/AC}$ =26.4mV



100µs/div.

Load Transient Response

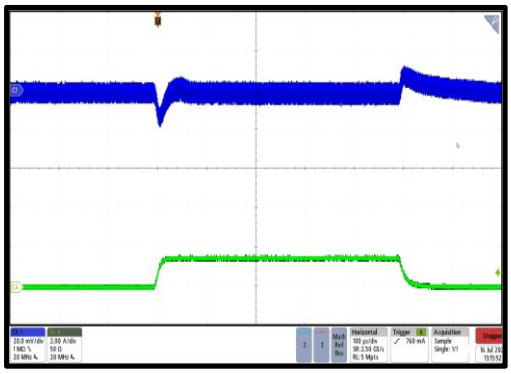
I_{OUT} = 3A to 6A, slew rate = 2.5A/µs e-load, paralleled mode, $V_{OUT/AC}$ = 26.4mV



100µs/div.

Load Transient Response

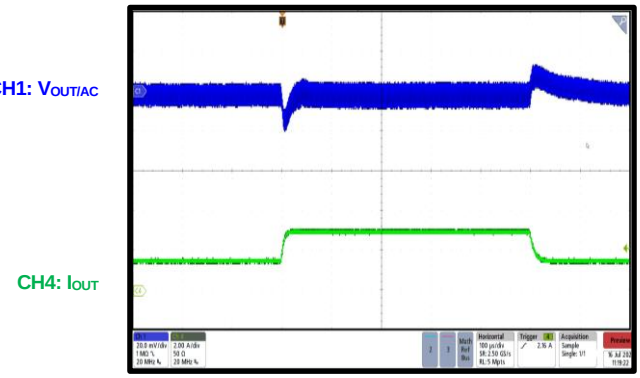
I_{OUT} = 0A to 1.5A, slew rate = 2.5A/µs e-load, independent mode, $V_{OUT/AC}$ = 31.2mV



100µs/div.

Load Transient Response

I_{OUT} = 1.5A to 3A, slew rate = 2.5A/µs e-load, independent mode, $V_{OUT/AC}$ = 33.6mV



100µs/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

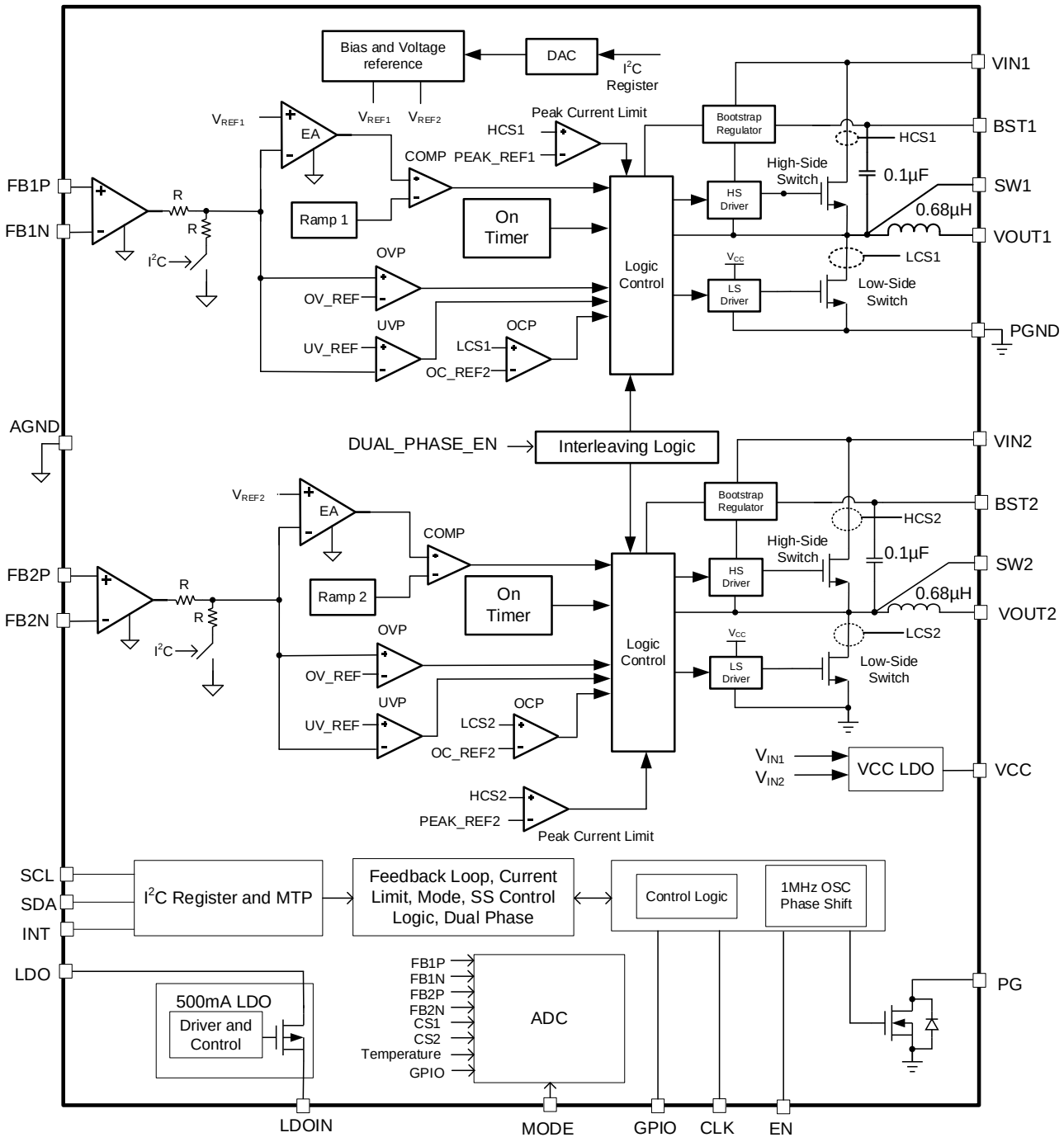


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

OPERATION

High-Efficiency Buck Regulators

The MPM54322 is dual-channel power module. Buck converter 1 (buck 1) and buck converter 2 (buck 2) are synchronous, step-down DC/DC converters with built-in soft start, compensation, and hiccup current-limit protection. Fixed-frequency constant-on-time (COT) control provides fast transient response.

VIN Power Supply

VIN1 is the power supply for buck 1, while VIN2 is the power supply for buck 2. VIN1 and VIN2 are connected together internally; it is recommended to connect VIN1 to VIN2 during application. When the input voltage (V_{INx}, where x = 1 or 2) exceeds the V_{INx} under-voltage lockout (UVLO) rising threshold, the corresponding buck starts up if all the other start-up conditions are met. The respective buck shuts down when V_{INx} falls below the V_{INx} UVLO falling threshold voltage.

Over-Temperature Warning and Thermal Shutdown

The MPM54322 employs over-temperature (OT) warning and critical temperature shutdown. The MPM54322 monitors the IC's junction temperature (T_J). If T_J exceeds the OT warning threshold set via register 0x0F, bits D[4:2], the MPM54322 sets the warning status in register 0x19, bit D[1]. The MPM54322 continues to operate as normal.

If the MPM54322's temperature exceeds the threshold set via register 0x0F, bits D[7:5], the MPM54322 internally generates a disable command and disables buck 1, buck 2, and the 500mA low-dropout (LDO) regulator. In addition, the OT status in register 0x19, bit D[0] is set, and the PG output signal de-asserts at the same time.

Soft Start and Soft Shutdown

The MPM54322 employs a soft-start and soft-shutdown mechanism to ensure that there is a smooth output during start-up and shutdown. When the part is enabled and the BST voltage reaches its rising threshold, the internal digital-to-analog converter (DAC) outputs a reference voltage (V_{REF}). The output voltage (V_{OUTx}, where x = 1 or 2) smoothly ramps up with the reference voltage. When the DAC output reaches the final voltage, it stops at that level. At this point, soft start is finished and the device enters steady-state operation.

When the part is disabled, the internal DAC output ramps down. V_{OUTx} smoothly ramps down with the reference voltage. When the DAC output reaches 300mV (if BUCK1_FB_HALF = 1 or BUCK2_FB_HALF = 1, the corresponding DAC output reaches 150mV), it stops at that level. At this point, soft shutdown is finished and the output gradually discharges to 0V via the FB1P- and FB2P-to-GND resistance.

The soft-start time and soft-shutdown time can be configured via registers 0x41 and 0x48.

Over-Voltage Protection (OVP)

An output over-voltage protection (OVP) mechanism is implemented to limit the voltages on the MPM54322's output regulators. The MPM54322 actively monitors the output voltage (V_{OUTx}) on each enabled regulator.

The potential OV events for the MPM54322 are listed below:

- Buck 1's output exceeds the threshold set via register 0x05, bits D[1:0].
- Buck 2's output exceeds the threshold set via register 0x0A, bits D[1:0].

The fault rail's output enters OVP mode once the output voltage exceeds the set regulation voltage for longer than 2.5µs. In OVP discharge mode, the low-side MOSFET (LS-FET) turns on and stays on until its current drops to the negative current limit. This process discharges the output and keeps the output voltage within the normal range. If the OV condition still exists, the LS-FET turns on again after a fixed delay to repeat the discharge behavior. The device exits discharge mode when the feedback voltage (V_{FB}) drops to the reference voltage threshold.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM54322 has valley current limit control. When the LS-FET is on, the inductor current is monitored.

The potential over-current (OC) events for the MPM54322 are listed below:

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

- Buck 1's inductor current exceeds the valley current limit threshold set via register 0x04, bits D[4:2].
- Buck 2's inductor current exceeds the valley current limit threshold set via register 0x09, bits D[4:2].

When the sensed inductor current exceeds the valley current limit threshold, the device enters over-current protection (OCP) mode. The HS-FET cannot turn on until the inductor current drops to the valley current limit. Meanwhile, the output voltage drops until it falls below the under-voltage (UV) threshold, which is typically 45% of the reference voltage.

If a UV and OC condition are both triggered, the MPM54322 enters hiccup mode to periodically restart the related power rail. The hiccup duty cycle is very small to reduce power dissipation during short-circuit (SC) conditions. During OCP, the device tries to recover from the OC fault with hiccup mode. During this period, the chip disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft start again. If the OC condition still exists when soft start is finished, the device repeats this operation. OCP is a non-latch protection.

Active Voltage Positioning (AVP)

The MPM54322 supports active voltage positioning (AVP) by setting the AVP_EN bit to 1 via the I²C. An internal current-sense circuit produces the droop current's (I_{DROOP}) current source, which is proportional to the internal sensing current. I_{DROOP} injects to the FB pin to produce the feedback voltage with a droop voltage. The actual output voltage (V_{OUT_AVP}) can be calculated with Equation (1):

$$V_{OUT_AVP}=V_{OUT}+AVP\times_OFFSET\text{-}AVP\times_GAIN\times I_{OUT}\times FB_FACTOR \quad (1)$$

Where V_{OUT} is the output voltage when the AVP function is disabled, and FB_FACTOR is a constant that is determined by BUCKx_FB_HALF (see Table 1). AVPx_GAIN and AVPx_OFFSET can be set via the I²C registers 0x1F and 0x20, respectively. These values can also be pre-configured to the MTP via registers 0x5C and 0x5D.

Table 1: FB_FACTOR Selection

BUCKx_FB_HALF (11)	FB_FACTOR
0	1
1	2

Note:

11) BUCKx_FB_HALF can be configured via bit[5] of the MTP registers 0x44 and 0x4B, as well as bits[7:6] of the MODE registers 0x72, 0x7D, 0x88, 0x93, 0x9E, 0xA9, 0xB4, and 0xBF.

Power Good (PG) Signal

The PG pin indicates the statuses of V_{INx} and all enabled output regulators (VOUT1, VOUT2, and LDO). The MPM54322 floats the PG pin (meaning it is high) when V_{INx} is valid and all enabled output regulator's (VOUT1, VOUT2, LDO) tolerances are maintained, as configured in the appropriate register space.

When the output voltages of the power rail for VOUTx and LDO are within the power good tolerance threshold, the bits for the internal power good register (register 0x21, bits D[6:4]) go low. If the output voltages of the power rail for VOUTx and LDO are out of the power good tolerance thresholds, the internal power good bits de-assert (go high).

The power good status of all the enabled power rails is used to determine following "and" logic. If all the enabled rails have a high PG status, the PG pin is high. If one or more enabled rails have a low PG status, or all the power rails are disabled, the PG pin is low.

Interleaving for Dual-Phase Operation

When interleaving mode is enabled (by setting register 0x54, bit D[7] = 1), buck 1 and buck 2 enter 2-phase interleaving operation, which is also known as dual-phase mode. The SET signal is triggered by comparing V_{FB} and V_{REF}. When the SET signal goes high, only one phase's PWM output goes high; the next time the SET signal goes high, the next phase's PWM output goes high. This process accomplishes interleaving.

When buck 1 and buck 2 operate in dual-phase interleaving mode, it senses both phase currents and auto-tunes the buck's on time (t_{ON}) to balance the current. Figure 3 on page 17 shows dual-phase operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

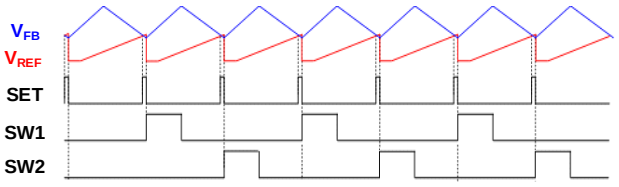


Figure 3: Buck 1/2 Interleaving for Dual-Phase Operation

Analog-to-Digital Converter (ADC)

The MPM54322 supports an analog-to-digital converter (ADC) to monitor the input supply voltages, output voltages (for buck 1, buck 2, the 500mA LDO, and GPIO), and output voltage regulator current (for buck 1 and buck 2). Register 0x10, bit D[7] enables the ADC. Registers 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, and 0x18 provide the actual measurements for V_{OUT1}, I_{OUT1}, V_{OUT2}, I_{OUT2}, LDO, GPIO, and V_{IN}, respectively.

MODE-Determined MTP Configuration

Some MTP configurations are determined by the resistor connected to the MODE pin. A 2% (or higher) accuracy is required for the MODE resistor to guarantee correct MODE configurations. Table 2 shows the configuration selections.

Table 2: Recommended MODE Resistors for MTP Configurations

MODE Resistor	MODE-Determined MTP Configuration
0Ω	Mode 0, 0x70~0x7A
7.87kΩ	Mode 1, 0x7B~0x85
16.5kΩ	Mode 2, 0x86~0x90
30kΩ	Mode 3, 0x91~0x9B
51kΩ	Mode 4, 0x9C~0xA6
75kΩ	Mode 5, 0xA7~0xB1
100kΩ	Mode 6, 0xB2~0xBC
No connection or VCC	Mode 7, 0xBD~0xC7

After start-up, if MODE_EN = 1, the MPM54322 detects the MODE pin's resistor configuration, and selects the corresponding MODEx. Next, the MODEx configurations are loaded into the corresponding MTP registers, and then into the I²C registers.

Otherwise, if MODE_EN = 0, the MTP registers maintain their original values, which are loaded into the I²C registers.

I²C Address Configuration

The I²C address is determined by register 0x60, bits D[6:0]. After start-up, if MODE_EN = 1, the MPM54322 detects the MODE pin's resistor configuration, and selects the corresponding MODEx. The 3-bit register (I2C_ADDRESS) in the MODE register region substitutes 0x60, bits D[2:0]; the newly selected 0x60, bits D[6:0] select the current I²C address.

For example, set register 0x60, bits D[6:0] = 0011000, and set register 0x98, bits D[4:2] = 011. When the MPM54322 selects Mode 3 via the MODE pin's resistor, register 0x60, bits D[2:0] is substituted by 0x98, bits D[4:2]. This means that the new value for register 0x60, bits D[6:0] = 0011011, which is the current I²C address.

Interrupt (INT)

The INT pin indicates the MPM54322's status. INT is specified as an open-drain signal. Interrupts have an active low latched signal. If any status bit in register 0x19 or 0x1A is changed to 1, the INT pin outputs low.

The INT pin stays low until both of the following requirements are met:

- The condition causing the interrupt no longer persists.
- The register is cleared through the I²C write-to-clear bit.

A status bit is latched to 1 if its related condition occurs. This bit stays latched to 1 until the clear bit is written to 1. If a status bit is cleared but the condition continues to persist, a new interrupt is generated (as if it is a new condition).

When the mask register bit is set to 1 (masked), the INT pin does not pull low, even though the corresponding status bit is triggered and set to 1.

FLEX-Timer Sequence Control

CLK-Based Power Sequence Control

The CLK-based FLEX-timer sequence control scheme uses a master-slave structure.

The EN pins and CLK pins for all the PMICs are connected for sequence control (see Figure 4 on page 18).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

The CLK pins are pulled up to any one of the VCCs via a resistor (typically 10kΩ). One PMIC is configured as the master PMIC, which generates a clock signal output on the CLK pin (denoted as PMIC1 in Figure 4). The other PMICs are configured as the slave PMICs, which receive the clock signal input on the CLK pin. The start-up/shutdown sequence of all the power rails are synchronized by the clock signal.

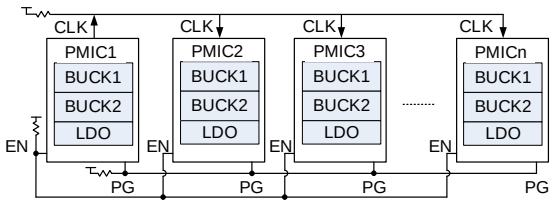


Figure 4: FLEX-Timer Sequence Control Connection

When the EN pin pulls high, the start-up sequence starts. The master PMIC starts generating the clock outputs, and the slave PMICs count the clock signal. For the relevant power rail in one master/slave PMIC, when the counted clock signal cycle reaches POWER_ON_DELAY (an internal NVM register), the power rail turns on. When the master PMIC clock cycle reaches CLK_NUMBER (an NVM register in the master PMIC) and PG goes high (all enabled power rails finish their soft-start process and the PG pin is pulled high by an external resistor), the master PMIC stops the clock output, and the start-up sequence finishes. The master PMIC does not stop the clock outputs if the PG pin is floating or pulled down.

When the EN pin is pulled low, the shutdown sequence starts, and the master PMIC starts generating the clock outputs. The slave PMICs count the clock signal. For the relevant power rail in one master/slave PMIC, when the counted clock signal cycle reaches POWER_OFF_DELAY (an internal NVM register), the power rail turns off. When the master PMIC clock cycle reaches CLK_NUMBER, the master PMIC stops the clock output, and the shutdown sequence finishes.

When there is only one MPM54322, the CLK pin should be pulled high, and CLK_MODE (register 0x5E, bit D[7]) must be set to 1.

Clock Pausing Function

Consider the following for each master/slave PMIC during the start-up/shutdown procedure:

- If CLK_PAUSE_EN = 1, the master/slave PMIC pulls the CLK pin down during the soft start/stop of any power rail(s). Figure 5 shows when CLK pauses during start-up. Figure 6 shows when CLK pauses during soft shutdown.

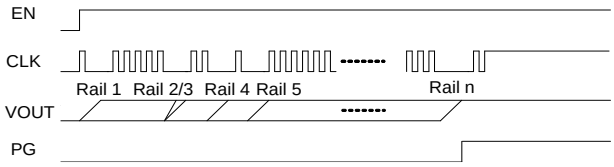


Figure 5: Soft Start when CLK Pulls Down (Pausing)

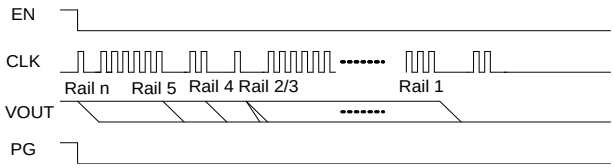


Figure 6: Soft Shutdown when CLK Pulls Down (Pausing)

- If CLK_PAUSE_EN = 0, the master/slave PMIC does not pull the CLK pin down during the soft start/stop of any power rails. Figure 7 shows soft start when CLK does not pull down. Figure 8 shows soft shutdown when CLK does not pull down.

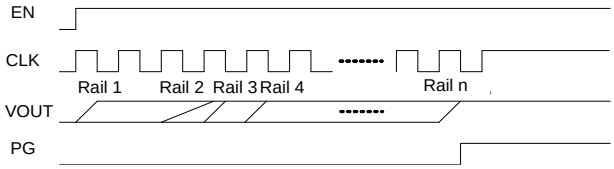


Figure 7: Soft Start when CLK Does Not Pull Down (Not Pausing)

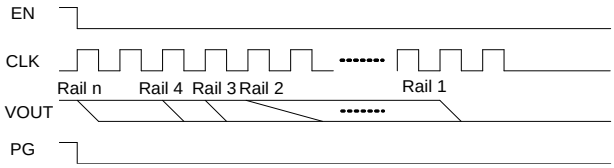


Figure 8 Soft Shutdown when CLK Does Not Pull Down (Not Pausing)

- If CLK_ON_ERROR_PAUSE_EN = 1, the master/slave PMIC pulls the CLK pin down if any error occurs during any power rail's soft start (see Figure 9 on page 19).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

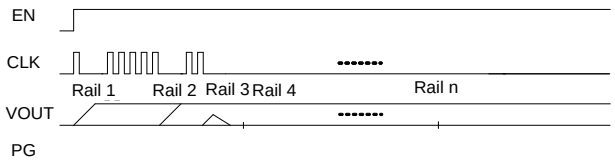


Figure 9: Soft Start during PMIC Error when CLK Pulls Down (CLK Pausing)

If CLK_ON_ERROR_PAUSE_EN = 0, the master/slave PMIC does not pull the CLK pin down, even if any error occurs during the soft start of any power rails (see Figure 10).

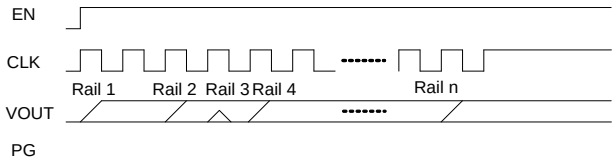


Figure 10: Soft Start during PMIC Error when CLK Does Not Pull Down (No CLK Pausing)

Meanwhile, the master PMIC generates a clock signal and monitors the CLK pin's status. When the master PMIC generates a clock high signal (open-drain output) on the CLK pin but the CLK pin stays low, the CLK pin must be pulled low by one or more master/slave PMIC(s). The master PMIC pauses the clock signal output until the CLK pin is released or detected to be high. If the CLK pin is not pulled low for clock pausing, the master PMIC should maintain the clock signal's output until the start-up or shutdown sequence finishes.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a 2-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPM54322's interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage (V_{OUT}), transition slew rate, and other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the clock's high period. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 11).

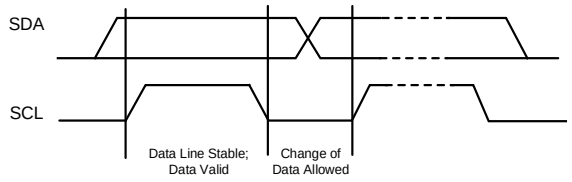


Figure 11: Bit Transfer on the I²C Bus

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start command is defined as the SDA signal transitioning from high to low while SCL is high. The stop command is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 12).

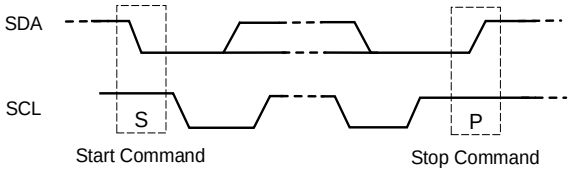


Figure 12: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is busy after the start condition, and it is considered to be free again a minimum of 4.7µs after the stop command. The bus remains busy if a repeated start (Sr) is generated instead of a stop command. The start and repeated start conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the clock pulse's high period.

Figure 13 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command, which is generated by the master. If the master still wants to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

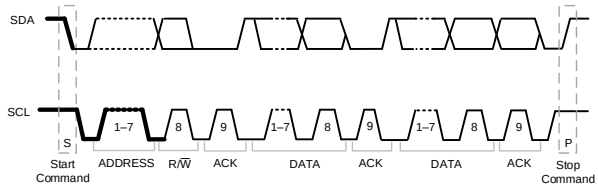


Figure 13: Complete Data Transfer

The MPM54322 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPM54322 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPM54322. The MPM54322 performs an update on the falling edge of the least significant bit (LSB) byte.

Figure 14 on page 21 shows an I²C write example. Figure 15 on page 21 shows an I²C read example.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

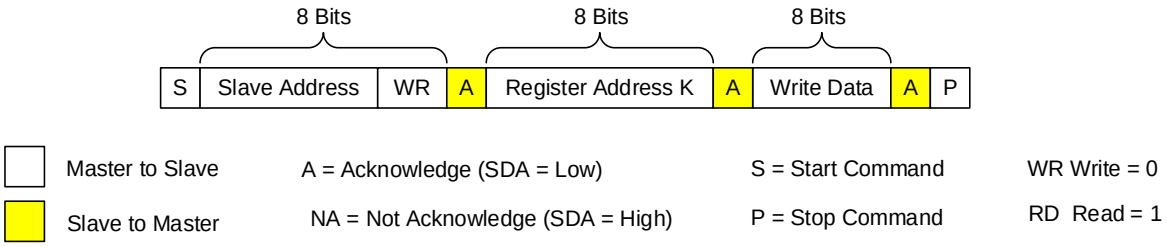


Figure 14: I²C Write Single Register Example

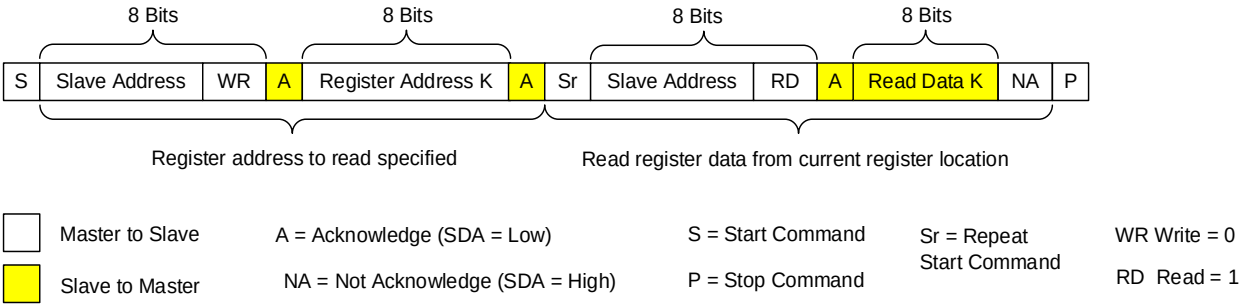


Figure 15: I²C Read Single Register Example

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER ATTRIBUTE DEFINITION

All volatile registers have base attributes (see Table 3).

Table 3: Register Base Attributes

Attribute	Abbreviation	Description
Read-Only	RO	This bit can be read by the host. Writes have no effect.
Read/Write	R/W	This bit can be read or written by the host.
Write-Only	W	This bit can only be written by the host. Reading from this bit returns 0.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by the host. The bit returns 0 when read. Writing to this bit has no effect.

Some register attributes can be further modified with attribute modifiers (see Table 4).

Table 4: Register Attribute Modifier

Attribute	Abbreviation	Description
Write 1 Only	1O	This bit can only be set (i.e. write 1) but not reset (i.e. write 0). Writing 0 to this bit has no effect.
Protected	P	This bit is protected by the password registers. This bit cannot be written to unless the password code has been written into the password register(s).
Persistent	E	This bit is persistent during the power cycle.

Table 5 goes into more detail on the register map regions.

Table 5: Register Map Breakdown

Register Range	Region	Description
0x0~0x21	I²C Region	Volatile memory registers.
0x40~0x64	MTP Region	NVM. These registers require a complete power cycle before they take effect. Changing these registers under normal operation is considered an illegal operation.
0x70~0xC7	MODE Region	NVM. These registers configure the default value for some registers in the MTP region.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER DESCRIPTION

I²C Region Register Map

Add. (0x)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	LOCK	R/W	RESERVED							I2C_LOCK_EN
01	BUCK1_CTRL1	R/W	VOUT1_GO_BIT	RESERVED					VOUT1_SLEW_RATE	
02	BUCK1_CTRL2	R/W	BUCK1_PWM/PFM		BUCK1_FSW		RESERVED	VOUT1_SETTING_LOW		
03	BUCK1_CTRL3	R/W	VOUT1_SETTING_HIGH							
04	BUCK1_CTRL4	R/W	VOUT1_DISCHRG_EN	VOUT1_OVP_EN	RESERVED	BUCK1_OC_TH			RESERVED	
05	BUCK1_CTRL7	R/W	VOUT1_PG_VTH_HIGH		VOUT1_PG_VTH_LOW	RESERVED	VOUT1_UV_VTH		VOUT1_OV_VTH	
06	BUCK2_CTRL1	R/W	VOUT2_GO_BIT	RESERVED					VOUT2_SLEW_RATE	
07	BUCK2_CTRL2	R/W	BUCK2_PWM/PFM		BUCK2_FSW		RESERVED	VOUT2_SETTING_LOW		
08	BUCK2_CTRL3	R/W	VOUT2_SETTING_HIGH							
09	BUCK2_CTRL4	R/W	VOUT2_DISCHRG_EN	VOUT2_OVP_EN	RESERVED	BUCK2_OC_TH			RESERVED	
0A	BUCK2_CTRL7	R/W	VOUT2_PG_VTH_HIGH		VOUT2_PG_VTH_LOW	RESERVED	VOUT2_UV_VTH		VOUT2_OV_VTH	
0B	LDO_CTRL1	R/W	LDO_GO_BIT	RESERVED			RESERVED		LDO_DISCHRG	LDO_PG_VTH
0C	LDO_CTRL2	R/W	RESERVED	LDO_SETTING						
0D	SYS_CTRL1	R/W	PMIC_EN	VOUT1_EN	VOUT2_EN	LDO_EN	RESERVED		GPIO_CTRL	
0E	SYS_CTRL3	R/W	VIN_PG_VTH			MASK_PG	RESERVED			
0F	SYS_CTRL4	R/W	OT_TH			OTW_TH			RESERVED	
10	ADC_CTRL1	R/W	ADC_EN	RESERVED					ADC_SAMPLE_FREQ	
11	TEMPERATURE	RO	TEMPERATURE			RESERVED				
12	VOUT1_ADC	RO	VOUT1_ADC							
13	IOUT1_ADC	RO	IOUT1_ADC							
14	VOUT2_ADC	RO	VOUT2_ADC							
15	IOUT2_ADC	RO	IOUT2_ADC							
16	LDO_ADC	RO	LDO_ADC							
17	GPIO_ADC	RO	GPIO_ADC							
18	VIN_ADC	RO	VIN_ADC							
19	FAULT_STATUS	RO	VIN_PG	VOUT1_PG	VOUT2_PG	LDO_PG	RESERVED		OTW	OT
1A	STATUS1	RO	VIN_OV	VIN_UV	VOUT1_OV	VOUT2_OV	VOUT1_UV	VOUT2_UV	VOUT1_OC	VOUT2_OC

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER DESCRIPTION *(continued)*

Add. (0x)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1B	MASK1	R/W	VIN_PG_MSK	VOUT1_PG_MSK	VOUT2_PG_MSK	LDO_PG_MSK	RESERVED		OTW_MSK	OT_MSK
1C	MASK2	R/W	VIN_OV_MSK	VIN_UV_MSK	VOUT1_OV_MSK	VOUT2_OV_MSK	VOUT1_UV_MSK	VOUT2_UV_MSK	VOUT1_OC_MSK	VOUT2_OC_MSK
1D	CLEAR1	1O	VIN_PG_CLEAR	VOUT1_FAULT_CLEAR	VOUT2_FAULT_CLEAR	LDO_FAULT_CLEAR	OTW_CLEAR	OT_CLEAR	RESERVED	ALL_STATUS_CLEAR
1E	CLEAR2	1O	VIN_OV_CLEAR	VIN_UV_CLEAR	VOUT1_OV_CLEAR	VOUT2_OV_CLEAR	VOUT1_UV_CLEAR	VOUT2_UV_CLEAR	VOUT1_OC_CLEAR	VOUT2_OC_CLEAR
1F	AVP_CTRL1	R/W	AVP1_EN	AVP1_GAIN		AVP1_OFFSET				
20	AVP_CTRL2	R/W	AVP2_EN	AVP2_GAIN		AVP2_OFFSET				
21	STATUS2	RO	VIN_PG_STATUS	VOUT1_PG_STATUS	VOUT2_PG_STATUS	LDO_PG_STATUS	RESERVED		OT_WARNING_STATUS	OT_FAULT_STATUS

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MTP REGION REGISTER MAP

Add. (0x)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
40	LOCK	R/W, P/E	MTP_REGION_ACCESS_PASSWORD							
41	BUCK1_CTRL1	R/W, P/E	RESERVED	VOUT1_SOFT_START			VOUT1_SOFT_STOP		VOUT1_SLEW_RATE	
42	BUCK1_CTRL2	R/W, P/E	BUCK1_PWM/PFM		BUCK1_FSW		RESERVED	VOUT1_SETTING_LOW		
43	BUCK1_CTRL3	R/W, P/E	VOUT1_SETTING_HIGH							
44	BUCK1_CTRL4	R/W, P/E	VOUT1_DISCHRG_EN	VOUT1_OVP_EN	BUCK1_FB_HALF	BUCK1_OC_TH			RESERVED	
45	BUCK1_CTRL5	R/W, P/E	BUCK1_POWER_ON_DELAY							
46	BUCK1_CTRL6	R/W, P/E	BUCK1_POWER_OFF_DELAY							
47	BUCK1_CTRL7	R/W, P/E	VOUT1_PG_VTH_HIGH		VOUT1_PG_VTH_LOW	RESERVED	VOUT1_UV_VTH		VOUT1_OV_VTH	
48	BUCK2_CTRL1	R/W, P/E	RESERVED	VOUT2_SOFT_START			VOUT2_SOFT_STOP		VOUT2_SLEW_RATE	
49	BUCK2_CTRL2	R/W, P/E	BUCK2_PWM/PFM		BUCK2_FSW		RESERVED	VOUT2_SETTING_LOW		
4A	BUCK2_CTRL3	R/W, P/E	VOUT2_SETTING_HIGH							
4B	BUCK2_CTRL4	R/W, P/E	VOUT2_DISCHRG_EN	VOUT2_OVP_EN	BUCK2_FB_HALF	BUCK2_OC_TH			RESERVED	
4C	BUCK2_CTRL5	R/W, P/E	BUCK2_POWER_ON_DELAY							
4D	BUCK2_CTRL6	R/W, P/E	BUCK2_POWER_OFF_DELAY							
4E	BUCK2_CTRL7	R/W, P/E	VOUT2_PG_VTH_HIGH		VOUT2_PG_VTH_LOW	RESERVED	VOUT2_UV_VTH		VOUT2_OV_VTH	
4F	LDO_CTRL1	R/W, P/E	RESERVED	LDO_SOFT_START			RESERVED		LDO_DISCHRG	LDO_PG_VTH
50	LDO_CTRL2	R/W, P/E	RESERVED	LDO_SETTING						
51	LDO_CTRL3	R/W, P/E	LDO_POWER_ON_DELAY							
52	LDO_CTRL4	R/W, P/E	LDO_POWER_OFF_DELAY							
53	SYS_CTRL1	R/W, P/E	PMIC_EN	VOUT1_EN	VOUT2_EN	LDO_EN	RESERVED		GPIO_CTRL	
54	SYS_CTRL3	R/W, P/E	SINGLE/DUAL	REV_CODE						
55	SYS_CTRL3	R/W, P/E	VIN_PG_VTH			MASK_PG	PG_DELAY_EN	VIN_OVP_EN	RESERVED	HICCUP
56	SYS_CTRL4	R/W, P/E	OT_TH			OTW_TH			VIN_UV_SEL	
57	GPIO_CONFIG	R/W, P/E	GPIO_POWER_ON_DELAY							
58	GPIO_CONFIG	R/W, P/E	GPIO_POWER_OFF_DELAY							
59	ADC_CTRL2	R/W, P/E	ADC_EN	RESERVED					ADC_SAMPLE_FREQ	
5A	MASK1	R/W, P/E	VIN_PG_MSK	VOUT1_PG_MSK	VOUT2_PG_MSK	LDO_PG_MSK	RESERVED		OTW_MSK	OT_MSK
5B	MASK2	R/W, P/E	VIN_OV_MSK	VIN_UV_MSK	VOUT1_OV_MSK	VOUT2_OV_MSK	VOUT1_UV_MSK	VOUT2_UV_MSK	VOUT1_OC_MSK	VOUT2_OC_MSK

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MTP REGION REGISTER MAP *(continued)*

Add. (0x)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
5C	AVP_ CTRL1	R/W, P/E	AVP1_EN	AVP1_GAIN		AVP1_OFFSET				
5D	AVP_ CTRL2	R/W, P/E	AVP2_EN	AVP2_GAIN		AVP2_OFFSET				
5E	CLK_ CTRL1	R/W, P/E	CLK_MODE	CLK_FREQUENCY			CLK_NUMBER			RESERVED
5F	CLK_ CTRL2	R/W, P/E	RESERVED					CLK_ PAUSE_ EN	CLK_ON_ ERROR_ PAUSE_EN	RESERVED
60	I2C_ CONFIG	R/W, P/E	MODE_EN	I2C_ADDRESS						
61	MTP_ CTRL1	R/W, P/E	MTP_PASSWORD							
62	MTP_ CTRL2	R/W, P/E	RESERVED						MTP_ RESTORE	MTP_ PROGRAM
63	RV	R/W, P/E	RESERVED							
64	ID2	R/W, P/E	MTP_CODE							

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MODE REGION REGISTER MAP

Add (0X)	R/W	D7	D6	D5	D4	D3	D2	D1	D0
70	R/W, P/E	MODE0_VOUT1_SETTING_HIGH							
71	R/W, P/E	MODE0_VOUT2_SETTING_HIGH							
72	R/W, P/E	MODE0_BUCK1_FB_HALF	MODE0_BUCK2_FB_HALF	MODE0_VOUT1_SETTING_LOW			MODE0_VOUT2_SETTING_LOW		
73	R/W, P/E	MODE0_CLK_MODE	MODE0_SINGLE/DUAL	RESERVED		MODE0_BUCK1_FSW		MODE0_BUCK2_FSW	
74	R/W, P/E	MODE0_BUCK1_POWER_ON_DELAY							
75	R/W, P/E	MODE0_BUCK2_POWER_ON_DELAY							
76	R/W, P/E	MODE0_VOUT1_SOFT_START_TIME			MODE0_VOUT2_SOFT_START_TIME			MODE0_LDO_EN	RESERVED
77	R/W, P/E	MODE0_LDO_SOFT_START_TIME			MODE0_I2C_ADDRESS			MODE0_GPIO_CTRL	
78	R/W, P/E	MODE0_LDO_SETTING							
79	R/W, P/E	MODE0_LDO_POWER_ON_DELAY							
7A	R/W, P/E	MODE0_GPIO_POWER_ON_DELAY							
7B	R/W, P/E	MODE1_VOUT1_SETTING_HIGH							
7C	R/W, P/E	MODE1_VOUT2_SETTING_HIGH							
7D	R/W, P/E	MODE1_BUCK1_FB_HALF	MODE1_BUCK2_FB_HALF	MODE1_VOUT1_SETTING_LOW			MODE1_VOUT2_SETTING_LOW		
7E	R/W, P/E	MODE1_CLK_MODE	MODE1_SINGLE/DUAL	RESERVED		MODE1_BUCK1_FSW		MODE1_BUCK2_FSW	
7F	R/W, P/E	MODE1_BUCK1_POWER_ON_DELAY							
80	R/W, P/E	MODE1_BUCK2_POWER_ON_DELAY							
81	R/W, P/E	MODE1_VOUT1_SOFT_START_TIME			MODE1_VOUT2_SOFT_START_TIME			MODE1_LDO_EN	RESERVED
82	R/W, P/E	MODE1_LDO_SOFT_START_TIME			MODE1_I2C_ADDRESS			MODE1_GPIO_CTRL	
83	R/W, P/E	MODE1_LDO_SETTING							
84	R/W, P/E	MODE1_LDO_POWER_ON_DELAY							
85	R/W, P/E	MODE1_GPIO_POWER_ON_DELAY							
86	R/W, P/E	MODE2_VOUT1_SETTING_HIGH							
87	R/W, P/E	MODE2_VOUT2_SETTING_HIGH							
88	R/W, P/E	MODE2_BUCK1_FB_HALF	MODE2_BUCK2_FB_HALF	MODE2_VOUT1_SETTING_LOW			MODE2_VOUT2_SETTING_LOW		
89	R/W, P/E	MODE2_CLK_MODE	MODE2_SINGLE/DUAL	RESERVED		MODE2_BUCK1_FSW		MODE2_BUCK2_FSW	
8A	R/W, P/E	MODE2_BUCK1_POWER_ON_DELAY							
8B	R/W, P/E	MODE2_BUCK2_POWER_ON_DELAY							
8C	R/W, P/E	MODE2_VOUT1_SOFT_START_TIME			MODE2_VOUT2_SOFT_START_TIME			MODE2_LDO_EN	RESERVED

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

8D	R/W, P/E	MODE2_LDO_SOFT_START_TIME			MODE2_I2C_ADDRESS		MODE2_GPIO_CTRL	
8E	R/W, P/E	MODE2_LDO_SETTING						
8F	R/W, P/E	MODE2_LDO_POWER_ON_DELAY						
90	R/W, P/E	MODE2_GPIO_POWER_ON_DELAY						
91	R/W, P/E	MODE3_VOUT1_SETTING_HIGH						
92	R/W, P/E	MODE3_VOUT2_SETTING_HIGH						
93	R/W, P/E	MODE3_BUCK1_FB_HALF	MODE3_BUCK2_FB_HALF	MODE3_VOUT1_SETTING_LOW		MODE3_VOUT2_SETTING_LOW		
94	R/W, P/E	MODE3_CLK_MODE	MODE3_SINGLE/DUAL	RESERVED	MODE3_BUCK1_FSW	MODE3_BUCK2_FSW		
95	R/W, P/E	MODE3_BUCK1_POWER_ON_DELAY						
96	R/W, P/E	MODE3_BUCK2_POWER_ON_DELAY						
97	R/W, P/E	MODE3_VOUT1_SOFT_START_TIME			MODE3_VOUT2_SOFT_START_TIME		MODE3_LDO_EN	RV
98	R/W, P/E	MODE3_LDO_SOFT_START_TIME			MODE3_I2C_ADDRESS		MODE3_GPIO_CTRL	
99	R/W, P/E	MODE3_LDO_SETTING						
9A	R/W, P/E	MODE3_LDO_POWER_ON_DELAY						
9B	R/W, P/E	MODE3_GPIO_POWER_ON_DELAY						
9C	R/W, P/E	MODE4_VOUT1_SETTING_HIGH						
9D	R/W, P/E	MODE4_VOUT2_SETTING_HIGH						
9E	R/W, P/E	MODE4_BUCK1_FB_HALF	MODE4_BUCK2_FB_HALF	MODE4_VOUT1_SETTING_LOW		MODE4_VOUT2_SETTING_LOW		
9F	R/W, P/E	MODE4_CLK_MODE	MODE4_SINGLE/DUAL	RESERVED	MODE4_BUCK1_FSW	MODE4_BUCK2_FSW		
A0	R/W, P/E	MODE4_BUCK1_POWER_ON_DELAY						
A1	R/W, P/E	MODE4_BUCK2_POWER_ON_DELAY						
A2	R/W, P/E	MODE4_VOUT1_SOFT_START_TIME			MODE4_VOUT2_SOFT_START_TIME		MODE4_LDO_EN	RV
A3	R/W, P/E	MODE4_LDO_SOFT_START_TIME			MODE4_I2C_ADDRESS		MODE4_GPIO_CTRL	
A4	R/W, P/E	MODE4_LDO_SETTING						
A5	R/W, P/E	MODE4_LDO_POWER_ON_DELAY						
A6	R/W, P/E	MODE4_GPIO_POWER_ON_DELAY						
A7	R/W, P/E	MODE5_VOUT1_SETTING_HIGH						
A8	R/W, P/E	MODE5_VOUT2_SETTING_HIGH						
A9	R/W, P/E	MODE5_BUCK1_FB_HALF	MODE5_BUCK2_FB_HALF	MODE5_VOUT1_SETTING_LOW		MODE5_VOUT2_SETTING_LOW		
AA	R/W, P/E	MODE5_CLK_MODE	MODE5_SINGLE/DUAL	RESERVED	MODE5_BUCK1_FSW	MODE5_BUCK2_FSW		
AB	R/W, P/E	MODE5_BUCK1_POWER_ON_DELAY						
AC	R/W, P/E	MODE5_BUCK2_POWER_ON_DELAY						

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

AD	R/W, P/E	MODE5_VOUT1_SOFT_START_TIME		MODE5_VOUT2_ SOFT_START_TIME	MODE5_ LDO EN	RESERVED
AE	R/W, P/E	MODE5_LDO_SOFT_START_TIME		MODE5_I2C_ ADDRESS	MODE5_GPIO_ CTRL	
AF	R/W, P/E	MODE5_LDO_SETTING				
B0	R/W, P/E	MODE5_LDO_POWER_ON_DELAY				
B1	R/W, P/E	MODE5_GPIO_POWER_ON_DELAY				
B2	R/W, P/E	MODE6_VOUT1_SETTING_HIGH				
B3	R/W, P/E	MODE6_VOUT2_SETTING_HIGH				
B4	R/W, P/E	MODE6_BUCK1_FB_HALF	MODE6_BUCK2_ FB_HALF	MODE6_VOUT1_ SETTING_LOW	MODE6_VOUT2_ SETTING_LOW	
B5	R/W, P/E	MODE6_CLK_MODE	MODE6_ SINGLE/DUAL	RESERVED	MODE6_ BUCK1_FSW	MODE6_BUCK2_ FSW
B6	R/W, P/E	MODE6_BUCK1_POWER_ON_DELAY				
B7	R/W, P/E	MODE6_BUCK2_POWER_ON_DELAY				
B8	R/W, P/E	MODE6_VOUT1_SOFT_START_TIME		MODE6_VOUT2_ SOFT_START_TIME	MODE6_ LDO_EN	RV
B9	R/W, P/E	MODE6_LDO_SOFT_START_TIME		MODE6_I2C_ ADDRESS	MODE6_GPIO_ CTRL	
BA	R/W, P/E	MODE6_LDO_SETTING				
BB	R/W, P/E	MODE6_LDO_POWER_ON_DELAY				
BC	R/W, P/E	MODE6_GPIO_POWER_ON_DELAY				
BD	R/W, P/E	MODE7_VOUT1_SETTING_HIGH				
BE	R/W, P/E	MODE7_VOUT2_SETTING_HIGH				
BF	R/W, P/E	MODE7_BUCK1_FB_HALF	MODE7_ BUCK2_FB_HALF	MODE7_VOUT1_ SETTING_LOW	MODE7_VOUT2_ SETTING LOW	
C0	R/W, P/E	MODE7_CLK_MODE	MODE7_ SINGLE/DUAL	RESERVED	MODE7_ BUCK1_FSW	MODE7_BUCK2_ FSW
C1	R/W, P/E	MODE7_BUCK1_POWER_ON_DELAY				
C2	R/W, P/E	MODE7_BUCK2_POWER_ON_DELAY				
C3	R/W, P/E	MODE7_VOUT1_SOFT_START_TIME		MODE7_VOUT2_ SOFT_START_TIME	MODE7_ LDO_EN	RESERVED
C4	R/W, P/E	MODE7_LDO_SOFT_START_TIME		MODE7_I2C_ ADDRESS	MODE7_GPIO_ CTRL	
C5	R/W, P/E	MODE7_LDO_SETTING				
C6	R/W, P/E	MODE7_LDO_POWER_ON_DELAY				
C7	R/W, P/E	MODE7_GPIO_POWER_ON_DELAY				

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

I²C REGISTER REGION DESCRIPTION

The I²C registers are volatile memories. These registers directly control PMIC operation.

LOCK (00h)

Format: Unsigned binary

The LOCK command locks the writes for the I²C registers.

Bits	Access	Bit Name	Default	Description
D[0]	R/W	I2C_LOCK_EN	1'b 1	Enables locking writes for the I²C registers. I²C writing is ineffective when LOCK_EN = 1. 0: Disabled 1: Enabled

BUCK1_CTRL1 (01h)

Format: Unsigned binary

The BUCK1_CTRL1 command sets GO_BIT and the slew rate for buck 1's output voltage (V_{OUT1}).

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT1_GO_BIT	1'b 0	VOUT1_GO_BIT is a self-clearing bit. Make the new VOUT1_SETTING configuration, then set VOUT1_GO_BIT = 1 to start dynamic voltage scaling. When V_{OUT1} reaches the new voltage target, VOUT1_GO_BIT is automatically cleared. 1'b 0: Disable changing VOUT1_SETTING 1'b 1: Enable changing VOUT1_SETTING on the fly
D[6:2]	R/W	RESERVED	5'b 0000 0	Reserved.
D[1:0]	R/W	VOUT1_SLEW_RATE	2'b 00	Sets the V_{OUT1} slew rate during dynamic voltage scaling (no external FB divider resistor). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK1_CTRL2 (02h)

Format: Unsigned binary

The BUCK1_CTRL2 command sets buck 1's operation mode and f_{SW}.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK1_PFM/PWM	2'b 11	Selects buck 1's mode. 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode at light loads 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK1_FSW	2'b 01	Sets buck 1's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RESERVED	1'b 0	Reserved.
D[2:0]	RW	VOUT1_SETTING_LOW	3'b 000 (Or MODE-Determined)	Works with VOUT1_SETTING_HIGH to set V_{OUT1}.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK1_CTRL3 (03h)

Format: Direct

The BUCK1_CTRL3 command sets V_{OUT1}.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT1_SETTING_HIGH	8'b 0011 0010 (Or MODE-Determined)	VOUT1_SETTING_HIGH works with VOUT1_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT1}. When BUCK1_FB_HALF = 0: If the bits value ≤ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100(300d) ≤ the bits value ≤ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK1_FB_HALF = 1: If the bits value ≤ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ≤ the bits value ≤ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ≥ 111 0110 1100 (1900d), the setting = 3800mV.

BUCK1_CTRL4 (04h)

Format: Unsigned binary

The BUCK1_CTRL4 command enables V_{OUT1} discharging and over-voltage protection (OVP), and it sets the over-current (OC) threshold.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT1_DISCHRGE_EN	1'b 1	Enables buck 1's output passive discharge function. If the passive discharge function is enabled, when buck 1 is disabled, a discharging resistor is connected to the VOUT1_FB_P pin to discharge V_{OUT1} until it reaches 100mV. 0: Disabled 1: Enabled
D[6]	R/W	VOUT1_OVP_EN	1'b 1	Enables buck 1's output active OVP function. If output OVP is enabled, buck 1 actively turns on the LS-FET to discharge V_{OUT1}. See the Over-Voltage Protection (OVP) section on page 15 for more details. 0: Disabled 1: Enabled
D[5]	R/W	RESERVED	1'b 0	Reserved.
D[4:2]	R/W	BUCK1_OC_TH	3'b 000	Sets buck 1's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RESERVED	2'b 00	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK1_CTRL7 (05h)

Format: Unsigned binary

The BUCK1_CTRL7 command sets thresholds for VOUT1_PG_HIGH, VOUT1_PG_LOW, VOUT1_UV, VOUT1_OV.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT1_PG_VTH_HIGH	2'b 00	Sets V_{OUT1}'s high-side voltage for the power good status (no external FB divider resistor). The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT1_SETTING 2'b 01: +10% from VOUT1_SETTING 2'b 10: +12.5% from VOUT1_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT1_PG_VTH_LOW	1'b 0	Sets V_{OUT1}'s low-side voltage threshold for the power good status. The hysteresis = 2.5%. 0: -7.5% from VOUT1_SETTING 1: -10% from VOUT1_SETTING
D[4]	R/W	RESERVED	1'b 0	Reserved.
D[3:2]	R//W	VOUT1_UV_VTH	2'b 00	Sets V_{OUT1}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT1_SETTING 2'b 01: -12.5% from VOUT1_SETTING 2'b 10: Reserved 2'b 11: Reserved
D[1:0]	R//W	VOUT1_OV_VTH	2'b 10	Sets V_{OUT1}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +8% from VOUT1_SETTING 2'b 01: +10.5% from VOUT1_SETTING 2'b 10:+13% from VOUT1_SETTING 2'b 11: Reserved

BUCK2_CTRL1 (06h)

Format: Unsigned binary

The BUCK2_CTRL1 command sets GO_BIT and the slew rate for buck 2's output voltage (V_{OUT2}).

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT2_GO_BIT	1'b 0	VOUT2_GO_BIT is a self-clearing bit. Make the new VOUT2_SETTING configuration, then set VOUT2_GO_BIT = 1 to start dynamic voltage scaling. When V_{OUT2} reaches the new voltage target, VOUT2_GO_BIT is automatically cleared. 1'b 0: Disable changing VOUT2_SETTING 1'b 1: Enable changing VOUT2_SETTING on the fly
D[6:2]	R/W	RESERVED	5'b 0000 0	Reserved.
D[1:0]	R/W	VOUT2_SLEW_RATE	2'b 00	Sets the V_{OUT2} slew rate during dynamic voltage scaling (no external FB divider resistor). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK2_CTRL2 (07h)

Format: Unsigned binary

The BUCK2_CTRL2 command sets buck 2's operation mode and f_{SW}.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK2_PFM/PWM	2'b 11	Selects buck 2's mode. 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK2_ FSW	2'b 01	Sets buck 2's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RESERVED	1'b 0	Reserved.
D[2:0]	RW	VOUT2_SETTING_ LOW	3'b 000 (Or MODE-Determined)	Works with VOUT2_SETTING_HIGH to set V_{OUT2}.

BUCK2_CTRL3 (08h)

Format: Direct

The BUCK2_CTRL3 command sets V_{OUT2}.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT2_SETTING_ HIGH	8'b 0011 0010 (Or MODE-Determined)	VOUT2_SETTING_HIGH works with VOUT2_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT2}. When BUCK2_FB_HALF = 0: If the bits value ≤ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100(300d) ≤ the bits value ≤ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK2_FB_HALF = 1: If the bits value ≤ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ≤ the bits value ≤ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ≥ 111 0110 1100 (1900d), the setting = 3800mV.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK2_CTRL4 (09h)

Format: Unsigned binary

The BUCK2_CTRL4 command enables V_{OUT2} discharge and over-voltage protection (OVP), and it sets the over-current (OC) threshold.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT2_DISCHRGE_EN	1'b 1	Enables buck 2's output passive discharge function. If the passive discharge function is enabled, when buck 2 is disabled, a discharging resistor is connected to the VOUT2_FB_P pin to discharge V_{OUT2} until it reaches 100mV. 0: Disabled 1: Enabled
D[6]	R/W	VOUT2_OVP_EN	1'b 1	Enables buck 2's output active OVP function. If output OVP is enabled, buck 2 actively turns on the LS-FET to discharge V_{OUT1}. See the Over-Voltage Protection (OVP) section on page 15 for more details. 0: Disabled 1: Enabled
D[5]	R/W	RESERVED	1'b 0	Reserved.
D[4:2]	R/W	BUCK2_OC_TH	3'b 000	Sets buck 2's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RESERVED	2'b 00	Reserved.

BUCK2_CTRL7 (0Ah)

Format: Unsigned binary

The BUCK2_CTRL7 command sets the thresholds for VOUT2_PG_HIGH, VOUT2_PG_LOW, VOUT2_UV, and VOUT2_OV.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT2_PG_VTH_HIGH	2'b 00	Sets V_{OUT2}'s high-side voltage for the power good status (no external FB divider resistor). The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT2_SETTING 2'b 01: +10% from VOUT2_SETTING 2'b 10: +12.5% from VOUT2_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT2_PG_VTH_LOW	1'b 0	Sets V_{OUT2}'s low-side voltage threshold for the power good status. The hysteresis = 2.5%. 0: -7.5% from VOUT2_SETTING 1: -10% from VOUT2_SETTING
D[4]	RW	RESERVED	1'b 0	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[3:2]	R/W	VOUT2_UV_VTH	2'b 00	Sets V_{OUT2}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT2_SETTING 2'b 01: -12.5% from VOUT2_SETTING 2'b 10: Reserved 2'b 11: Reserved
D[1:0]	R/W	VOUT2_OV_VTH	2'b 10	Sets V_{OUT2}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +8% from VOUT2_SETTING 2'b 01: +10.5% from VOUT2_SETTING 2'b 10:+13% from VOUT2_SETTING 2'b 11: Reserved

LDO_CTRL1 (0Bh)

Format: Unsigned binary

The LDO_CTRL1 command sets GO_BIT, discharge function, and PG threshold for the low-dropout (LDO) regulator.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	LDO_GO_BIT	1'b 0	0: Disable changing LDO_SETTING on the fly 1: Enable changing LDO_SETTING on the fly
D[6:2]	RV	RESERVED	5'b 0000 0	Reserved.
D[1]	R/W	LDO_DISCHG	1'b 1	0: Disable LDO discharge 1: Enable LDO discharge
D[0]	R/W	LDO_PG_VTH	1'b 0	Sets the LDO output threshold voltage for the power good status. The hysteresis = 5%. 0: -10% from LDO_SETTING 1: -15% from LDO_SETTING

LDO_CTRL2 (0Ch)

Format: Direct

The LDO_CTRL2 command sets the LDO's output voltage.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RESERVED	1'b 0	Reserved.
D[6:0]	R/W	LDO_SETTING	7'b 011 1100 (Or MODE-determined)	Sets the LDO's output voltage. 30mV per LSB from 0.6V to 3.6V. All lower settings: Reserved 001 0100: 600mV 001 0101: 630mV … 111 1000: 3600 mV All higher settings: Reserved

SYS_CTRL1 (0Dh)

Format: Unsigned binary

The SYS_CTRL1 command enables the PMIC, VOUT1, VOUT2, LDO, and GPIO.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	PMIC_EN	1'b 1	0: Buck 1, buck 2, and the LDO are all disabled 1: Buck 1, buck 2, and the LDO are all enabled (must enable each regulator via I²C set-up)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[6]	R/W	VOUT1_EN	1'b 1	0: Disable buck 1 1: Enable buck 1
D[5]	R/W	VOUT2_EN	1'b 1	0: Disable buck 2 1: Enable buck 2
D[4]	R/W	LDO_EN	1'b 0	0: Disable LDO 1: Enable LDO
D[3:2]	R/W	RESERVED	2'b 00	Reserved.
D[1:0]	R/W	GPIO_CTRL	2'b 10	Sets GPIO's open-drain output control. 2'b 00: The GPIO output is low 2'b 01: GPIO is an analog input for the ADC 2'b 10: GPIO is part of flex-time control and used as the external converter's enable signal. GPIO outputs as an EN signal for the external converter and its on/off sequence can be configured via the 0x57 and 0x58 registers 2'b 11: The GPIO output is floating/high

SYS_CTRL3 (0Eh)

Format: Unsigned binary

The SYS_CTRL3 command sets the VIN_PG threshold and PG mask.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	VIN_PG_VTH	3'b 110	Sets the V_{IN} rising threshold for VIN_PG. VIN_PG (0x19) is 0 (power good) even if V_{IN} < V_{IN} PG falling threshold after V_{IN} start-up. Then ramp up V_{IN} to be ≥ V_{IN} rising threshold. If V_{IN} triggers the V_{IN} PG falling threshold again, VIN_PG changes to 1 (power not good). The hysteresis = 0.5V. 3'b 000: 9.5V (same as 001) 3'b 001: 9.5V 3'b 010: 8.5V 3'b 011: 7.5V 3'b 100: 6.5V 101: 5.5V 110: 4.25V 111: Reserved
D[4]	R/W	MASK_PG	1'b 0	Masks the INT pin behavior. The STATUS register still indicates the PG status. 0: Not masked 1: Masked
D[3:0]	R/W	RESERVED	4'b 0000	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

SYS_CTRL4 (0Fh)

Format: Unsigned binary

The SYS_CTRL4 command sets the over-temperature (OT) threshold and OT warning threshold.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	OT_TH	3'b 100	Sets the converter's temperature shutdown threshold. The hysteresis = 20°C. 3'b 000: 125°C 3'b 001: 135°C 3'b 010: 145°C 3'b 011: 155°C 3'b 100: 165°C 3'b 101: Reserved 3'b 110: Reserved 3'b 111:Reserved
D[4:2]	R/W	OTW_TH	3'b 110	Sets the OT warning threshold. The hysteresis = 20°C. 3'b 000: Reserved 3'b 001: 100°C 3'b 010: 110°C 3'b 011: 120°C 3'b 100: 130°C 3'b 101: 140°C 3'b 110: 150°C 3'b 111: Reserved
D[1:0]	R/W	RESERVED	2'b 00	Reserved.

ADC_CTRL1 (10h)

Format: Unsigned binary

The ADC_CTRL1 command sets ADC_EN and ADC_SAMPLE_FREQ.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	ADC_EN	1'b 1	0: Disable the ADC 1: Enable the ADC
D[6:2]	R/W	RESERVED	5'b 00000	Reserved.
D[1:0]	R/W	ADC_SAMPLE_ FREQ	2'b 01	Sets the frequency to refresh all the ADC channels 00: 4kHz 01: 2kHz 10: 1kHz 11: 0.5kHz

TEMPERATURE (11h)

Format: Unsigned binary

The TEMPERATURE command monitors the IC's temperature.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/O	TEMPERATURE	3'b 000	Monitors the PMIC's temperature. 000: < 80°C 001: 85°C 010: 95°C 011: 105°C 100: 115°C 101: 125°C 110: 135°C 111: ≥ 140°C

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[4:0]	R/W	RESERVED	5’b 00000	Reserved.

VOUT1_ADC (12h)

Format: Direct

The VOUT1_ADC command monitors V_{OUT1}.

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	VOUT1_ADC	8’b 0000 0000	Returns V_{OUT1}. 16mV per LSB. 0000 0000: Undefined 0000 0001: 16mV 0000 0010: 32mV … 1111 1110: 4064mV 1111 1111: ≥ 4080mV

IOUT1_ADC (13h)

Format: Direct

The IOUT1_ADC command monitors buck 1’s output current.

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	IOUT1_ADC	8’b 0000 0000	Returns buck 1’s output current. 50mA per LSB. 0000 0000: 0 A 0000 0001: 0.05A 0000 0010: 0.1A … 1111 1110: 12.7A 1111 1111: 12.75A

VOUT2_ADC (14h)

Format: Direct

The VOUT2_ADC command monitors V_{OUT2}.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	VOUT2_ADC	8’b 0000 0000	Returns V_{OUT2}. 16mV per LSB. 0000 0000: Undefined 0000 0001: 16mV 0000 0010: 32mV … 1111 1110: 4064mV 1111 1111: ≥ 4080mV

IOUT2_ADC (15h)

Format: Direct

The IOUT2_ADC command monitors buck 2’ output current.

Bits	Access	Bit name	Default	Description
D[7:0]	RO	IOUT2_ADC	8’b 0000 0000	Returns buck 2’s output current. 50mA per LSB. 0000 0000: 0 A 0000 0001: 0.05A 0000 0010: 0.1A … 1111 1110: 12.7A 1111 1111: 12.75A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

LDO_ADC (16h)

Format: Direct

The LDO_ADC command monitors the LDO's output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	LDO_ADC	8'b 0000 0000	Sets the LDO 's output voltage. 16mV per LSB. 0000 0000: Undefined 0000 0001: 16mV 0000 0010: 32mV … 1111 1110: 4064mV 1111 1111: ≥ 4080mV

GPIO_ADC (17h)

Format: Direct

The GPIO_ADC command monitors GPIO output voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	GPIO_ADC	8'b 0000 0000	Returns the GPIO's output voltage. 8mV per LSB. 0000 0000: 0mV 0000 0001 : 8mV … 1111 1111: 2040mV

VIN_ADC (18h)

Format: Direct

The VIN_ADC command monitors the input voltage.

Bits	Access	Bit Name	Default	Description
D[7:0]	RO	VIN_ADC	8'b 0000 0000	Returns the input voltage. 64mV per LSB. 0000 0000: 0mV 0000 0001: 64mV 0000 0010: 128mV … 1111 1111: ≥ 16320mV

FAULT_STATUS (19h)

Format: Direct

The FAULT_STATUS command monitors the fault statuses of V_{IN}, V_{OUT1}, V_{OUT2}, the LDO, and over-temperature warning (OTW) and OT conditions.

Bits	Access	Bit Name	Default	Description
D[7]	RO	VIN_PG	1'b 0	Indicates V_{IN}'s power good status. If a V_{IN} over-voltage (OV) or under-voltage (UV) fault occurs, this bit is set and latched. Send a CLEAR1 (1Dh) command to reset this bit. 0: Power good 1: Power not good
D[6]	RO	VOUT1_FAULT	1'b 0	Indicates V_{OUT1}'s fault status. If a V_{OUT1} fault occurs, this bit is set and latched. Send a CLEAR1 (1Dh) command to reset this bit. 0: Normal start-up (or EN is off) 1: A V_{OUT1} fault has occurred when EN is on

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[5]	RO	VOUT2_FAULT	1'b 0	Indicates V_{OUT2}'s fault status. If a V_{OUT2} fault occurs, this bit is set and latched. Send a CLEAR1 (1Dh) command to reset this bit. 0: Normal start-up (or EN is off) 1: A V_{OUT2} fault has occurred when EN is on
D[4]	RO	LDO_FAULT	1'b 0	Indicates the LDO's fault status. If an LDO fault occurs, this bit is set and latched. Send a CLEAR1 (1Dh) command to reset this bit. 0: Power good (or EN is off) 1: An LDO fault has occurred when EN is on
D[3:2]	R/W	RESERVED	2'b 00	Reserved.
D[1]	RO	OTW	1'b 0	Indicates the over-temperature warning status. If an OTW occurs, this bit is set and latched. Send a CLEAR1 (1Dh) command to reset this bit. 0: The temperature is below the warning threshold 1: The temperature exceeds the warning threshold
D[0]	RO	OT	1'b 0	Indicates the temperature shutdown status. If an OT fault occurs, this bit is set and latched. Send a CLEAR1 (1Dh) command to reset this bit. 0: No temperature shutdown has occurred 1: Temperature shutdown has occurred

STATUS1 (1Ah)

Format: Direct

The STATUS1 command monitors fault statuses.

Bits	Access	Bit Name	Default	Description
D[7]	RO	VIN_OV	1'b 0	Indicates the V_{IN} over-voltage (OV) status. 0: No OV condition 1: There is an OV condition
D[6]	RO	VIN_UV	1'b 0	Indicates the V_{IN} under-voltage (UV) status. 0: No UV condition 1: There is an UV condition
D[5]	RO	VOUT1_OV	1'b 0	Indicates the V_{OUT1} OV status. 0: No OV condition 1: There is an OV condition
D[4]	RO	VOUT2_OV	1'b 0	Indicates the V_{OUT2} OV status. 0: No OV condition 1: There is an OV condition
D[3]	RO	VOUT1_UV	1'b 0	Indicates the V_{OUT1} UV status. 0: No UV condition 1: There is an UV condition
D[2]	RO	VOUT2_UV	1'b 0	Indicates the V_{OUT2} UV status. 0: No UV condition 1: There is an UV condition

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[1]	RO	VOUT1_OC	1'b 0	Indicates buck 1's output current limit warning status. 0: No current-limit event has occurred 1: A current-limit event has occurred
D[0]	RO	VOUT2_OC	1'b 0	Indicates buck 2's output current limit warning status. 0: No current-limit event has occurred 1: A current-limit event has occurred

MASK1 (1Bh)

Format: Unsigned binary

The MASK1 command masks the INT pin's behavior. The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	RW	VIN_PG_MSK	1'b 0	0: Do not mask 1: Mask
D[6]	RW	VOUT1_PG_MSK	1'b 0	0: Do not mask 1: Mask
D[5]	RW	VOUT2_PG_MSK	1'b 0	0: Do not mask 1: Mask
D[4]	RW	LDO_PG_MSK	1'b 0	0: Do not mask 1: Mask
D[3:2]	RW	RV	2'b 00	Reserved.
D[1]	RW	OTW_MSK	1'b 0	0: Do not mask 1: Mask
D[0]	RW	OT_MSK	1'b 0	0: Do not mask 1: Mask

MASK2 (1Ch)

Format: Unsigned binary

The MASK2 command masks the INT pin's behavior. The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	RW	VIN_OV_MSK	1'b 0	0: Do not mask 1: Mask
D[6]	RW	VIN_UV_MSK	1'b 0	0: Do not mask 1: Mask
D[5]	RW	VOUT1_OV_MSK	1'b 0	0: Do not mask 1: Mask
D[4]	RW	VOUT2_OV_MSK	1'b 0	0: Do not mask 1: Mask
D[3]	RW	VOUT1_UV_MSK	1'b 0	0: Do not mask 1: Mask
D[2]	RW	VOUT2_UV_MSK	1'b 0	0: Do not mask 1: Mask
D[1]	RW	VOUT1_OC_MSK	1'b 0	0: Do not mask 1: Mask
D[0]	RW	VOUT2_OC_MSK	1'b 0	0: Do not mask 1: Mask

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CLEAR1 (1Dh)

Format: Direct

This CLEAR1 command clears the corresponding fault bits that have been set.

Bits	Access	Bit Name	Default	Description
D[7]	1O	VIN_PG_CLEAR	1'b 0	Clears the V_{IN} power good status. 1: Clear the status
D[6]	1O	VOUT1_FAULT_ CLEAR	1'b 0	Clears the V_{OUT1} fault status from FAULT_STATUS (19h). 1: Clear the status
D[5]	1O	VOUT2_FAULT_ CLEAR	1'b 0	Clears the V_{OUT2} fault status from FAULT_STATUS (19h). 1: Clear the status
D[4]	1O	LDO_FAULT_CLEAR	1'b 0	Clears the LDO fault status from FAULT_STATUS (19h). 1: Clear the status
D[3]	1O	OTW_CLEAR	1'b 0	Clears the over-temperature (OT) warning status. 1: Clear the status
D[2]	1O	OT_CLEAR	1'b 0	Clears the OT status. 1: Clear the status
D[1]	R/W	RESERVED	1'b 0	Reserved
D[0]	1O	ALL_STATUS_CLEAR	1'b 0	1: Clears all the status bits

CLEAR2 (1Eh)

Format: Direct

This CLEAR2 command clears the corresponding fault bits that have been set.

Bits	Access	Bit Name	Default	Description
D[7]	1O	VIN_OV_CLEAR	1'b 0	Clears the V_{IN} over-voltage (OV) status. 1: Clear the status
D[6]	1O	VIN_UV_CLEAR	1'b 0	Clears the V_{IN} under-voltage (UV) status. 1: Clear the status
D[5]	1O	VOUT1_OV_CLEAR	1'b 0	Clears the V_{OUT1} OV status. 1: Clear the status
D[4]	1O	VOUT2_OV_CLEAR	1'b 0	Clears the V_{OUT2} OV status. 1: Clear the status
D[3]	1O	VOUT1_UV_CLEAR	1'b 0	Clears the V_{OUT1} UV status. 1: Clear the status
D[2]	1O	VOUT2_UV_CLEAR	1'b 0	Clears the V_{OUT2} UV status. 1: Clear the status
D[1]	1O	VOUT1_OC_CLEAR	1'b 0	Clears buck 1's output current limit warning status. 1: Clear the status
D[0]	1O	VOUT2_OC_CLEAR	1'b 0	Clear buck 2's output current limit warning status. 1: Clear the status

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

AVP_CTRL1 (1Fh)

Format: Unsigned binary

This AVP_CTRL1 command enables the AVP function for buck 1.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP1_EN	1'b 0	Enables buck 1's AVP function. 0: Disabled 1: Enabled
D[6:5]	R/W	AVP1_GAIN	2'b 00	Sets the AVP gain. 00: 2.6mV/A 01: 5.7mV/A 10: 8.6mV/A 11:11.3mV/A
D[4:0]	R/W	AVP1_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV per step. x0000: 0mV 00001: 2mV … 01111: 30mV 10001: -2mV … 11111: -30mV

AVP_CTRL2 (20h)

Format: Unsigned binary

This AVP_CTRL2 command enables the AVP function for buck 2.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP2_EN	1'b 0	Enables buck 2's AVP function. In dual-phase, single-output mode, this function is invalid. 0: Disabled 1: Enabled
D[6:5]	R/W	AVP2_GAIN	2'b 00	Sets the AVP gain. In dual-phase, single-output mode, this function is invalid. 00: 2.6mV/A 01: 5.7mV/A 10: 8.6mV/A 11:11.3mV/A
D[4:0]	R/W	AVP2_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV per step. x0000: 0mV 00001: 2mV … 01111: 30mV 10001: -2mV … 11111: -30mV

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

STATUS2 (21h)

Format: Direct

The STATUS2 command monitors the statuses of VIN_PG, VOUT1_PG, VOUT2_PG, LDO_PG, OT_WARNING, and OT_FAULT.

Bits	Access	Bit Name	Default	Description
D[7]	R	VIN_PG_STATUS	1'b 0	Indicates the V_{IN} power good status. This is an active bit that does not have to be cleared. 0: Normal start-up 1: A V_{IN} fault has occurred
D[6]	R	VOUT1_PG_STATUS	1'b 0	Indicates the V_{OUT1} power good status. This is an active bit that does not have to be cleared. 0: Normal start-up 1: V_{OUT1} is not at its target
D[5]	R	VOUT2_PG_STATUS	1'b 0	Indicates the V_{OUT2} power good status. This is an active bit that does not have to be cleared. 0: Normal start-up 1: V_{OUT2} is not at its target
D[4]	R	LDO_PG_STATUS	1'b 0	Indicates the LDO power good status. This is an active bit that does not have to be cleared. 0: Normal start-up 1: The LDO voltage is not at its target
D[3:2]	R	RESERVED	2'b 00	Reserved.
D[1]	R	OT_WARNING_ STATUS	1'b 0	Indicates the over-temperature warning (OTW) status. This is an active bit that does not have to be cleared. 0: Normal start-up 1: An OTW has occurred
D[0]	R	OT_FAULT_STATUS	1'b 0	Indicates the OT fault status. This is an active bit that does not have to be cleared. 0: Normal start-up 1: An OT fault has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MTP REGISTER REGION DESCRIPTION

The MTP registers are non-volatile memories. Most of the MTP registers are related to the registers from the I²C. The MTP registers do not directly control the converter's operation. During start-up through VIN, the settings are copied from the MTP registers to the I²C registers.

LOCK (40h)

Format: Direct

The LOCK command sets the MTP region's access password.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MTP_REGION_ ACCESS_ PASSWORD	8'b 0000 0000	The correct password must be used to access the MTP register region and MODE register region. Contact an MPS FAE for the password.

BUCK1_CTRL1 (41h)

The BUCK1_CTRL1 command sets the default settings for BUCK1_CTRL1 (01h). The only bits that have direct control of converter operation are VOUT1_SOFT_START and VOUT1_SOFT_STOP.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RV	1'b 0	Reserved
D[6:4]	R/W	VOUT1_SOFT_ START	3'b 001	Sets buck 1's soft-start time after being enabled. The output is between 0% and 100% of V_{OUT1}. 3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 6ms 3'b 100: 8ms 3'b 101: 10ms 3'b 110:12ms 3'b 111: 14ms
D[3:2]	R/W	VOUT1_SOFT_STOP	2'b 00	Sets buck 1's soft-stop time after being enabled. The output is between 0% and 100% of V_{OUT1}. 2'b 00: 0.5ms 2'b 01: 1ms 2'b 10: 2ms 2'b 11: 4ms
D[1:0]	R/W	VOUT1_SLEW_RATE	2'b 00	Sets V_{OUT1}'s slew rate during dynamic voltage scaling (no external FB divider resistor). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK1_CTRL2 (42h)

The BUCK1_CTRL2 command sets the default setting for BUCK1_CTRL2 (02h). This command does not have direct control of converter operation. In single-phase, dual-output mode, it is recommended to set BUCK1_FSW and BUCK2_FSW to the same frequency.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK1_PFM/PWM	2'b 11	Selects buck 1's mode. 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode at light loads 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK1_FSW	2'b 01	Sets buck 1's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RESERVED	1'b 0	Reserved.
D[2:0]	RW	VOUT1_SETTING_ LOW	3'b 000 (Or MODE-Determined)	Works with VOUT1_SETTING_HIGH to set V_{OUT1}.

BUCK1_CTRL3 (43h)

The BUCK1_CTRL3 command sets the default setting for BUCK1_CTRL3 (03h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT1_SETTING_ HIGH	8'b 0011 0010 (Or MODE-Determined)	VOUT1_SETTING_HIGH works with VOUT1_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT1}. When BUCK1_FB_HALF = 0: If the bits value ≤ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100(300d) ≤ the bits value ≤ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK1_FB_HALF = 1: If the bits value ≤ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ≤ the bits value ≤ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ≥ 111 0110 1100 (1900d), the setting = 3800mV.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK1_CTRL4 (44h)

The BUCK1_CTRL4 command sets the default setting for BUCK1_CTRL4 (04h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT1_DISCHRGE_EN	1'b 1	Enables buck 1's output passive discharge function. If the passive discharge function is enabled, when buck 1 is disabled, a discharging resistor is connected to the VOUT1_FB_P pin to discharge V_{OUT1} until it reaches 100mV. 0: Disabled 1: Enabled
D[6]	R/W	VOUT1_OVP_EN	1'b 1	Enables buck 1's output active OVP function. If output OVP is enabled, buck 1 actively turns on the LS-FET to discharge V_{OUT1}. See the Over-Voltage Protection (OVP) section on page 15 for more details. 0: Disabled 1: Enabled
D[5]	R/W	BUCK1_FB_HALF	1'b 0	Enables buck 1's internal FB half divider. 0: There is no internal FB divider 1: The internal 1/2 divider for FB divider is enabled
D[4:2]	R/W	BUCK1_OC_TH	3'b 000	Sets buck 1's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RESERVED	2'b 00	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK1_CTRL5 (45h)

The BUCK1_CTRL5 command sets buck 1's soft-start delay by counting a set number of CLK pulses.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK1_POWER_ON_DELAY	8'b 0000 0100 (Or MODE-Determined)	Sets buck 1's soft-start delay via CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001: 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

BUCK1_CTRL6 (46h)

The BUCK1_CTRL6 command sets buck 1's soft-stop delay by counting a set number of CLK pulses.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK1_POWER_OFF_DELAY	8'b 0000 0100	Sets buck 1's soft-stop delay via CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001 = 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK1_CTRL7 (47h)

The BUCK1_CTRL7 command sets the default setting for BUCK1_CTRL7 (05h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT1_PG_VTH_ HIGH	2'b 00	Sets V_{OUT1}'s high-side voltage for the power good status (no external FB divider resistor). The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT1_SETTING 2'b 01: +10% from VOUT1_SETTING 2'b 10: +12.5% from VOUT1_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT1_PG_VTH_LOW	1'b 0	Sets V_{OUT1}'s low-side voltage threshold for the power good status. The hysteresis = 2.5%. 0: -7.5% from VOUT1_SETTING 1: -10% from VOUT1_SETTING
D[4]	R/W	RESERVED	1'b 0	Reserved.
D[3:2]	R//W	VOUT1_UV_VTH	2'b 00	Sets V_{OUT1}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT1_SETTING 2'b 01: -12.5% from VOUT1_SETTING 2'b 10: Reserved 2'b 11: Reserved
D[1:0]	R//W	VOUT1_OV_VTH	2'b 10	Sets V_{OUT1}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +8% from VOUT1_SETTING 2'b 01: +10.5% from VOUT1_SETTING 2'b 10:+13% from VOUT1_SETTING 2'b 11: Reserved

BUCK2_CTRL1 (48h)

The BUCK2_CTRL1 command sets the default setting for BUCK2_CTRL1 (06h). The only bits that have direct control of converter operation are VOUT2_SOFT_START and VOUT2_SOFT_STOP.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RESERVED	1'b0	Reserved.
D[6:4]	R/W	VOUT2_SOFT_ START	3'b 001 (Or MODE-Determined)	Sets buck 2's soft-start time after being enabled. The output is between 0% and 100% of V_{OUT2}. 3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 6ms 3'b 100: 8ms 3'b 101: 10ms 3'b 110:12ms 3'b 111: 14ms
D[3:2]	R/W	VOUT2_SOFT_STOP	2'b 00	Sets buck 2's soft-stop time after being enabled. The output is between 0% and 100% of V_{OUT2}. 2'b 00: 0.5ms 2'b 01: 1ms 2'b 10: 2ms 2'b 11: 4ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[1:0]	R/W	VOUT2_SLEW_RATE	2'b 00	Sets V_{OUT2}'s slew rate during dynamic voltage scaling (no external FB divider resistor). 2'b 00: 0.5mV/μs 2'b 01: 1mV/μs 2'b 10: 2mV/μs 2'b 11: 4mV/μs

BUCK2_CTRL2 (49h)

The BUCK2_CTRL2 command sets the default settings for BUCK2_CTRL2 (07h). This command does not have direct control of converter operation. In dual-phase, single-output mode, the BUCK2_FSW, BUCK2_PFM/PWM, and VOUT2 settings are masked; instead, these values are determined by buck 1's corresponding setting.

In single-phase, dual-output mode, it is recommended to set BUCK1_FSW and BUCK2_FSW to the same frequency.

Bits	Access	Bit Name	Default	Description
D[7:6]	RW	BUCK2_PFM/PWM	2'b 11	Selects buck 2's mode. 00, 01: Reserved 2'b 10: Constant-on-time (COT); discontinuous conduction mode 2'b 11: COT; forced continuous current mode (FCCM)
D[5:4]	RW	BUCK2_ FSW	2'b 01	Sets buck 2's switching frequency. 2'b 00: 500kHz 2'b 01: 750kHz 2'b 10: 1000kHz 2'b 11: 1250kHz
D[3]	RW	RESERVED	1'b 0	Reserved.
D[2:0]	RW	VOUT2_SETTING_ LOW	3'b 000 (Or MODE-Determined)	Works with VOUT2_SETTING_HIGH to set V_{OUT2}.

BUCK2_CTRL3 (4Ah)

The BUCK2_CTRL3 command sets the default settings for BUCK2_CTRL3 (08h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	VOUT2_SETTING_ HIGH	8'b 0011 0010 (Or MODE-Determined)	VOUT2_SETTING_HIGH works with VOUT2_SETTING_LOW. By adding these bits together, an 11-bit register controls V_{OUT2}. When BUCK2_FB_HALF = 0: If the bits value ≤ 001 0010 1100 (300d), the setting = 300mV. If 001 0010 1100(300d) ≤ the bits value ≤ 111 1111 1111 (2047d), then the bits value is defined as equal to *X*, with the setting = *X*(mV). 1mV/step. When BUCK2_FB_HALF = 1: If the bits value ≤ 000 1001 0110 (150d), the setting = 300mV. If 000 1001 0110 (150d) ≤ the bits value ≤ 111 0110 1100 (1900d), then the bits value is defined as equal to *X*, with the setting = 2 x *X*(mV). 2mV/step. If the bits value ≥ 111 0110 1100 (1900d), the setting = 3800mV.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK2_CTRL4 (4Bh)

The BUCK2_CTRL4 command sets the default setting for BUCK2_CTRL4 (09h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	VOUT2_DISCHRGE_EN	1'b 1	Enables buck 2's output passive discharge function. If the passive discharge function is enabled, when buck 2 is disabled, a discharging resistor is connected to the VOUT2_FB_P pin to discharge V_{OUT2} until it reaches 100mV. 0: Disabled 1: Enabled
D[6]	R/W	VOUT2_OVP_EN	1'b 1	Enables buck 2's output active OVP function. If output OVP is enabled, buck 2 actively turns on the LS-FET to discharge V_{OUT1}. See the Over-Voltage Protection (OVP) section on page 15 for more details. 0: Disabled 1: Enabled
D[5]	R/W	RESERVED	1'b 0	Reserved.
D[4:2]	R/W	BUCK2_OC_TH	3'b 000	Sets buck 2's valley current limit threshold. 3'b 000: 4A 3'b 001: 4.5A 3'b 010: 5A 3'b 011: 5.5A 3'b 100: 6A 3'b 101: 6.5A 3'b 110: 7A 3'b 111: 7.5A
D[1:0]	R/W	RESERVED	2'b 00	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK2_CTRL5 (4Ch)

The BUCK2_CTRL5 command sets buck 2's soft-start delay by counting a set number of CLK pulses.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK2_POWER_ON_DELAY	8'b 0000 0100 (Or MODE-Determined)	Sets buck 2's soft-start delay via CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001: 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

BUCK2_CTRL6 (46h)

The BUCK2_CTRL6 command sets buck 2's soft-stop delay by counting a set number of CLK pulses.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	BUCK2_POWER_OFF_DELAY	8'b 0000 0100	Sets buck 2's soft-stop delay via CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001 = 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

BUCK2_CTRL7 (4Eh)

The BUCK2_CTRL7 command sets the default setting for BUCK2_CTRL7 (0Ah). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	VOUT2_PG_VTH_HIGH	2'b 00	Sets V_{OUT2}'s high-side voltage for the power good status (no external FB divider resistor). The hysteresis = 2.5%. 2'b 00: +7.5% from VOUT2_SETTING 2'b 01: +10% from VOUT2_SETTING 2'b 10: +12.5% from VOUT2_SETTING 2'b 11: Reserved
D[5]	R/W	VOUT2_PG_VTH_LOW	1'b 0	Sets V_{OUT2}'s low-side voltage threshold for the power good status. The hysteresis = 2.5%. 0: -7.5% from VOUT2_SETTING 1: -10% from VOUT2_SETTING
D[4]	RW	RESERVED	1'b 0	Reserved.
D[3:2]	R/W	VOUT2_UV_VTH	2'b 00	Sets V_{OUT2}'s under-voltage (UV) status threshold. The hysteresis = 2.5%. 2'b 00: -10% from VOUT2_SETTING 2'b 01: -12.5% from VOUT2_SETTING 2'b 10: Reserved 2'b 11: Reserved
D[1:0]	R/W	VOUT2_OV_VTH	2'b 10	Sets V_{OUT2}'s over-voltage (OV) status threshold. The hysteresis = 2.5%. 2'b 00: +8% from VOUT2_SETTING 2'b 01: +10.5% from VOUT2_SETTING 2'b 10:+13% from VOUT2_SETTING 2'b 11: Reserved

LDO_CTRL1 (4Fh)

The LDO_CTRL1 command sets the default setting for LDO_CTRL1 (0Bh). The only bits that have direct control of converter operation are LDO_SOFT_START.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RESERVED	1'b 0	Reserved
D[6:4]	R/W	LDO_SOFT_START	3'b 001 (Or MODE-Determined)	Sets the LDO soft-start time after being enabled. The output is between 0% and 100% of V_{OUT}. 3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 6ms 3'b 100: 8ms 3'b 101: 10ms 3'b 110: 12ms 3'b 111: 14ms
D[3:2]	RV	RESERVED	2'b 00	Reserved.
D[1]	R/W	LDO_DISCHG	1'b 1	0: Disable LDO discharge 1: Enable LDO discharge
D[0]	R/W	LDO_PG_VTH	1'b 0	Sets the LDO output threshold voltage for the power good status. The hysteresis = 5%. 0: -10% from LDO_SETTING 1: -15% from LDO_SETTING

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

LDO_CTRL2 (50h)

The LDO_CTRL2 command sets the default setting for LDO_CTRL2 (0Ch). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	RESERVED	1'b 0	Reserved.
D[6:0]	R/W	LDO_SETTING	7'b 011 1100 (Or MODE-Determined)	Sets the LDO's output voltage. 30mV per LSB from 0.6V to 3.6V. All lower settings: Reserved 001 0100: 600mV 001 0101: 630mV … 111 1000: 3600 mV All higher settings: Reserved

LDO_CTRL3 (51h)

The LDO_CTRL3 command sets the LDO's soft-start delay by counting a set number of CLK pulses.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	LDO_POWER_ON_ DELAY	8'b 0000 0000 (Or MODE-Determined)	Sets the LDO's soft-start delay via CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001: 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

LDO_CTRL4 (52h)

The LDO_CTRL4 command sets the LDO's soft-stop delay by counting a set number of CLK pulses.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	LDO_POWER_OFF_DELAY	8'b 0000 0000	Sets the LDO's soft-stop delay via CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001: 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

SYS_CTRL1 (53h)

The SYS_CTRL1 command sets the default setting for SYS_CTRL1 (0Dh). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	CONVERTER_EN	1'b 1	0: Buck 1, buck 2, and the LDO are all disabled 1: Buck 1, buck 2, and the LDO are all enabled (must enable each regulator)
D[6]	R/W	VOUT1_EN	1'b 1	0: Disable buck 1 1: Enable buck 1
D[5]	R/W	VOUT2_EN	1'b 1	0: Disable buck 2 1: Enable buck 2
D[4]	R/W	LDO_EN	1'b 0	0: Disable LDO 1: Enable LDO
D[3:2]	R/W	RESERVED	2'b 00	Reserved.
D[1:0]	R/W	GPIO_CTRL	2'b 10	Sets GPIO's open-drain output control. 2'b 00: The GPIO output is low 2'b 01: GPIO is an analog input for the ADC 2'b 10: GPIO is part of flex-time control and used as the external converter's enable signal. GPIO outputs as an EN signal for the external converter and its on/off sequence can be configured via the 0x57 and 0x58 registers 2'b 11: The GPIO output is floating/high

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

SYS_CTRL2 (54h)

The SYS_CTRL2 command sets buck 1 and buck 2's operation mode.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	SINGLE/DUAL	1'b 1 (Or MODE-Determined)	Sets whether buck 1 and buck 2 operate in single-phase, dual-output mode or dual-phase, single-output output. 0: Single-phase, dual-output 1: Dual-phase, single-output
D[6:0]	R/W	RESERVED	0000000	Reserved

SYS_CTRL3 (55h)

The SYS_CTRL3 command sets the default settings for SYS_CTRL3 (0Eh). The only bit that has direct control of converter operation is PROTECT_MODE.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	VIN_PG_VTH	3'b 110	Sets the V_{IN} rising threshold for VIN_PG. VIN_PG (0x19) is 0 (power good) even if V_{IN} < V_{IN} PG falling threshold after V_{IN} start-up. Then ramp up V_{IN} to be ≥ V_{IN} rising threshold. If V_{IN} triggers the V_{IN} PG falling threshold again, VIN_PG changes to 1 (power not good). The hysteresis = 0.5V. 3'b 000: 9.5V (same as 001) 3'b 001: 9.5V 3'b 010: 8.5V 3'b 011: 7.5V 3'b 100: 6.5V 3'b 101: 5.5V 3'b 110: 4.25V 3'b 111: Reserved
D[4]	R/W	MASK_PG	1'b 0	Masks the PG pin's output. 0: No mask 1: Masked
D[3]	R/W	PG_DELAY_EN	1'b 0	0: No delay on PG 1: There is a 100μs delay on PG
D[2]	R/W	VIN_OVP_EN	1'b 1	0: Enable V_{IN} over-voltage protection (OVP) 1: Disable V_{IN} OVP
D[1]	R/W	RESERVED	1'b 0	Reserved.
D[0]	R/W	PROTECT_MODE	1'b 1	Sets the protection mode for the buck converters. 0: Latch-off mode 1: Hiccup mode

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

SYS_CTRL4 (56h)

The SYS_CTRL4 command has direct control of the converter operation.

Bits	Access	Bit Name	Default	Description
D[7:5]	R/W	OT_TH	3'b 100	Sets the converter's temperature shutdown threshold. The hysteresis = 20°C. 3'b 000: 125°C 3'b 001: 135°C 3'b 010: 145°C 3'b 011: 155°C 3'b 100: 165°C 3'b 101: Reserved 3'b 110: Reserved 3'b 111:Reserved
D[4:2]	R/W	OTW_TH	3'b 110	Sets the over-temperature (OT) warning threshold. The hysteresis = 20°C. 3'b 000: Reserved 3'b 001: 100°C 3'b 010: 110°C 3'b 011: 120°C 3'b 100: 130°C 3'b 101: 140°C 3'b 110: 150°C 3'b 111: Reserved
D[1:0]	R/W	VIN_UV_SEL	2'b 00	Sets the buck V_{IN} under-voltage lockout (UVLO) rising threshold. 2'b 00: The default value in the Electrical Characteristics section starting on page 6 2'b 01: 2.9V 2'b 10: 4V 2'b 11: 6V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

GPIO_CONFIG (57h)

The GPIO_CONFIG command controls converter operation (GPIO) directly.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	GPIO_POWER_ON_DELAY	8'b 0000 0100 (Or MODE-Determined)	If GPIO_CTL = 10, GPIO goes high when counting this number of CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001: 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

GPIO_CONFIG (58h)

The GPIO_CONFIG command controls converter operation (GPIO) directly.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	GPIO_POWER_OFF_DELAY	8'b 0000 0000 (Or MODE-Determined)	If GPIO_CTL = 10, GPIO goes low when counting this number of CLK pulses. 0000 0000: 0 0000 0001: 1 0000 0010: 2 0000 0011: 3 …… 0110 0100: 100 0110 0101: 102 0110 0110: 104 ……. 1001 0110: 200 1001 0111: 204 1001 1000: 208 …… 1100 1000: 400 1100 1001: 408 1100 1010: 416 …… 1110 0001: 600 1110 0010: 616 1110 0011: 632 …… 1111 1010: 1000 1111 1011: 1024 1111 1100~1111 1111: Reserved

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ADC_CTRL2 (59h)

The ADC_CTRL2 command enables the ADC and sets the sample frequency.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	ADC_EN	1’b 1	0: Disable the ADC 1: Enable the ADC
D[6:2]	R/W	RESERVED	5’b 00000	Reserved.
D[1:0]	R/W	ADC_SAMPLE_ FREQ	2’b 01	Sets the frequency to refresh all the ADC channels. 00: 4kHz 01: 2kHz 10: 1kHz 11: 0.5kHz

MASK1 (5Ah)

The MASK1 command sets the default setting for MASK1 (1Bh). This command does not have direct control of converter operation. The MASK1 command masks the INT pin’s behavior. The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	RW	VIN_PG_MSK	1’b 0	0: Do not mask 1: Mask
D[6]	RW	VOUT1_PG_MSK	1’b 0	0: Do not mask 1: Mask
D[5]	RW	VOUT2_PG_MSK	1’b 0	0: Do not mask 1: Mask
D[4]	RW	LDO_PG_MSK	1’b 0	0: Do not mask 1: Mask
D[3:2]	RW	RESERVED	2’b 00	Reserved.
D[1]	RW	OTW_MSK	1’b 0	0: Do not mask 1: Mask
D[0]	RW	OT_MSK	1’b 0	0: Do not mask 1: Mask

MASK2 (5Bh)

The MASK2 command sets the default setting for MASK2 (1Ch). This command does not have direct control of converter operation. The MASK2 command masks the INT pin’s behavior. The STATUS register still indicates each event.

Bits	Access	Bit Name	Default	Description
D[7]	RW	VIN_OV_MSK	1’b 0	0: Do not mask 1: Mask
D[6]	RW	VIN_UV_MSK	1’b 0	0: Do not mask 1: Mask
D[5]	RW	VOUT1_OV_MSK	1’b 0	0: Do not mask 1: Mask
D[4]	RW	VOUT2_OV_MSK	1’b 0	0: Do not mask 1: Mask
D[3]	RW	VOUT1_UV_MSK	1’b 0	0: Do not mask 1: Mask
D[2]	RW	VOUT2_UV_MSK	1’b 0	0: Do not mask 1: Mask

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

D[1]	RW	VOUT1_OC_MSK	1'b 0	0: Do not mask 1: Mask
D[0]	RW	VOUT2_OC_MSK	1'b 0	0: Do not mask 1: Mask

AVP_CTRL1 (5Ch)

The AVP_CTRL1 command sets the default setting for AVP_CTRL1 (1Fh). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP1_EN	1'b 0	Enables buck 1's AVP function. 0: Disabled 1: Enabled
D[6:5]	R/W	AVP1_GAIN	2'b 00	Sets the AVP gain. 00: 2.6mV/A 01: 5.7mV/A 10: 8.6mV/A 11:11.3mV/A
D[4:0]	R/W	AVP1_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV per step. x0000: 0mV 00001: 2mV … 01111: 30mV 10001: -2mV … 11111: -30mV

AVP_CTRL1 (5Dh)

The AVP_CTRL1 sets the default setting for AVP_CTRL2 (20h). This command does not have direct control of converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	AVP2_EN	1'b 0	Enables buck 2's AVP function. In dual-phase, single-output mode, this function is invalid. 0: Disabled 1: Enabled
D[6:5]	R/W	AVP2_GAIN	2'b 00	Sets the AVP gain. In dual-phase, single-output mode, this function is invalid. 00: 2.6mV/A 01: 5.7mV/A 10: 8.6mV/A 11: 11.3mV/A
D[4:0]	R/W	AVP2_OFFSET	5'b 0000 1	Sets the DC offset voltage for the output voltage command value when AVP is enabled. This offset ranges between -30mV and +30mV. 2mV per step. x0000: 0mV 00001: 2mV … 01111: 30mV 10001: -2mV … 11111: -30mV

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CLK_CTRL1 (5Eh)

The CLK_CTRL1 command has direct control over converter operation.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	CLK_MODE	1'b 1 (Or MODE-Determined)	Sets the master/slave configuration for the power sequence. 0: Slave converter 1: Master converter
D[6:4]	RW	CLK_FREQUENCY	3'b 100	Configures the CLK pin's clock frequency. 3'b 000: 100Hz 3'b 001: 200Hz 3'b 010: 500Hz 3'b 011: 1kHz 3'b 100: 2kHz 101: 5kHz 110: 10kHz 111: 20kHz
D[3:1]	RW	CLK_NUMBER	3'b 001	Configures the CLK pin's maximum clock output number. If the PG pin is pulled up, and the maximum POWER_ON_DELAY or maximum POWER_ON_DELAY CLK number of the enabled power rails is less than CLK_NUMBER, CLK outputs CLK_NUMBER clocks during turning EN on/off. If the on/off delay CLK number exceeds CLK_NUMBER, CLK continues outputting clocks until the on/off sequence is complete. If the PG pin is floating or below 2.3V, CLK does not stop outputting clocks until the EN turns off or V_{IN} < UVLO. Enable or disable the power channel via the I²C; CLK stays high. 3'b 000: 8 3'b 001: 16 3'b 010: 32 3'b 011: 64 3'b 100: 128 3'b 101: 256 3'b 110: 512 3'b 111: 1024
D[0]	R/W	RESERVED	1'b 0	Reserved.

CLK_CTRL2 (5Fh)

The CLK_CTRL2 command has direct control over converter operation.

Bits	Access	Bit Name	Default	Description
D[7:3]	R/W	RV	5'b 0000 0	Reserved.
D[2]	RW	CLK_PAUSE_EN	1'b 0	Enables the pausing feature of the CLK clock's output. 0: Disabled. The converter does not pull the CLK pin low during soft start/soft shutdown 1: Enabled. The converter pulls the CLK pin low during soft start/stop
D[1]	RW	CLK_ON_ERROR_ PAUSE_EN	1'b 0	Enables the pausing feature if an error occurs during soft start. 0: Disabled. The converter does not pull the CLK pin low if an error occurs during soft start 1: Enabled. The converter pulls the CLK pin low if an error occurs during soft start
D[0]	R/W	RESERVED	1'b 0	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

I2C_CONFIG (60h)

The I2C_CONFIG command enables MODE control and sets the I²C address.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	MODE_EN	1'b 1	Enables MODE control. 0: MODE is disabled. The MODE-determined MTP registers keep the original value as the default value 1: MODE is enabled. The MODE-determined MTP registers load the default value based on MODE selection
D[6:0]	R/W	I2C_ADDRESS	7'b 000 0000	Sets the I²C 7-bit address.

MTP_CTRL1 (61h)

The MTP_CTRL1 command has direct control over converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	WO	MTP_PASSWORD	-	Sets the password for MTP configuration.

MTP_CTRL1 (62h)

The MTP_CTRL1 command controls MTP configurations.

Bits	Access	Bit Name	Default	Description
D[7:2]	R/W	RESERVED	6'b 0000 00	Reserved
D[1]	R/W	MTP_RESTORE	1'b 0	Restores MTP control. Write 1 to this bit to restore all register values to the MTP registers' values.
D[0]	R/W	MTP_PROGRAM	1'b 0	Controls MTP configuration. Write 1 to this bit to start MTP configuration. Write 0xc8 to MTP_CTRL1 (61h) before configuration.

ID2 (64h)

The ID2 command has direct control over converter operation.

Bits	Access	Bit Name	Default	Description
D[7:0]	R/W	MTP_CODE	8'b 0000 0000	Sets the MTP suffix code. MPS defines this register.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MODE REGION REGISTERS (12)

When MODE_EN = 1, some of the MTP region registers load their default values from the MODE region registers, depending on the MODE pin's resistance.

For the following register settings, their configurations are copied from the corresponding registers in 0x70~0xC7. There are 8 sets of configuration settings listed in MODE0–MODE7 for each of the following bits (see Table 6). The MODE resistor determines which mode is selected.

Table 6: Registers Selected According to MODE0~MODE7

Command Code (0X)	Command Name	Tape	D7	D6	D5	D4	D3	D2	D1	D0
41	BUCK1_CTRL1	R/W		VOUT1_SOFT_START						
42	BUCK1_CTRL2	R/W			BUCK1_FSW			VOUT1_SETTING_LOW		
43	BUCK1_CTRL3	R/W	VOUT1_SETTING_HIGH							
44	BUCK1_CTRL4	R/W			BUCK1_FB_HALF					
45	BUCK1_CTRL5	R/W	BUCK1_POWER_ON_DELAY							
48	BUCK2_CTRL1	R/W		VOUT2_SOFT_START						
49	BUCK2_CTRL2	R/W			BUCK2_FSW			VOUT2_SETTING_LOW		
4A	BUCK2_CTRL3	R/W	VOUT2_SETTING_HIGH							
4B	BUCK2_CTRL4	R/W			BUCK2_FB_HALF					
4C	BUCK2_CTRL5	R/W	BUCK2_POWER_ON_DELAY							
4F	LDO_CTRL1	R/W		LDO_SOFT_START						
50	LDO_CTRL2	R/W		LDO_SETTING						
51	LDO_CTRL3	R/W	LDO_POWER_ON_DELAY							
53	SYS_CTRL1	R/W				LDO_EN			GPIO_CTRL	
54	SYS_CTRL3	R/W	SINGLE/DUAL							
57	GPIO_CONFIG	R/W	GPIO_POWER_ON_DELAY							
5E	CLK_CTRL1	R/W	CLK_MODE							
60	I2C_CONFIG	R/W		I2C_ADDRESS						

Note:

12) When VIN starts up, the MODEx registers (see the MODE Region Register Description section on page 65) is loaded into the MTP set via the registers from Table 6. The blank values in Table 6 are not replaced by the MODEx registers.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MODE REGION REGISTER DESCRIPTION

Bit Name (13)	Description
MODEx_VOUT1_SETTING	Sets the default value for VOUT1_SETTING_HIGH (BUCK1_CTRL3 (43h), bits D[7:0]) and VOUT1_SETTING_LOW (BUCK1_CTRL2 (42h), bits D[2:0]).
MODEx_VOUT2_SETTING	Sets the default value for VOUT2_SETTING_HIGH (BUCK2_CTRL3 (4Ah), bits D[7:0]).
MODEx_BUCK1_FB_HALF	Sets the default value for BUCK1_FB_HALF (BUCK1_CTRL4 (44h), bit D[5]).
MODEx_BUCK2_FB_HALF	Sets the default value for BUCK2_FB_HALF (BUCK2_CTRL4 (4Bh), bit D[5]).
MODEx_BUCK1_FSW	Sets the default value for BUCK1_FSW (BUCK1_CTRL2 (42h), bits D[5:4]).
MODEx_BUCK2_FSW	Sets the default value for BUCK2_FSW (BUCK2_CTRL2 (49h), bits D[5:4]).
MODEx_CLK_MODE	Sets the default value for CLK_MODE (CLK_CTRL1 (5Eh), bit D[7]).
MODEx_SINGLE/DUAL	Sets the default value for SINGLE/DUAL (SYS_CTRL2 (54h), bit D[7]).
MODEx_BUCK1_POWER_ON_DELAY	Sets the default value for BUCK1_POWER_ON_DELAY (BUCK1_CTRL5 (45h), bits D[7:0]).
MODEx_BUCK2_POWER_ON_DELAY	Sets the default value for BUCK2_POWER_ON_DELAY (BUCK2_CTRL5 (4Ch), bits D[7:0]).
MODEx_VOUT1_SOFT_START_TIME	Sets the default value for VOUT1_SOFT_START (BUCK1_CTRL1 (41h), bits D[6:4]).
MODEx_VOUT2_SOFT_START_TIME	Sets the default value for VOUT2_SOFT_START (BUCK2_CTRL1 (48h), bits D[6:4]).
MODEx_LDO_EN	Sets the default value for LDO_EN (SYS_CTRL1 (53h), bit D[4]).
MODEx_LDO_SOFT_START_TIME	Sets the default value for LDO_SOFT_START (LDO_CTRL1 (4Fh), bits D[6:4]).
MODEx_I2C_ADDRESS	Sets the default value for the last three digits of I2C_ADDRESS (I2C_CONFIG (60h), bits D[2:0]).
MODEx_GPIO_CTRL	Sets the default value for GPIO_CTRL (SYS_CTRL1 (53h), bits D[1:0]).
MODEx_LDO_SETTING	Sets the default value for LDO_SETTING (LDO_CTRL2 (50h), bits D[6:0]).
MODEx_LDO_POWER_ON_DELAY	Sets the default value for LDO_POWER_ON_DELAY (LDO_CTRL3 (51h), bits D[7:0]).
MODEx_GPIO_POWER_ON_DELAY	Sets the default value for GPIO_POWER_ON_DELAY (GPIO_CONFIG (57h), bits D[7:0]).

Note:

13) MODEx represents MODE0–MODE7.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

When using an external resistor divider, set the VOUTx_SETTING to a proper value. The feedback resistance (R_{FB1}) cannot be too large or too small considering the tradeoff for stability and dynamics. There is no strict requirement for the feedback resistor.

Figure 16 shows the circuit connection for the external divider. To optimize the load transient response, a feed-forward capacitor (C_{FF}) can be placed in parallel with R_{FB1}.

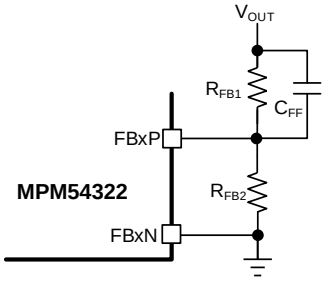


Figure 16: Feedback (FB) Network

R_{FB2} can be estimated with Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{V_{FB}} - 1} \quad (2)$$

V_{FB} is generated by the internal DAC, which can be adjusted from 0.4V to 2V. For example, if V_{FB} = 0.6V, choose the recommended resistor value. Table 7 shows the common output voltages for the resistor divider.

Table 7: Feedback Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)
1.0	20 (1%)	30 (1%)	NS
1.2	20 (1%)	20 (1%)	
1.8	20 (1%)	10 (1%)	
2.5	20 (1%)	6.34 (1%)	
3.3	20 (1%)	4.42 (1%)	
5	20 (1%)	2.7 (1%)	100

When using the internal resistor divider, remove R_{FB2} and use R_{FB1} = 0Ω. The maximum V_{OUT} can only be set to 3.8V.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for the best results due to their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The input capacitor's RMS current can be calculated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, estimated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Step-Down Regulator's Output Capacitor

The step-down regulator's output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low.

The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (6)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Where L_1 is the inductance and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the regulation stability.

PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation, especially for the high switching frequency converter. If the layout is not carefully considered, the regulator could show poor line or load regulation, as well as stability issues. It is recommended to use a 4-layer PCB for thermal improvement. For the best results, refer to Figure 17 and follow the guidelines below:

1. Place the input capacitor and output capacitor close to VIN1/2, VOUT1/2, and PGND.
2. Place the ceramic capacitor, especially the small package size (0402) bypass capacitor, as close to the VIN1/2 and PGND pins as possible to minimize high-frequency noise.
3. Place the VCC decoupling capacitor close to VCC and AGND.
4. Place the FB resistor divider as close as possible to the FB1P, FB1N, FB2P, and FB2N pins.
5. Avoid routing sensitive traces close to the input plane and SW node.
6. Connect the FB1P, FB1N, FB2P, and FB2Npins to VOUT1/2 and GND via a Kelvin connection.

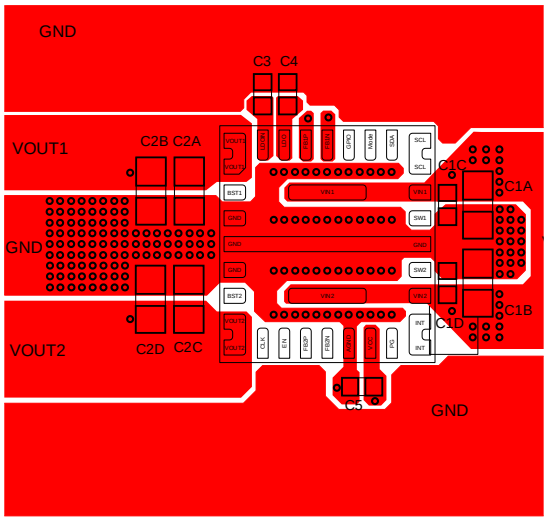


Figure 17: Recommended PCB Layout (Placement and Top Layer)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MTP CONFIGURATION

Table 6: 0000 Suffix Code Configuration

Items		Buck 1	Buck 2	LDO
MTP	Switching Mode	FCCM	FCCM	-
	V_{OUT} Slew Rate	0.5mV/µs	0.5mV/µs	-
	V_{OUT} Discharge	Enabled	Enabled	Enabled
	V_{OUT} Over-Voltage Protection (OVP)	Enabled	Enabled	-
	Valley Current Limit	4A	4A	-
	Power Off Delay	4 CLK cycles	4 CLK cycles	0 CLK cycles
	V_{OUT} PG Threshold High	7.5%	7.5%	
	V_{OUT} PG Threshold Low	-7.5%	-7.5%	-10%
	V_{OUT} OV Threshold	13%	13%	-
	V_{OUT} UV Threshold	-10%	-10%	-
	PG Delay	0µs		
	V_{IN} OVP	Disabled		
	Protection Mode	Hiccup		
	Over-Temperature Threshold	165°C		
	Over-Temperature Warning Threshold	150°C		
	ADC	Enabled		
	ADC Sample rate	2kHz		
	Active Voltage Positioning (AVP)	Disabled		
	AVP Gain	2.6mV/A		
	AVP Offset	2mV		
	CLK Frequency	2kHz		
	CLK Number	16		
	MODE Control	Enable MODE (determine MTP registers)		
	MTP Code	00		
Mode 0	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 400mV	FB voltage = 400mV	-
	CLK Mode	Master mode		
	Working Mode	Dual phase		-
	Switching Frequency	750kHz	750kHz	-
	Buck Start-Up Delay	4 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	2ms
	I²C Address	0		
	GPIO_CTRL	GPIO is a flex-time control and used as the external converter's enable signal		
	LDO Setting	-	-	1.8V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Mode 1	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 600mV	FB voltage = 600mV	-
	CLK Mode	Master mode		
	Working Mode	Dual phase		-
	Switching Frequency	1000kHz	1000kHz	-
	Buck Start-Up Delay	4 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	2ms
	I²C Address	1		
	GPIO_CTRL	GPIO is low		
	LDO Setting	-	-	1.8V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		
Mode 2	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 400mV	FB voltage = 400mV	-
	CLK Mode	Master mode		
	Working Mode	Single phase		-
	Switching Frequency	750kHz	750kHz	-
	Buck Start-Up Delay	4 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	1ms
	I²C Address	2		
	GPIO_CTRL	GPIO is low		
	LDO Setting	-	-	1.8V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		
Mode 3	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 600mV	FB voltage = 600mV	-
	CLK Mode	Master mode		
	Working Mode	Single phase		-
	Switching Frequency	1000kHz	1000kHz	-
	Buck Start-Up Delay	4 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	2ms
	I²C Address	3		
	GPIO_CTRL	GPIO is low		
	LDO Setting	-	-	3.6V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Mode 4	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 600mV	FB voltage = 600mV	-
	CLK Mode	Master mode		
	Working Mode	Single phase		-
	Switching Frequency	750kHz	1000kHz	-
	Buck Start-Up Delay	4 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	1ms
	I²C Address	4		
	GPIO_CTRL	GPIO is low		
	LDO Setting	-	-	1.8V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		
Mode 5	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 600mV	FB voltage = 600mV	-
	CLK Mode	Master mode		
	Working Mode	Single phase		-
	Switching Frequency	1000kHz	750kHz	-
	Buck Start-Up Delay	4 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	1ms
	I²C Address	5		
	GPIO_CTRL	GPIO is low		
	LDO Setting	-	-	1.8V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		
Mode 6	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 400mV	FB voltage = 400mV	-
	CLK Mode	Master mode		
	Working Mode	Single phase		-
	Switching Frequency	750kHz	750kHz	-
	Buck Start-Up Delay	0 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	1ms
	I²C Address	6		
	GPIO_CTRL	GPIO is low		
	LDO Setting	-	-	1.8V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Mode 7	LDO Enable	-	-	Disabled
	Voltage Setting	FB voltage = 400mV	FB voltage = 400mV	-
	CLK Mode	Master mode		
	Working Mode	Single phase		-
	Switching Frequency	1000kHz	1000kHz	-
	Buck Start-Up Delay	4 CLK cycles	4 CLK cycles	-
	V_{OUT} Soft-Start Time	2ms	2ms	-
	LDO Soft-Start Time	-	-	1ms
	I²C Address	7		
	GPIO_CTRL	GPIO is low		
	LDO Setting	-	-	1.8V
	LDO Start-Up Delay	-	-	0 CLK cycles
	GPIO Start-Up Delay	4 CLK cycles		

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Table 7: 0000 Suffix Code Register Value

Register	Hex Value	Register	Hex Value	Register	Hex Value
0x41	10h	0x79	0h	0xA1	4h
0x42	D0h	0x7A	4h	0xA2	24h
0x43	32h	0x7B	4Bh	0xA3	10h
0x44	C0h	0x7C	4Bh	0xA4	3Ch
0x45	4h	0x7D	0h	0xA5	0h
0x46	4h	0x7E	CAh	0xA6	4h
0x47	2h	0x7F	4h	0xA7	4Bh
0x48	10h	0x80	4h	0xA8	4Bh
0x49	D0h	0x81	24h	0xA9	0h
0x4A	32h	0x82	24h	0xAA	89h
0x4B	C0h	0x83	3Ch	0xAB	4h
0x4C	4h	0x84	0h	0xAC	4h
0x4D	4h	0x85	4h	0xAD	24h
0x4E	2h	0x86	32h	0xAE	14h
0x4F	12h	0x87	32h	0xAF	3Ch
0x50	3Ch	0x88	0h	0xB0	0h
0x51	0h	0x89	85h	0xB1	4h
0x52	0h	0x8A	4h	0xB2	32h
0x53	E2h	0x8B	4h	0xB3	32h
0x54	80h	0x8C	24h	0xB4	0h
0x55	C5h	0x8D	8h	0xB5	85h
0x56	98h	0x8E	3Ch	0xB6	0h
0x57	4h	0x8F	0h	0xB7	4h
0x58	0h	0x90	4h	0xB8	24h
0x59	81h	0x91	4Bh	0xB9	18h
0x5C	1h	0x92	4Bh	0xBA	3Ch
0x5D	1h	0x93	0h	0xBB	0h
0x5E	C2h	0x94	8Ah	0xBC	4h
0x5F	0h	0x95	4h	0xBD	32h
0x60	80h	0x96	4h	0xBE	32h
0x64	0h	0x97	24h	0xBF	0h
0x70	32h	0x98	2Ch	0xC0	8Ah
0x71	32h	0x99	7Dh	0xC1	4h
0x72	0h	0x9A	0h	0xC2	4h
0x73	C5h	0x9B	4h	0xC3	24h
0x74	4h	0x9C	4Bh	0xC4	1Ch
0x75	4h	0x9D	4Bh	0xC5	3Ch
0x76	24h	0x9E	0h	0xC6	0h
0x77	22h	0x9F	86h	0xC7	4h
0x78	3Ch	0xA0	4h	-	-

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

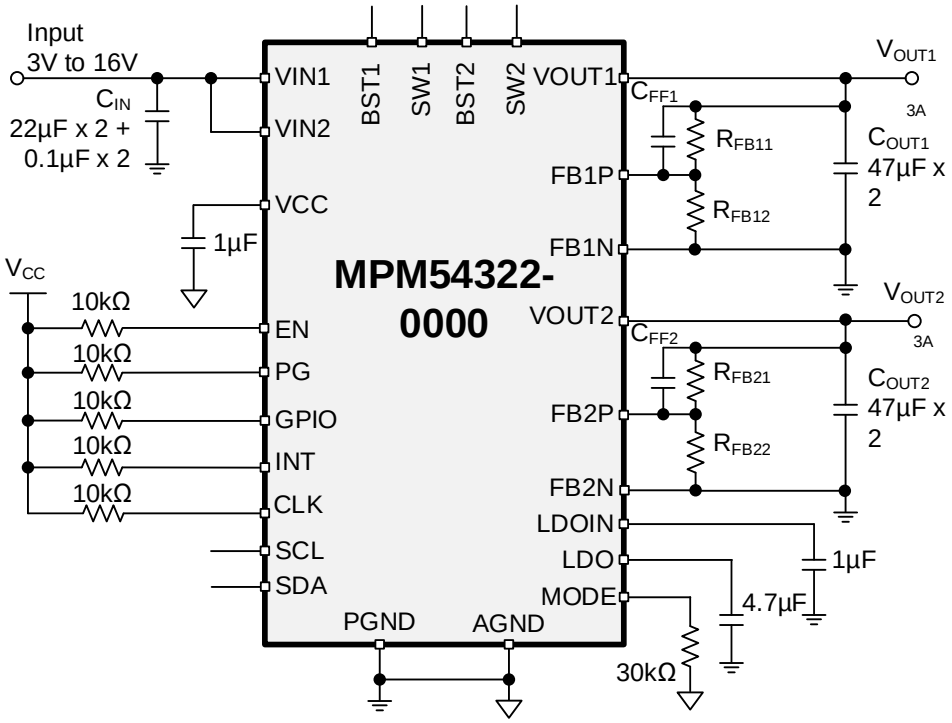


Figure 18: Typical Application Circuit (Dual-Output Operation with External Divider)

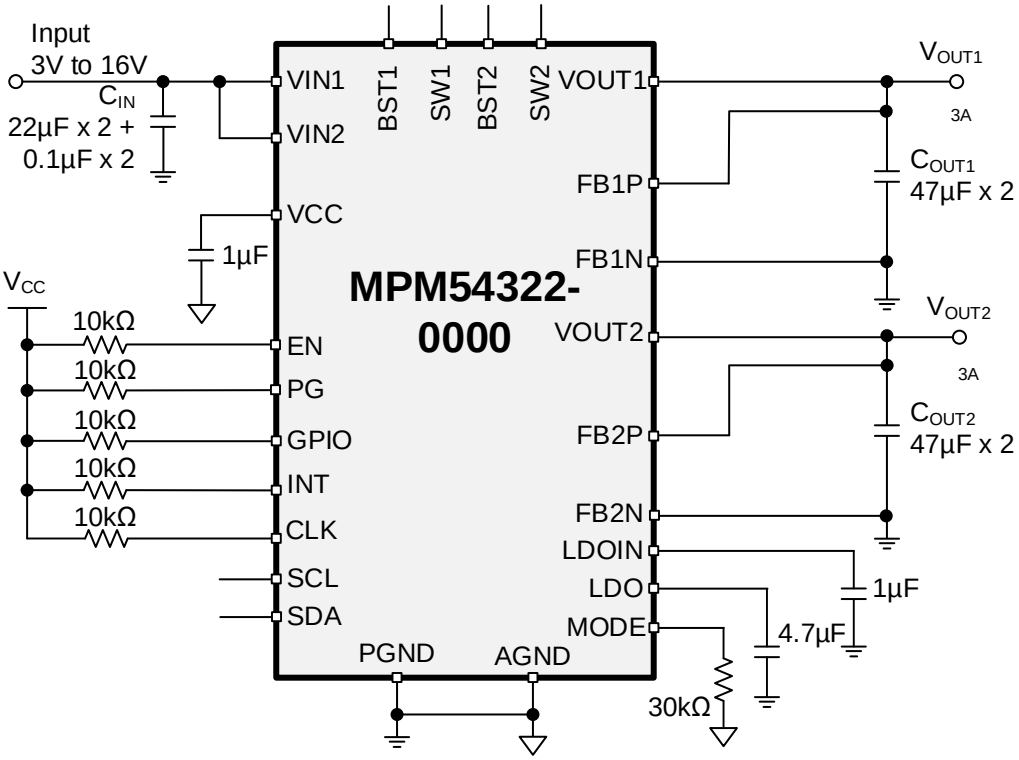


Figure 19: Typical Application Circuit (Dual-Output Operation with Internal Divider)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

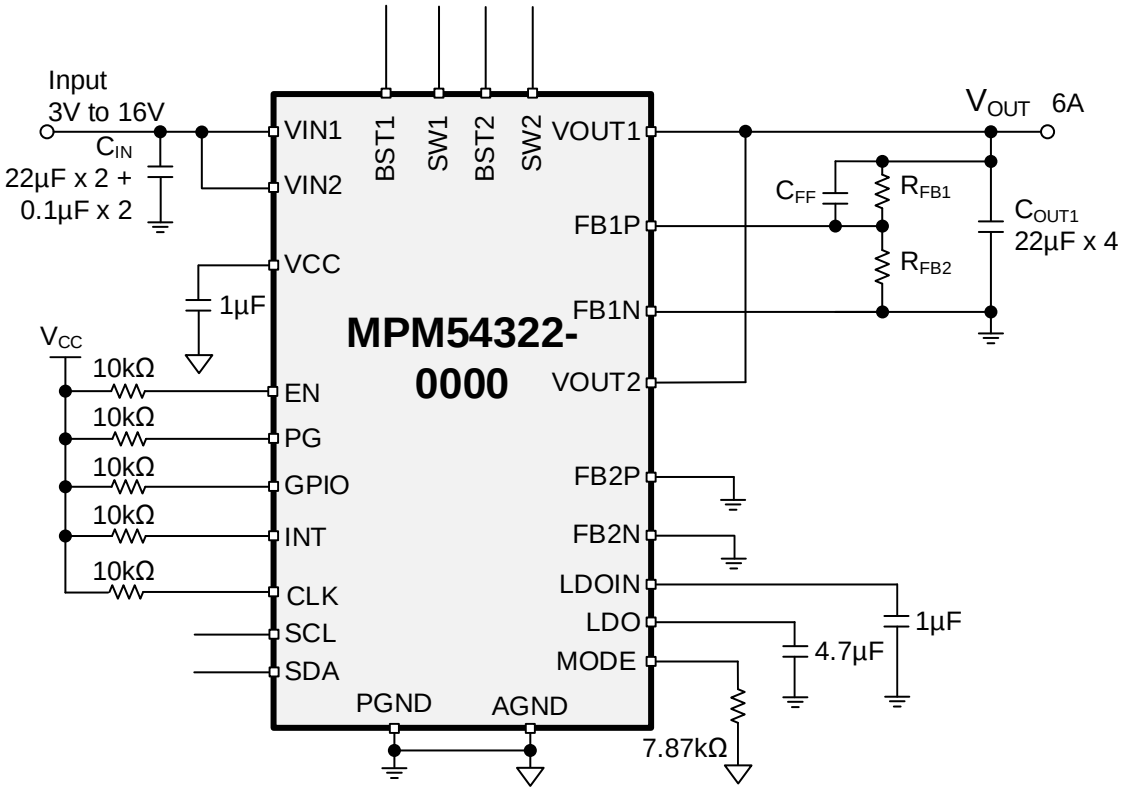


Figure 20: Typical Application Circuit (Dual-Phase Operation with External Divider)

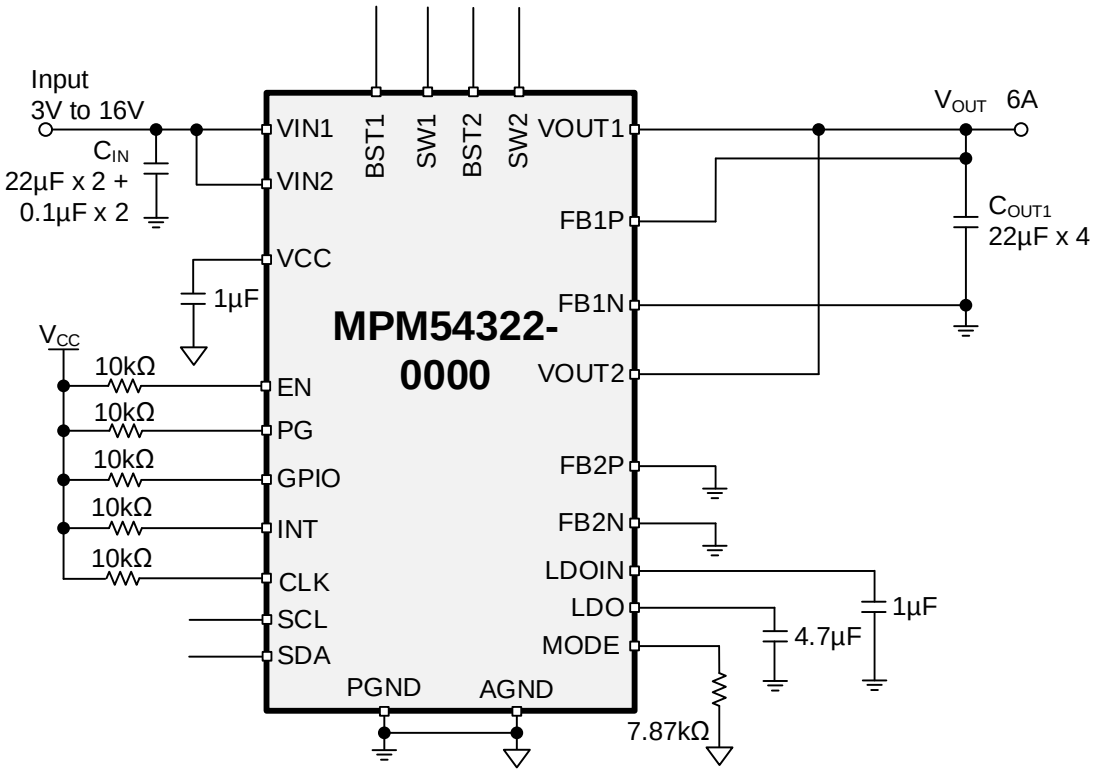
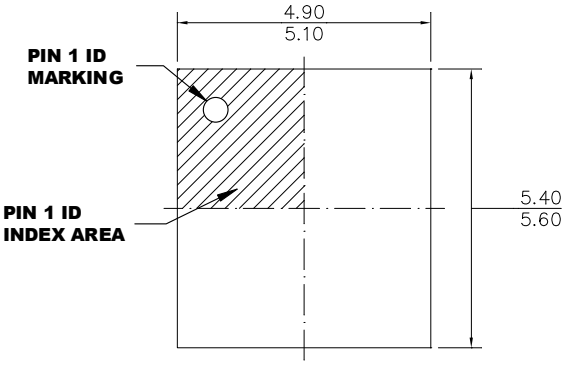


Figure 21: Typical Application Circuit (Dual-Phase Operation with Internal Divider)

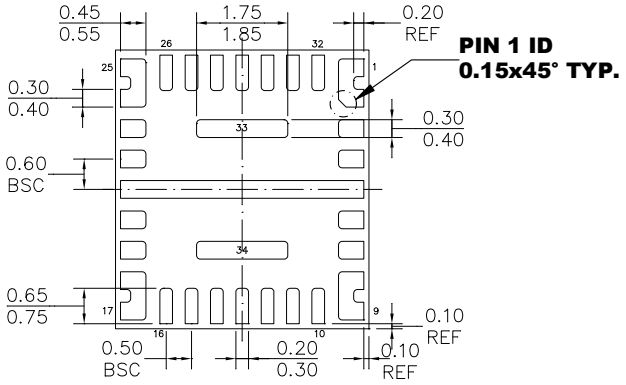
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE INFORMATION

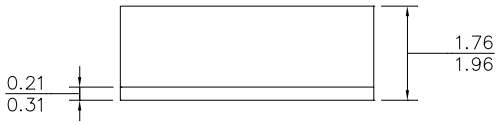
ECLGA (5mmx5.5mmx1.85mm)



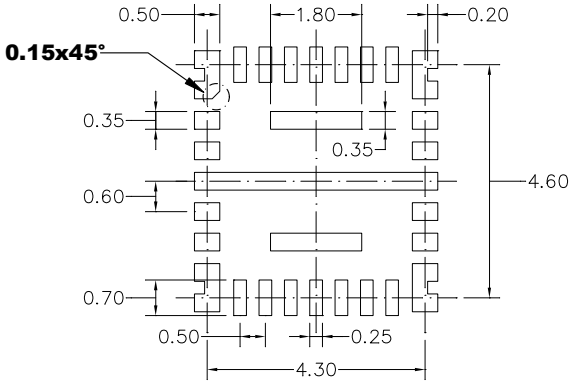
TOP VIEW



BOTTOM VIEW



SIDE VIEW



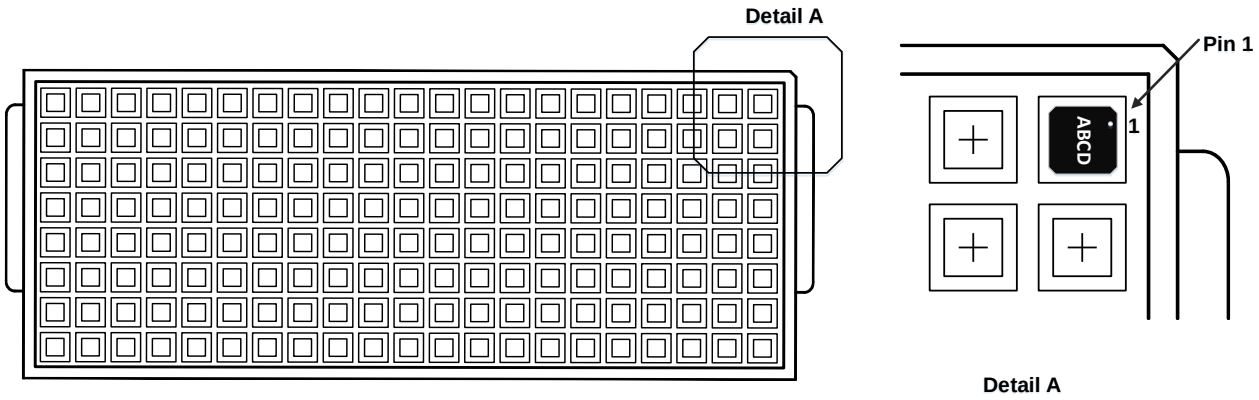
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

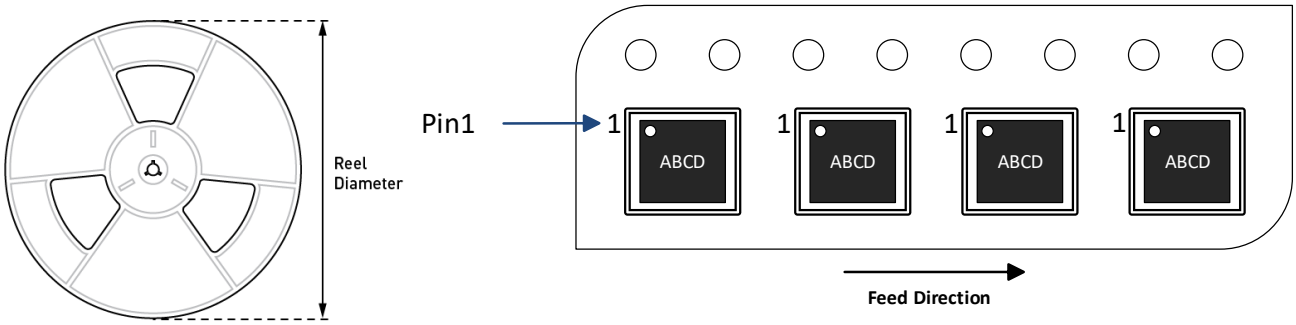
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CARRIER INFORMATION

Tray (14)



Reel (15)



Notes:

14) This is a schematic diagram of a tray. Different packages correspond to different trays with different lengths, widths, and heights.
15) This is a schematic diagram of a reel. Different packages correspond to different reels with different lengths, widths, and heights.

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM54322GPB-xxxx-T	ECLGA (5mmx5mmx1.85mm)	N/A	N/A	490	N/A	N/A	N/A
MPM54322GPB-xxxx-Z	ECLGA (5mmx5mmx1.85mm)	2500	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	7/3/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.