MPM3840

2.8V-5.5V, 4A, Power Module, Synchronous Step-Down Converter with Integrated Inductor

The Future of Analog IC Technology

DESCRIPTION

The MPM3840 is a DC/DC module that includes a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs and an inductor. The MPM3840 can provide 4A of continuous output current from a 2.8V to 5.5V input voltage with excellent load and line regulation. The MPM3840 is ideal for powering portable equipment that run on a single-cell Lithium-ion (Li+) battery. The output voltage can be regulated as low as 0.6V. Only input capacitors, output capacitors, and feedback (FB) resistors are required to complete the design.

The constant-on-time (COT) control scheme provides a fast transient response, high light-load efficiency, and easy loop stabilization.

Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPM3840 requires a minimal number of readily available, standard, external components and is available in an ultra-small QFN-20 (3mmx5mmx1.6mm) package.

FEATURES

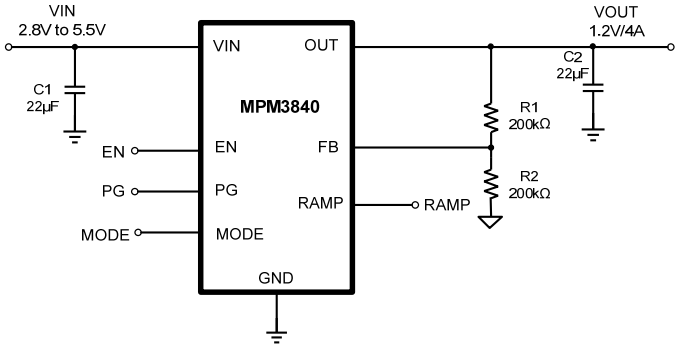
- >80% Light-Load Efficiency
- Low I_Q: 40μA
- Wide 2.8V to 5.5V Operating Input Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- 4A Output Current
- 25mΩ and 12mΩ Internal Power MOSFETs
- 1.2MHz Frequency
- External Mode Control
- External Mode Control (PWM.PFM) and Dynamic Analog Voltage
- EN and Power Good for Power Sequencing
- Cycle-by-Cycle Over-Current Protection (OCP)
- 1.5ms Internal Soft-Start Time with Pre-Biased Start-Up
- Short-Circuit Protection (SCP) with Hiccup Mode
- Thermal Shutdown
- Stable with Low ESR Output Ceramic Capacitors
- Available in a QFN-20 (3mmx5mmx1.6mm) Package

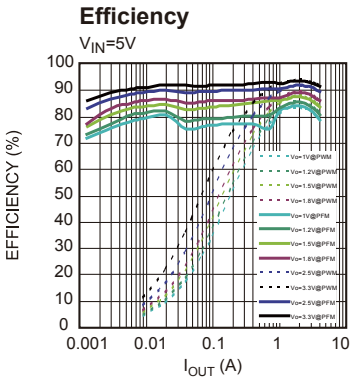
APPLICATIONS

- Networking/Servers
- Space-Constraint Applications
- Industrial Products
- Low-Voltage I/O System Power

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3840GQV	QFN-20 (3mmx5mmx1.6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPM3840GQV–Z)

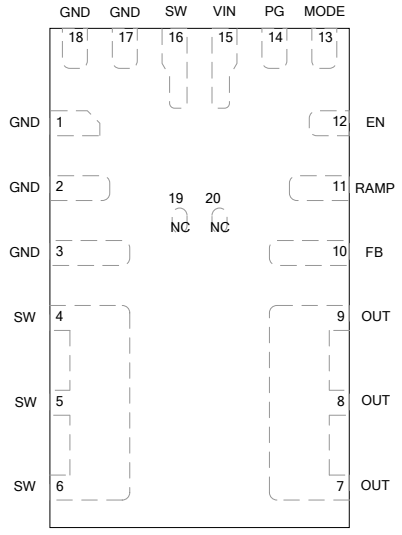
TOP MARKING

MPYW
3840
LLL
M

MP: MPS prefix
Y: Year code
W: Week code
3840: First four digits of the part number
LLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



QFN-20 (3mmx5mmx1.6mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 6V
V_{SW} ..... -0.3V (-5V for <10ns) to 6V (10V for <10ns)
All other pins ..... -0.3V to 6V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = +25°C) (2) 2.8W
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (VIN) ..... 2.8V to 5.5V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-20 (3mmx5mmx1.6mm)	46	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, V_{OUT} = 1.2V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	V_{FB}	2.8V ≤ V_{IN} ≤ 5.5V	0.594	0.600	0.606	V
Feedback current	I_{FB}	V_{FB} = 0.65V		50		nA
P-FET switch on resistance	R_{DSON_P}			25		mΩ
N-FET switch on resistance	R_{DSON_N}			12		mΩ
Dropout resistance	R_{DR}	100% on duty		47		mΩ
Switch leakage		T_J = 25°C		0	1	μA
P-FET peak current limit			4.5	5.5	6.5	A
N-FET valley current limit				4		A
On time		T_J = 25°C	216	270	324	ns
		T_J = -40°C to 85°C	202		338	
Switching frequency	f_s	V_{OUT} = 1.2V		1200		kHz
Minimum off time	$T_{MIN-OFF}$			60		ns
Minimum on time(5)	T_{MIN-On}			50		ns
Soft-start time	T_{SS-ON}			1.5		ms
PG UV threshold rising	PGTH_Hi			0.9		VFB
PG UV threshold falling	PGTH_Lo			0.85		VFB
PG OV threshold rising	PGTH_Hi			1.15		VFB
PG OV threshold falling	PGTH_Lo			1.1		VFB
Power good delay				140		μs
Power good sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
Power good logic-high voltage	V_{PG_HI}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
Power good internal pull-up resistor	R_{PG}			500		kΩ
Under-voltage lockout threshold rising			2.4	2.55	2.7	V
Under-voltage lockout threshold hysteresis				300		mV
EN input logic-low voltage					0.4	V
EN input logic-high voltage			1.2			V
EN input current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		μA
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0.1	1	μA
Supply current (quiescent)		V_{IN} = 3.6V, V_{EN} = 2V, V_{FB} = 0.65V, T_J = 25°C		40	60	μA
Thermal shutdown(5)				150		°C
Thermal hysteresis(5)				20		°C
Inductor L value				0.47		μH
Inductor DC resistance				22		mΩ

NOTE:
5) Guaranteed by design.

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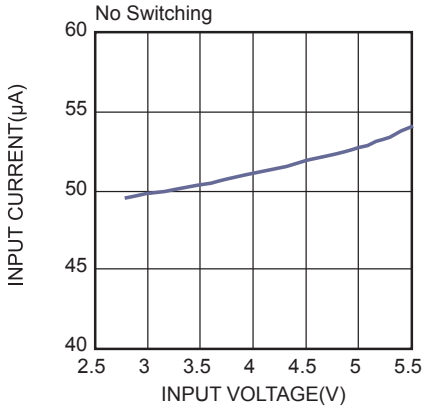
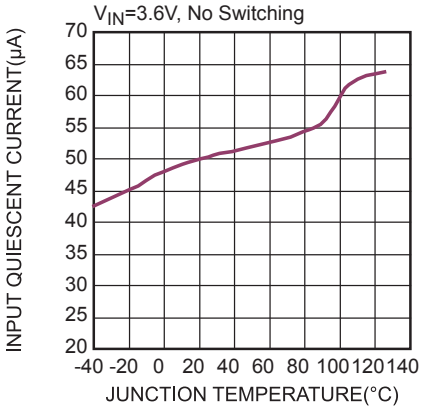
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF*2, T_A = +25°C, unless otherwise noted.

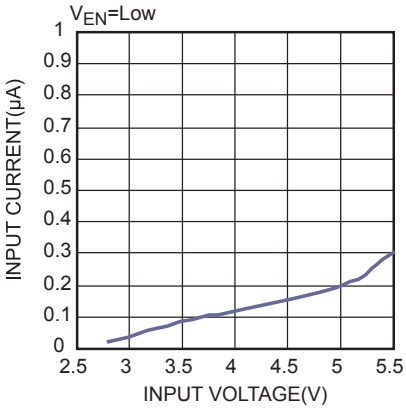
Quiescent Current vs. Input Voltage



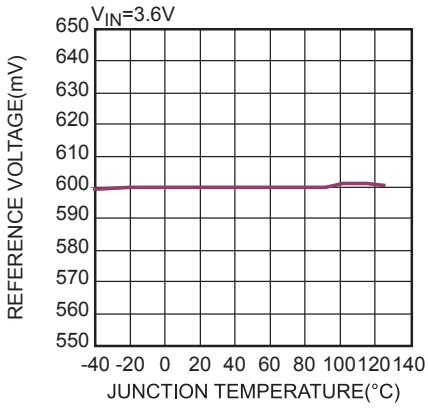
Quiescent Current vs. Temperature



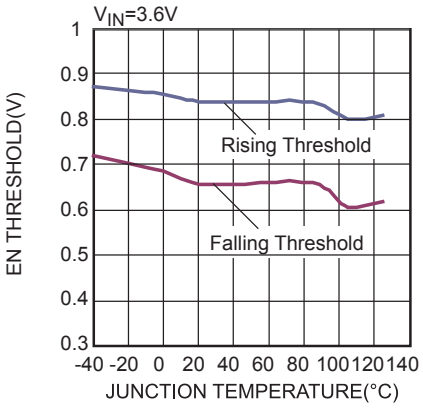
Shutdown Current vs. Input Voltage



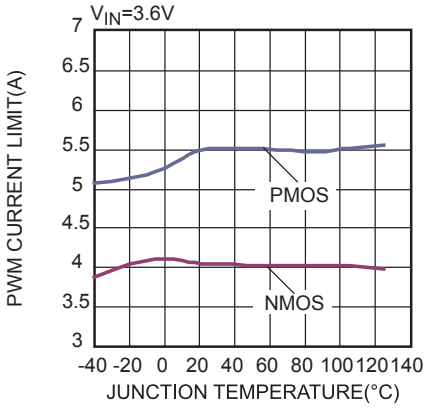
Reference Voltage vs. Temperature



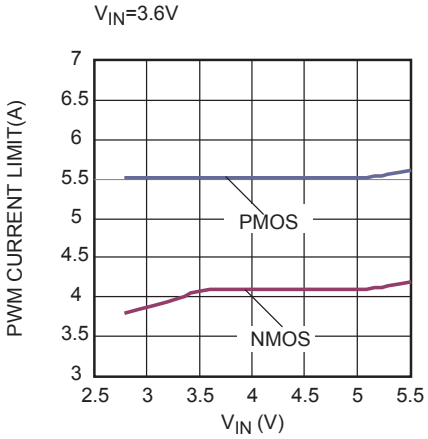
EN Threshold vs. Temperature



Current Limit vs. Temperature



Current Limit vs. VIN



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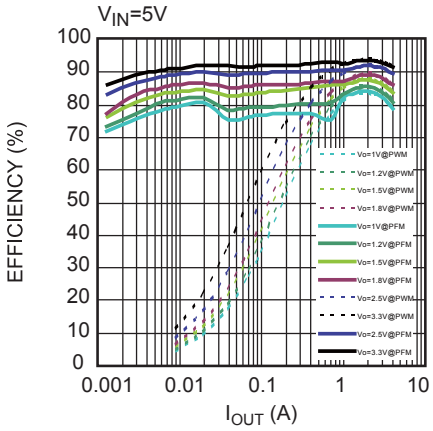
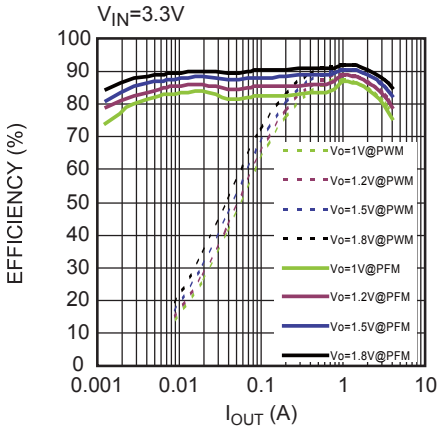
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF*2, T_A = +25°C, unless otherwise noted.

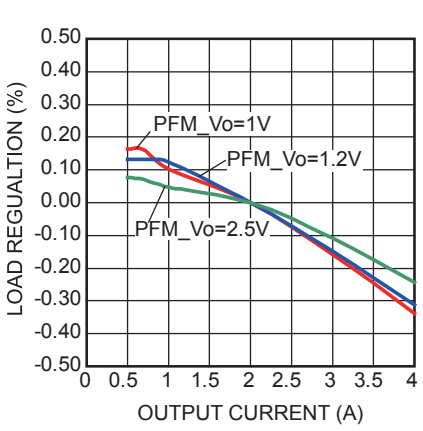
Efficiency



Efficiency



Load Regulation



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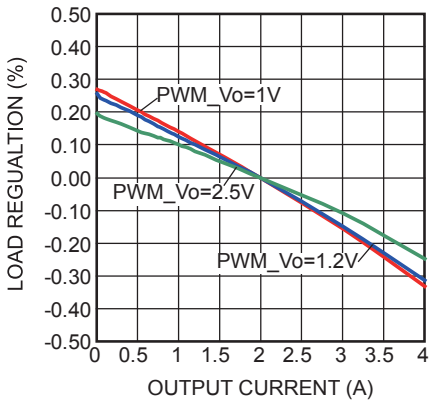

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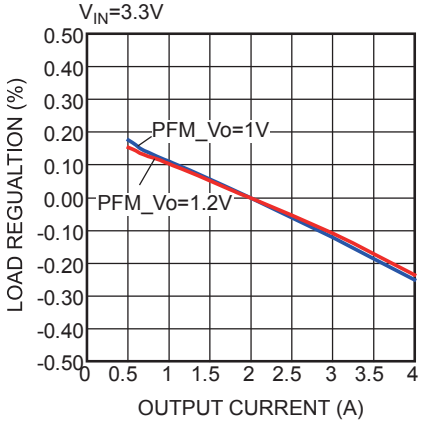
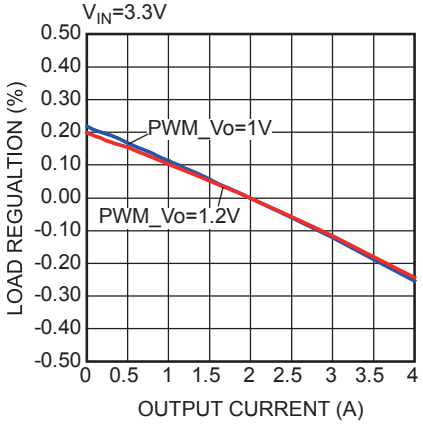
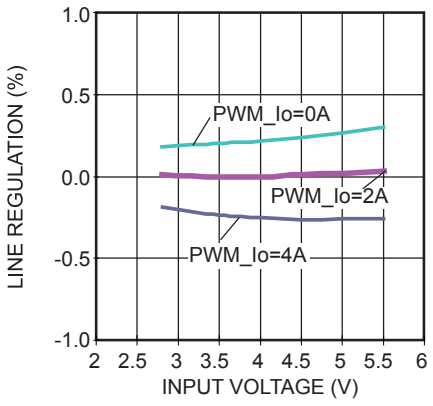


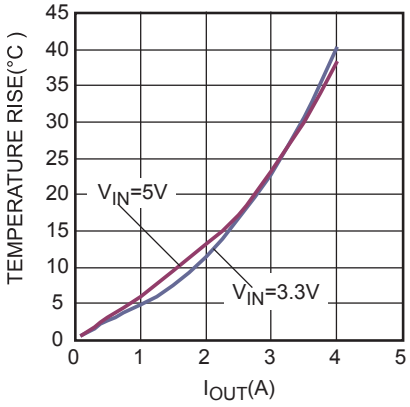
Load Regulation



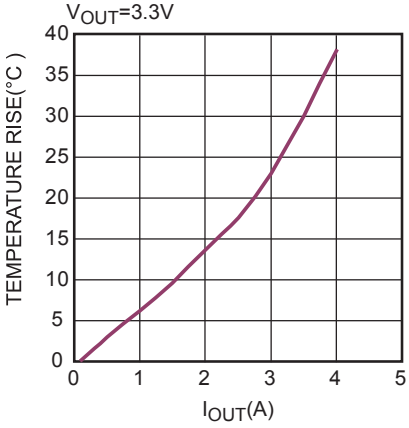
Line Regulation



Case Temperature Rise



Case Temperature Rise



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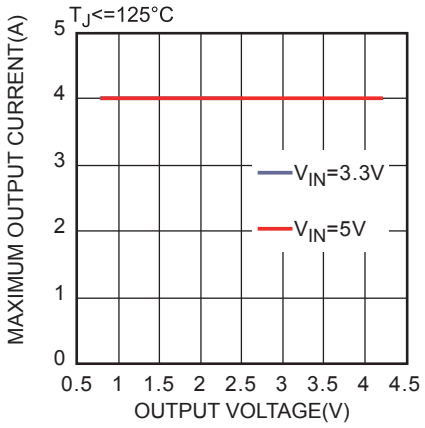
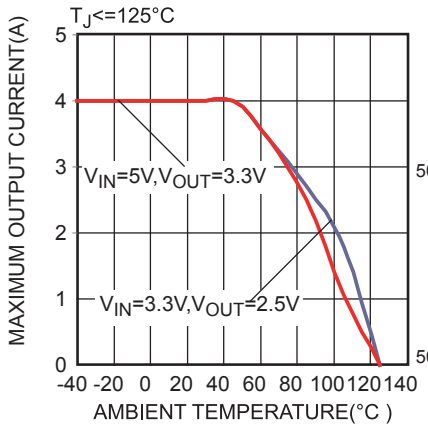
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF*2, T_A = +25°C, unless otherwise noted.

Output Current Derating vs. Output Voltage

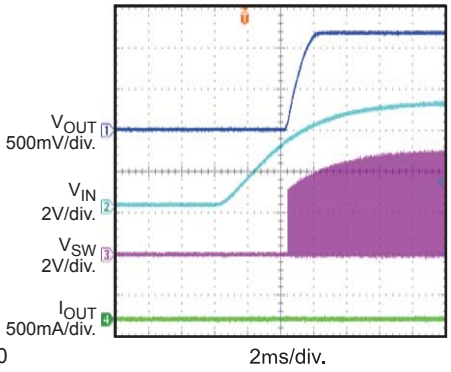


Output Current Derating vs. Ambient Temperature



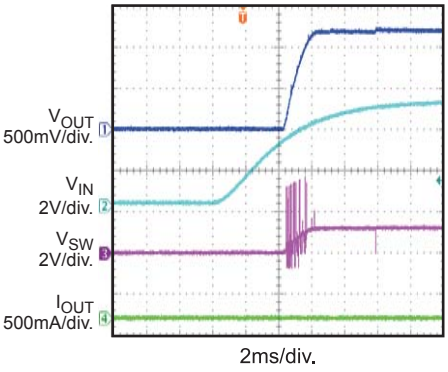
Power On

IOUT=0A, PWM Mode



Power On

IOUT=0A, PFM Mode



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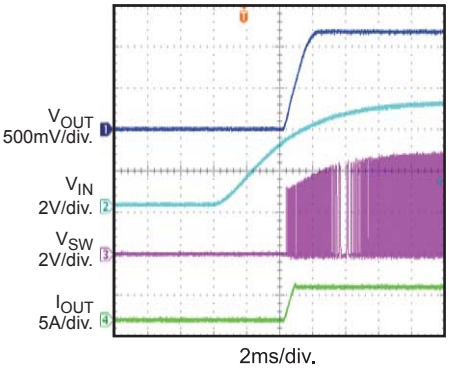

Power On

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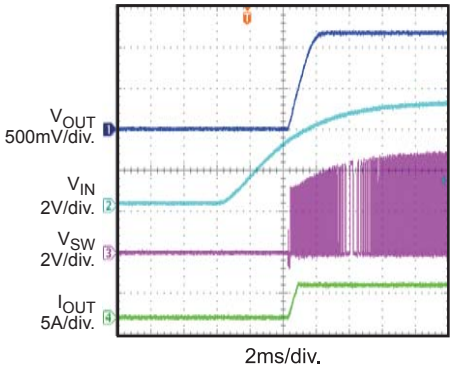
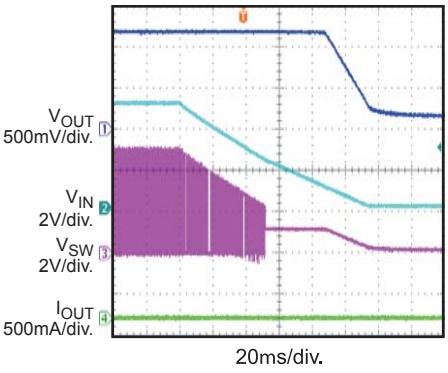


Power Off

IOUT=0A, PWM Mode



Power Off

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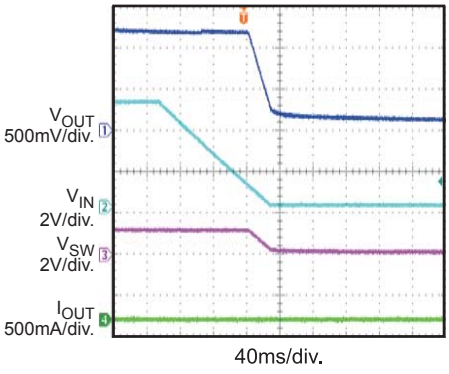
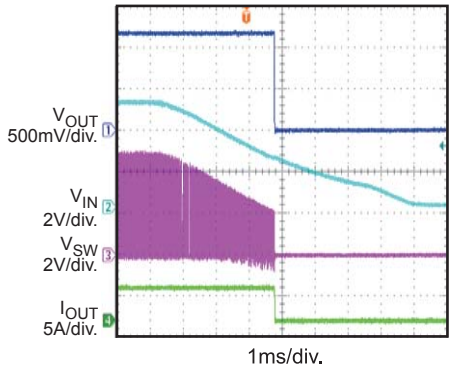


Power Off

IOUT=4A, PWM Mode



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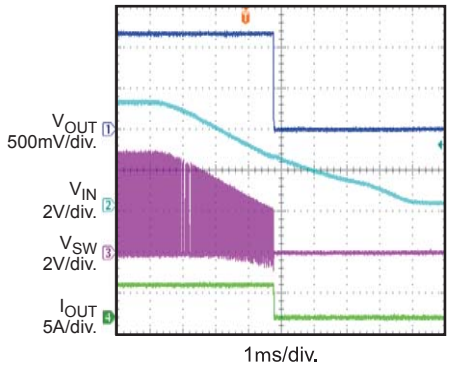
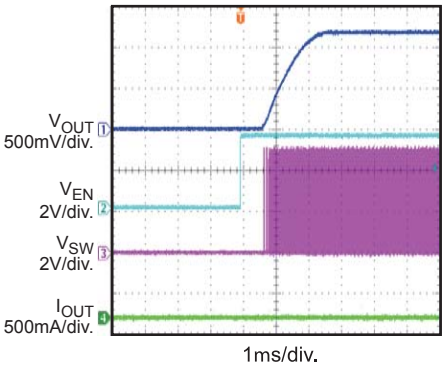
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF*2, T_A = +25°C, unless otherwise noted.

Power Off
I_{OUT}=4A, PFM Mode



Enable Turn-On
I_{OUT}=0A, PFM Mode



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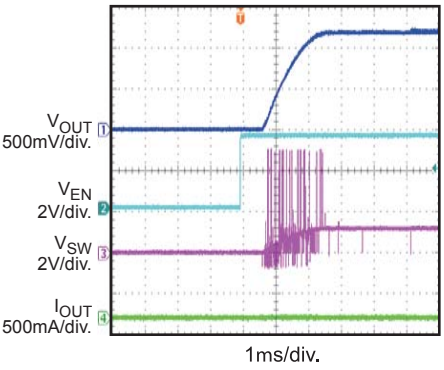

Enable Turn-On
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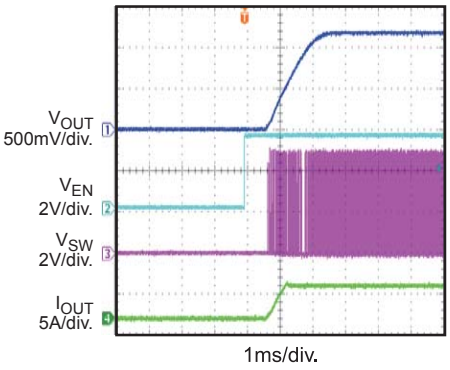

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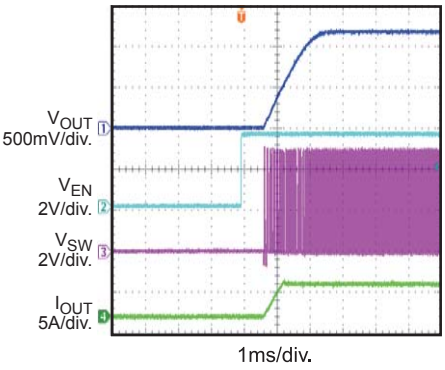

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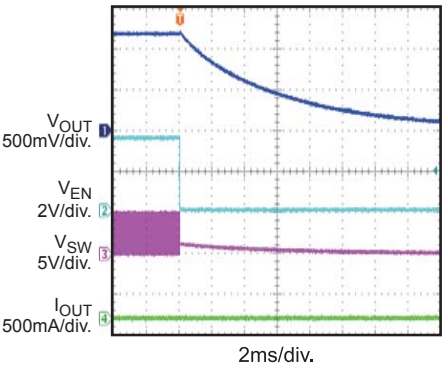
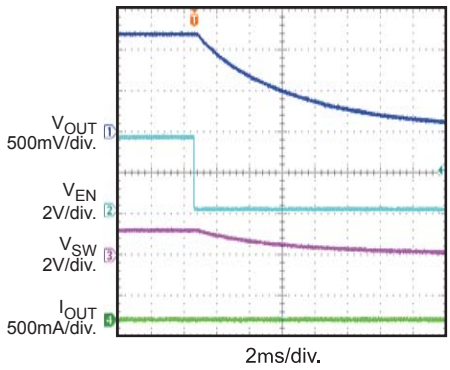


Enable Turn-Off
I_{OUT}=0A, PFM Mode



Enable Turn-Off
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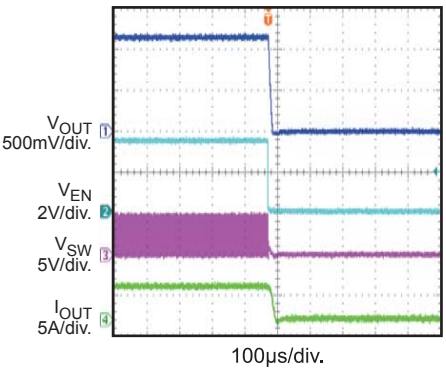
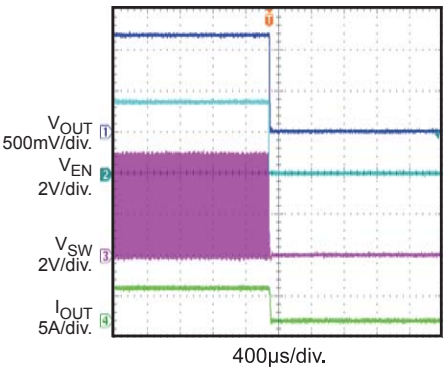


Enable Turn-Off
I_{OUT}=4A, PFM Mode



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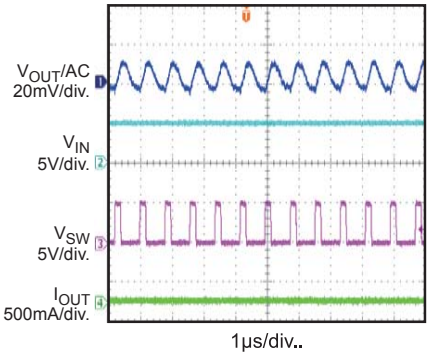
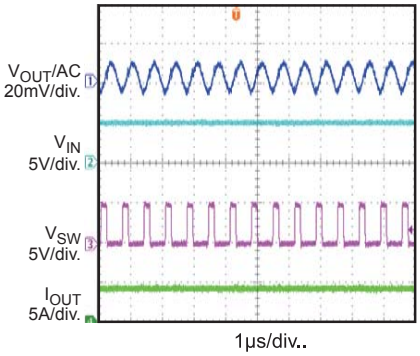
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF*2, T_A = +25°C, unless otherwise noted.

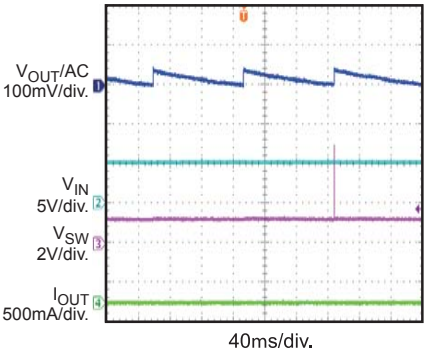
Steady State
I_{OUT}=0A, PWM Mode



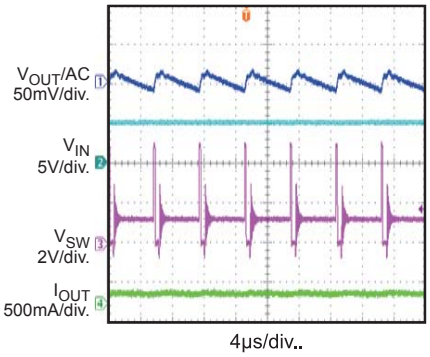
Steady State
I_{OUT}=4A, PWM/PFM Mode



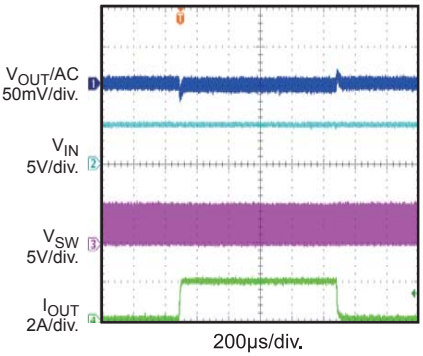
Steady State
I_{OUT}=0A, PFM Mode



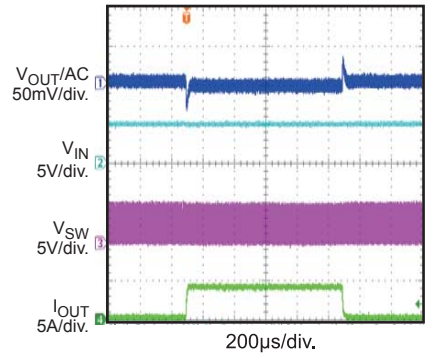
Steady State
I_{OUT}=0.1A, PFM Mode



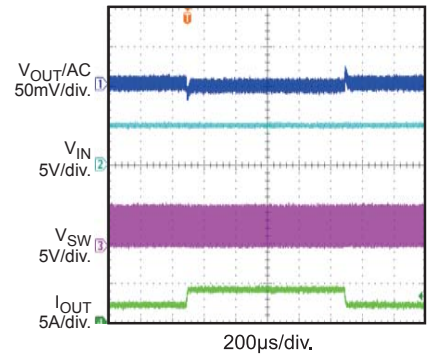
Response to Transient Load
I_{OUT}=0 to 2A, PWM Mode



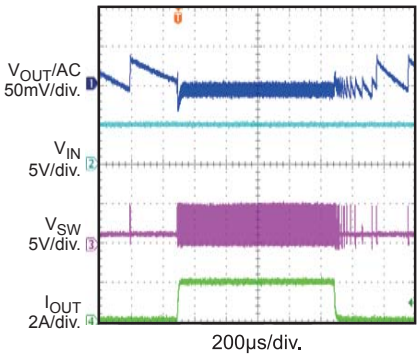
Response to Transient Load
I_{OUT}=0 to 4A, PWM Mode



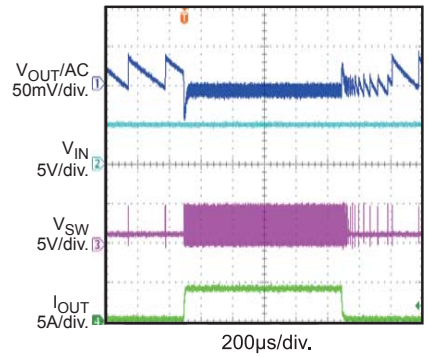
Response to Transient Load
I_{OUT}=2A to 4A, PWM/PFM Mode



Response to Transient Load
I_{OUT}=0 to 2A, PFM Mode



Response to Transient Load
I_{OUT}=0 to 4A, PFM Mode



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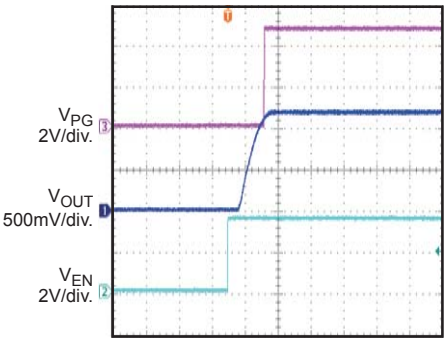
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

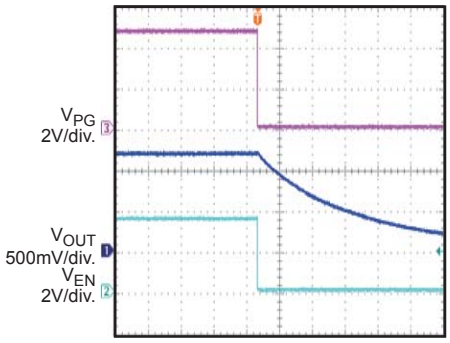
V_{IN} = 5V, V_{OUT} = 1.2V, C_{OUT} = 22µF*2, T_A = +25°C, unless otherwise noted.

Power Good
I_{OUT}=0A



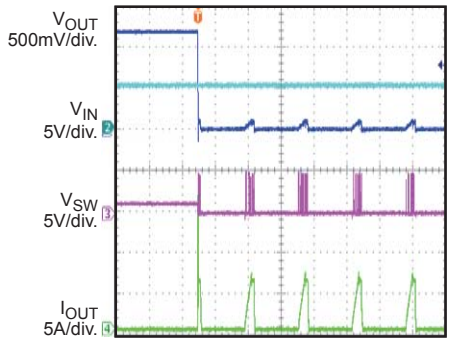
2ms/div..

Power Bad
I_{OUT}=0A



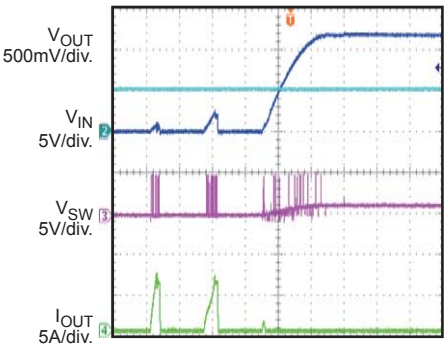
2ms/div..

Output Short Entry
I_{OUT}=0A, PFM Mode



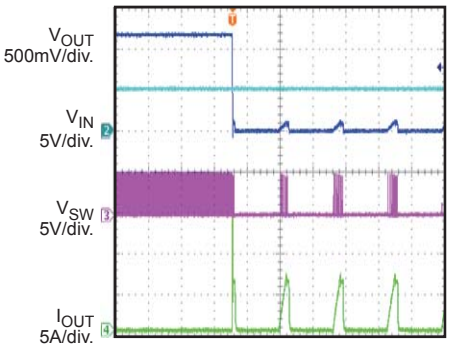
1ms/div.

Output Short Recovery
I_{OUT}=0A, PFM Mode



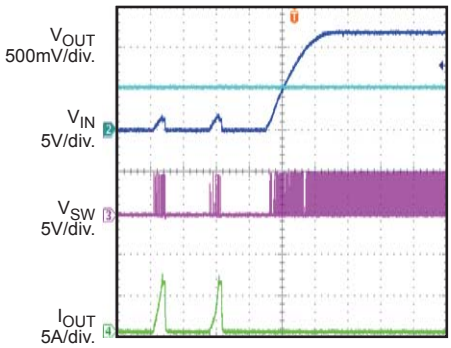
1ms/div..

Output Short Entry
I_{OUT}=0A, PWM Mode



1ms/div.

Output Short Recovery
I_{OUT}=0A, PWM Mode



1ms/div.

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 17, 18	GND	**IC ground.** Connect the GND pins to larger copper areas to the negative terminals of the input and output capacitors.
4, 5, 6, 16	SW	**Switch node.** Connect SW to the inductor. SW also connects to the internal high-side and low-side power MOSFET switches.
7, 8, 9	OUT	**Output voltage sense.**
10	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage.
11	RAMP	**External ramp.** RAMP sets the ramp to optimize transient performance. Connect a ceramic capacitor (10pF to 47pF) between OUT and RAMP to improve transient performance.
12	EN	**Enable.** Set EN to a high voltage level to enable the MPM3840. For automatic start-up, connect EN to VIN with a pull-up resistor.
13	MODE	**Multi-use pin.** MODE is also denoted as $V_{CON.}$ For PWM and PFM selection: When V_{MODE} is more than 1.2V, the MPM3840 enters PWM, and the internal reference is 0.6V. When V_{MODE} is lower than 0.4V or is floating, the MPM3840 enters PFM. For analog voltage dynamic regulation: When V_{MODE} is between 0.6V and 1.1V, the reference voltage can be controlled by V_{MODE}, and the MPM3840 works in PWM. Avoid setting V_{MODE} between 0.4V and 0.6V as the MPM3840 may operate in an unknown mode.
14	PG	**Power good.** PG has an internal, 500kΩ, pull-up resistor. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level; otherwise, PG is low. There is a 140μs delay between the moment when V_{FB} reaches the PG threshold and when PG goes high.
15	VIN	**Input supply.** VIN requires a decoupling capacitor to ground to reduce switching spikes.
19, 20	NC	**Do not connect.** NC must be left floating.

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BLOCK DIAGRAM

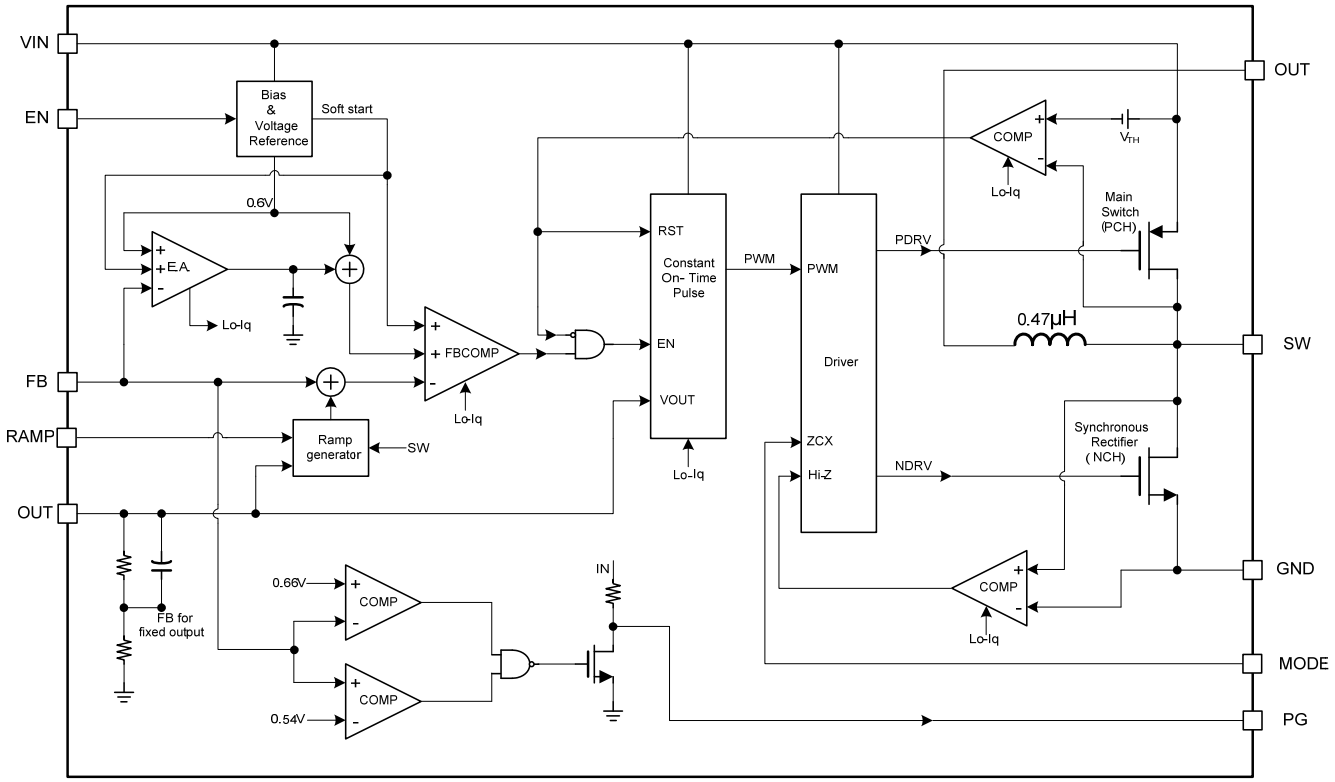

Figure 1: Functional Block Diagram

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OPERATION

The MPM3840 uses a constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over the full input range. At light load, the MPM3840 employs a proprietary control of low-side switching and inductor current on the switching node to improve efficiency. The module has an integrated inductor that makes the schematic and layout design very simple. Only input capacitors, output capacitors, and FB resistors are required to complete the design.

Constant-On-Time (COT) Control

Compared to fixed-frequency PWM control, constant-on-time (COT) control offers a simpler control loop and faster transient response. By using an input voltage feed-forward, the MPM3840 maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.83\mu s \quad (1)$$

To prevent inductor current runaway during the load transient, the MPM3840 has a constant minimum off-time of 60ns. This minimum off time limit will not affect operation in steady state in any way.

Light-Load Operation

During light loads, the MPM3840 uses a proprietary control scheme to save power and improve efficiency. A zero-current cross detection (ZCD) circuit is used to detect when the inductor current starts to reverse. The low-side MOSFET (LS-FET) turns off immediately when the inductor current starts to reverse and triggers ZCD in discontinuous conduction mode (DCM) operation. Considering the internal circuit propagation time, the typical delay is 50ns. This means that the inductor current continues falling after the ZCD is triggered in this delay time. If the inductor current falling slew rate is fast (V_{OUT} is high or close to VIN), the LS-FET is turned off, and the inductor current may be negative. This prevents the MPM3840 from entering DCM operation. For example, if VIN is 3.6V, and V_{OUT} is 3.3V, then the off time in CCM is 70ns. It is difficult to enter DCM at light load.

Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.55V), the MPM3840 can be enabled by pulling EN higher than 1.2V. Leave EN floating or pull EN down to ground to disable the MPM3840. There is an internal 1MΩ resistor from EN to ground.

MODE Selection and Analog Voltage Dynamic Regulation

The MPM3840 has programmable pulse-width modulation (PWM) and pulse-frequency modulation (PFM) work modes. When the voltage on MODE (V_{MODE}) is higher than 1.2V, the MPM3840 operates in PWM. When V_{MODE} is lower than 0.4V or is floating, the MPM3840 operates in PFM, which can achieve high efficiency in light-load condition. PWM mode can maintain a constant switching frequency and small V_{OUT} ripple, but has low efficiency at light load.

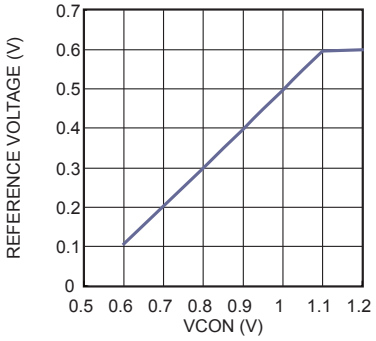

Figure 2: Reference Voltage Change with VCON

The MPM3840 can regulate the output voltage by dynamically changing the MODE voltage (V_{CON}) to meet a situation where the output voltage must be adjusted directly. When V_{CON} is an appropriate value (0.6V to 1.1V), the MPM3840 works in PWM, and the internal reference voltage changes smoothly as V_{CON} changes to provide a new output voltage without changing the external resistor divider. When the V_{CON} function is enabled, set the reference voltage (V_{ref}) to be from 0.35V to 0.6V. The accuracy is typically 3%. When setting the V_{ref} value from 0.1V to 0.35V, the accuracy is

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typically 10%. The detailed V_{Ref} curve is shown in Figure 2. Calculate V_{ref} with Equation (2):

$$Ref(V)=0.985\times VCON(V)-0.486 \quad (2)$$

Soft Start (SS)

The MPM3840 has a built-in soft start (SS) that ramps up the output voltage at a constant slew rate to avoid overshooting at start-up. The soft-start time is about 1.5ms, typically.

Pre-Bias Start-Up

The MPM3840 can start up with a pre-biased output voltage. If the internal SS voltage is lower than the FB voltage, the HS-FET and LS-FET remain off until the SS voltage crosses the FB voltage.

Power Good (PG) Indicator

The MPM3840 has an open drain with a 500kΩ pull-up resistor as a power good (PG) indicator.

PG is pulled up to VIN when the FB voltage is within 10% of the regulation level; otherwise, PG is low. There is a 140μs delay between the moment when V_{FB} reaches the PG threshold and when PG goes high. The MOSFET has a maximum $R_{DS(ON)}$ of 100Ω.

Current Limit

The MPM3840 has a 5.5A current limit for the HS-FET. When the HS-FET reaches its current limit, the MPM3840 enters hiccup mode until the current drops to prevent the inductor current from rising and damaging the components.

Short Circuit and Recovery

The MPM3840 enters short-circuit protection (SCP) mode when it reaches the current limit and attempts to recover with hiccup mode. The MPM3840 disables the output power stage, discharges the soft-start capacitor, and attempts to soft start. If the short-circuit condition remains after the soft start ends, the MPM3840 repeats this operation until the short circuit is removed and the output rises back to regulation levels.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application Circuit on page 17). Select the feedback resistor (R1) to reduce V_{OUT} leakage current, typically between 40kΩ to 200kΩ. There is no strict requirement on the feedback resistor. R1 > 10kΩ is reasonable for most applications. R2 can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown in Figure 3.

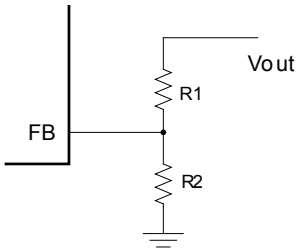

Figure 3: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. For higher output voltages, a 47µF capacitor may be needed to improve system stability.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality, 0.1µF, ceramic capacitor placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

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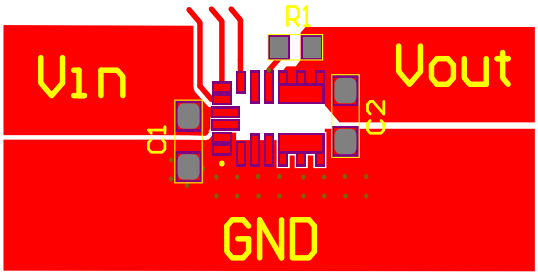
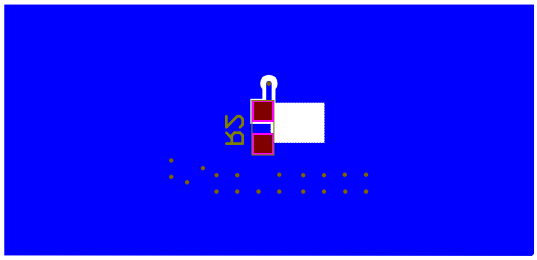
PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. Especially considering the high-switching converter, if the layout is not done carefully, the regulator could show poor performance. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the input capacitor as close to VIN and GND as possible.
2. Place the FB resistor very close to FB and GND. Ensure that the trace is not wide.
3. Place the output capacitor close to chip.
4. Make the VIN, VOUT, and GND traces wide enough to carry a high current.
5. Places several vias on the GND copper for better thermal performance.



Top Layer



Bottom Layer

Figure 3: Recommended PCB Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below.

Table 2: Design Example

V_{IN}	2.8V - 5.5V
V_{OUT}	1.2V
I_{OUT}	0A - 4A

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUIT

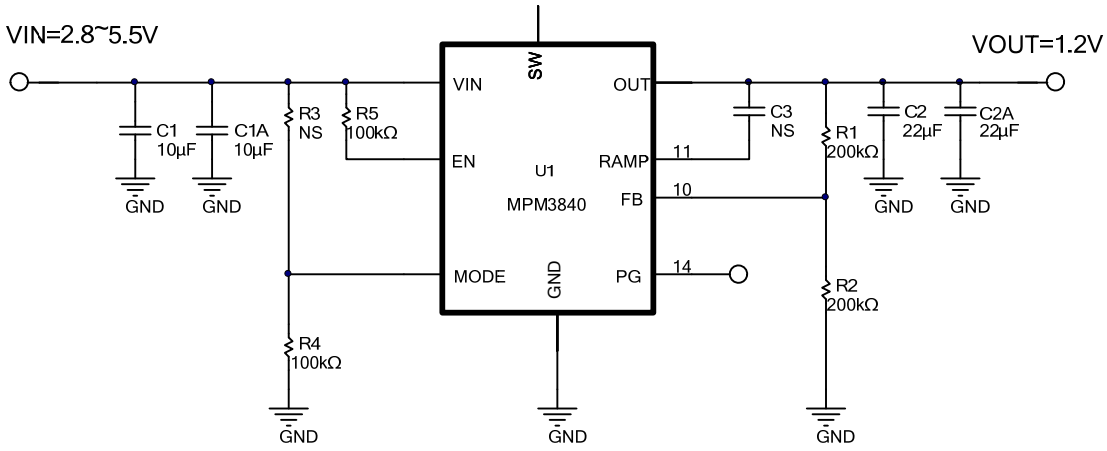

Figure 4: Application for 1.2V Output

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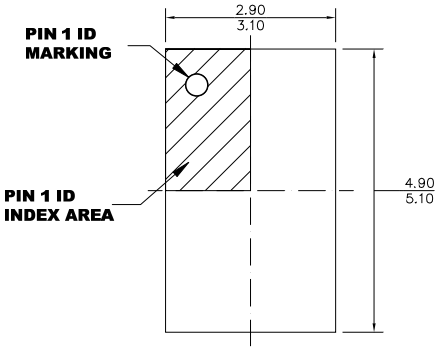
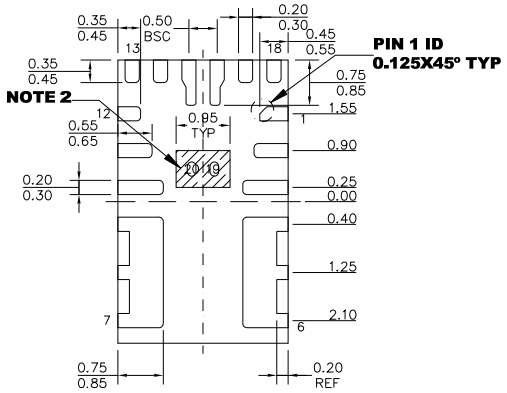
PACKAGE INFORMATION

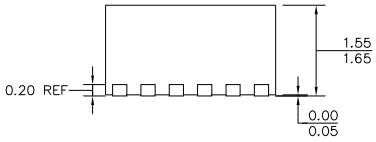
QFN-20 (3mmx5mmx1.6mm)



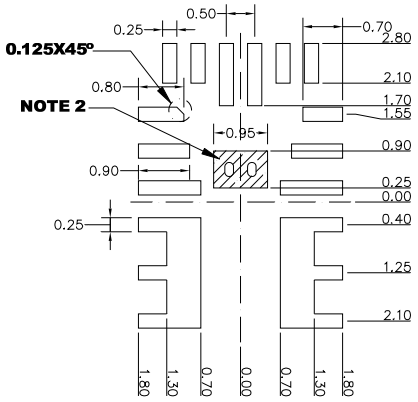
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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