MPM3695-10

16V, 10A, Scalable, Ultra-Thin DC/DC Power Module with PMBus

DESCRIPTION

The MPM3695-10 is a scalable, ultra-thin, fully integrated power module with a PMBus interface. It offers a complete power solution that achieves up to 10A of output current with excellent load and line regulation across a wide input voltage range. The device's 2mm height enables it to be placed on the backside of a PCB for space optimization. It operates at high efficiency over a wide load range, and can be paralleled to deliver higher current.

MPS's proprietary, multi-phase, constant-on-time (MCOT) control provides the MPM3695-10 with ultra-fast transient response and simple loop compensation. The PMBus interface monitors key parameters and offers module configurability.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPM3695-10 requires a minimal number of readily available external components, and is available in an LGA-45 (8mmx8mmx2mm) package.

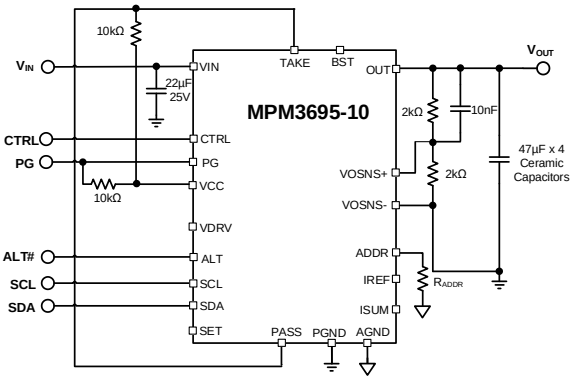
FEATURES

- Wide Input Voltage Range from 3.3V
  - 3.3V to 16V Input Voltage with an External VCC Bias
  - 4V to 16V Input Voltage with Internal VCC
- 0.5V to 5V Output Voltage Range
- Auto-Interleaving for Multi-Phase Operation
- Output Voltage Remote Sense
- PMBus 1.3 Compliant
- Telemetry Readback including V_{IN}, V_{OUT}, I_{OUT}, Temperature, and Faults
- Configurable via the PMBus interface:
  - Output Voltage, Soft-Start Time
  - OC, OT, OV, UV, and UVLO Limits
  - PWM Mode and Switching Frequency
- Available in an LGA-45 (8mmx8mmx2mm) Package

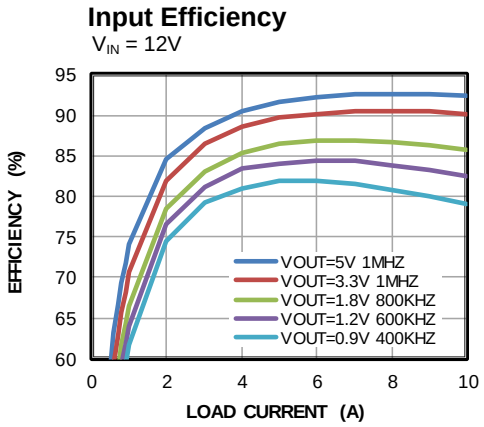
APPLICATIONS

- Telecom and Networking Systems
- Industrial Equipment
- Servers and Computing
- FPGA and ASIC Power

TYPICAL APPLICATION



Application circuit for single-phase operation at 1.2V output



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3695GMQ-10-xxxx	LGA-45 (8mmx8mmx2mm)	*See Below*	3
MPM3695GMQ-10-0022	LGA-45 (8mmx8mmx2mm)	*See Below*	
EVKT-MPM3695-10-A	N/A	NA	

* "xxxx" is the configuration code identifier for the register settings stored in the MTP memory. The default number is "0022." Work with an MPS FAE to create this unique number. See Table 6 and Table 7 on page 50 for the detailed configuration information and the register map of codes "0022."

TOP MARKING

MPSYYWW
MP3695
LLLLLLLLL
10M

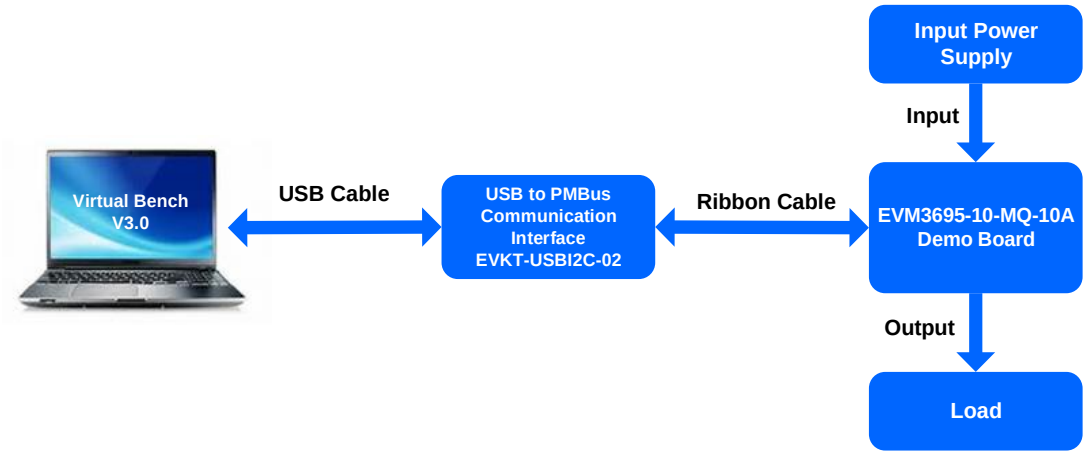
MPS: MPS prefix
YY: Year code
WW: Week code
MP3695: Part number
LLLLLLLLL: Lot number
10: Suffix of part number
M: Module

EVALUATION KIT EVKT-MPM3695-10-A

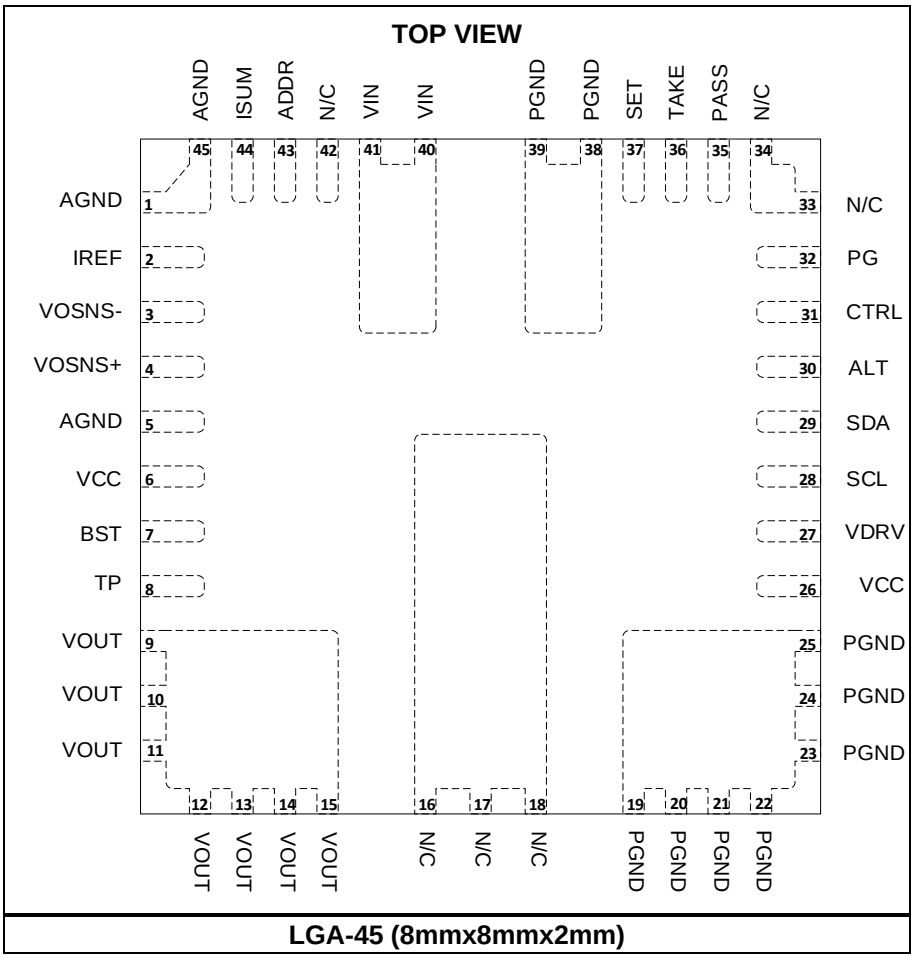
EVKT-MPM3695-10-A kit contents (items listed below can be ordered separately, and the GUI installation file and supplemental documents can be downloaded from the MPS website):

#	Part Number	Item	Quantity
1	EVM3695-10-MQ-10A	MPM3695-10 single-phase evaluation board	1
2	MPM3695GMQ-10-0022	1pcs MPM3695-10 module with default configurations	1
3	EVKT-USBI2C-02**	Includes one USB to PMBus communication interface device, one USB cable, and one ribbon cable	1

**** Order directly from MonolithicPower.com or our distributors**



PACKAGE REFERENCE



LGA-45 (8mmx8mmx2mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 5, 45	AGND	**Analog ground.** Use the AGND pins as the control circuit reference point. Connect ANGD to a ground plane using a single via.
2	IREF	**Current reference output.** Keep this pin floating.
3	VOSNS-	**Output voltage-sense negative return.** Connect directly to the GND sense point of the load. Short to GND if remote sense is not used.
4	VOSNS+	**Output voltage-sense positive return.** Connect this pin to the output voltage-sense positive side to provide the system with a feedback voltage. Do not place vias on the VOSNS traces.
6, 26	VCC	**Output of the internal 3.3V LDO.** The VCC voltage supplies power to the driver and control circuits. Pins 6 and 26 must be connected together.
7	BST	**Bootstrap.** Keep this pin floating.
8	TP	**Test pin.** Keep this pin floating.
9-15	VOUT	**Module output voltage node.** Connect with a wide PCB plane.
16-18	N/C	**Not connected.** Keep this pin floating.
19-25, 38, 39	PGND	**Power ground.** PGND is the reference point of the regulated output voltage. Connect with a wide PCB plane.
27	VDRV	**Decoupling pin for 3.3V driver power supply.** Keep this pin floating.
28	SCL	**PMBus serial clock.**
29	SDA	**PMBus serial data.**
30	ALT	**PMBus alert.** Open drain output, active low. A pull-up resistor must be connected to a 3.3V rail.
31	CTRL	**Converter control.** CTRL is a digital input that turns the regulator on or off. Drive CTRL high to turn the regulator on; drive it low to turn the regulator off. Do not float this pin.
32	PG	**Multi-purpose power good output.** Connect a pull-up resistor to the DC voltage to indicate a high status if the output voltage exceeds 90% of the nominal voltage. There is a delay for when PG goes from low to high.
33, 34, 42	N/C	**Not connected.** Keep these pins floating.
35	PASS	**Passes RUN signal to next phase.** See the Application Information section for connection.
36	TAKE	**Receives RUN signal from previous phase.** See the Application Information section for connection.
37	SET	**Set of PWM signal.** The SET signal turns on the high-side MOSFET (HS-FET) when a run signal is presented. For multi-phase operation, tie the SET pins of all the phases together.
40, 41	VIN	**Supply voltage.** This pin provides power to the module. Connect decoupling capacitors between VIN and GND.
43	ADDR	**PMBus slave address setting pin.** Connect a resistor between this pin to AGND to set the device address.
44	ISUM	**Reference current output.** For single-phase operation, keep this pin floating. For multi-phase operation, connect the ISUM pins of all the phases together.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{OUT} 5.5V
V_{BST} ..... V_{SW} + 4V
V_{CC} 4.5V
$V_{CC(1s)}$ (2) 6V
CTRL current (I_{CTRL}) 2.5mA
All other pins .....-0.3V to +4.3V
All other pins$_{(1s)}$ (2).....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (3) 8.5W
Junction temperature .....170°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +170°C

ESD Rating

Human body model (HBM) ..... ±1000V
Charged device model (CDM)..... ±2000V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4V to 16V
Supply voltage (V_{IN}) (5).....3.3V to 16V
Output voltage (V_{OUT}).....0.5V to 5V
External V_{CC} bias .....3.12V to 3.6V
CTRL current (I_{CTRL})..... 1mA
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

LGA-45 (8mmx8mmx2mm)	17.06	8.8... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Voltage rating during MTP programming.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
4) The device is not guaranteed to function outside of its operating conditions.
5) An external 3.3V VCC bias is required. Writing to the MTP memory is not supported with an external 3.3V VCC bias.
6) Measured on the EVM3695-10-MQ-10A evaluation board.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Supply Current						
Shutdown supply current	I_{IN}	V_{CTRL} = 0V		2.5	4	mA
Input Voltage						
Input voltage range	V_{IN}	Internal VCC	4		16	V
		With external 3.3V VCC	3.3		16	V
Output Voltage						
Output voltage range	V_{OUT_RANGE}		0.5		5	V
Load regulation (7)	$V_{OUT\_DC\_LOAD}$	I_{OUT} from 0A to 10A		±0.5		%V_{OUT}
Line regulation (7)	$V_{OUT\_DC\_LINE}$	V_{IN} from 4V to 16V, I_{OUT} = 5A		±0.5		%V_{OUT}
Current Limit						
Valley current limit	I_{LIM}	D7h = 0x07h		10.5		A
Min configurable valley current limit value (7)				3		A
Max configurable valley current limit value (7)				15		A
Low-side negative current limit in OVP	$I_{LIM\_NEG\_OVP}$			-13		A
CTRL						
CTRL ON threshold	$CTRL_{ON}$		2.2			V
CTRL OFF threshold	$CTRL_{OFF}$				1.2	V
Timing and Frequency						
Switching frequency	f_{SW}	D2h[2:1] = 2b'10		800		kHz
Minimum on time (7)	t_{ON_MIN}	f_{SW} = 1000kHz, V_O = 0.6V		50		ns
Minimum off time (7)	t_{OFF_MIN}	V_{FB} = 580mV		220		ns
Output Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}	D4h[1:0] = 2b'00	111	115	119	%V_{REF}
UVP threshold	V_{UVP}	D9h[3:2] = 2b'10	75	79	83	%V_{REF}
Max configurable OVP threshold	V_{OVP_MAX}	D4h[1:0] = 2b'11	126	130	134	%V_{REF}
Min configurable OVP threshold	V_{OVP_MIN}	D4h[1:0] = 2b'00	111	115	119	%V_{REF}
Max configurable UVP threshold	V_{UVP_MAX}	D9h[3:2] = 2b'11	80	84	88	%V_{REF}
Min configurable UVP threshold	V_{UVP_MIN}	D9h[3:2] = 2b'00	65	69	73	%V_{REF}
OSM threshold rising	V_{OSM_RISE}			104		%V_{REF}
OSM threshold falling	V_{OSM_FALL}			102		%V_{REF}
ADC (7)						
Voltage range			0		1.28	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
ADC resolution				10		bits
DNL				1		LSB
Sample rate				3		kHz
DAC (Feedback Voltage)						
Range			500	600	672	mV
Feedback accuracy	V_{FB}	21h = 0x258C, 29h = 0x1F4, D1h[1:0] = 2b'00	594	600	606	mV
Resolution		Per LSB		2		mV
Feedback voltage with margin high (7)	$V_{FB\_MG\_HIGH}$			672		mV
Feedback voltage with margin low (7)	$V_{FB\_MG\_LOW}$			500		mV
Soft Start and Turn-On/Off Delay						
Soft-start time	t_{SS}	61h[2:0] = 3b'001		2		ms
Turn-on delay	t_{ON_DELAY}	60h[10:0] = 0x000h		0		ms
Turn-off delay	t_{OFF_DELAY}	64h[10:0] = 0x000h		0		ms
Error Amplifier						
Feedback current	I_{FB}	V_{FB} = 0.65V		50	100	nA
Soft Shutdown						
Soft shutdown discharge FET	R_{ON_DISCH}			60		Ω
Under-Voltage Lockout (UVLO)						
VCC under-voltage lockout rising threshold	VCC_{Vth}		2.6	2.75	2.9	V
VCC under-voltage lockout hysteresis threshold	VCC_{HYS}			250		mV
Min configurable input turn-on voltage	$V_{IN\_ON\_MIN}$	VCC = 3.3V	2.65	2.9	3.15	V
Max configurable input turn-on voltage	$V_{IN\_ON\_MAX}$			16		V
Min configurable input turn-off voltage	$V_{IN\_OFF\_MIN}$	VCC = 3.3V		2.75		V
Max configurable input turn-off voltage	$V_{IN\_OFF\_MAX}$			15.75		V
Power Good						
Power good high threshold	PG_{VTH_HI}	FB from low to high, D9h[1:0] = 2b'01		94		$\%V_{REF}$
Power good low threshold	PG_{VTH_LO}	FB from high to low, D9h[3:2] = 2b'10		79		$\%V_{REF}$

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power good low-to-high delay	PG_{Td}	D1h[5:2] = 2b'0000		2		ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.3	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3V		1.5		µA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PG up to 3.3V through a 100kΩ resistor, T_J = 25°C		600	720	mV
	V_{OL_10}	V_{IN} = 0V, pull PG up to 3.3V through a 10kΩ resistor, T_J = 25°C		700	820	
Thermal Protection (TP)						
TP fault rising threshold (7)	T_{SD_Rise}	4Fh = 0x0091h		145		°C
TP fault hysteresis (7)	T_{SD_HYS}	D6h[2:1] = 2b'00		20		°C
TP warning rising threshold (7)	T_{WARN_Rise}	51h = 0x0082h		130		°C
TP warning hysteresis (7)	T_{WARN_HYS}	D6h[2:1] = 2b'00		20		°C
Min TP warning temp (7)	$T_{SD\_WARN\_MIN}$			35		°C
Max TP warning temp (7)	$T_{SD\_WARN\_MAX}$			160		°C
Monitoring Parameters						
Output voltage bit resolution				1.5		mV
Output current bit resolution (7)				63		mA
Input voltage bit resolution (8)				25		mV
PMBus DC Characteristics (SDA, SCL, ALERT, CTRL) (6)						
Input high voltage	V_{IH}				2.1	V
Input low voltage	V_{IL}		0.8			V
Output low voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Input leakage current	I_{LEAK}	SDA, SCL, ALERT = 5V	-10		+10	µA
Maximum voltage (SDA, SCL, ALERT, CTRL)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	+3.6	V
Pin capacitance on SDA, SCL	C_{PIN}				10	pF
PMBus Timing Characteristics (7)						
Min operating frequency				10		kHz
Max operating frequency				1000		kHz
Bus free time		Between stop and start condition	4.7			µs

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Holding time			4.0			µs
Repeated start condition set-up time			4.7			µs
Stop condition set-up time			4.0			µs
Data hold time			300			ns
Data set-up time			250			ns
Clock low timeout			25		35	ms
Clock low period			4.7			µs
Clock high period			4.0		50	µs
Clock/data falling time					300	ns
Clock/data rising time					1000	ns

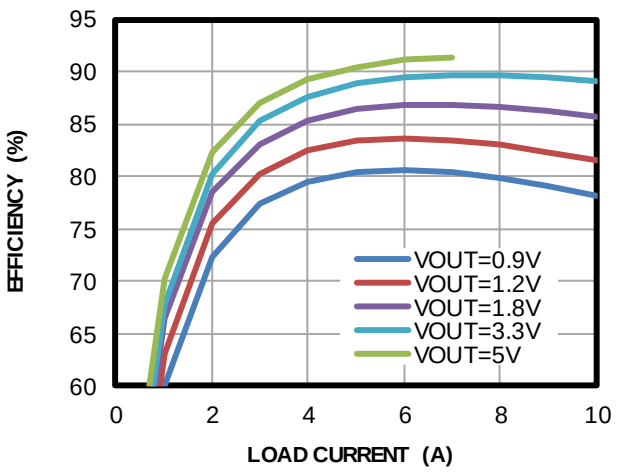
Notes:

7) Guaranteed by design.
8) Guaranteed by design. Not tested in production. The parameter is tested during parameters characterization.

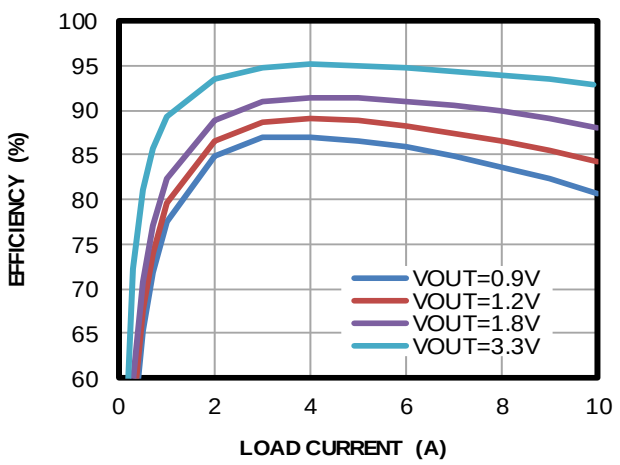
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, T_A = 25°C, single-phase full load = 10A, dual-phase full load = 20A, unless otherwise noted.

12V Input Efficiency

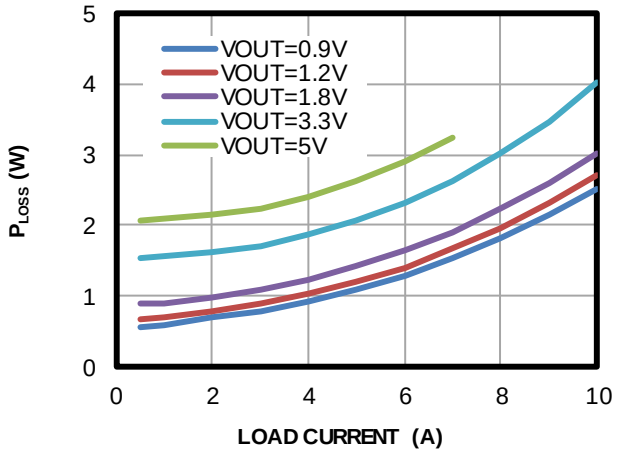


5V Input Efficiency



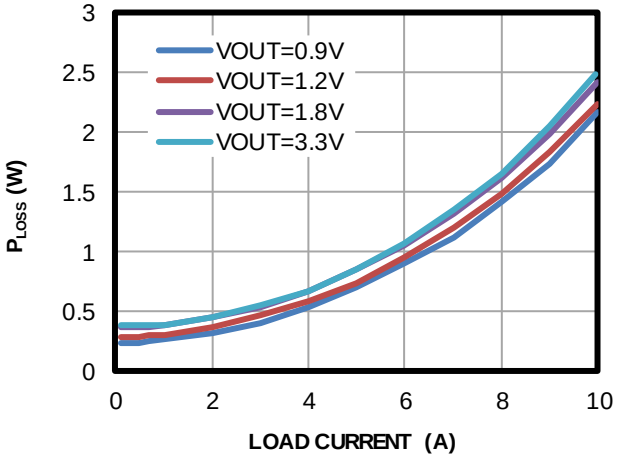
P_{LOSS} vs. Load Current

V_{IN} = 12V

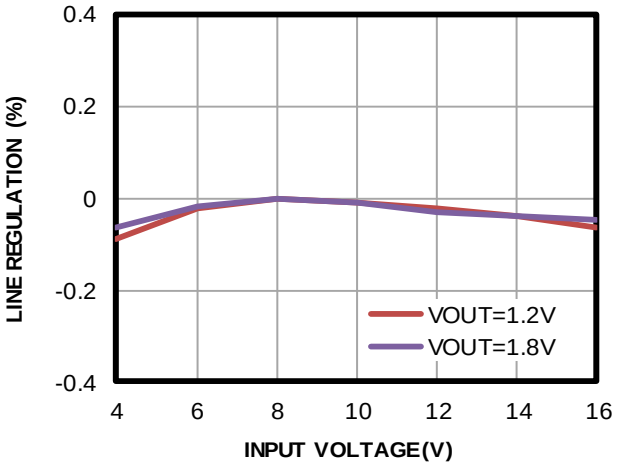


P_{LOSS} vs. Load Current

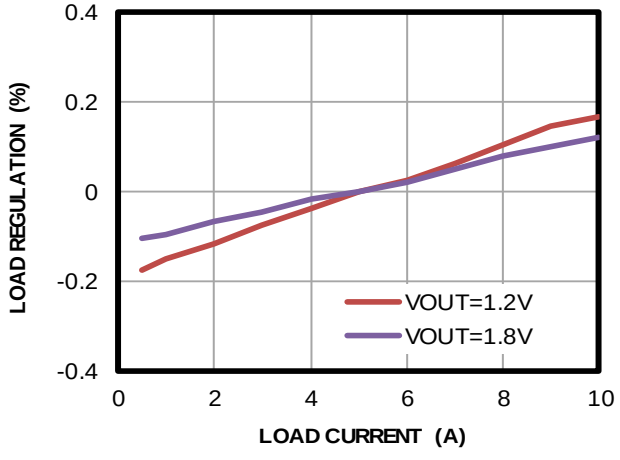
V_{IN} = 12V



Line Regulation



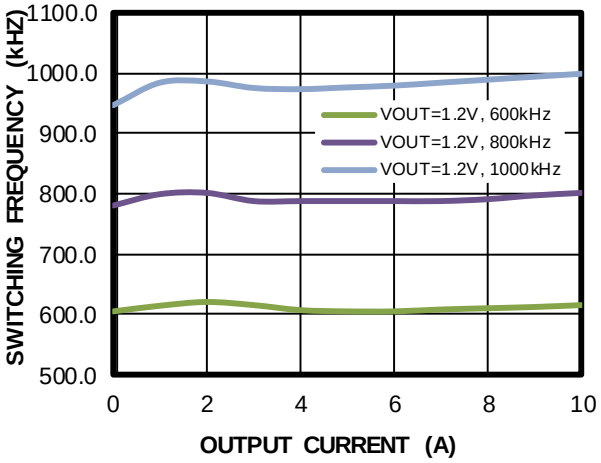
Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

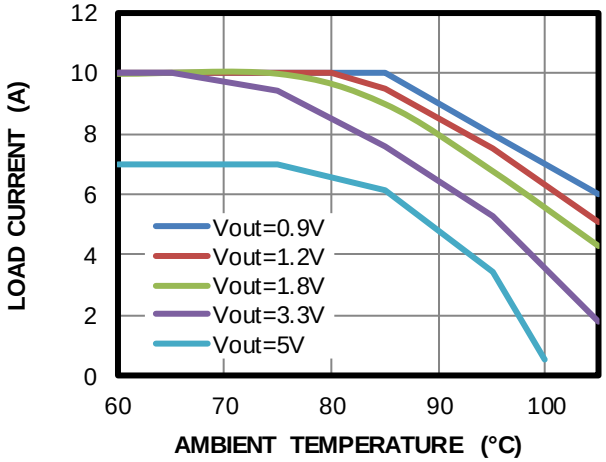
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, T_A = 25°C, single-phase full load = 10A, dual-phase full load = 20A, unless otherwise noted.

Switching Frequency Variation



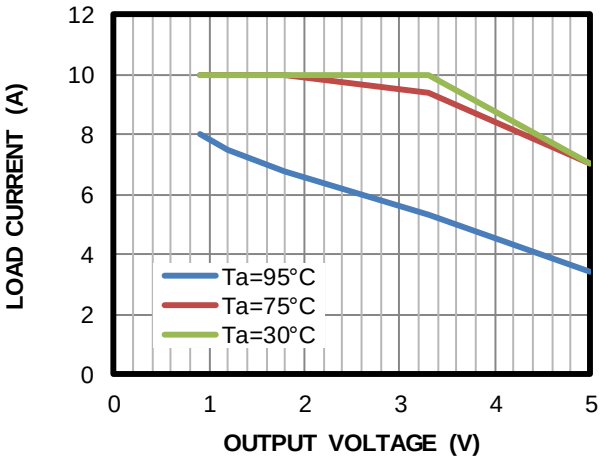
Thermal Derating

V_{IN} = 12V



Output Voltage Derating

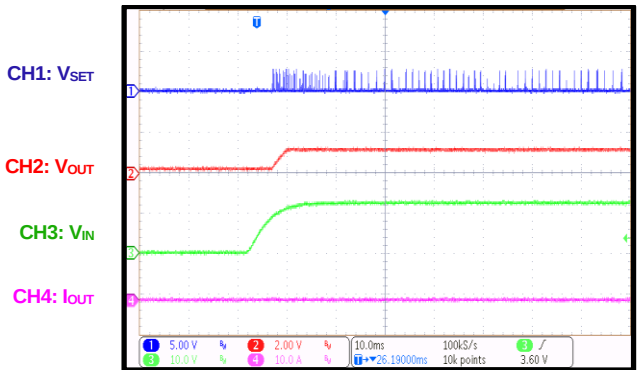
V_{IN} = 12V



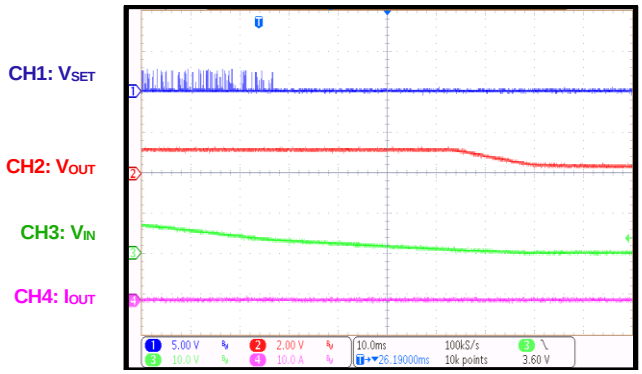
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, T_A = 25°C, single-phase full load = 10A, dual-phase full load = 20A, unless otherwise noted.

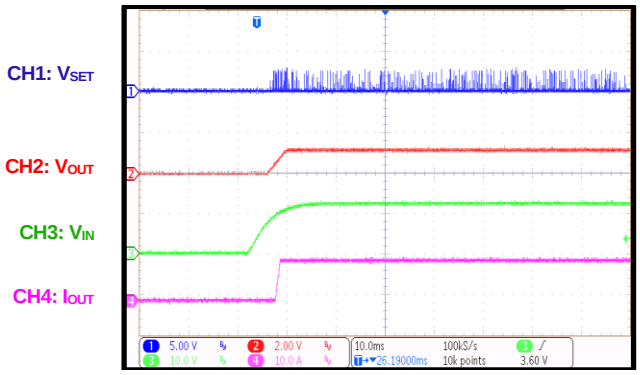
Input Start-Up
No load



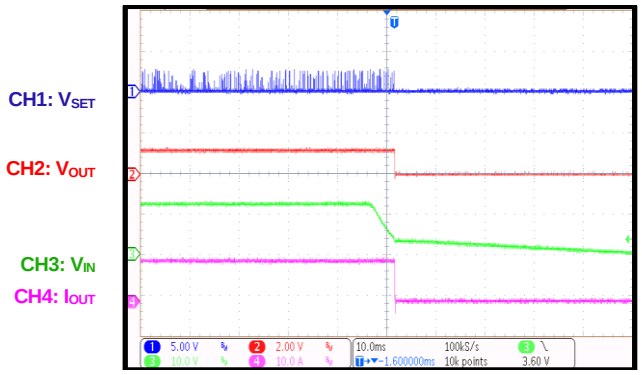
Input Shutdown
No load



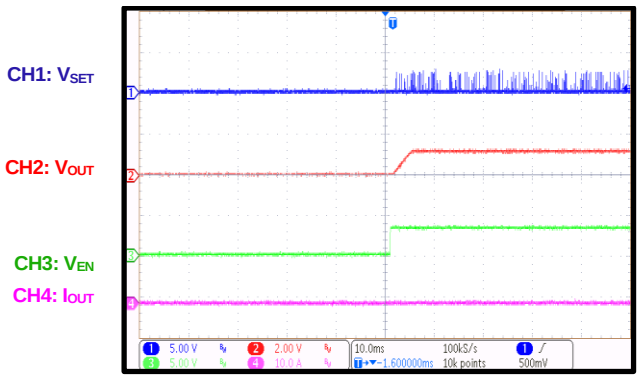
Input Start-Up
Full load



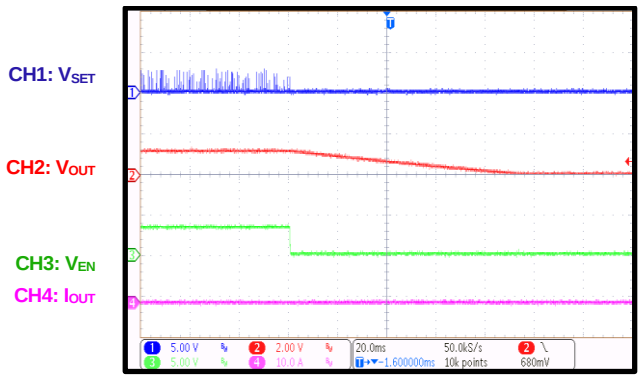
Input Shutdown
Full load



EN Start-Up
No load



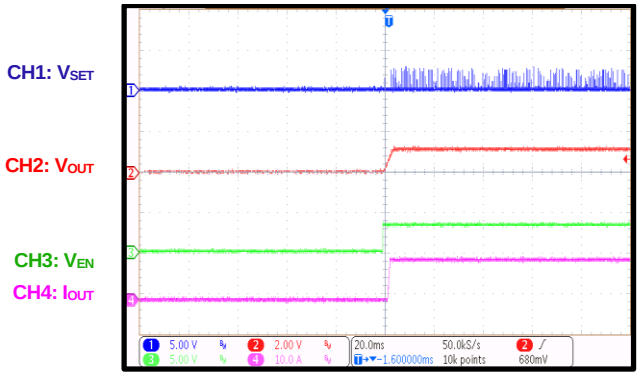
EN Shutdown
No load



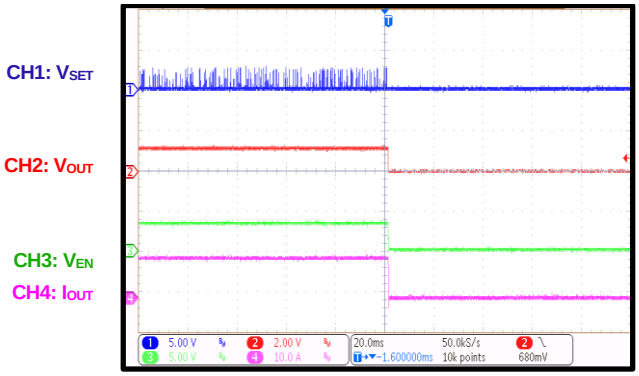
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, T_A = 25°C, single-phase full load = 10A, dual-phase full load = 20A, unless otherwise noted.

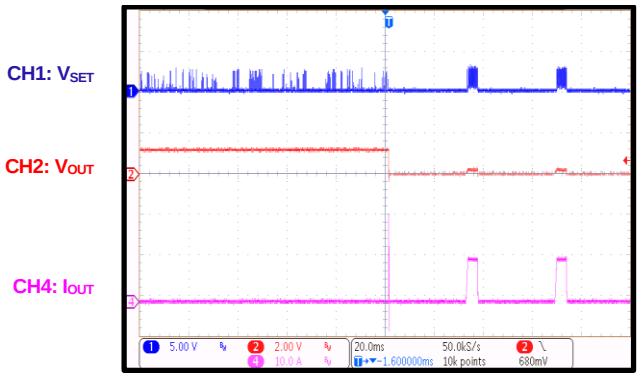
EN Start-Up
10A load



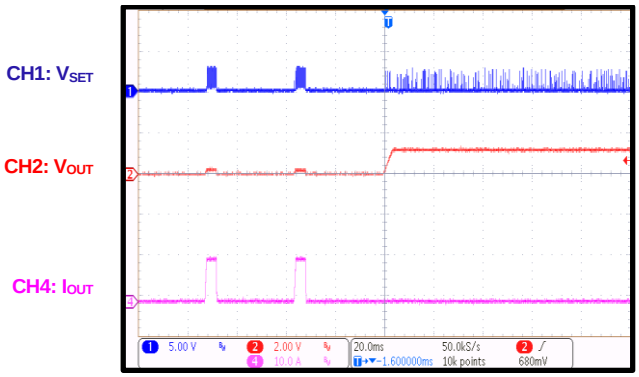
EN Shutdown
10A load



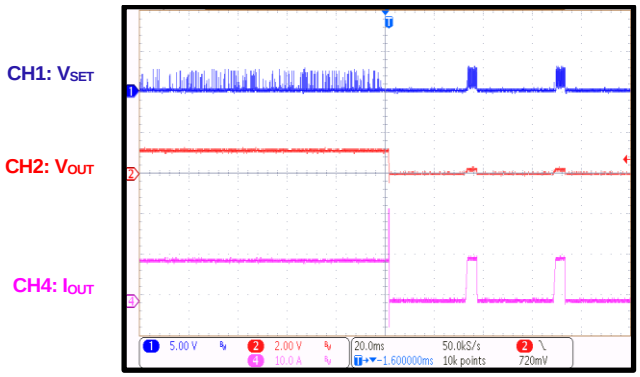
Short-Circuit Protection
No load



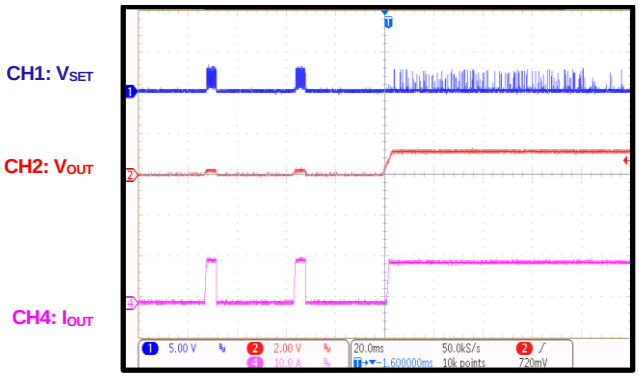
Short-Circuit Protection Recovery
No load



Short-Circuit Protection
Full load



Short-Circuit Protection Recovery
Full load

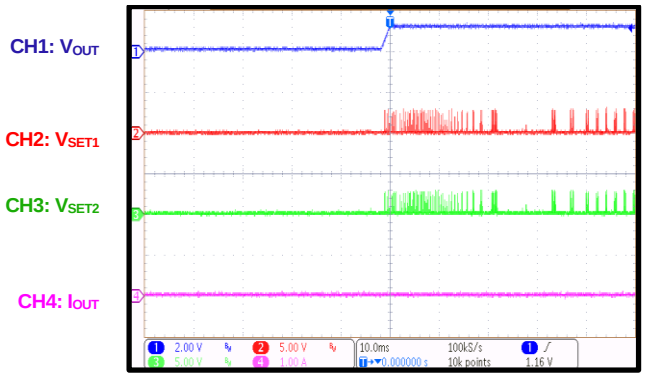


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, T_A = 25°C, single-phase full load = 10A, dual-phase full load = 20A, unless otherwise noted.

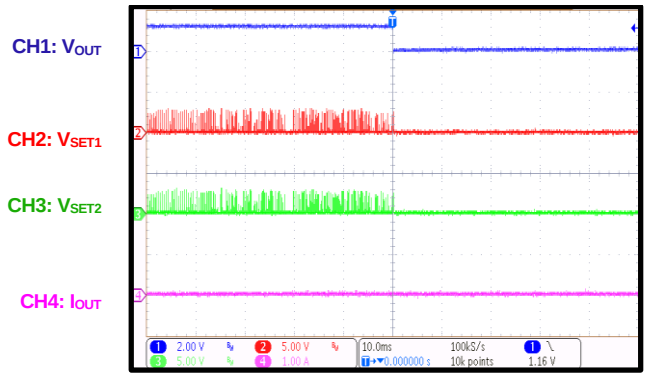
VIN Start-Up

No load, dual-phase operation



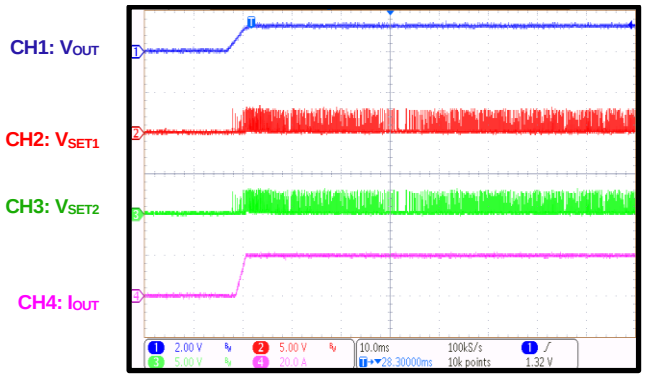
VIN Shutdown

No load, dual-phase operation



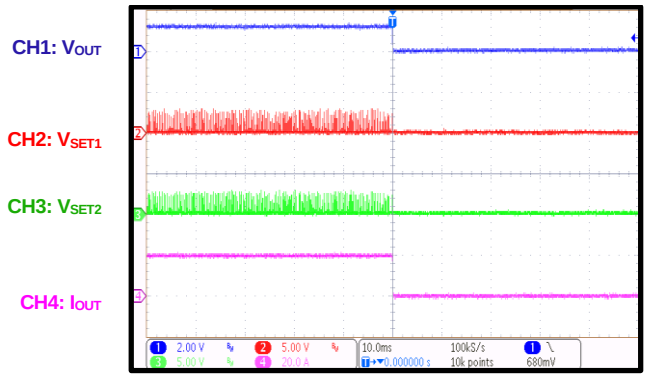
VIN Start-Up

Full load, dual-phase operation



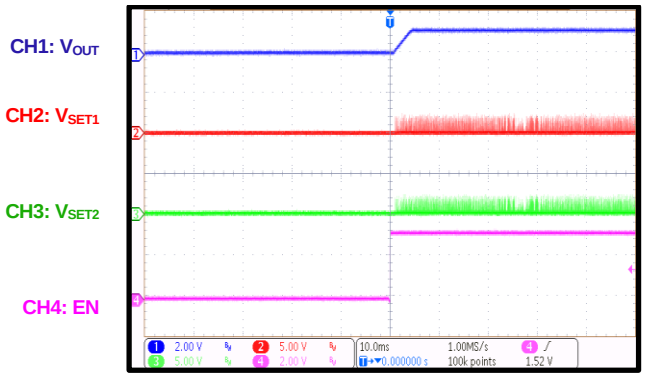
VIN Shutdown

Full load, dual-phase operation



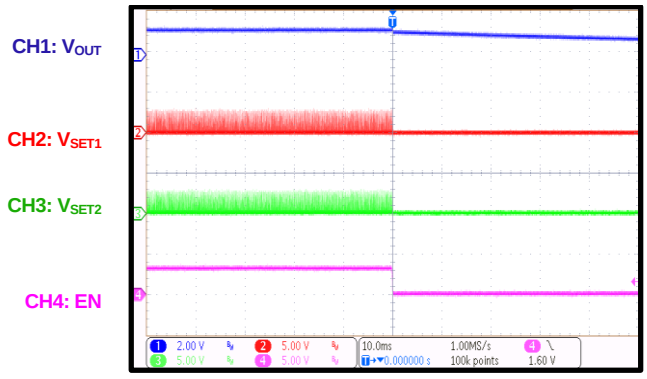
EN Start-Up

No load, dual-phase operation



EN Shutdown

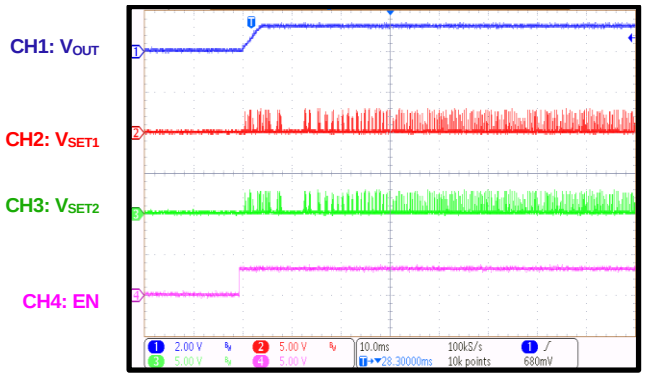
No load, dual-phase operation



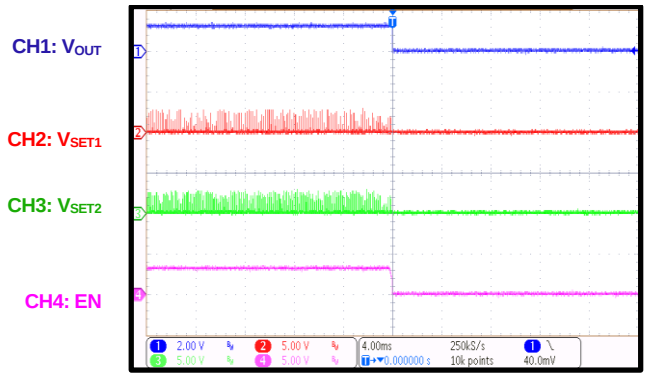
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, T_A = 25°C, single-phase full load = 10A, dual-phase full load = 20A, unless otherwise noted.

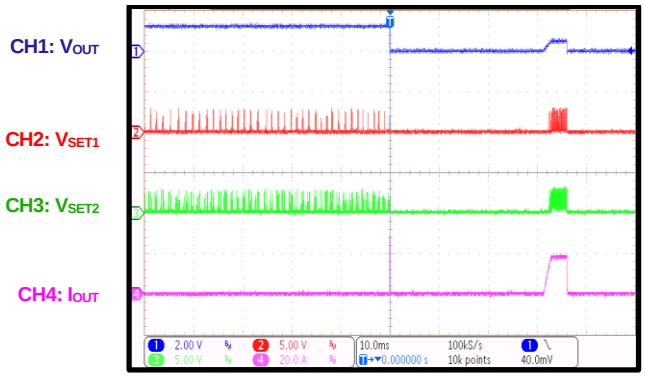
EN Start-Up
Full load, dual-phase operation



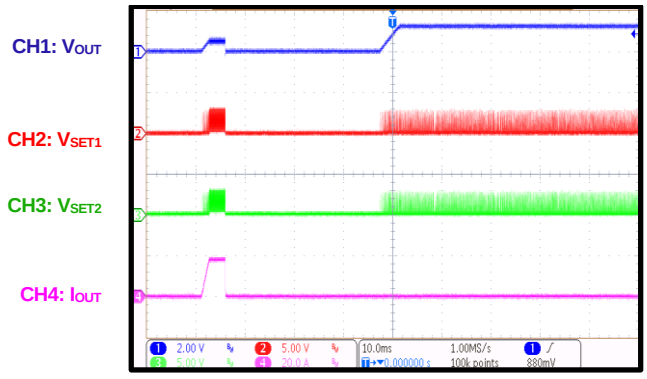
EN Shutdown
Full load, dual-phase operation



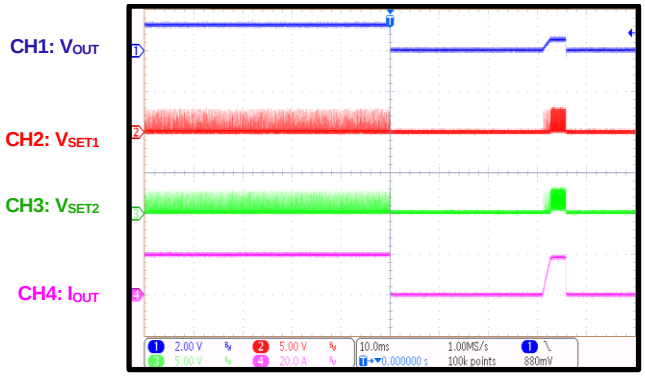
Short-Circuit Protection
No load



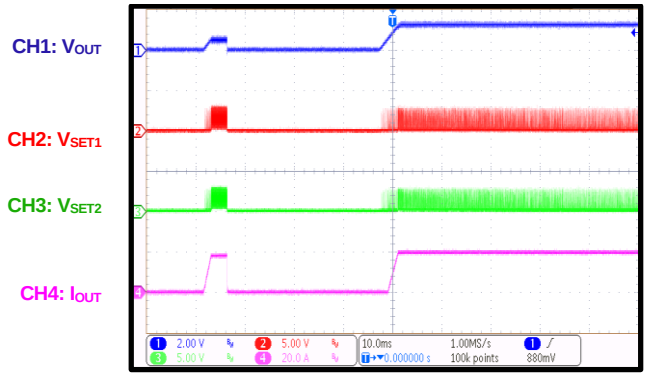
Short-Circuit Protection Recovery
No load



Short-Circuit Protection
20A load



Short-Circuit Protection Recovery
20A load

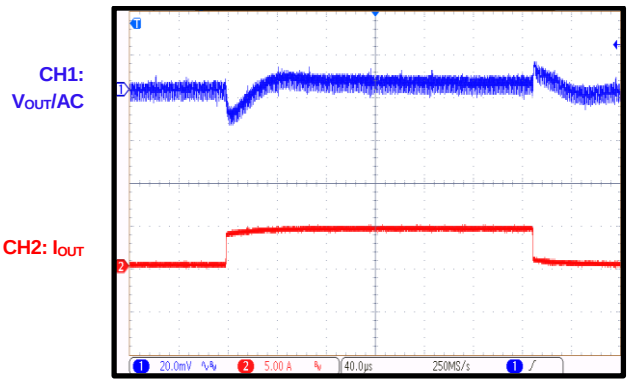


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 800kHz, T_A = 25°C, single-phase full load = 10A, dual-phase full load = 20A, unless otherwise noted.

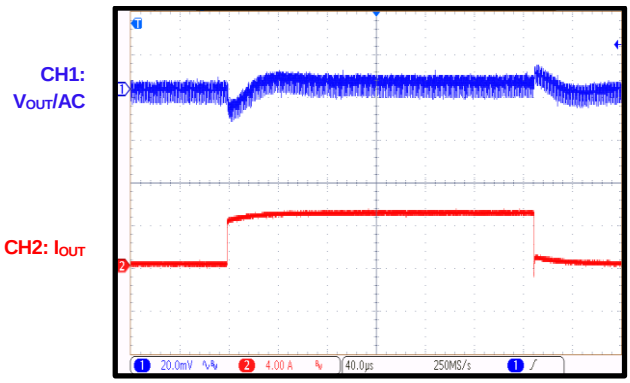
Transient Response

I_{OUT} = 0A to 5A, 20A/µs, V_{OUT} = 0.85V, C_{OUT} = 100µF x 4



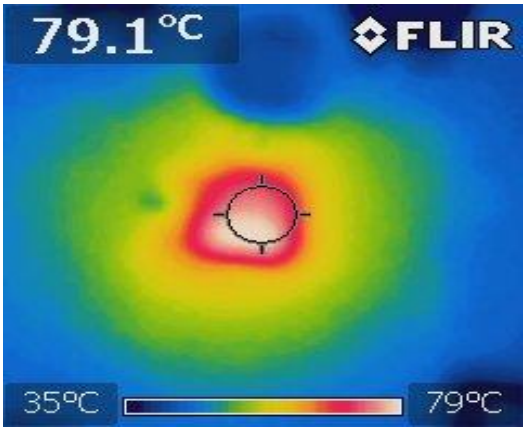
Transient Response

I_{OUT} = 0A to 5A, 20A/µs, V_{OUT} = 1.2V, C_{OUT} = 100µF x 4



Thermal Image

I_{OUT} = 10A, V_{OUT} = 1.2V, no air flow, no heatsink



FUNCTIONAL BLOCK DIAGRAM

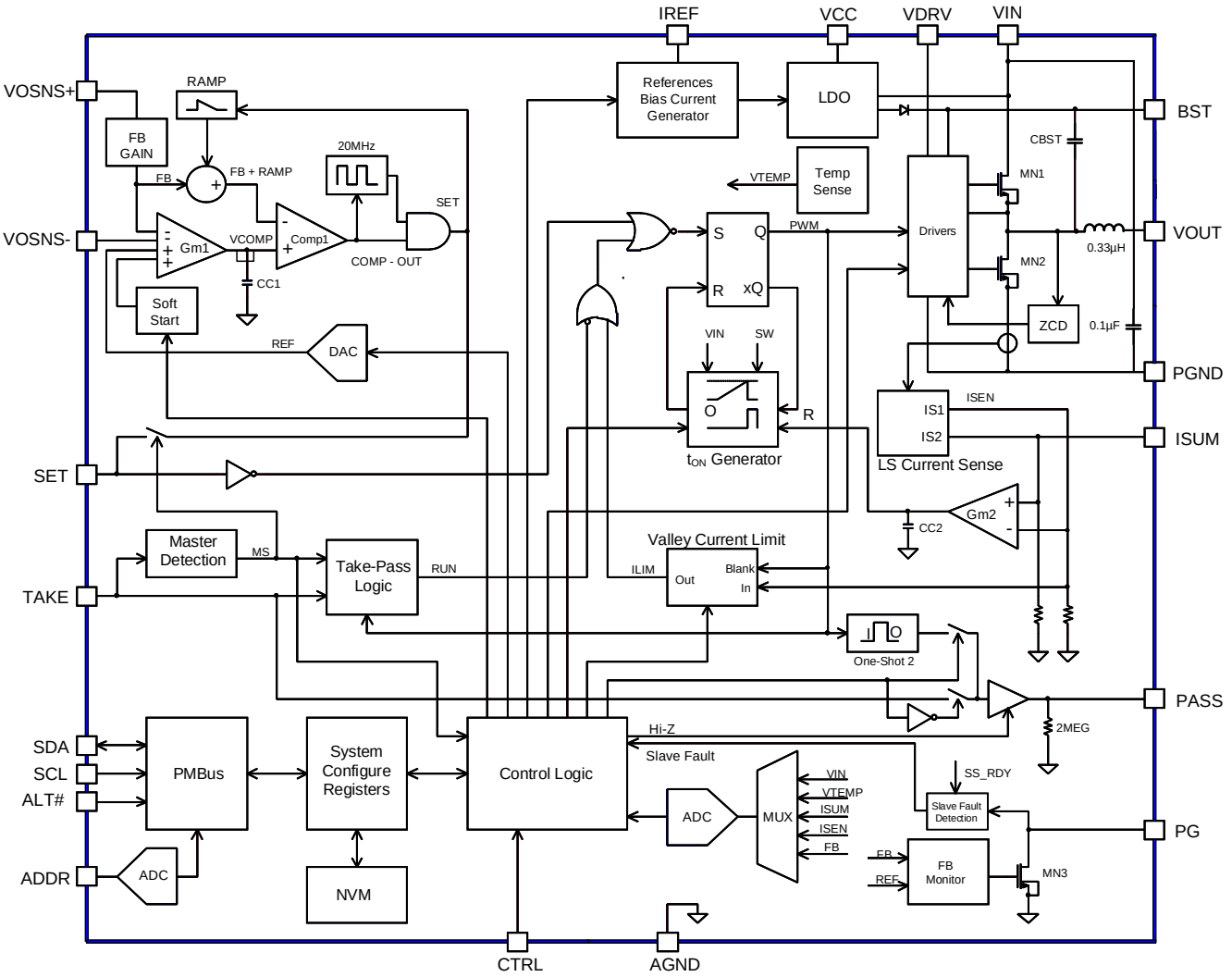


Figure 1: Functional Block Diagram

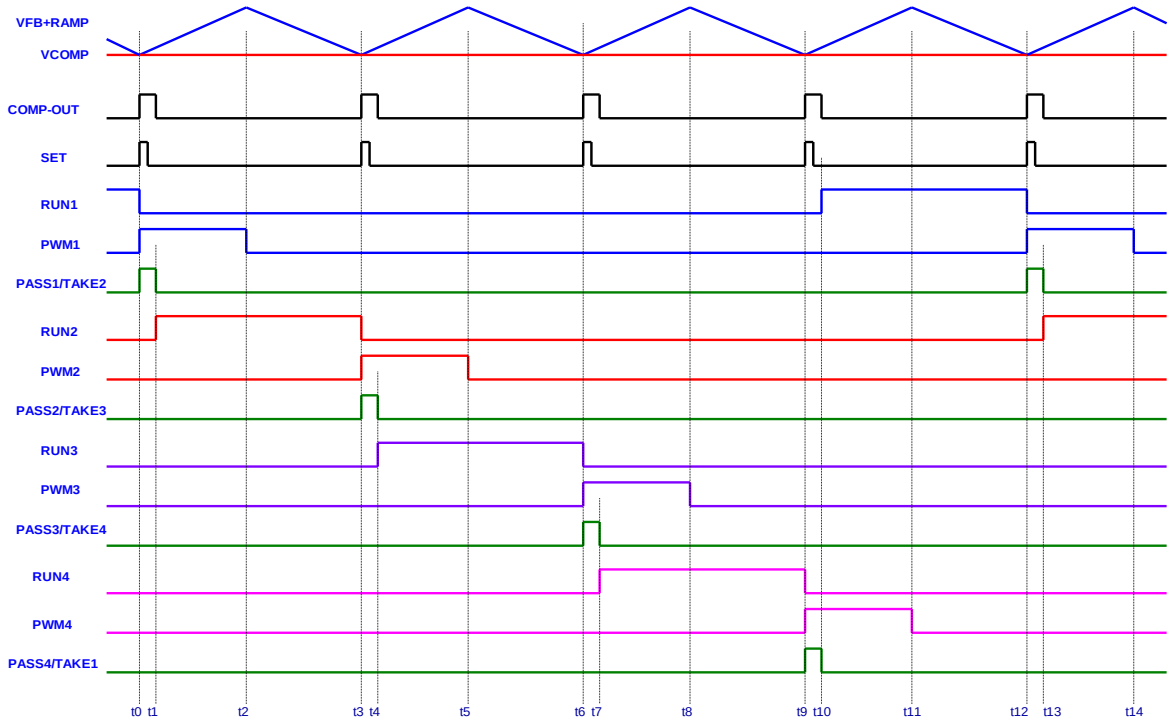


Figure 2: Multi-Phase Operation Timing Diagram (Steady State)

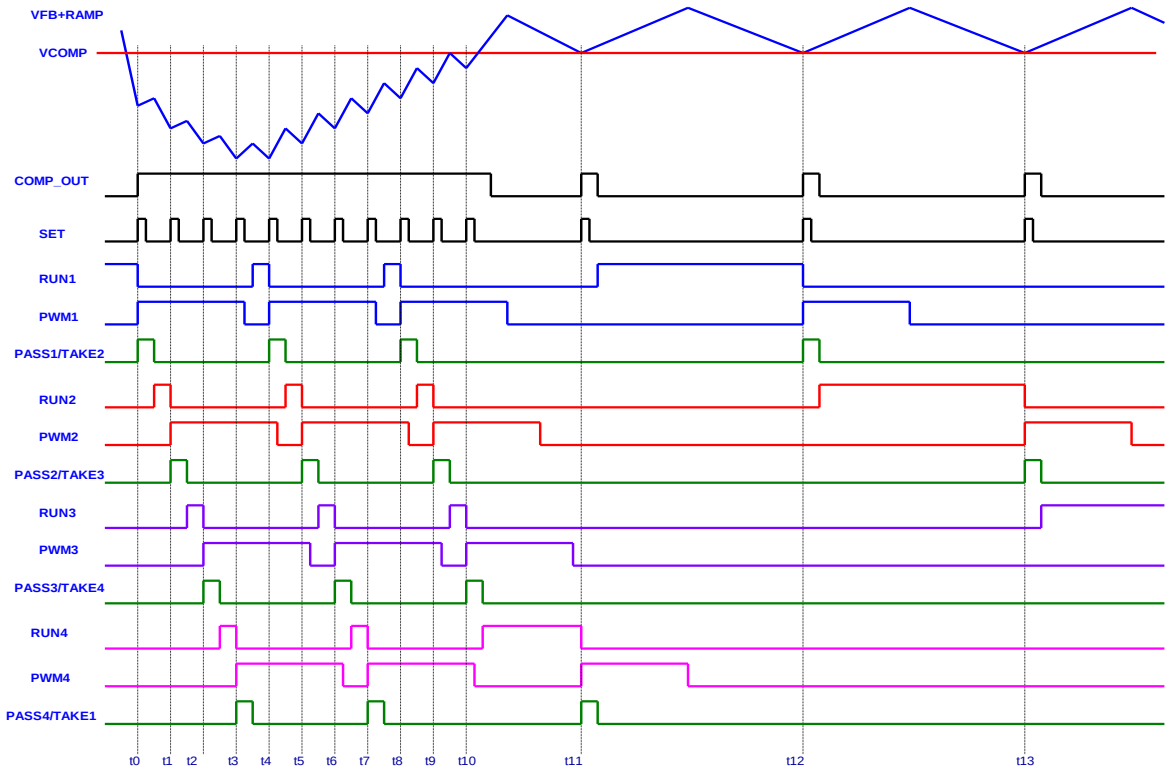


Figure 3: Multi-Phase Operation Timing Diagram (Transient)

OPERATION

The MPM3695-10 is a fully integrated power solution with up to 10A of continuous output current in an ultra-thin (8mmx8xmm2mm) package. For applications that require more than 10A, the MPM3695-10 can be connected in parallel for up to six phases, delivering an output peak current of up to 60A. Constant-on-time (COT) control to provide a fast transient response, and internal ramp compensation guarantees stable operation for applications using zero-ESR ceramic output capacitors.

Multi-Phase Operation

In a multi-phase configuration, one master phase and up to five slave phases are connected in parallel. The output current is equally shared among all phases. The typical application circuit integrates two MPM3695-10s in multi-phase configuration. The TAKE pin of the master phase must be pulled up to a voltage source through a resistor.

The MPM3695-10 detects its master/slave configuration by monitoring the state of the TAKE pin during start-up. The PASS and TAKE pins of all phases are connected in a cascade (see the Typical Application Circuits section on page 25). The PASS pin of the last slave phase is connected back to the TAKE pin of the master phase.

MCOT Operation: Master Phase

In multi-phase constant-on-time (MCOT) operation, a master phase performs the following functions:

- Accepts both write and read commands from a host through PMBus
- Generates the SET signal
- Manages start-up, shutdown, and all the protection functions
- Monitors fault alerts from the slave phases through the PG pin
- Generates the first on pulse
- Generates the on pulse when receiving run and set signals
- Dynamically adjusts its on time to ensure equal current sharing
- Generates the PASS signal

MCOT Operation: Slave Phases

In multi-phase constant-on-time (MCOT) operation, the slave phase has the following functions:

- Accepts write commands from a host through the PMBus
- Receives a SET signal from the master phase
- Sends OV/UV/OT fault alerts to the master phase through the PG pin
- Starts the on pulse when receiving run and set signals
- Dynamically adjusts its on time to ensure equal current sharing based on the per-phase and total current
- Generates the PASS signal

Figure 2 on page 18 shows MCOT operation, described below:

t0: At t0, a SET pulse is generated by the master phase when V_{FB} + RAMP drops below the reference level (V_{COMP}). All the phases receive this SET signal, but only the phase (e.g. the master) that has an active RUN signal activates.

The master turns on the high-side MOSFET (HS-FET), then generates a pulse with a fixed width on the PASS pin. This pulse is passed to the TAKE pin of slave 1.

t1: At t1, the falling edge of slave 1's TAKE pin activates the RUN signal. Then slave 1 waits for the SET signal to turn on its HS-FET.

t2: At t2, the on time of the master phase's PWM signal expires, and the HS-FET turns off. The PWM signal on time is fixed for a given input voltage, output voltage, and switching frequency. The on time of each phase is fine-tuned based on the per-phase and total current to ensure equal current sharing between phases.

t3: At t3, V_{FB} + RAMP drops below the reference level (V_{COMP}) in the master phase again. Only slave 1 has an active run signal, so it turns on the HS-FET. All other phases ignore this SET signal. Meanwhile, slave 1 generates a pulse with a fixed width on its PASS pin, and passes the pulse to slave 2's TAKE pin.

The MPM3695-10 maintains the above operation, and each phase turns on its HS-FET one by one for a fixed on time. Each phase receives a pulse on its TAKE pin, which activates a RUN signal. The RUN signal then generates a SET signal to turn on the HS-FET. Lastly, the phase generates a new pulse on its PASS pin, which is sent to the next phase's TAKE pin.

The device uses MCOT control to achieve ultra-fast load transient response. Figure 3 on page 18 shows that the SET signal is generated more frequently during a load transient than during steady state. Consequently, energy is delivered to the load at a higher rate, which minimizes the output deviation during a load transient event. In the MPM3695-10, the SET pulses can be generated with a minimum 50ns interval, meaning the next phase can be turned on as fast as 50ns after the previous phase's start-up.

Ramp Compensation

The MPM3695-10 guarantees stable operation with zero-ESR ceramic output capacitors by using internal ramp compensation. A triangular ramp signal is generated internally and is superimposed on the FB signal. The triangular ramp signal starts to rise once RAMP + FB drops below the REF signal, and a SET pulse is generated. The rising time of the RAMP signal is fixed.

The amplitude of the ramp compensation is selectable through register D0h[3:1] to support a wide range of operation configurations. There is a tradeoff between the stability and load transient response. A larger RAMP signal provides higher stability but slower load transient response, and a smaller RAMP signal provides the inverse. It is recommended to optimize the ramp compensation selection based on the design criteria for each application.

Operation Mode Selection

The MPM3695-10 provides both forced CCM and pulse skip operations under light-load conditions. Four switching frequencies are available for the MPM3695-10. The PMBus can designate the switching frequency and operation mode under light-load conditions.

Soft Start (SS)

The soft-start (SS) time can be configured via register 61h. The minimum SS time is 1ms, but it can also be configured to 2ms, 4ms, 8ms, or 16ms.

Pre-Biased Start-Up

The MPM3695-10 is designed for monotonic start-up into pre-biased loads. If the output voltage is pre-biased to a certain voltage during start-up, both the high-side and low-side switches are disabled until the internal reference voltage exceeds the sensed output voltage at the FB pin.

Output Voltage Discharge

Output voltage discharge mode is enabled if the MPM3695-10 is disabled through the CTRL pin. In this case, both the high-side and low-side switches are latched off. A discharge FET connected between SW and GND turns on to discharge the output capacitor. The discharge FET's on resistance is about 60Ω. Once the FB voltages drops below 10% of the reference output voltage, the discharge FET turns off.

APPLICATION INFORMATION

Output Voltage Setting

Two feedback resistors are required to set the appropriate feedback gain. The values of the feedback resistors can be calculated with Equation (1):

$$R_2(k\Omega) = \frac{0.6}{V_O - 0.6} \times R_1(k\Omega) \quad (1)$$

Where V_O is the output voltage. The output voltage feedback gain (G_{FB}) is estimated with Equation (2):

$$G_{FB} = \frac{R_2}{R_1 + R_2} \quad (2)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) must be placed in parallel with R1. Table 1 lists the values of feedback resistors and feed-forward capacitor for common output voltages.

Table 1: Common Output Voltages

V_O	R_1 (kΩ)	R_2 (kΩ)	C_{FF} (nF)
0.9	2	4	10
1.2	2	2	10
1.8	4.99	2.49	10
3.3	4.99	1.07	10

The MPM3695-10 offers output voltage configurability through the PMBus. In addition, the output voltage can be adjusted within a certain range through the PMBus by adjusting the internal reference voltage of the PMW controller (V_{REF}). V_{REF} has a default value of 0.6V, and can be adjusted to be between 0.5V and 0.672V.

For a given feedback resistor network, the upper limit of the output voltage (V_{O_MAX}) is estimated with Equation (3):

$$V_{O\_MAX} = \frac{0.67}{G_{FB}} \quad (3)$$

The lower limit of the output voltage (V_{O_MIN}) can be calculated with Equation (4):

$$V_{O\_MIN} = \frac{0.5}{G_{FB}} \quad (4)$$

To program the output voltage through PMBus, follow these two steps:

1. Write the G_{FB} value determined by Equation (2) to the register VOUT_SCALE_LOOP.
2. Write the output voltage command to the register VOUT_COMMAND.

V_{REF} is automatically updated based on the output voltage command and G_{FB}. Output voltage monitoring through the PMBus is enabled by setting register VOUT_SCALE_LOOP to the value that matches G_{FB}.

For application in which the PMBus interface is not required, V_{REF} = 0.6V by default, and the MPM3695-10 operates in analog mode. The feedback resistors should be estimated with Equation (1).

Current Sense and Over-Current Protection (OCP)

The MPM3695-10 features on-die current sensing and a configurable valley current limit threshold, which can be set via PMBus register D7h.

Inductor Valley Over-Current Protection (D7h)

When the low-side MOSFET (LS-FET) is on, the inductor current is sensed and monitored cycle by cycle. When FB drops below the reference, the high-side MOSFET (HS-FET) can only turn on if an over-current (OC) condition is not detected while the LS-FET is on.

The inductor current is limited cycle by cycle. If an OC condition is detected for 31 consecutive cycles, OCP is triggered. In addition, if the output voltage drops below the under-voltage protection (UVP) threshold during an over-current condition or output short-circuit condition, the MPM3695-10 enters OCP immediately.

Once OCP is triggered, the MPM3695-10 enters either hiccup or latch-off mode, depending on the register setting. To re-enable the device once it latches off, cycle the power on either VCC or CRTL.

The inductor valley over-current limit can be configured through PMBus command D7h, which sets the per-phase inductor valley current limit for both single- and multi-phase operation.

Negative Inductor Current Limit

If a negative current below the value set in register D5h[2] is detected on the LS-FET, the MPM3695-10 turns off its LS-FET for a certain period (set in register D5h[3]) to limit the negative current.

Under-Voltage Protection (UVP)

The MPM3695-10 monitors the output voltage through the FB pin. If the FB voltage drops below the under-voltage protection (UVP) threshold, then UVP is triggered and the MPM3695-10 enters either hiccup or latch-off mode depending on the register setting. To re-enable the device once it latches off, cycle the power on either VCC or CRTL.

Over-Voltage Protection (OVP)

If the FB voltage exceeds the over-voltage protection (OVP) threshold, OVP is triggered. See command VOUT_OV_FAULT_RESPONSE on page X for detailed OVP responses.

Output Sinking Mode (OSM)

When the output voltage reaches 104% of the reference voltage but remains below the OVP threshold, the device enters output sinking mode (OSM). Once OSM is triggered, the MPM3695-10 runs operates in forced CCM mode. The device exits OSM mode when the HS-FET turns back on.

Over Temperature Protection (OTP)

The MPM3695-10 monitors the junction temperature. When the junction temperature exceeds the over-temperature protection (OTP) threshold (about 170°C), the module enters either hiccup or latch-off mode depending on the PMBus selection. To re-enable the MPM3695-10, cycle the power on either VCC or CTRL.

Power Good (PG)

The MPM3695-10 has an open-drain power good (PG) output. The PG pin must be pulled high to V_{CC} or a voltage source below 3.6V through a pull-up resistor (about 100kΩ). PG is initially pulled low once an input voltage is applied to the MPM3695-10. After the FB voltage reaches the threshold set by the register POWER_GOOD_ON, the PG pin is pulled high after a delay set by the register. The delay can be designated through the PMBus MFR_CTRL_VOUT command.

PG latches low if any fault occurs and a protection is triggered (e.g. UV, OV, OT, UVLO). After PG latches off, it cannot be pulled high again until a soft start is initiated.

If the input supply fails to power the MPM3695-10, PG latches off. Figure 4 shows the relationship between the PG voltage and the pull-up current.

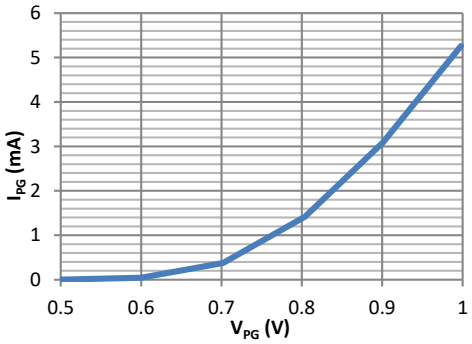


Figure 4: Power Good Current vs. Power Good Voltage

Input Capacitor

The buck converter has a discontinuous input current, and requires a capacitor to supply the AC current to the module while maintaining the DC input voltage. Use ceramic capacitors for the best performance. When designing the PCB layout, place the input capacitors as close to the IN pin as possible.

Capacitance can vary significantly with temperature. Ceramic capacitors with X5R and X7R dielectrics are recommended because they are fairly stable across a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. The input ripple current can be calculated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter's input voltage ripple. Select a capacitor value that meets the input voltage ripple requirements.

Estimate the input voltage ripple with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Output Capacitor

The output capacitor maintains the DC output voltage. It is recommended to use ceramic or POSCAP capacitors. Estimate the output voltage ripple with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

The ESR contributes minimally to the output voltage ripple, so an external ramp is required to stabilize the system. The external ramp can be designed with R4 and C4 as per Equation (5), Equation (8), and Equation (9).

The ESR dominates the impedance at the switching frequency for POSCAP capacitors. A sufficient ESR ramp voltage stabilizes the system and eliminates the need for an external ramp. Select a minimum ESR value of about 12mΩ to ensure stable operation. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

PCB Layout Guidelines

PCB layout is vital for stable operation. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the input ceramic capacitors as close to the VIN and PGND pins as possible, on the same layer as the MPM3695-10.
2. Maximize the VIN and PGND copper planes to minimize parasitic impedance.
3. Place sufficient PGND vias close to the PGND pins to minimize parasitic impedance.
4. Float the ISUM pin for single-phase configurations.
5. Keep the ISUM trace as short as possible for multi-phase configurations.
6. Avoid placing vias on ISUM.
7. Connect VOSNS+ and VOSNS- to the difference line to decrease noise.
8. Maintain a clean keepout area.

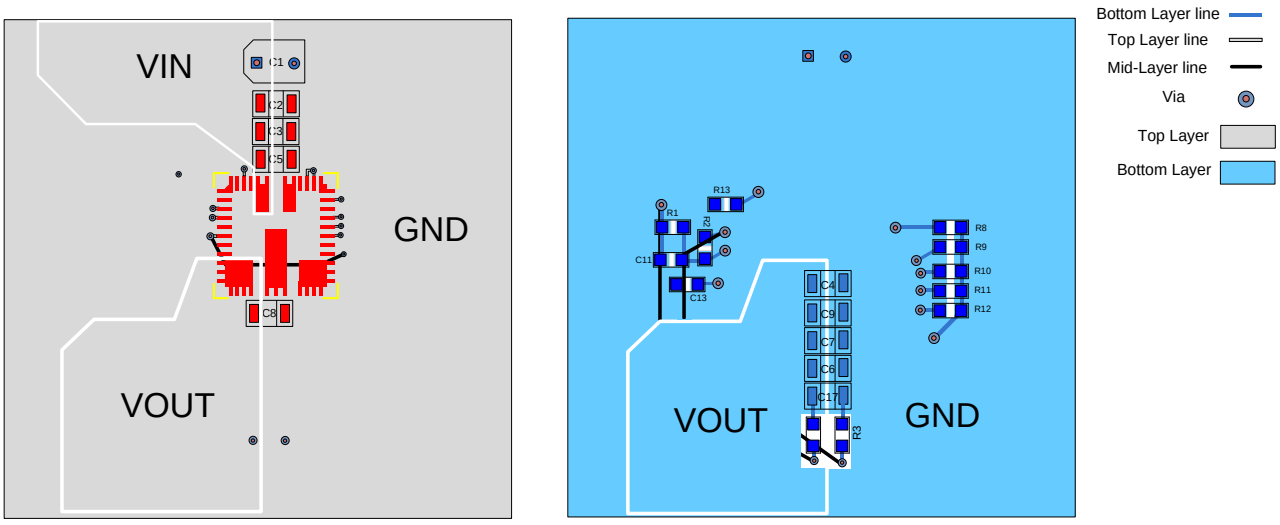


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

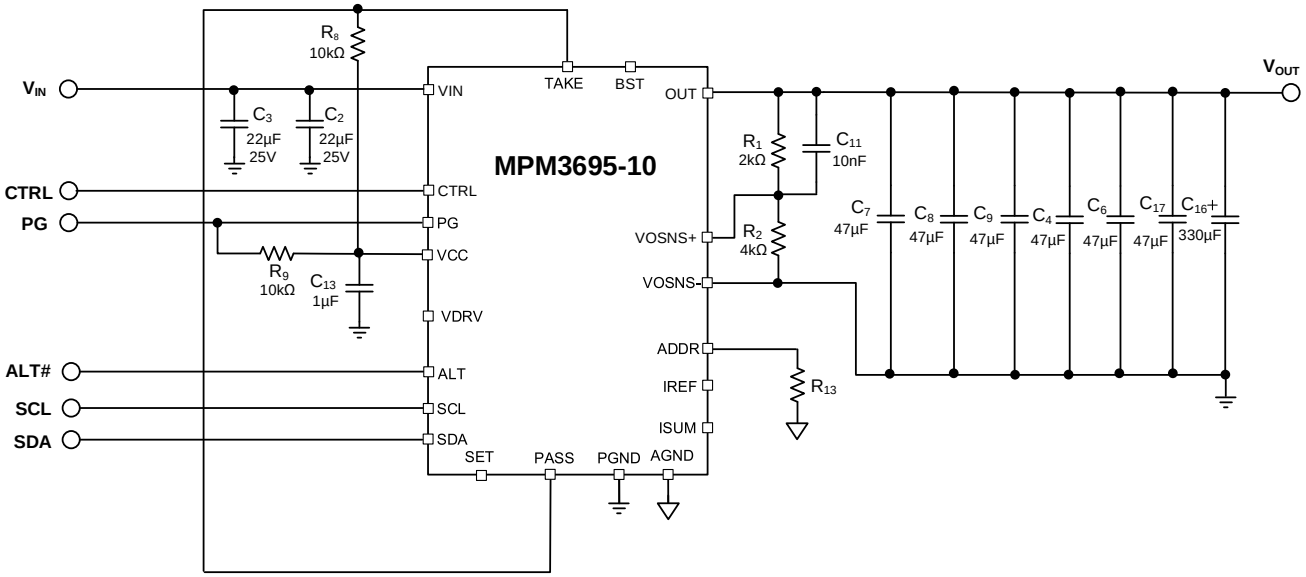


Figure 6: Typical Application Circuit – Single-Phase, V_{IN} = 4V to 16V, V_{OUT} = 0.9V at 10A Output

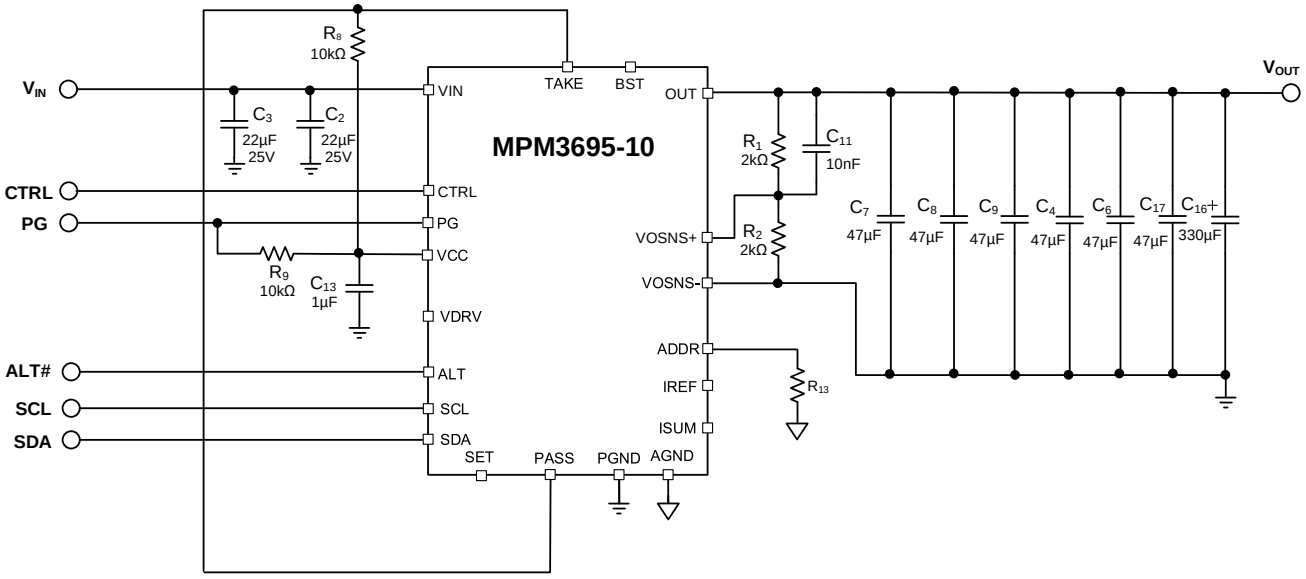


Figure 7: Typical Application Circuit – Single-Phase, V_{IN} = 4V to 16V, V_{OUT} = 1.2V at 10A Output

TYPICAL APPLICATION CIRCUITS *(continued)*

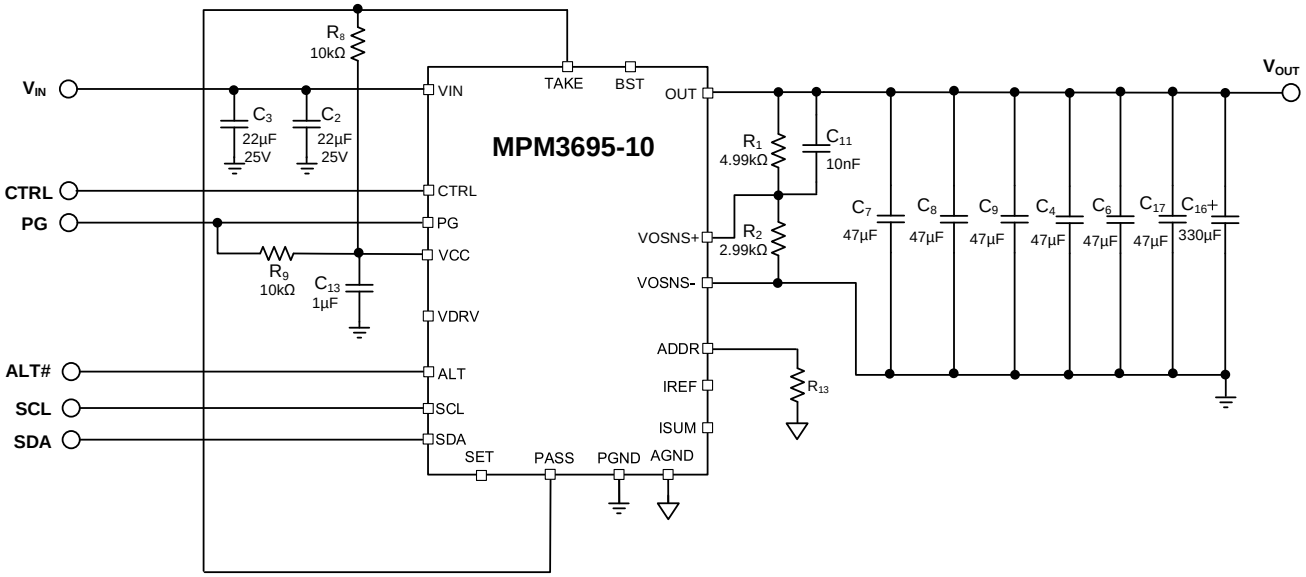


Figure 8: Typical Application Circuit – Single-Phase, V_{IN} = 4V to 16V, V_{OUT} = 1.8V at 10A Output

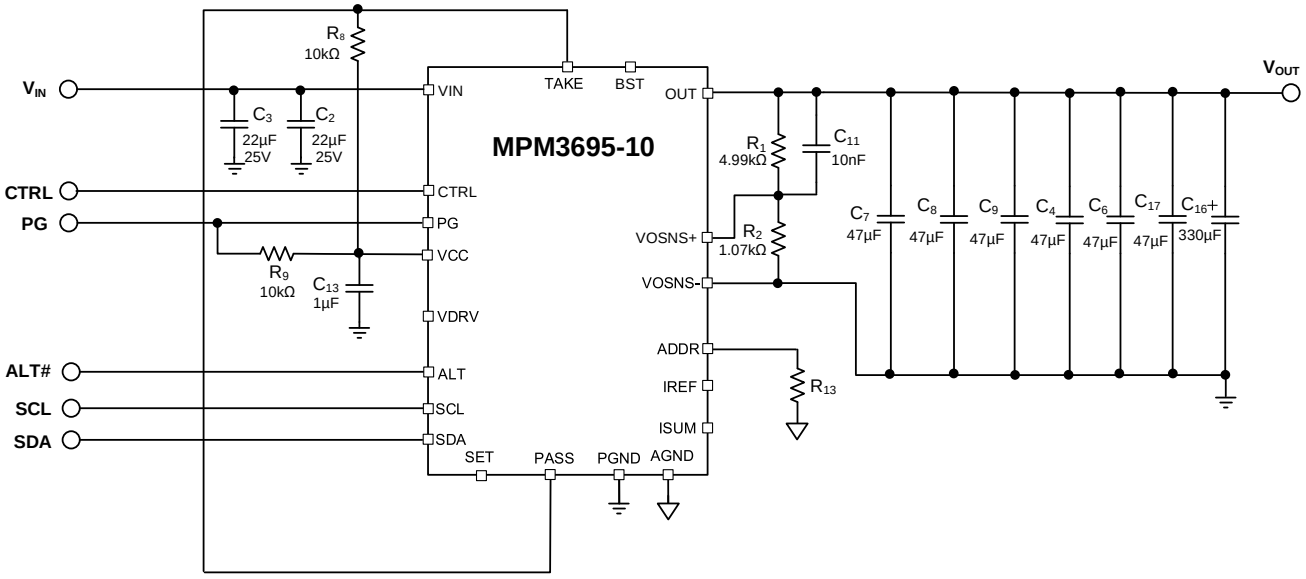


Figure 9: Typical Application Circuit – Single-Phase V_{IN} = 4V to 16V, V_{OUT} = 3.3V at 10A Output

TYPICAL APPLICATION CIRCUITS *(continued)*

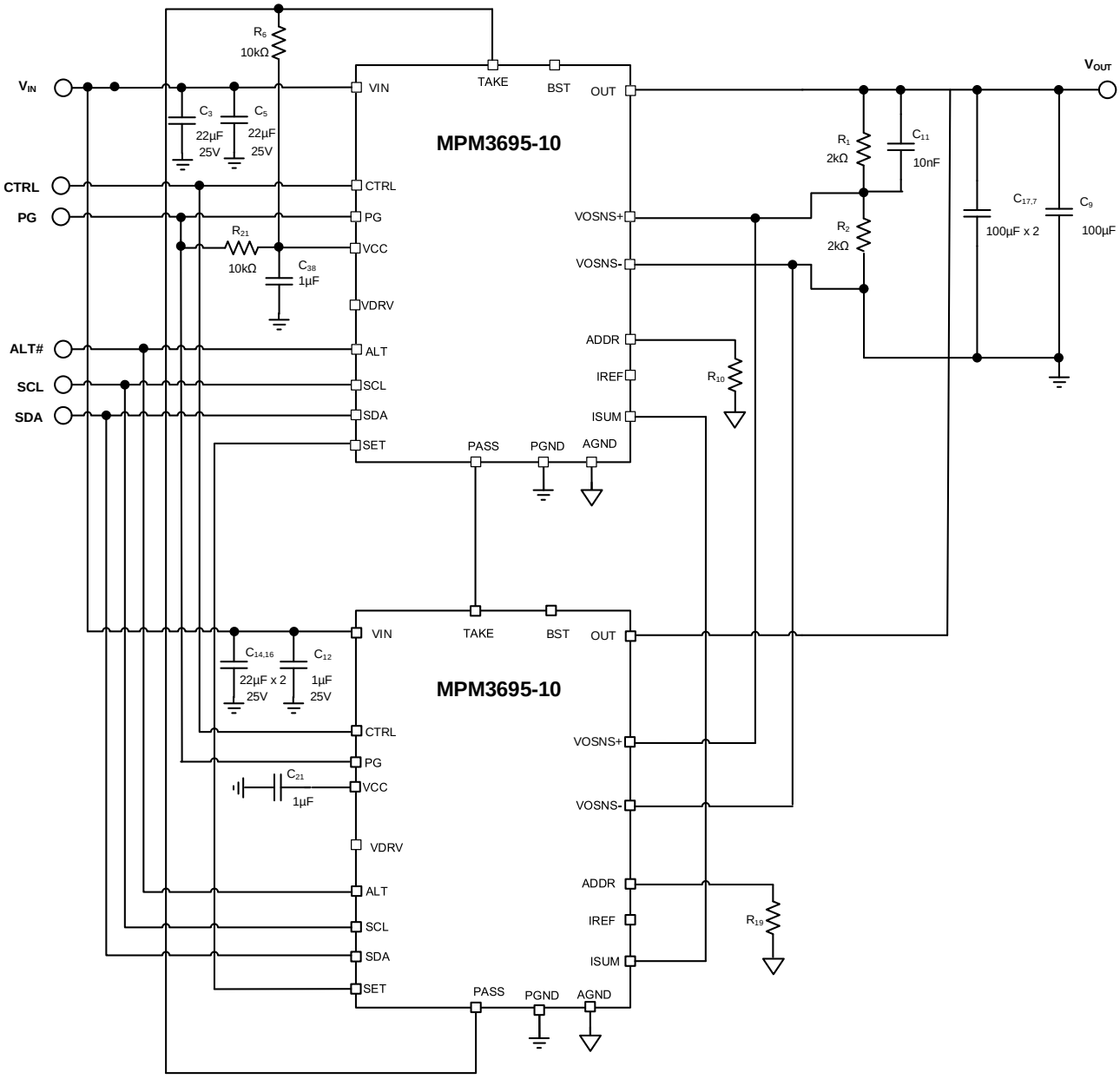


Figure 10: Typical Application Circuit – Dual-Phase, V_{IN} = 4V to 16V, V_{OUT} = 1.2V at 20A Output

PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled up to a bus voltage when they are idle. When connecting the lines, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPM3695-10 is a PMBus slave device that supports both standard mode (100kHz) and fast modes (400kHz and 1000kHz).

Slave Address

A unique address should be set for each slave device that is connected to the same PMBus. The ADDR pin programs the address of each MPM3695-10. There is a 10μA current flowing out of the ADDR pin. Connect a resistor between the ADDR and AGND pins to set the ADDR voltage. The internal ADC converts the pin voltage of the ADDR pin to set the PMBus address. A maximum of 16 addresses can be set by the ADDR pin. Table 2 lists the PMBus address for different resistor values.

Table 2: PMBus™ Address vs. ADDR resistor

R_{ADDR} (kΩ)	Slave Address
4.99	30h
15	31h
24.9	32h
34.8	33h
45.3	34h
54.9	35h
64.9	36h
75	37h
84.5	38h
95.3	39h
105	3Ah
115	3Bh
124	3Ch
133	3Dh
147	3Eh
154	3Fh

The MFR_ADDR_PMBUS (D3h) register can set the PMBus address digitally.

For multi-phase configuration, the slave phases can share the same address as the master, or they can have different addresses based on the application. The master phase can accept read (R) and write (W) commands from the PMBus master, but the slave phases can only accept write commands.

Start and Stop Conditions

The start (S) and stop (P) commands are signaled by the master device, and signify the beginning and the end of the PMBus transfer. A start command is when the SDA signal transfers from high to low while SCL is high. A stop command is when the SDA signal transfers from low to high while SCL is high (see Figure 10).

The master generates the SCL clocks, and transmits the device's address as well as the read/write direction bit (R/W) on the SDA line. Data is transferred in 8-bit bytes by an SDA line. Each data byte should be followed by an acknowledge (ACK) bit.

PMBus Update Sequence

The MPM3695-10 requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data update. After each byte is received, the MPM3695-10 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPM3695-10. The MPM3695-10 thenperforms an update on the falling edge of the LSB byte.

Protocol Usage

All PMBus transactions on the MPM3695-10 are done using defined bus protocols. The following protocols can be implemented:

- Send byte with PEC
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

Packet Error Checking (PEC)

The MPM3695-10 PMBus interface supports a packet error checking (PEC) byte.

The PEC byte is transmitted by the MPM3695-10 during a read transaction, or sent by the bus host to the MPM3695-10 during a write transaction.

The PEC byte detects errors during a bus transaction based on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide whether to repeat the read. If the MPM3695-10 determines that the PEC byte sent during a write transaction is incorrect, it does not execute the command (called an ignore) and sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the MPM3695-10.

PMBus Alert Response Address (ARA)

The PMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices that it must talk to. A host typically uses a hardware interrupt pin to monitor the PMBus ALERT pins on a number of devices. When the host interrupts, the host issues a message on the bus using the PMBus receive byte, or a receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices with a PMBus alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active PMBus alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds in transmitting its address disables its PMBus alert signal. If the host sees that the PMBus alert signal is still low, it continues to read addresses until all devices have successfully transmitted their addresses.

PMBus Bus Message Format

In Figure 12, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the MPM3695-10 is driving the bus. The following abbreviations may be used:

- S = start condition
- Sr = repeated start condition
- P = stop condition
- R = read bit
- $\overline{W}$ = write bit
- A = acknowledge bit (0)
- $\overline{A}$ = acknowledge bit (1)

“A” represents the ACK (acknowledge) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is logic 1, indicated by $\overline{A}$.

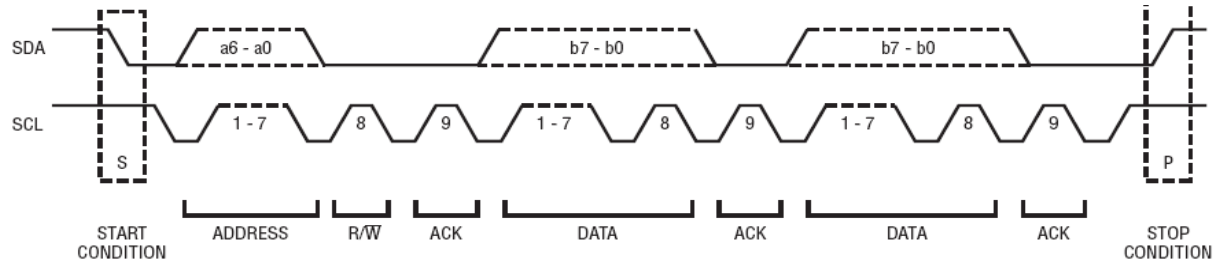


Figure 11: Data Transfer over PMBus

1. Send Byte and Send Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	W	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Data Byte	A	PEC	A	P

2. Receive Byte and Receive Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	R	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	R	A	Data Byte	A	PEC	A	P

3. Write Byte and Write Byte with PEC

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	P

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	PEC	A	P

4. Write Word and Write Word with PEC

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC	A	P

5. Read Byte and Read Byte with PEC

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte	A	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte	A	PEC	A	P

6. Read Word and Read Word with PEC

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A

8	1	1
Data Byte High	A	P

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	W	A	Command Code	A	S	Slave Address	R	A	Data Byte Low	A

8	1	8	1	1
Data Byte High	A	PEC	A	P

7. Block Read with PEC

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	W	A	Command Code	A	Sr	Slave Address	R	A	Byte Count = N	A	...

8	1	8	1	...	8	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	P

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	W	A	Command Code	A	Sr	Slave Address	R	A	Byte Count = N	A	...

8	1	8	1	...	8	1	8	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	PEC	A	P

Figure 12: PMBus Message Format

Data and Numerical Formats

The MPM3695-10 uses a direct internal format to represent real-world values such as voltage, current, power, and temperature.

All numbers with no suffix in this document are decimals, unless explicitly designated otherwise.

Numbers in binary format are indicated by the prefix “n’b”, where n is the binary count. For example, 5’b01010 indicates a 5-bit binary data, where the data is 01010.

The suffix “h” indicates hexadecimal format, which is generally used for the register address numbers in this document.

The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number whose hexadecimal value is A3.

PMBus Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults, listed below:

- Sending too little data
- Reading too little data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

PMBus Reporting and Status Monitoring

The PMBus supports real-time monitoring for certain operation parameters and statuses (see Table 3).

Table 3: Parameters and Statuses Monitored by the PMBus

Parameter/Status	PMBus
Output voltage	1.25mV/LSB
Output current	62.5mA/LSB
Temperature	1°C/LSB
Input voltage	25mV/LSB
V_{IN} OV	✓
V_{IN} UV	✓
V_{IN} OV warn	✓
V_{IN} UV warn	✓
V_O OV	✓
V_O UV	✓
Over-temperature (OT)	✓
OT warn	✓
V_O OC	✓
V_O OC warn	✓

MTP Programming

The MPM3695-10 has built-in multiple time programmable (MTP) cells to store user configurations. The standard command of 15h (STORE_USER_ALL) is not supported by the MPM3695-10. Alternatively, the MTP cells can be configured through the following command combination:

1. E7h(2800h)
2. E7h(1800h)
3. E7h(4800h)

In MPS’s GUI for the MPM3695-10, the above commands are integrated together and named 15h (STORE_USER_ALL). MPS’s GUI supports the 15h command.

When the MTP is being configured, the VCC voltage may go up as high as 5V. It is recommended to connect VCC only to a circuit that can handle such a high voltage.

It takes about 300ms to configure the MTP.

REGISTER MAP

Name	Code	Type	Bytes	Default Value	MTP?
OPERATION	01h	R/W w/ PEC	1	0x80	Yes
ON_OFF_CONFIG	02h	R/W w/ PEC	1	0x1E	Yes
CLEAR_FAULTS	03h	Send byte w/ PEC	0	-	
WRITE_PROTECT	10h	R/W w/ PEC	1	0x00	Yes
STORE_USER_ALL	15h	Send byte w/ PEC	0	-	-
RESTORE_USER_ALL	16h	Send byte w/ PEC	0	-	-
CAPABILITY	19h	R w/ PEC	1	0xB0	-
VOUT_MODE	20h	R w/ PEC	1	0x40	-
VOUT_COMMAND	21h	R/W w/ PEC	2	0x0258 (1.2V)	Yes
VOUT_MAX	24h	R/W w/ PEC	2	0x0BB8 (6V)	Yes
VOUT_MARGIN_HIGH	25h	R/W w/ PEC	2	0x02A0 (1.344V)	Yes
VOUT_MARGIN_LOW	26h	R/W w/ PEC	2	0x01FE (1.02V)	Yes
VOUT_SCALE_LOOP	29h	R/W w/ PEC	2	0x01F4 (0.5)	Yes
VOUT_MIN	2Bh	R/W w/ PEC	2	0x00FA (0.5V)	Yes
VIN_ON	35h	R/W w/ PEC	2	0x0010 (4V)	Yes
VIN_OFF	36h	R/W w/ PEC	2	0x000B (2.75V)	Yes
OT_FAULT_LIMIT	4Fh	R/W w/ PEC	2	0x00A0 (160°C)	Yes
OT_WARN_LIMIT	51h	R/W w/ PEC	2	0x008C (140°C)	Yes
VIN_OV_FAULT_LIMIT	55h	R/W w/ PEC	2	0x0024 (18V)	Yes
VIN_OV_WARN_LIMIT	57h	R/W w/ PEC	2	0x0020 (16V)	Yes
VIN_UV_WARN_LIMIT	58h	R/W w/ PEC	2	0x000C (3V)	Yes
TON_DELAY	60h	R/W w/ PEC	2	0x0000 (0ms)	Yes
TON_RISE	61h	R/W w/ PEC	2	0x0002 (4ms)	Yes
TOFF_DELAY	64h	R/W w/ PEC	2	0x0000 (0ms)	Yes
STATUS_BYTE	78h	R w/ PEC	1	-	-
STATUS_WORD	79h	R w/ PEC	2	-	-
STATUS_VOUT	7Ah	R w/PEC	1	-	-
STATUS_IOUT	7Bh	R w/ PEC	1	-	-
STATUS_INPUT	7Ch	R w/ PEC	1	-	-
STATUS_TEMPERATURE	7Dh	R w/ PEC	1	-	-
STATUS_CML	7Eh	R w/ PEC	1	-	-
READ_VIN	88h	R w/ PEC	2	-	-
READ_VOUT	8Bh	R w/ PEC	2	-	-
READ_IOUT	8Ch	R w/ PEC	2	-	-
READ_TEMPERATURE_1	8Dh	R w/ PEC	2	-	-

PMBus_REVISION	98h	R w/ PEC	1	0x33h, ASCII “13” (PMBus 1.3)	-
MFR_ID	99h	Block read w/ PEC	1 (byte) + 3 (data)	0x4D 0x50 0x53, ASCII”MPS”	Yes (9)
MFR_CTRL_COMP	D0h	R/W w/ PEC	1	0x0D	Yes
MFR_CTRL_VOUT	D1h	R/W w/ PEC	1	0x00	Yes
MFR_CTRL_OPS	D2h	R/W w/ PEC	1	0x05	Yes
MFR_ADDR_PMBUS	D3h	R/W w/ PEC	1	0x30	Yes
MFR_VOUT_OVP_FAULT_LIMIT	D4h	R/W w/ PEC	1	0x03	Yes
MFR_OVP_NOCP_SET	D5h	R/W w/ PEC	1	0x02	Yes
MFR_OT_OC_SET	D6h	R/W w/ PEC	1	0x09	Yes
MFR_OC_PHASE_LIMIT	D7h	R/W w/ PEC	1	0x06 (9A)	Yes
MFR_HICCUP_ITV_SET	D8h	R/W w/ PEC	1	0x00	Yes
MFR_PGOOD_ON_OFF	D9h	R/W w/ PEC	1	0x00	Yes
MFR_VOUT_STEP	DAh	R/W w/ PEC	1	0x04	Yes
MFR_LOW_POWER	E5h	R/W w/ PEC	1	0x00	Yes
MFR_CTRL	EAh	R/W w/ PEC	2	bit[9] = 0, bit[3] = 0	Yes

Note:

9) For manufactuer use only.

OPERATION (01h)

OPERATION is a paged register. The OPERATION command turns the converter output on/off in conjunction with input from the CTRL pin. It also sets the output voltage to the upper or lower margin voltages.

The device stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the CTRL pin instructs the converter to change to another mode. This OPERATION command also re-enables the converter after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown does not clear the fault registers.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Function							X	
Default	1	0	0	0	0	0	X	X

Bit[7:6]	Bit[5:4]	Bit[3:2]	Bit[1:0]	On/Off	Margin State	01h
00	XX	XX	XX	Immediate off	N/A	0x00
01	XX	XX	XX	Soft-off	N/A	0x40
10	00	XX	XX	On	Off	0x80
10	01	01	XX	On	Margin low (ignore fault)	0x94
10	01	10	XX	On	Margin low (act on fault)	0x98
10	10	01	XX	On	Margin high (ignore fault)	0xA4
10	10	10	XX	On	Margin high (act on fault)	0xA8

ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CTRL pin input and PMBus commands that turn the converter on and off. This includes how the converter responds when an input voltage is applied.

Command	ON_OFF_CONFIG							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R/W	R/W	R/W	R/W	R
Function	X			ON	OP	CTRL	POL_CTRL	DELAY
Default	0	0	0	1	1	1	1	0

on

The on bit indicates if the device starts up whenever an input voltage is present, or if starts up when commanded by the CTRL pin and PMBus.

Bit[4] Value	Description
0	The converter starts up any time the input voltage is present, regardless of state of the CTRL pin.
1	The converter does not start up until commanded by the CTRL pin and OPERATION command (as programmed in bit[3:0]).

op

The op bit controls how the converter responds to OPERATION commands.

Bit[3] Value	Description
0	The converter ignores the on bit from the OPERATION command.
1	The converter responds to the on bit from the OPERATION command.

ctrl

The ctrl bit controls how the converter responds to the CTRL pin.

Bit[2] Value	Description
0	The converter ignores the CTRL pin (on/off functionality is controlled only by the OPERATION command).
1	The converter does not start up until the CTRL pin is asserted. Based on the op bit (bit[3]), the OPERATION command may also be required to instruct the converter to start up.

pol_ctrl

This pol_ctrl bit sets the polarity of the CTRL pin.

Bit[1] Value	Description
0	Active low (pull the CTRL pin low to start the converter).
1	Active high (pull the CTRL pin high to start the converter).

delay

This delay bit sets the turn-off action when the converter is commanded to turn off. This bit is read-only and cannot be modified by the end user.

Bit[0] Value	Description
0	TOFF_DELAY, TOFF_FALL

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command resets all stored warnings and fault flags. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the ALT# signal may not be cleared, or it reasserts almost immediately. Issuing a CLEAR_FAULTS command does not force the converter to restart in the event of a fault-related shutdown. To restart the device, an OPERATION command must be issued after the fault condition is cleared. This command uses the PMBus to send byte protocols.

WRITE PROTECT (10h)

The WRITE_PROTECT command controls writing to the converter. This command helps prevent accidental changes, but it does not protect from deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bit[7:0] Value								Description
0	0	0	0	0	0	0	0	Enables writes to all commands.
0	0	1	0	0	0	0	0	Disables all writes except writes made to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands.
0	1	0	0	0	0	0	0	Disable all writes except writes made to the WRITE_PROTECT, OPERATION, and PAGE commands.
1	0	0	0	0	0	0	0	Disable all writes except writes made to the WRITE_PROTECT command.

To program the MTP when 10h is set to a value other than 0x00, use command 15h through MPS's GUI. The MTP programming command E7h cannot be used. See the MTP Programming section on page 31 for additional details on MTP programming.

The default value of 10h is 0x00.

STORE_USER_ALL (15h)

This command writes all the data from the registers to the internal MTPs. This process is initiated when the MPM3695-10 receives a STORE_USER_ALL command from the PMBus interface. The MPM3695-10 currently does not support the standard 15h command, but it can accept the 15h command from MPS's GUI. See the MTP Programming section on page 31 for additional details on MTP programming.

The following registers can be stored using STORE_USER_ALL:

OPERATION (01h)	TON_DELAY (60h)
ON_OFF_CONFIG (02h)	TON_RISE (61h)
WRITE_PROTECT (10h)	TOFF_DELAY (64h)
VOUT_COMMAND (21h)	MFR_CTRL_COMP (D0h)
VOUT_MAX (24h)	MFR_CTRL_VOUT (D1h)
VOUT_MARGIN_HIGH (25h)	MFR_CTRL_OPS (D2h)
VOUT_MARGIN_LOW (26h)	MFR_ADDR_PMBUS (D3h)
VOUT_SCALE_LOOP (29h)	MFR_VOUT_OVP_FAULT_LIMIT (D4h)
VOUT_MIN (2Bh)	MFR_OVP_NOCP_SET (D5h)
VIN_ON (35h)	MFR_OT_OC_SET (D6h)
VIN_OFF (36h)	MFR_OC_PHASE_LIMIT (D7h)
OT_FAULT_LIMIT (4Fh)	MFR_HICCUP_ITV_SET (D8h)
OT_WARN_LIMIT (51h)	MFR_PGOOD_ON_OFF (D9h)
VIN_OV_FAULT_LIMIT (55h)	MFR_VOUT_STEP (DAh)
VIN_OV_WARN_LIMIT (57h)	MFR_LOW_POWER (E5h)
VIN_UV_WARN_LIMIT (58h)	MFR_CTRL (EAh)

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the MPM3695-10 to copy the entire contents of the MTP values to the matching locations in the registers. The values in the registers are overwritten by the value retrieved from the MTP. Any items in the MTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be issued while the MPM3695-10 is operating. However, this is not recommended, and may cause the MPM3695-10 to become unresponsive. This command is write-only.

CAPABILITY (19h)

The CAPABILITY command returns information about the PMBus functions supported by the MPM3695-10. This command is read-only with the PMBus read byte protocol. The default value is 0xB0.

Command	CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	PEC	MAX BUS SPEED		ALERT	X			
Default	1	0	1	1	0	0	0	0
	PEC supported, max speed 1MHz, supports PMBus Alert and ARA							

Bit[6:5] Value		Description
0	0	Maximum supported bus speed is 100KHz.
0	1	Maximum supported bus speed is 400KHz.
1	0	Maximum supported bus speed is 1MHz.
1	1	Reserved.

VOUT_MODE (20h)

The VOUT_MODE command specifies the mode for reading and setting the output voltage. The 3 most significant bits determine the data format (only direct format is supported in the MPM3695-10), and the remaining 5 bits represent the exponent used in the output voltage read/write commands. The default value of 20h is 0x40.

VOUT_COMMAND (21h)

The VOUT_COMMAND sets the output voltage of the MPM3695-10. The VOUT_COMMAND and VOUT_SCALE_LOOP commands determine the feedback reference voltage with the following equation: VOUT_COMMAND x VOUT_SCALE_LOOP. The Output Voltage Setting section on page 21 shows additional details on how to set the output voltage.

Command	VOUT_COMMAND															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0

The value is unsigned and 1LSB = 2mV. The default value of 21h is 0x0258, which is 1.2V.

VOUT_MAX (24h)

The VOUT_MAX command sets an upper limit on the converter's output voltage, regardless of any other commands or combinations. This command provides a safeguard against accidentally setting the output voltage to a destructive level. It is not the primary output over-voltage protection (OVP) method.

Command	VOUT_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0

If an attempt is made to program the output voltage above the limit set by this command, the device responds as follows:

1. The commanded output voltage is set to VOUT_MAX
2. The VOUT bit is set in STATUS_WORD
3. The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register
4. The device notifies the host

The value is unsigned and 1LSB = 2mV. The maximum value of VOUT_MAX is 6V, and the default value is 6V, which means the default value of 24h is 0x0BB8h.

VOUT_MARGIN_HIGH (25h)

Command	VOUT_MARGIN_HIGH															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0

The value is unsigned and 1LSB = 2mV. The default value is 1.344V, which means the default value of 25h is 0x02A0.

VOUT_MARGIN_LOW (26h)

Command	VOUT_MARGIN_LOW															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0

The value is unsigned and 1LSB = 2mV. The default value is 1.02V, which means the default value of 26h is 0x01FE.

VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command sets the feedback resistor divider ratio, which is equal to V_{FB} / V_{OUT}. Regardless of whether an external or internal feedback resistor divider is used, VOUT_SCALE_LOOP should match the value of the feedback resistor divider.

Command	VOUT_SCALE_LOOP															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X						0.001/LSB									
Default	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0

The value is unsigned and 1LSB = 0.001. The default value is 0.5, which means the default value of 29h is 0x01F4.

VOUT_MIN (2Bh)

The VOUT_MIN command sets a lower limit on the output voltage, regardless of any other commands or combinations. This command provides a safeguard against accidentally setting the output voltage to a potentially destructive level. It is not the primary output under-voltage protection (UVP) method.

Command	VOUT_MIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X				2mV/LSB											
Default	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0

If an attempt is made to program the output voltage below the limit set by this command, the device responds as follows:

1. The commanded output voltage is set to VOUT_MIN
2. The VOUT bit is set in STATUS_WORD
3. The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register
4. The device notifies the host

The minimum value of VOUT_MIN is 0.5V. The value is unsigned and 1LSB = 2mV. The default value is 0.5V, which means the default value for 2Bh is 0x00FA.

VIN_ON (35h)

The VIN_ON command sets the value of the input voltage (in V) at which the converter should operate if all other start-up conditions are met. The VIN_ON value can be set between 4V and 15V, with 0.25V increments. The VIN_ON value should always exceed VIN_OFF with a high enough margin, that there is no bouncing between VIN_ON and VIN_OFF during power conversions.

Command	VIN_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										250mV/LSB					
Default	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

The value is unsigned and 1LSB = 250mV. The default value is 4V.

VIN_OFF (36h)

The VIN_OFF command sets the value of the input voltage (in V) at which the converter should stop power conversions once the device has begun operating. The VIN_OFF value can be set between 3V and 14.75V with 0.25V increments. VIN_OFF should be set below VIN_ON with enough margin, that there is no bouncing between VIN_OFF and VIN_ON during power conversions.

Command	VIN_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										250mV/LSB					
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

The value is unsigned and 1 LSB = 250mV. The default value is 2.75V.

OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command configures or reads the threshold for over-temperature (OT) fault detection. If the measured temperature exceeds this value, an OT fault is triggered. After OTP, the MPM3695-10 operates based on the setting in the auto bin from register MFR_CTRL (F0h).

OT fault flags are set in STATUS_BYTE (78h) and STATUS_WORD (79h), respectively, and the ALT# signal is asserted. After the temperature falls below the value in this register, the MOSFET may switch back on with the OPERATION command when the part works in latch-off mode. The minimum temperature fault detection time should be shorter than 20ms. The temperature range is between 0°C and 255°C.

When the temperature rises above this register value, an OT fault occurs. The part will automatically restart when the temperature drops OT_HYST. OT_HYST is set in register MFR_OT_OC_SET (D6h), and is 20°C by default.

Command	OT_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								1°C/LSB							
Default	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

The value is unsigned and 1LSB = 1°C. The default value is 00A0h. The corresponding value is 160°C. The OT_FAULT_LIMIT setting should be below 160°C. If the OT_FAULT_LIMIT value is set above 160°C, this register is ignored. The MPM3695-10 enters thermal shutdown when the junction temperature reaches 160°C.

Table 4 shows the relationship between direct and real-world values.

Table 4: Direct and Real-World Values for OT_FAULT_LIMIT

Direct Value	Real World Value (°C)
0000 0000	0
0000 0001	1
1111 1111	255

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command configures or reads the threshold for over-temperature (OT) warning detection. If the sensed temperature exceeds this value, an OT warning is triggered, and the OT warning flags are set in STATUS_BYTE (78h) and STATUS_WORD (79h), respectively. The ALT# signal is asserted. The minimum temperature warning detection time should be shorter than 20ms.

Command	OT_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								1°C/LSB							
Default	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

The value is unsigned and 1LSB = 1°C. The default value is 0x008Ch. The corresponding value is 140°C. OT_WARN_LIMIT should be set below 160°C. The relationship between direct and real-world values is the same as with OT_FAULT_LIMIT.

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command configures or reads the threshold for input over-voltage (OV) fault detection. If V_{IN} rises above the value in this register, V_{IN} OV fault flags are set in the respective registers, and the MPM3695-10 disables the power stage. When V_{IN} drops below VIN_OV_FAULT_LIMIT, the MPM3695-10 begins working again.

Command	VIN_OV_FAULT_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										500mV/LSB					
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0

The value is unsigned, and 1LSB = 500mV. The value for VIN_OV_FAULT_LIMIT should not be set above 18V.

VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command configures or reads the threshold for input over-voltage (OV) warning detection. If the measured value of V_{IN} rises above the value in this register, V_{IN} OV warning flags are set in the respective registers, and the ALT# signal is asserted.

Command	VIN_OV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										500mV/LSB					
Default	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

The value is unsigned and 1LSB = 500mV. The value for VIN_OV_WARN_LIMIT should not exceed 16V.

VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command configures or reads the threshold for input under-voltage (UV) fault detection. If V_{IN} falls below the value in this register, V_{IN} UV warning flags are set in the respective registers, and the ALT# signal is asserted.

Command	VIN_UV_WARN_LIMIT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Function	X										250mV/LSB					
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

The value is unsigned and 1LSB = 250mV. The default value is 0x0C. The corresponding value is 3V.

TON_DELAY (60h)

The TON_DELAY command sets the time (in ms) from when a start condition is received (as configured by the ON_OFF_CONFIG command) until the output voltage starts to rise.

Command	TON_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								4ms/LSB							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value is unsigned and 1LSB = 4ms. The maximum value is FFh (1020ms). The default value is 0ms.

TON_RISE (61h)

The TON_RISE command sets the soft-start time (in ms) from when the output starts to rise until the voltage has reached the regulation point.

Command	TON_RISE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W
Function	X													1ms/LSB		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

The only supported values are as follows:

- 3’b000: 1ms
- 3’b001: 2ms
- 3’b010: 4ms
- 3’b011: 8ms
- 3’b100 and up: 16ms

The default value is 0x02 (i.e. 4ms for soft-start time).

TOFF_DELAY (64h)

The TOFF_DELAY command sets the time (in ms) from when EN turns off to when the output starts to fall.

Command	TOFF_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X								4ms/LSB							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value is unsigned and 1LSB = 4ms. The maximum value is FFh (1020ms). The default value is 0ms.

STATUS_BYTE (78h)

The STATUS_BYTE command returns the value of a number of flags indicating the state of the MPM3695-10. Access to this command should use the read byte protocol. To clear bits in this register, the underlying fault should be removed, and a CLEAR_FAULTS command must be issued.

Bits	Bit Name	Behavior	Default	Description
[7]	RESERVED	-	0	Always read as 0.
[6]	OFF	Live	0	0: Part enabled 1: Part disabled from either V_{IN} under-voltage or over-voltage fault, and the OPERATION command to turn off has been received
[5]	VOUT_OV	-	0	An output over-voltage fault has occurred.
[4]	IOUT_OC_FAULT	Latched	0	0: No over-current fault detected 1: Over-current fault detected
[3]	VIN_UV	-	0	Not supported, always read as 0.
[2]	OT_FAULT_WARN	Live	0	0: No over-temperature warning or fault detected 1: Over-temperature warning or fault is detected
[1]	COMM_ERROR	Latched	0	0: No communication error detected 1: Communication error has been detected
[0]	NONE_OF_THE_ABOVE	Live	0	0: No faults or warnings have occurred 1: A fault or warning not listed in bits [7:1] has occurred

STATUS WORD (79h)

The STATUS_WORD command returns the value of a number of flags indicating the state of the MPM3695-10. To clear the bits in this register, the underlying fault should be removed, and a CLEAR_FAULTS command should be issued.

Bits	Bit Name	Behavior	Default	Description
[15]	VOUT_STATUS	Live	0	0: No output fault or warning 1: Output fault or warning
[14]	IOUT_STATUS	Live	0	0: No I_{OUT} fault 1: I_{OUT} fault
[13]	VIN_STATUS	Live	0	0: No V_{IN} fault 1: A V_{IN} fault has occurred. When V_{IN} starts up, the initial flag is 1 before V_{IN} passes the under-voltage lockout (UVLO) threshold. This fault clears once V_{IN} passes UVLO
[12]	MFR_STATUS	-	0	Always read as 0
[11]	POWER_GOOD#	Live	0	0: Power good signal is asserted 1: Power good signal is not asserted
[10]	RESERVED	-	0	Always read as 0.
[9]	RESERVED	-	0	Always read as 0.
[8]	UNKNOWN	Latched	0	0: No other fault type has occurred 1: A fault type not specified in bits [15:1] of STATUS_WORD has been detected
Low Byte	STATUS_BYTE	-		The same as STATUS_BYTE.

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns 1 data byte with the contents listed below.

Bits	Bit Name	Behavior	Default	Description
[7]	VOUT_OV_FAULT	Live	0	0: No output over-voltage (OV) fault 1: Output OV fault
[6]	RESERVED	Latched	0	Always read as 0.
[5]	RESERVED	Latched	0	Always read as 0.
[4]	VOUT_UV_FAULT	Live	0	0: No output UV fault 1: Output UV fault
[3]	VOUT_MAX_MIN	Live	0	0: No VOUT_MAX or VOUT_MIN warning 1: An attempt has been made to set the output voltage to a value above the limit set by the VOUT_MAX command or below the limit set by the VOUT_MIN command
[2]	RESERVED	-	0	Always read as 0.
[1]	RESERVED	-	0	Always read as 0.
[0]	UNKNOWN	Latched	0	0: No other fault type has been detected 1: A fault type not specified in bits [15:1] of STATUS_WORD has been detected

STATUS_IOUT (7Bh)

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	IOUT_OC	IOUT_OC and VOUT_UV	IOUT_OC_WARNING	X				
Default	0	0	0	0	0	0	0	0

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns the value of flags that indicate the status of the MPM3695-10's input voltage. To clear the bits in this register, the underlying fault or warning should be removed, and a CLEAR_FAULTS command should be issued.

Bits	Name	Behavior	Default	Description
[7]	VIN_OV_FAULT	Latched	0	0: The OV pin does not detect an over-voltage (OV) condition 1: The OV pin detects an OV condition
[6]	VIN_OV_WARN	Latched	0	0: An over-voltage (OV) condition on V_{IN} has not occurred 1: An OV condition on V_{IN} has occurred
[5]	VIN_UV_WARN	Latched	0	0: An under-voltage (UV) condition on V_{IN} has not occurred 1: A UV condition on V_{IN} has occurred
[4:0]	RESERVED	-	0	Always read as 0000.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns the value of flags indicating the over-temperature fault or over-temperature waring of the MPM3695-10. To clear bits in this register, the underlying fault should be removed and a CLEAR_FAULTS command issued.

Bits	Name	Behavior	Default	Description
[7]	OT_FAULT	Latched	0	1: An over-temperature fault has occurred
[6]	OT_WARNING	Latched	0	1: An over-temperature warning has occurred
[5:0]	RESERVED	-	0	Always read as 0

STATUS_ CML (7Eh)

Command	STATUS_CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	Invalid or unsupported command	Invalid or unsupported data		Memory fault detected	X	X	Other fault	Memory busy
Default	0	0	0	0	0	0	0	0

READ_VIN (88h)

The READ_VIN command returns the 10-bit measured value of the input voltage.

Command	READ_VIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X						25mV/LSB									
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_VOUT (8Bh)

The READ_VOUT command returns the 10-bit measured value of the output voltage.

Command	READ_VOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X			1.25mV/LSB												
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_IOUT (8Ch)

The READ_IOUT command returns the 10-bit measured value of the output current.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	X		62.5mA/LSB													
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns the internal sensed temperature. This value is also used internally for over-temperature fault and warning detection. This data has a range between -255°C and +255°C.

Command	READ_TEMPERATURE_1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	X						Sign	1°C/LSB								
Default	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

READ_TEMPERATURE_1 is a 2-byte, twos complement integer. The sign bit is bit[9]. Table 5 shows the relationship between direct and real-world values.

Table 5: Direct and Real-World Values for READ_TEMPERATURE_1

Sign	Direct Value	Real World Value (°C)
0	0 0000 0000	0
0	0 0000 0001	1
0	1 1111 1111	+511
1	0 0000 0001	-511
1	1 1111 1111	-1

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the protocol revision. Accesses to this command should use the read byte protocol. Bits [7:4] indicate the PMBus revision of Part I to which the device is compliant. Bits [3:0] indicate the revision of specification Part II to which the device is compliant.

Command	PMBUS_REVISION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Default	0	0	1	1	0	0	1	1

Bits [7:4] always reads as 4’b0011, specification PMBus Part I Revison 1.3.
Bits [3:0] always reads as 4’b0011, specification PMBus Part II Revison 1.3.

MFR_ID (99h)

The MFR_ID command returns the company identification.

Byte	Byte Name	Value	Description
0	Byte Count	0x03	Always reads as 0x03, the number of data bytes that the block read command expects to read.
1	Character 1	0x4D, ASCII of “M”	Always reads as 0x4D.
2	Character 2	0x50, ASCII of “P”	Always reads as 0x50.

3	Character 3	0x53, ASCII of “S”	Always reads as 0x53.

MFR_CTRL_COMP (D0h)

The MFR_CTRL_COMP command adjusts the loop compensation.

Bits	Name	Access	Behavior	Default	Description
[7:5]	RESERVED	R/W	Live	000	
[4]	CFF	R/W	Live	0	Sets the feed-forward capacitance when the internal feedback resistor divider is selected. 0: 20pF 1: 50pF
[3:1]	RAMP	R/W	Live	110	Sets the internal ramp compensation to stabilize the loop. Ensure that the actual ramp amplitude is related to the selection of register bit of EAh[3]. See register EAh on page X for details.
[0]	SLAVE FAULT DETECTION	R/W	Live	1	Enables or disables the slave fault detection function through the PG pin. 0: Slave-phase fault detection is enabled 1: Slave-phase fault detection is disabled

EAh[3] = 0 (Single-Phase)	EAh[3] = 1 (Multi-Phase)
000: 5.6mV ramp	000: 8.6mV ramp
001: 9.8mV ramp	001: 15mV ramp
010: 18mV ramp	010: 27mV ramp
011: 30mV ramp	011: 45mV ramp
100: 8.5mV ramp	100: 13mV ramp
101: 15.1mV ramp	101: 23mV ramp
110: 27mV ramp	110: 41mV ramp
111: 44mV ramp	111: 68mV ramp

The default value of D0h is 0x0D.

MFR_CTRL_VOUT (D1h)

The MFR_CTRL_VOUT command adjusts the output voltage behaviors of the MPM3695-10.

Bits	Bit Name	Access	Behavior	Default	Description
[7]	RESERVED	R/W	Live	0	Reserved.
[6]	VO DISCHARGE	R/W	Live	0	Enables or disables active output voltage discharging when the MPM3695-10 is commanded off through the CTRL pin or OPERATION command. 1: Active output voltage discharging when CTRL is low 0: No active output voltage discharging
[5:2]	PG DELAY	R/W	Live	0000	Sets the PG pull-high time after soft start finishes. 0000:1ms 0001: 2ms …… 1111: 0ms
[1:0]	VO_RANGE	R/W	Live	00	00: External voltage divider 01: Internal voltage divider: V_{REF} / V_O = 0.4V to 1.344V 10: Internal voltage divider: V_{REF} / V_O = 0.7V to 2.688V 11: Internal voltage divider: V_{REF} / V_O = 1.3V to 5.376V

MFR_CTRL_OPS (D2h)

The MFR_CTRL_OPS command sets the switching frequency and light-load operation mode. The default value of D2h is 0x05.

Bits	Name	Access	Behavior	Default	Description
[7:3]	RESERVED	-	-	00000	
[2:1]	SWITCHING_FREQUENCY	R/W	Live	10	00: Set f_{SW} to 400kHz 01: Set f_{SW} to 600kHz 10: Set f_{SW} to 800kHz 11: Set f_{SW} to 1000khz
[0]	SKIP_CCM (SYNC)	R/W	Live	1	0: Pulse skip mode at light load. 1: Forced CCM at light load.

MFR_ADDR_PMBUS (D3h)

PMBus address setting register.

Command	MFR_ADDR_PMBUS							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Enable	ADDR						
Default	0	0	1	1	0	0	0	0

Bits	Bit Name	Access	Behavior	Default	Description
[7]	Enable	R/W	-	0x30	Enable bit. 0: The address is determined by MFR_ADDR_PMBUS [6:0] 1: The address is determined by the ADDR pin

The default value of D3h is 0x30.

MFR_VOUT_OVP_FAULT_LIMIT (D4h)

This MFR_VOUT_OVP_FAULT_LIMIT command sets the exit and entry thresholds for over-voltage protection (OVP).

Bits	Bit Name	Access	Behavior	Default	Description
[7:4]	RESERVED	-	-	0000	Reserved.
[3:2]	OV_EXIT_TH	R/W	Live	00	Sets the over-voltage protection (OVP) exit threshold. 00: 10% of V_{REF} 01: 50% of V_{REF} 10: 80% of V_{REF} 11: 102.5% of V_{REF}
[1:0]	OV_ENTRY_TH	R/W	Live	0011	Sets the over-voltage protection (OVP) entry threshold. 00: 115% of V_{REF} 01: 120% of V_{REF} 10: 125% of V_{REF} 11: 130% of V_{REF}

The default value of D4h is 0x03.

MFR_OVP_NOCP_SET (D5h)

This MFR_OVP_SET command sets the response to output over-voltage protection (OVP).

Bits	Name	Access	Behavior	Default	Description
[7:4]	RESERVED	-	-	0000	
[3]	DELAY_NOCP (D400)	R/W	Live	0	0: 100ns delay after negative over-current protection (NOCP) 1: 200ns delay after NOCP
[2]	NOCP	R/W	Live	0	0: Set NOCP to -10A. 1: Set NOCP to -15A.
[1:0]	VOUT_OV_RESPONSE	R/W	Live	10	00: Latch-off with output voltage discharge 01: Latch-off without output voltage discharge when in DCM 10: Hiccup with output voltage discharge 11: Hiccup without output voltage discharge when in DCM

Bit[1:0] of MFR_OVP_NOCP_SET determines how the converter responds during an output over-voltage fault. The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE command
- Sets the VOUT bit in the STATUS_WORD command
- Sets the VOUT Overvoltage Fault bit in the STATUS_VOUT command
- Notifies the host by asserting the ALERT pin

There are four potential responses to an output over-voltage fault. They are designated through bit[1:0] of MFR_VOUT_OVP_NOCP_SET, and described below:

1. Latch off with output discharge: Once the device reaches the over-voltage (OV) entry threshold, the LS-FET turns on until it reaches NOCP. Then LS-FET turns off for a fixed time before turning on again. The operation repeats until V_{FB} drops below the OVP exit threshold set by register D4[3:2], and then the LS-FET turns off. If V_{FB} exceeds the OV entry threshold again, the LS-FET turns on to discharge the output voltage. After the second fault, the device does not restart until power is cycled on either VIN, VCC, or CTRL.

2. Latch off without output discharge (only effective in DCM): Once the device reaches the over-voltage (OV) entry threshold, the LS-FET turns on. When the inductor current reaches zero, the converter enters Hi-Z (output disabled). The converter stops discharging the output voltage. The converter will not attempt to restart until power is cycled on either VIN, VCC, or CTRL.

3. Hiccup with output discharge: Once the device reaches the over-voltage (OV) entry threshold, the LS-FET turns on until it reaches NOCP. Then LS-FET turns off for a fixed time before turning on again. It repeats this operation until V_{FB} drops below the OVP exit threshold set by register D4[3:2]; then the LSFET turns off. A new SS is then initiated.

4. Hiccup without output discharge: Once the device reaches the over-voltage (OV) entry threshold, the LS-FET turns on until it reaches NOCP, then it initiates a new SS.

The default value of D5h is 0x02.

MFR_OT_OC_SET (D6h)

This MFR_OT_OC_SET command determines how the device responds to over-current protection (OCP) as well as the responses and hysteresis for over-temperature protection (OTP). It is a 1-byte command.

Bits	Bit Name	Access	Behavior	Default	Description
[7:4]	RESERVED	-	-	0000	
[3]	OC_RESPONSE	R/W	Live	1	Sets the over-current protection (OCP) response. 0: Latch off, never retry 1: Retry
[2:1]	OT_HYST	R/W	Live	00	00: 20°C 01: 25°C 10: 30°C 11: 35°C
[0]	OT_RESPONSE	R/W	Live	1	Sets the over-temperature protection (OTP) response. 0: Latch-off, never retry 1:Retry after the temp drops by the value set by bits [2:1]

The default value of D6h is 0x09.

MFR_OC_PHASE_SET (D7h)

This MFR_OC_PHASE_SET command sets the inductor valley current limit of each individual phase. This is a cycle-by-cycle current limit. After 31 consecutive cycles of an over-current (OC) condition, it triggers OCP. It's a 1-byte command.

Bits	Bit Name	Access	Behavior	Default	Description
[7:5]	RESERVED	-	-	000	Reserved.
[4:0]	OC_LIMIT	R/W	Live	00110	Current limit. 1.5A/LSB [00000] = 0A.

The value is unsigned and 1LSB = 1.5A. The default inductor valley current limit is 9A.

When EAh[10] is set to 0, or when reaches inductor valley current limit set by MFR_OC_PHASE_LIMIT, the OCP hiccup time is about 5 times of the soft-start time set by TON_RISE (61h).

MFR_UVP_PGOOD_ON_LIMIT (D9h)

This MFR_UVP_PGOOD_ON_LIMIT command sets the thresholds under-voltage protection (UVP) and PG on.

Bits	Bit Name	Access	Behavior	Default	Description
[7:4]	RESERVED	-	-	0000	Reserved.
[3:2]	UV_TH	R/W	Live	00	Sets the under-voltage protection (UVP) threshold. When V_{FB} drops below the UV_TH level, it enters UVP. The response for UVP is the same as for over-current protection (OCP). 00: 69% of V_{REF} 01: 74% of V_{REF} 10: 79% of V_{REF} 11: 84% of V_{REF}

[1:0]	PG_ON	R/W	Live	00	Sets the FB threshold at which the PG is pulled high during soft start. Once FB reaches the threshold, PG is pulled high after the delay set by D1[5:2]. 00: 90% of V_{REF} 01: 92.5% of V_{REF} 10: 95% of V_{REF} 11: 97.5% of V_{REF}

PG pulls low for any fault condition. The default value of D9h is 0x00.

MFR_VOUT _STEP (DAh)

This MFR_VOUT_STEP command sets the output voltage transition slew rate after soft start finishes. It does not determine the output voltage transition slew rate during soft start.

Bits	Bit Name	Access	Behavior	Default	Description
[7:4]	RESERVED	-	-	0000	Reserved.
[3:0]	VOUT_STEP	R/W	Live	0100	0000 = 20µs/2mV 1LSB = 2.5µs/2mV

The default value of DAh is 0x04.

MFR_LOW _POWER (E5h)

This MFR_LOW_POWER is used to enable/disable the slave phase(s) in multi-phase configuration.

Bits	Bit Name	Access	Behavior	Default	Description
[7:2]	RESERVED	-	-	000000	Reserved.
[1]	LP_PS#	R/W	Live	0	0: Low power mode is disabled regardless of PS# 1: Low power mode is enabled when PS# is low, and is disabled when PS# is high
[0]	LP_PMBUS	R/W	Live	0	0: Low power mode is disabled 1: Low power mode is enabled

The slave phase(s) can be enabled/disabled directly through bit[0], and when bit[1] is set to 1. The master phase cannot be disabled through MFR_LOW_POWER. The default value of E5h is 0x00.

MFR_CTRL (EAh)

The MFR_CTRL command enables and disables certain functions.

Bits	Bit Name	Access	Behavior	Default	Description
[15:10]	RESERVED	R	Live	-	For manufacturer use only.
[9]	OSM	R/W	Live	0	0: Enable output sinking mode (OSM) 1: Disable OSM
[8:4]	RESERVED	R	Live	-	For manufacturer use only.
[3]	PHASE_OPERATION	R/W	Live	-	0: For single-phase operation 1: For multi-phase operation
[2:0]	RESERVED	R	Live	-	For manufacturer use only.

Only bit[9] and bit[3] are accessible; all other bits are for manufacturer use only. The selection for bit[3] affects the actual RAMP amplitude determined by register D0h[3:1]. See MFR_CTRL_COMP (D0h) on page 45 for more details.

MTP CONFIGURATION

Table 6: 0022 Suffix Code Configuration

Configure Code	0022
Output Voltage	1.2V
Frequency	800kHz
Mode	Forced CCM
V_{IN} UVLO	4V
Ramp	27mV
V_{IN} OV	18V
V_{OUT} OV	V_{FB} x 130%
V_{OUT} UV	V_{FB} x 50%
Over-Temperature Protection	160°C
Inductor Valley Current Limit	9A
VOUT_STEP	30.2µs/2mV
Address	0x30

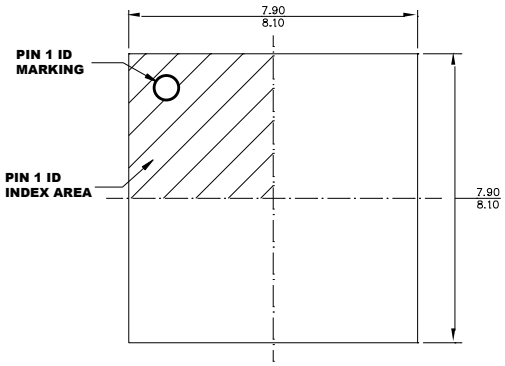
MTP CONFIGURATION *(continued)*

Table 7: 0022 Suffix Code Register Value

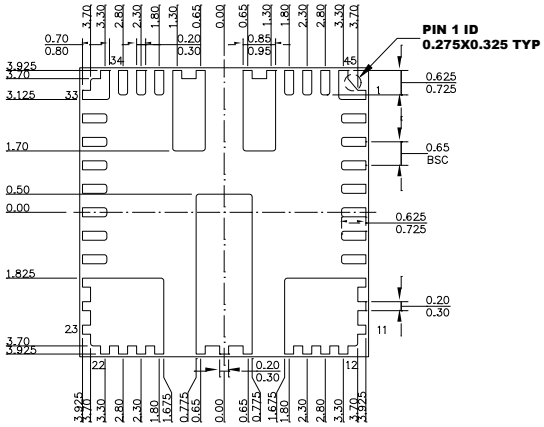
Suffix Code	Register	Hex Value
0022	0x01	80h
0022	0x02	1Eh
0022	0x10	00h
0022	0x21	0258h
0022	0x24	0BB8h
0022	0x25	02A0h
0022	0x26	01FEh
0022	0x29	01F4h
0022	0x2B	00FAh
0022	0x35	0010h
0022	0x36	000Bh
0022	0x46	0FFBh
0022	0x4A	0FFBh
0022	0x4F	00A0h
0022	0x51	008Ch
0022	0x55	0024h
0022	0x57	0020h
0022	0x58	000Ch
0022	0x60	0000h
0022	0x61	0002h
0022	0x64	0000h
0022	0xD0	0Dh
0022	0xD1	00h
0022	0xD2	05h
0022	0xD3	30h
0022	0xD4	03h
0022	0xD5	02h
0022	0xD6	09h
0022	0xD7	06h
0022	0xD8	00h
0022	0xD9	00h
0022	0xDA	04h

PACKAGE INFORMATION

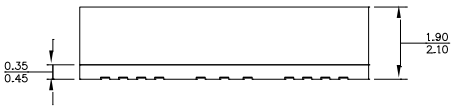
LGA-45 (8mmx8mmx2mm)



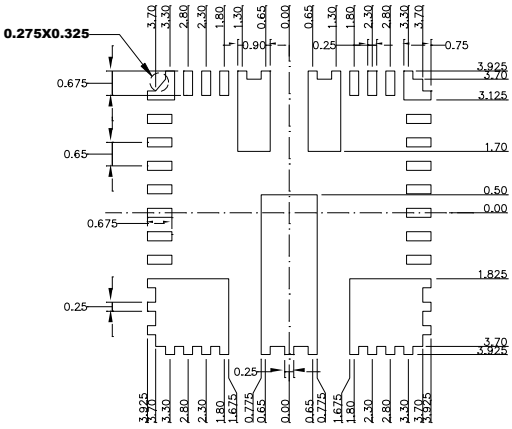
TOP VIEW



BOTTOM VIEW



SIDE VIEW

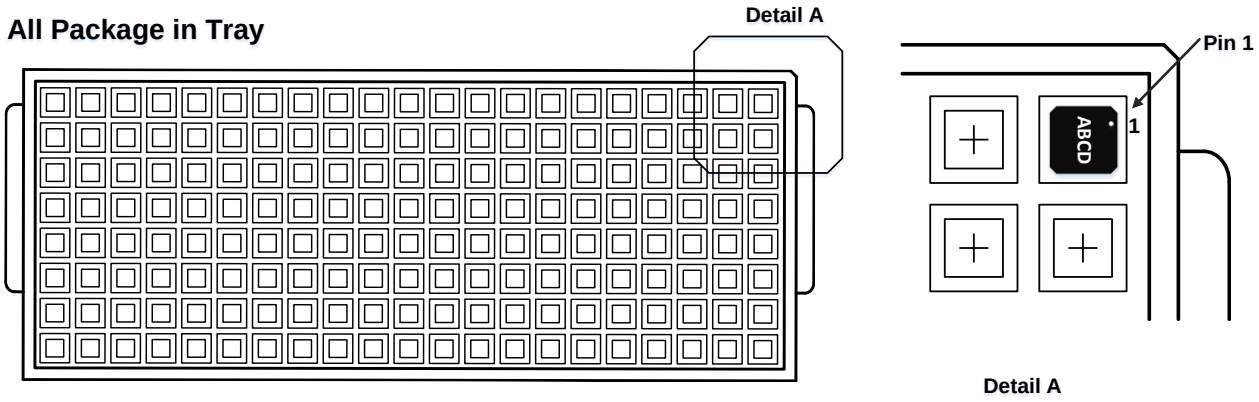


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Note:

10) This is a schematic diagram of a tray. Different packages correspond to different trays, with different lengths, widths, and heights.

Part Number	Package Description	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3695GMQ-10-xxxx	LGA-45 (8mmx8mmx2mm)	N/A	250	N/A	N/A	N/A