MPM3650C

2.75 to 17V, 6A, 1.2MHz, Ultra-Thin, Synchronous, Step-Down Power Module with Forced Continuous Conduction Mode

DESCRIPTION

The MPM3650C is a fully integrated high-frequency, synchronous, rectified, step-down power module with an internal inductor. It offers a highly compact solution to achieve 6A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range, with excellent load and line regulation. The MPM3650C offers synchronous mode for high efficiency across the entire output current load range.

Constant-on-time (COT) control provides fast transient response, easy loop design, and tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MPM3650C requires a minimal number of readily available, standard external components, and is available in a space-saving QFN-24 (4mmx6mm) package.

FEATURES

- Wide 2.75V to 17V Operating Input Voltage (V_{IN}) Range
- Output Current (I_{OUT}):
  - 0.6V to 1.8V, 6A I_{OUT}
  - 1.8V to 3.3V, 5A I_{OUT}
- Internal Power MOSFETs
- Adjustable Output from 0.6V
- High-Efficiency Synchronous Mode
- Forced Continuous Conduction Mode (FCCM) for Low Output Voltage Ripple
- Supports Pre-Biased Start-Up
- 1200kHz Fixed Switching Frequency (f_{SW})
- Configurable External Soft-Start Time (t_{SS})
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) with Hiccup Mode
- Available in a QFN-24 (4mmx6mmx1.6mm) package

APPLICATIONS

- Field-Programmable Gate Array (FPGA) Power Systems
- Optical Modules
- Telecommunications
- Networking
- Industrial Equipment

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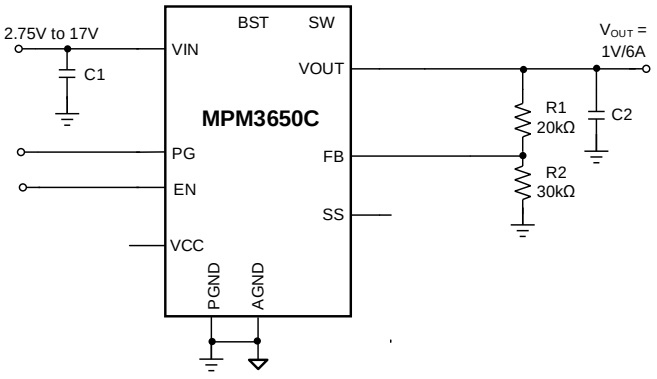
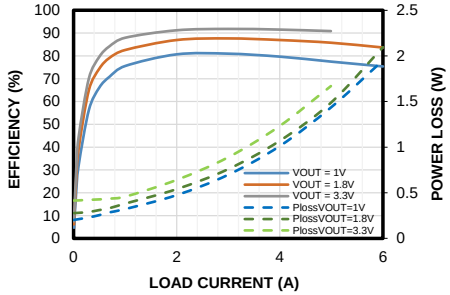
TYPICAL APPLICATION



Efficiency vs. Load Current vs. Power Loss

V_{IN} = 12V



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3650CGQW	QFN-24 (4mmx6mmx1.6mm)	*See Below*	3

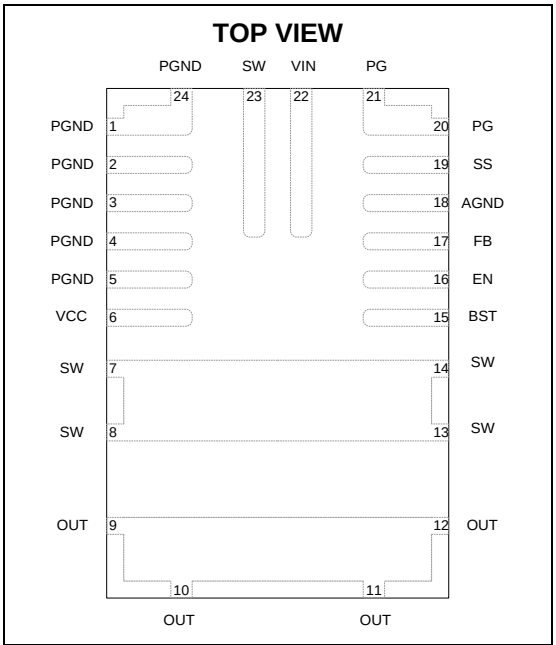
* For Tape & Reel, add suffix -Z (e.g. MPM3650CGQW-Z).

TOP MARKING

MPSYWW
M3650C
LLLLLL
M

MPS: MPS prefix
Y: Year code
WW: Week code
M3650C: Part number
LLLLLL: Lot number
M: Module

PACKAGE REFERENCE



QFN-24 (4mmx6mmx1.6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 4, 5, 24	PGND	**System ground.** The PGND pin is the regulated output voltage's (V_{OUT}'s) reference ground. Careful consideration must be taken when designing the PCB layout. Connect PGND to ground with multiple copper pours and vias.
6	VCC	**Internal bias supply output.**
7, 8, 13, 14, 23	SW	**Switch output.** Float the SW pins.
9, 10, 11, 12	OUT	**Output pin.** Connect the OUT pin to the output capacitor (C_{OUT}).
15	BST	**Bootstrap.** Float the BST pin.
16	EN	**Enable.** Pull the EN pin high to turn the part on; float EN to turn it off. EN is pulled to AGND via an internal 1.2MΩ pull-down resistor (R_{EN_PD}).
17	FB	**Feedback.** To set V_{OUT}, connect the FB pin to the tap of an external resistor divider connected between the output and AGND.
18	AGND	**Signal ground.** The AGND pin is not connected internally to the system ground. When designing the PCB layout, ensure that AGND is connected to the system ground.
19	SS	**Soft start.** Connect a capacitor between the SS pin and AGND to set the soft-start time (t_{SS}) and to avoid start-up inrush current. SS has an internal 22nF capacitor (C_{SS}).
20, 21	PG	**Power good output.** The PG pin is an open-drain output. PG's state changes if one of the following protections is triggered: under-voltage protection (UVP), over-current protection (OCP), or over-temperature protection (OTP). PG's state also changes if an over-voltage (OV) condition occurs.
22	VIN	**Supply voltage.** The MPM3650 operates from a 2.75V to 17V input rail. Use a 0.1µF input capacitor (C_{IN}) in a 0402 package to decouple the input rail. Use wide PCB traces to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +20V
V_{SW}.....
- 0.3V (-5V < 10ns) to V_{IN} + 0.7V (23V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} ..... V_{IN}
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2)
..... 3.816W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +125°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM).....2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.75V to 17V
Output voltage (V_{OUT})..... 0.6V to 3.3V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVM3650C-QW-00A (4)……32.75...10.217 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation on EVM3650C-QW-00A board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVM3650C-QW-00A, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C (5), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage	V_{IN}		2.75		17	V
Supply Current						
Shutdown current	I_{SD}	V_{EN} = 0V		2	5	µA
Quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	µA
MOSFET						
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SW} = 7V			5	µA
Current Limit						
Valley current limit	I_{LIMIT_VALLEY}		6	7		A
Short hiccup duty cycle (6)	D_{HICCUP}			10		%
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}		0.9	1.2	1.6	MHz
Minimum on time (6)	t_{ON_MIN}			50		ns
Minimum off time (6)	t_{OFF_MIN}			100		ns
Reference and Soft Start (SS)						
Feedback (FB) voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
FB current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	µA
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.19	1.23	1.27	V
EN falling threshold	$V_{EN_FALLING}$		0.96	1	1.04	V
EN pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC UVLO rising threshold	$V_{CC_UVLO_RISING}$		2.4	2.5	2.6	V
VCC UVLO threshold hysteresis	$V_{CC_UVLO_HYS}$			200		mV
VCC regulator voltage	V_{CC}	V_{IN} = 5V		3.5		V
VCC load regulation	REG_{VCC}	I_{CC} = 5mA		3		%
Power Good (PG)						
PG under-voltage (UV) rising threshold	$V_{PG_UV_RISING}$		0.85	0.9	0.95	V_{FB}
PG UV falling threshold	$V_{PG_UV_FALLING}$		0.75	0.8	0.85	V_{FB}
PG over-voltage (OV) rising threshold	$V_{PG_OV_RISING}$		1.15	1.2	1.25	V_{FB}
PG OV falling threshold	$V_{PG_OV_FALLING}$		1.05	1.1	1.15	V_{FB}
PG delay	t_{DELAY_PG}	Both edges		50		µs
PG sink current capability	V_{PG_SINK}	4mA sink			0.4	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown (6)	T_{SD}			150		°C
Thermal hysteresis (6)	T_{SD_HYS}			20		°C

Notes:

5) Not tested in production. Guaranteed by over-temperature correlation.
6) Guaranteed by design and characterization testing.

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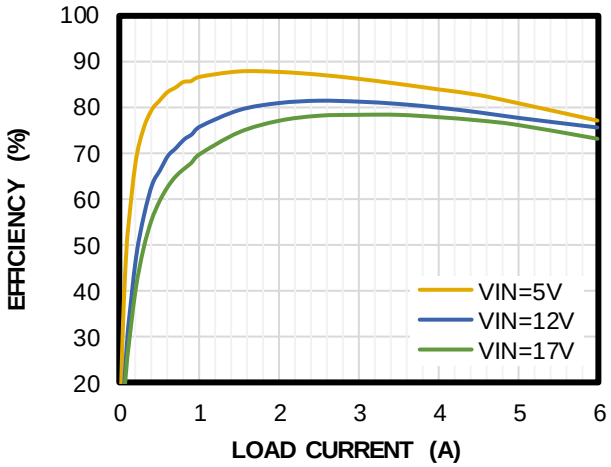
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

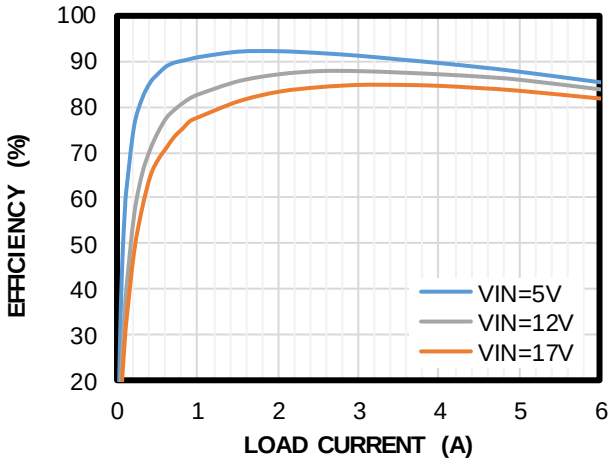
Efficiency vs. Load Current

V_{OUT} = 1V



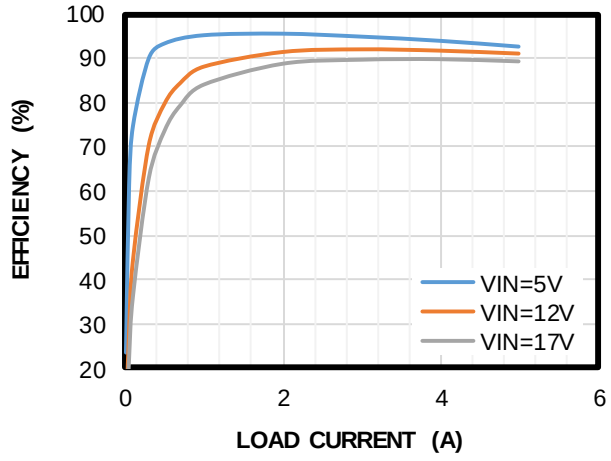
Efficiency vs. Load Current

V_{OUT} = 1.8V



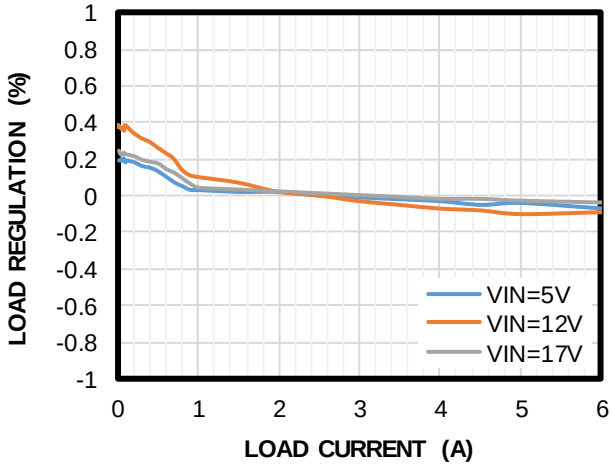
Efficiency vs. Load Current

V_{OUT} = 3.3V



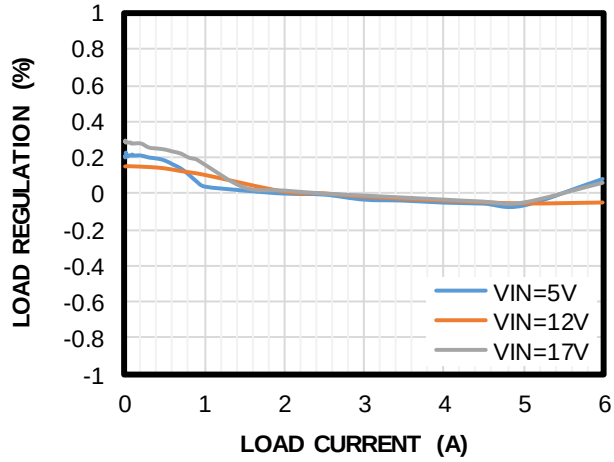
Load Regulation

V_{OUT} = 1V



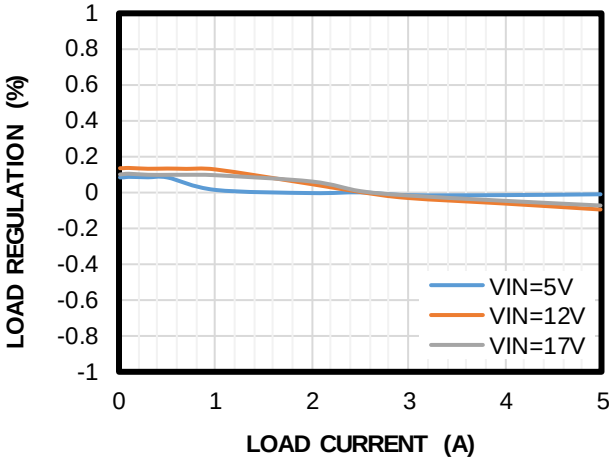
Load Regulation

V_{OUT} = 1.8V



Load Regulation

V_{OUT} = 3.3V



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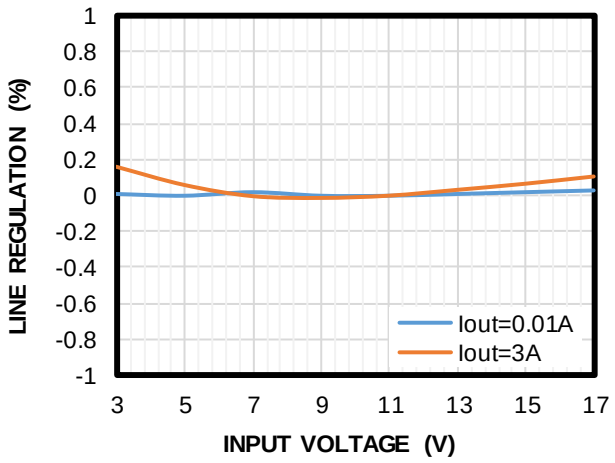
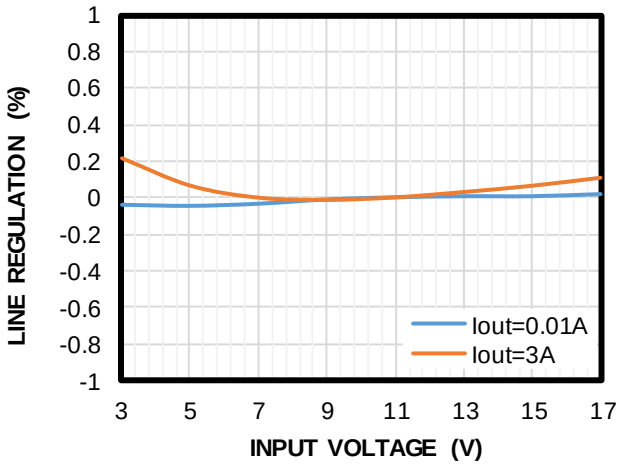
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

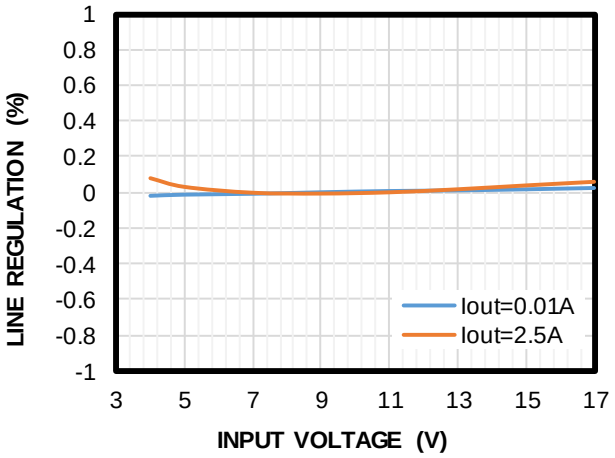
Line Regulation
V_{OUT} = 1V



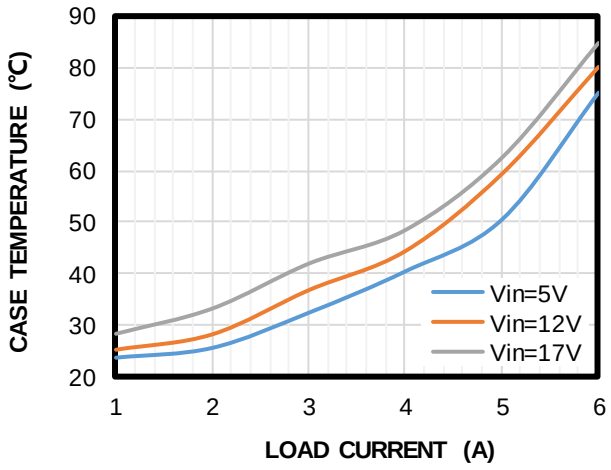
Line Regulation
V_{OUT} = 1.8V



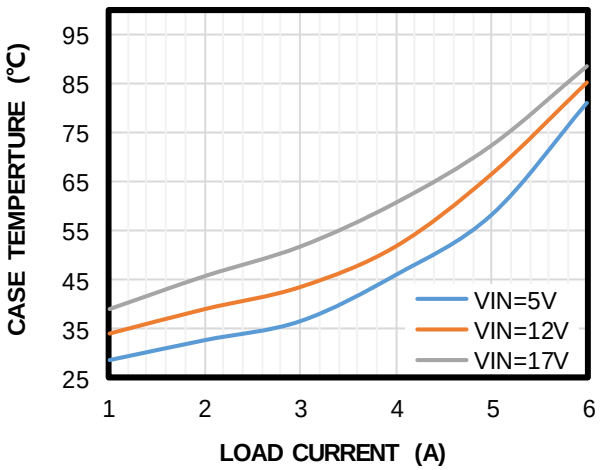
Line Regulation
V_{OUT} = 3.3V



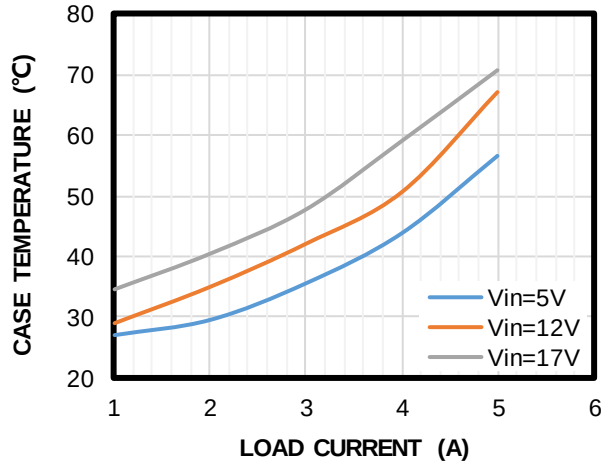
Case Temperature vs. Load Current
V_{OUT} = 1V, T_A = 15°C



Case Temperature vs. Load Current
V_{OUT} = 1.8V, T_A = 15°C



Case Temperature vs. Load Current
V_{OUT} = 3.3V, T_A = 15°C



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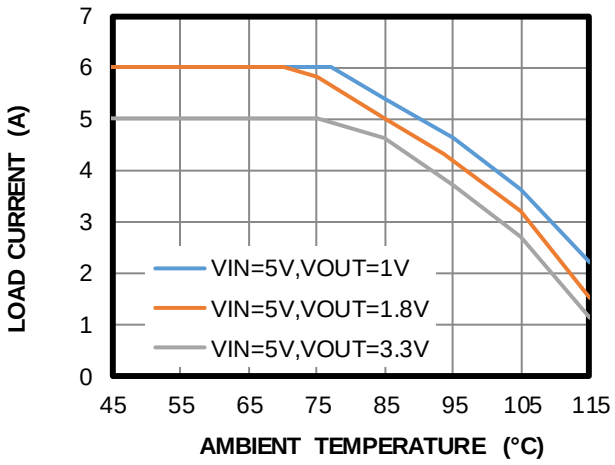
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

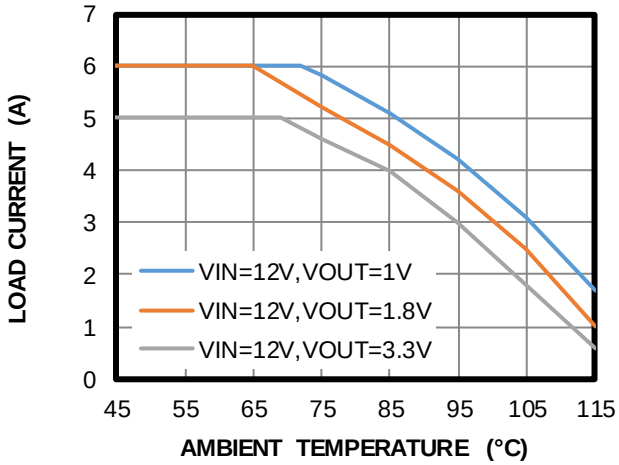
Thermal Derating

V_{IN} = 5V, no airflow



Thermal Derating

V_{IN} = 12V, no airflow



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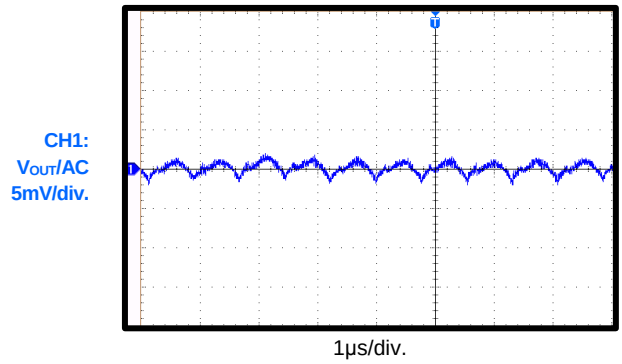
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

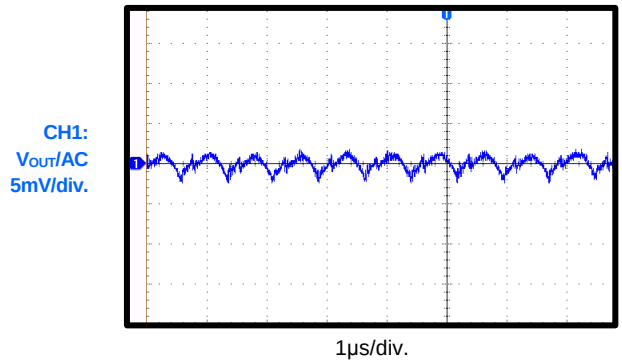
V_{OUT} Ripple

I_{OUT} = 0A



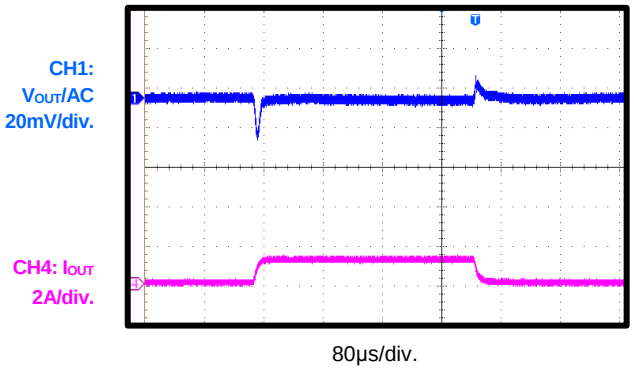
V_{OUT} Ripple

I_{OUT} = 6A



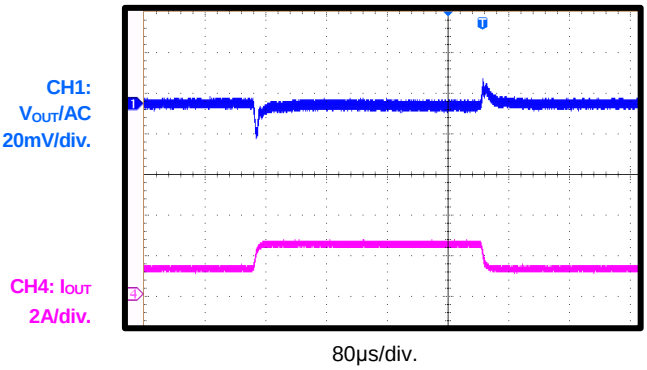
Load Transient

I_{OUT} = 0A to 3A



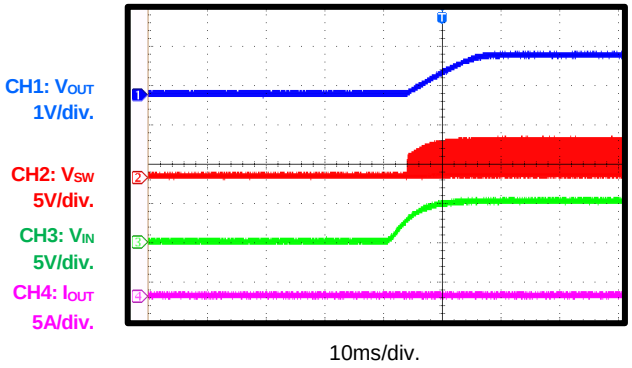
Load Transient

I_{OUT} = 3A to 6A



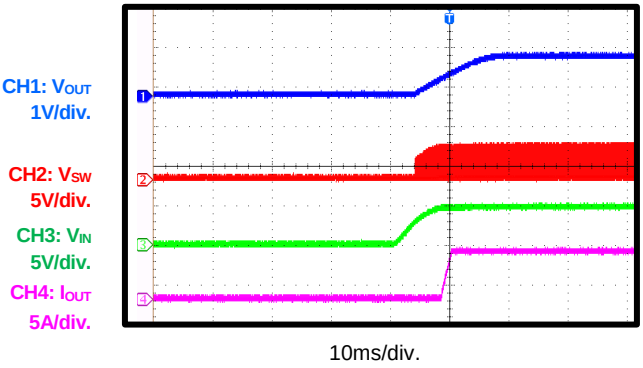
Start-Up through VIN

I_{OUT} = 0A



Start-Up through VIN

I_{OUT} = 6A



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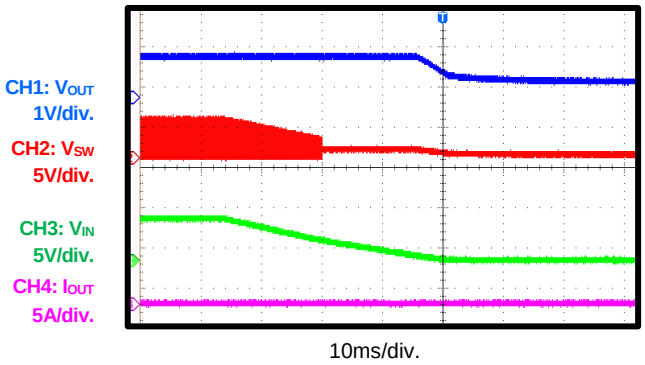
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

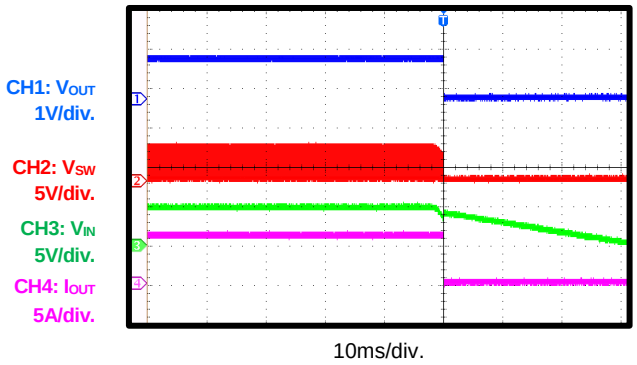
Shutdown through VIN

I_{OUT} = 0A



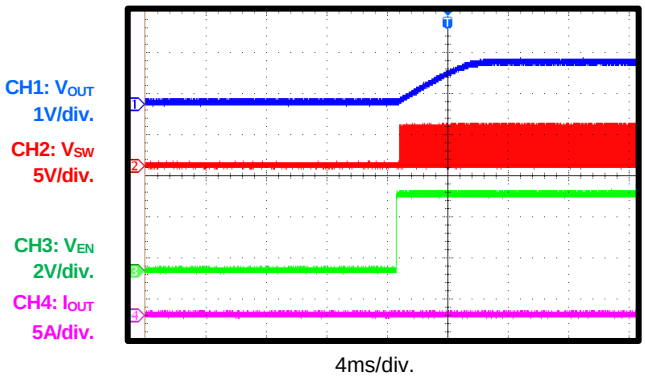
Shutdown through VIN

I_{OUT} = 6A



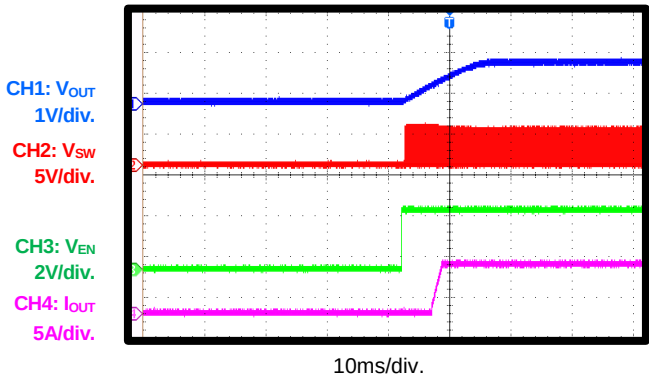
Start-Up through EN

I_{OUT} = 0A



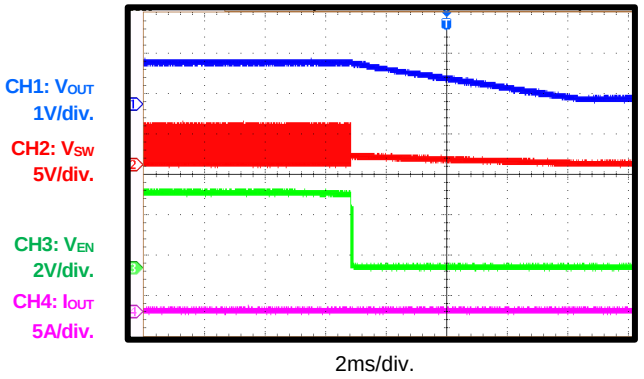
Start-Up through EN

I_{OUT} = 6A



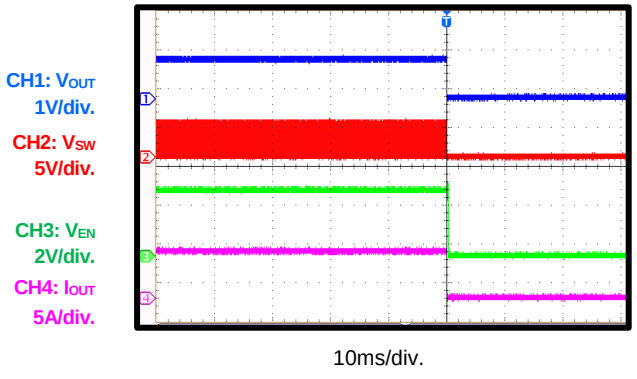
Shutdown through EN

I_{OUT} = 0A



Shutdown through EN

I_{OUT} = 6A



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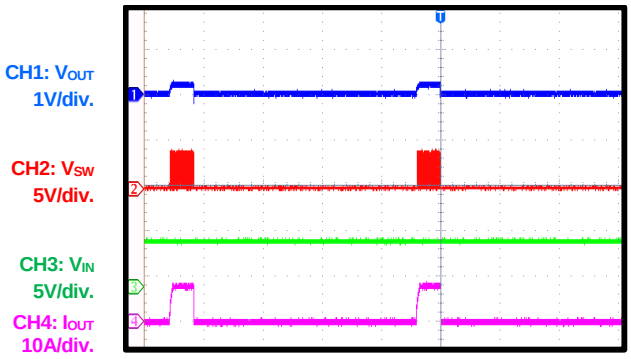
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

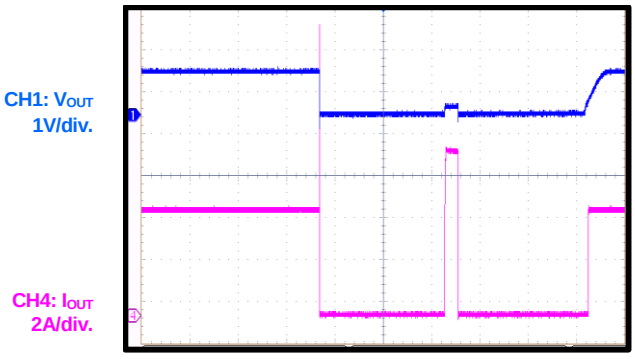
V_{IN} = 5V, V_{OUT} = 1V, C_{OUT} = 4x22µF, f_{SW} = 1200kHz, T_A = 25°C, unless otherwise noted.

Steady State



20ms/div.

SCP Entry and Recovery



200ms/div.

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FUNCTIONAL BLOCK DIAGRAM

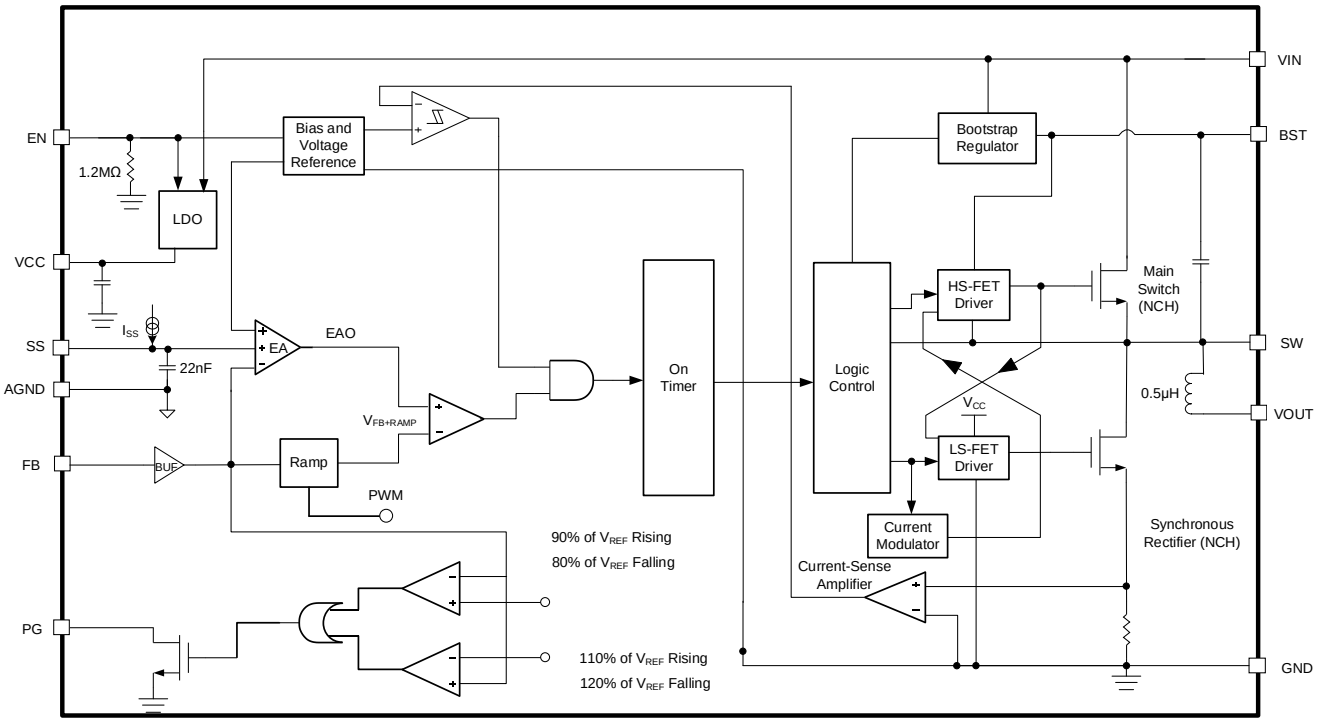

Figure 1: Functional Block Diagram

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OPERATION

The MPM3650C is a fully integrated, synchronous, rectified, step-down power module. Constant-on-time (COT) control provides fast transient response and easy loop stabilization. Figure 2 shows the MPM3650C's simplified ramp compensation block.

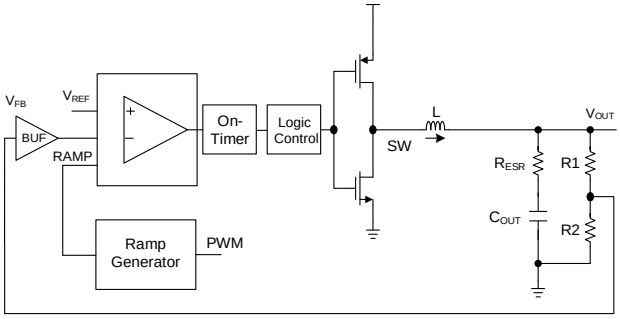

Figure 2: Simplified Ramp Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}), and indicates there is an insufficient output voltage (V_{OUT}). The on time (t_{ON}) is determined by both V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the entire V_{IN} range.

After t_{ON} elapses, the HS-FET turns off. Once V_{FB} drops below V_{REF}, it turns on again. The converter regulates V_{OUT} by repeating this operation. The integrated low-side MOSFET (LS-FET) turns on once the HS-FET turns off to minimize conduction loss. If both the HS-FET and LS-FET are on at the same time, a dead short occurs between input and PGND. This is called shoot-through. To avoid shoot-through, a dead-time (DT) is internally generated between the HS-FET off time (t_{OFF}) and LS-FET t_{ON}, and vice versa.

Internal compensation is applied during COT control to ensure stable operation even when ceramic capacitors are being used as the output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

Forced Continuous Conduction Mode (FCCM)

The MPM3650C can operate in forced continuous conduction mode (FCCM). If $V_{FB+RAMP}$ drops below the error amplifier output (V_{EAO}), then the HS-FET turns on for a fixed interval, which is determined by the one-shot on-timer. Once the HS-FET turns off, the LS-FET turns on and remains on until the next period. Figure 3 shows FCCM operation.

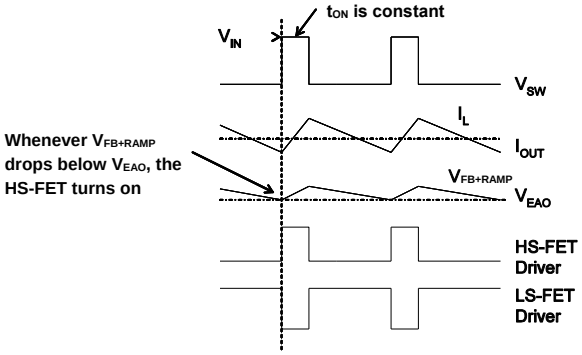

Figure 3: FCCM Operation

During FCCM, the f_{SW} is fairly constant. This constant f_{SW} during FCCM is called pulse-width modulation (PWM) mode.

VCC Regulator

The 3.5V internal regulator powers most of the internal circuitries. This regulator takes the VIN input and operates across the full V_{IN} range. If V_{IN} exceeds 3.5V, the regulator output is in full regulation. If V_{IN} drops below 3.5V, the regulator output decreases following V_{IN}. The device includes an internal, 1μF decoupling ceramic capacitor.

Enable (EN)

EN is a digital control pin that turns the converter on and off. Drive EN above 1.23V to turn the converter on; drive EN below 1V to turn it off.

When floating EN, pull EN down to AGND via an internal 1.2MΩ resistor.

EN can be connected directly to the VIN pin. It supports a V_{IN} range up to 17V.

Under-Voltage Lockout (UVLO) Protection

Under-voltage lockout (UVLO) protects the MPM3650C from operating at an insufficient supply voltage. The UVLO comparator monitors the output voltage of the internal regulator VCC. The VCC UVLO rising threshold is about 2.5V, and its falling threshold is about 2.3V.

Once V_{IN} exceeds the UVLO rising threshold voltage, the MPM3650C starts up. If V_{IN} drops below the UVLO falling threshold, the device shuts down. UVLO is a non-latch protection.

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Soft Start (SS)

The MPM3650C employs soft start (SS) to ensure that the output ramps up smoothly during start-up. If the EN pin goes high, an internal current source (6μA) charges the SS capacitor (C_{SS}). As the device starts up, the SS voltage (V_{SS}) takes over V_{REF} to the PWM comparator. V_{OUT} ramps up smoothly with V_{SS}. V_{SS} continues to ramp up until V_{SS} = V_{REF}, at which point V_{REF} takes over. Then SS finishes, and the device enters steady state operation. The SS capacitance (C_{SS}) can be calculated with Equation (1):

$$C_{SS}(nF) = 0.83 \times \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

The MPM3650C has an internal, 22nF soft start capacitor. If the output capacitor (C_{OUT}) has a large capacitance, it is not recommended to set the soft-start time (t_{SS}) too short, or else the device could too easily reach the current limit during SS.

Power Good (PG) Indicator

The PG pin is the open drain of a MOSFET that connects to VCC or another voltage source via a resistor (e.g. 100kΩ). If V_{IN} is applied before SS completes, then the MOSFET turns on and the PG pin is pulled to PGND. Once V_{FB} reaches 90% of V_{REF}, PG is pulled high after a 50μs delay. Once V_{FB} drops below 80% of V_{REF}, PG is pulled low.

If UVLO or over-temperature protection (OTP) occurs, PG is pulled low. If an over-current (OC) condition occurs and V_{FB} drops below 80% of V_{REF}, PG is pulled low after a 0.05ms delay. If an over-voltage (OV) condition occurs and V_{FB} exceeds 120% of V_{REF}, PG is pulled low after a 0.05ms delay. If V_{FB} drops below 110% of V_{REF}, PG is pulled high after a 0.05ms delay.

If the input supply fails to power the MPM3650C, PG is clamped low, even if PG is tied to an external DC source via a pull-up resistor. Figure 4 shows the relationship between the PG voltage (V_{PG}) and the pull-up current.

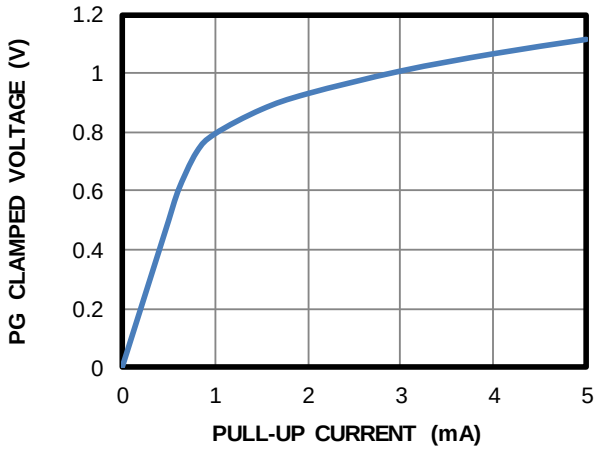

Figure 4: Clamped V_{PG} vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM3650C offers valley limit control. The LS-FET monitors the current flow through itself. The HS-FET waits until the valley current limit is not triggered before turning on again. V_{OUT} decreases until V_{FB} drops below the under-voltage (UV) threshold (typically 50% V_{REF}). Once a UV fault occurs, the MPM3650C enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the device tries to recover from an OC fault using hiccup mode. OCP includes short-circuit protection (SCP). The MPM3650C disables the output power stage, discharges C_{SS}, and initiates a SS. If the OC condition remains after SS is complete, the device repeats this operation until the OC condition disappears, and the output rises back to its regulation level. OCP is a non-latch protection.

Pre-Biased Start-Up

The MPM3650 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, and the bootstrap (BST) voltage (V_{BST}) is refreshed and charged, then the V_{SS} is also charged. If V_{BST} exceeds its rising threshold and V_{SS} exceeds the sensed V_{OUT} at the FB pin, the part resumes normal operation.

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Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 150°C, the MPM3650C shuts down. Once the temperature drops below its lower threshold (typically 130°C), the chip starts up again.

Start-Up and Shutdown Circuit

If both V_{IN} and the EN voltage (V_{EN}) exceed their respective thresholds, the chip starts up. The reference block starts up first to generate a stable V_{REF} and currents. Then the internal regulator starts up to provide a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, VIN going low, and thermal shutdown. The shutdown procedure first blocks the signaling path to avoid any fault triggering, then the internal supply rail is pulled down to ground.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets V_{OUT}. First, choose a value for R2. Too small of an R2 value leads to considerable quiescent current (I_Q) loss, while too large an R2 value makes FB noise sensitive. It is recommended that R2 be between 2kΩ and 100kΩ. Typically, set the current flowing through R2 below 250μA to balance system stability and minimize load loss. Then R1 can be calculated with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 5 shows the feedback circuit.

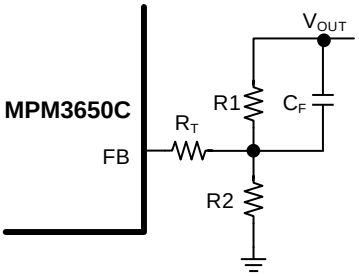

Figure 5: Feedback Network

Table 1 shows recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_F (pF)	R_T (Ω)
1	20	30	39	0
1.2	20	20	39	0
1.5	20	13	39	0
1.8	20	10	39	0
2.5	20	6.34	39	0

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply the AC current to the converter while maintaining the DC V_{IN}. Ceramic capacitors are recommended for the best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended for their stability amid temperature fluctuations.

The capacitor should have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose C_{IN} to have an RMS current rating greater than half of the maximum load current (I_{LOAD}).

The input capacitance determines the converter's input voltage ripple (ΔV_{IN}). If the system has an ΔV_{IN} requirement, choose an input capacitor that meets the relevant specifications.

ΔV_{IN} ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) is required to maintain the DC V_{OUT}. Ceramic or POSCAP capacitors are recommended. The output voltage ripple (ΔV_{OUT}) can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

With ceramic capacitors, the capacitance dominates the impedance at f_{SW}, and causes most of ΔV_{OUT}.

For simplification, ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

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With POSCAP capacitors, the ESR dominates the impedance at f_{SW}.

For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

In addition to accounting for the output ripple, a larger-value C_{OUT} provides better load transient response. However, if C_{OUT} is too large, V_{OUT} is unable to reach the design value during the soft-start time (t_{SS}), and the device will fail to regulate. The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (10):

$$C_{OUT_MAX} = (I_{LIM_AVG}) \times t_{SS} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period.

PCB Layout Guidelines [7]

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to improve thermal performance. For the best results, refer to Figure 6 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Connect a large ground plane directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor, as close to the VIN and PGND pins as possible to minimize high-frequency noise.
4. Keep the paths between C_{IN} and VIN as short and wide as possible.
5. Place a VCC decoupling capacitor close to the IC.
6. Connect AGND and PGND at the VCC capacitor's ground connection.
7. Connect VIN, VOUT, and PGND to a large copper area to improve thermal performance and long-term reliability.
8. Connect the PGND areas at the internal layers and bottom layer with multiple vias.
9. Ensure that there is a complete ground plane on either the internal layer or the bottom layer.
10. Place all signal traces far away from SW.
11. Connect the power planes to the internal layers with multiple vias.

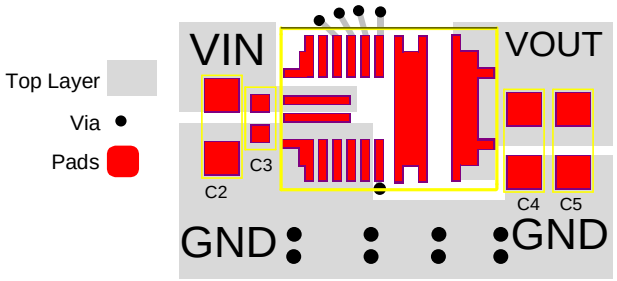

Figure 6: Recommended PCB Layout

Note:

7) The recommended layout is based on Figure 7 (see the Typical Application Circuits section on page 17).

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TYPICAL APPLICATION CIRCUITS

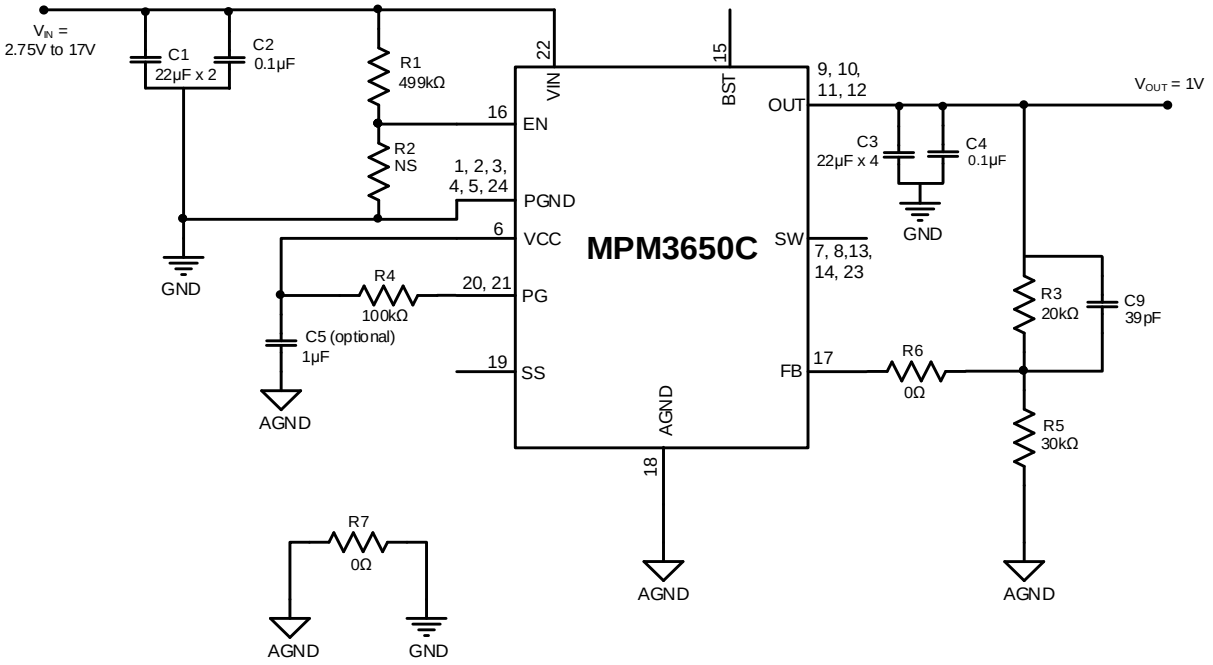

Figure 7: Typical Application Circuit (1V Output)

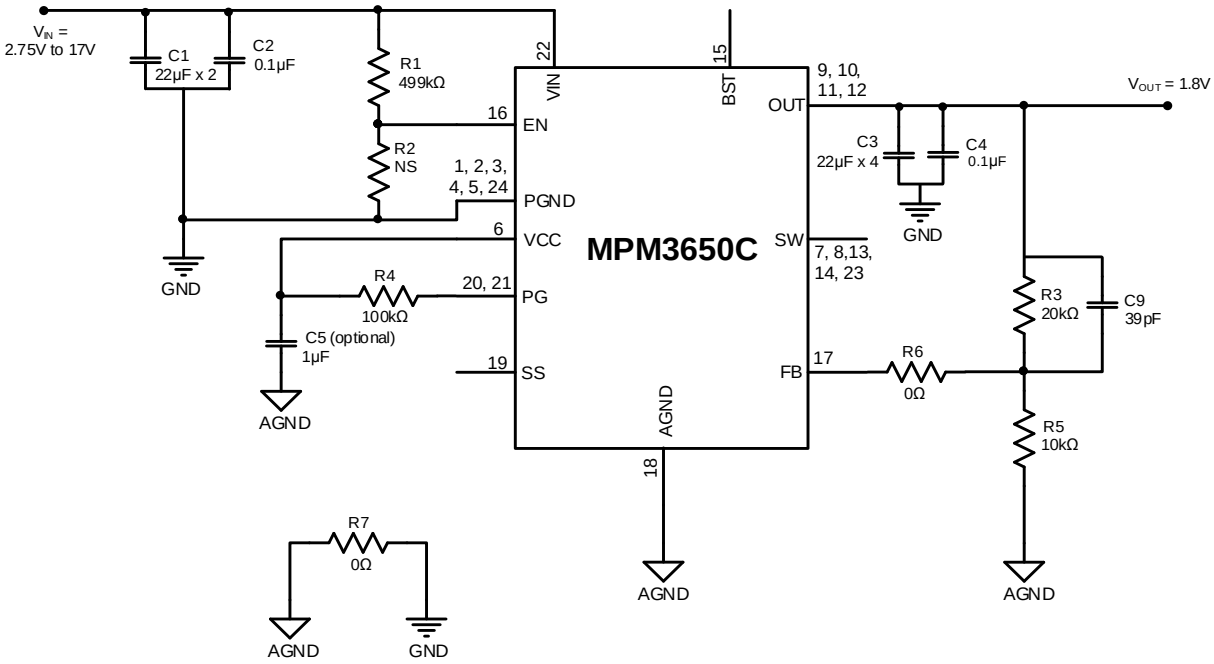

Figure 8: Typical Application Circuit (1.8V Output)

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TYPICAL APPLICATION CIRCUITS *(continued)*

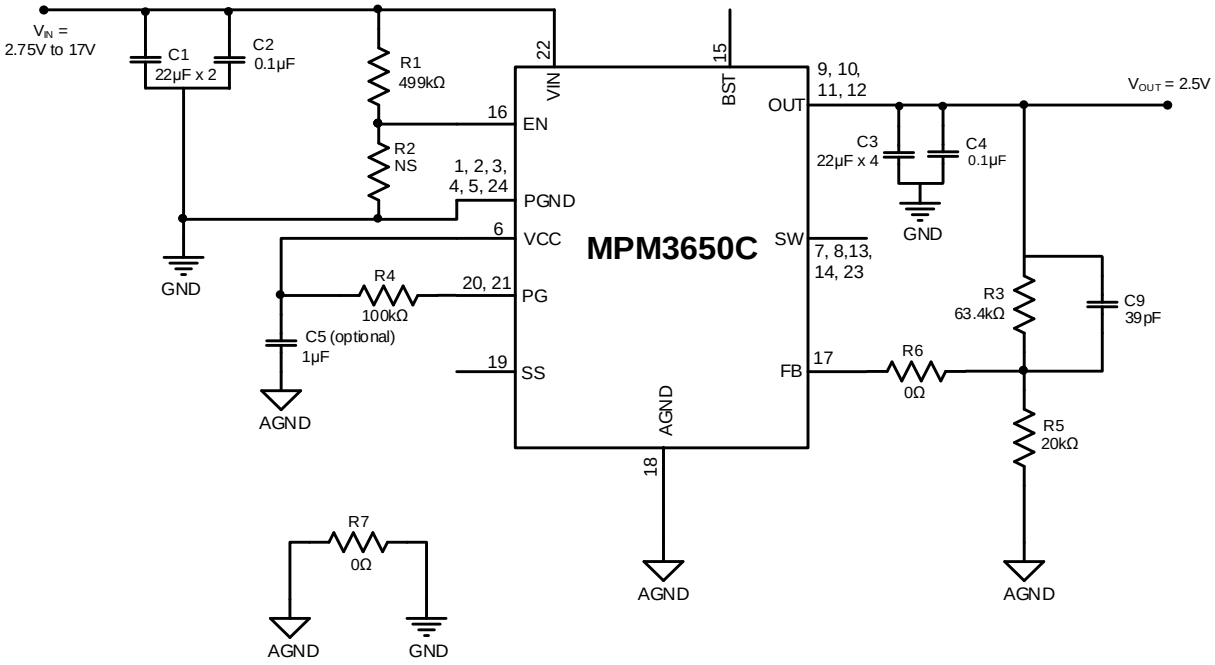

Figure 9: Typical Application Circuit (2.5V Output)

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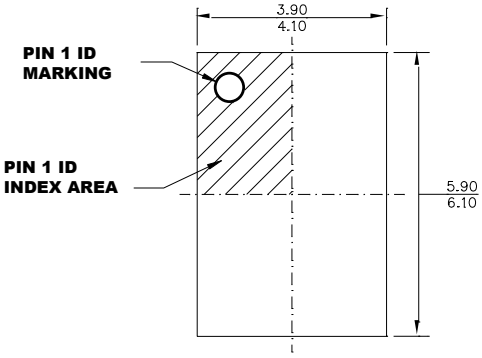
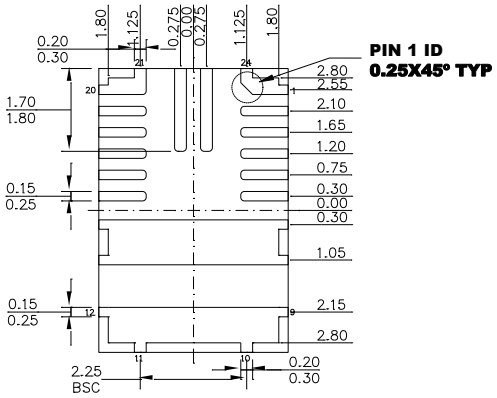
PACKAGE INFORMATION

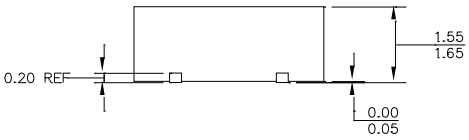
QFN-24 (4mmx6mmx1.6mm)



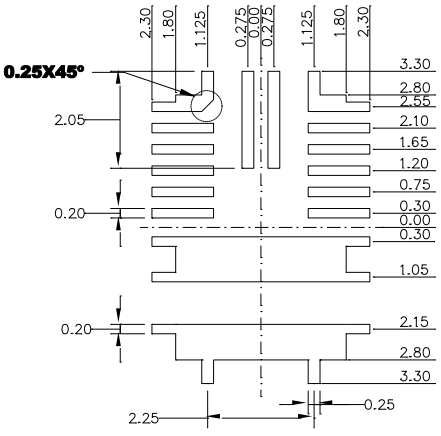
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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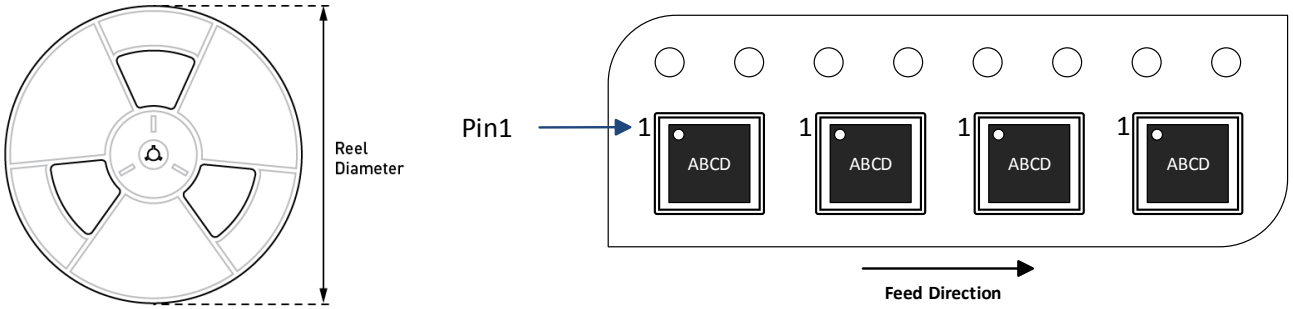
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3650CGQW-Z	QFN-24 (4mmx6mmx1.6mm)	2500	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/22/2020	Initial Release	-
1.1	9/24/2021	Updated the efficiency curve	1
		Updated “–Z” to “-Z” in the Ordering Information and Carrier Information sections	2, 20
		Updated the step numbers in the PCB Layout Guidelines section	16
		Updated the VIN and PGND pin numbers	17–18
		Grammar and formatting updates; updated pagination; updated page headers; added technical abbreviations and shorthand (e.g. V_{OUT}, V_{REF}, C_{SS}, ΔV_{IN}, f_{SW}, etc.)	All

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