MP9989

CCM/DCM Flyback Ideal Diode with Integrated 100V/10mΩ MOSFET and No Need for Auxiliary Winding

DESCRIPTION

The MP9989 is a fast turn-off, intelligent rectifier for flyback converters that integrates a 100V MOSFET. It can replace a diode rectifier for higher efficiency and power density. The chip regulates the forward voltage drop of the internal power switch to 40mV[(1)] and turns off before the drain-source voltage reverses.

The MP9989 can generate its own supply voltage without the need for auxiliary winding, which makes it suitable for charger applications with a low output voltage requirement or any other adaptor applications with high-side set-up. The internal ringing detection circuitry prevents the MP9989 from falsely turning on during discontinuous conduction mode (DCM) or quasi-resonant operations.

The MP9989 is available in SOIC-8 and QFN4x5-8 packages.

FEATURES

- Integrated 100V/10mΩ MOSFET
- Wide Output Range down to 0V
- No Need for Auxiliary Winding for High-Side or Low-Side Rectification
- Ringing Detection Prevents False Turn-On during DCM Operations
- Compatible with Energy Star
- 110μA Quiescent Current
- Supports DCM, CCM, and Quasi-Resonant Operations
- Available in SOIC-8 and QFN4x5-8 Packages

APPLICATIONS

- Laptop Adapters
- QC and USB PD Charger
- High-Efficiency Flyback Converters

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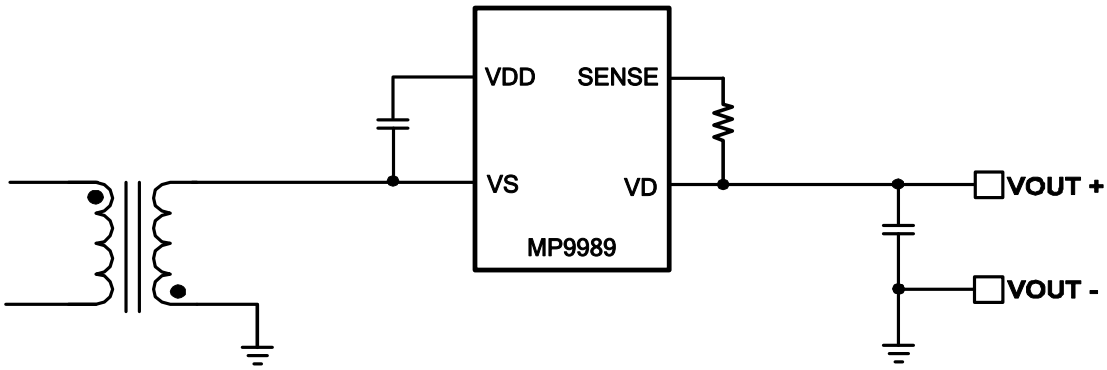
Note:

1) Related issued patent: US Patent US8, 067,973; US8,400,790. CN Patent ZL201010504140.4. Other patents pending.

TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP9989GS*	SOIC-8	*See Below*	2
MP9989GV**	QFN4x5-8	*See Below*	2

* For Tape & Reel, add suffix –Z (e.g. MP9989GS–Z).

** For Tape & Reel, add suffix –Z (e.g. MP9989GV–Z).

TOP MARKING (MP9989GS)

MP9989
LLLLLLLL
MPSYWW

MP9989: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

TOP MARKING (MP9989GV)

MPSYWW
MP9989
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP9989: Part number
LLLLLL: Lot number

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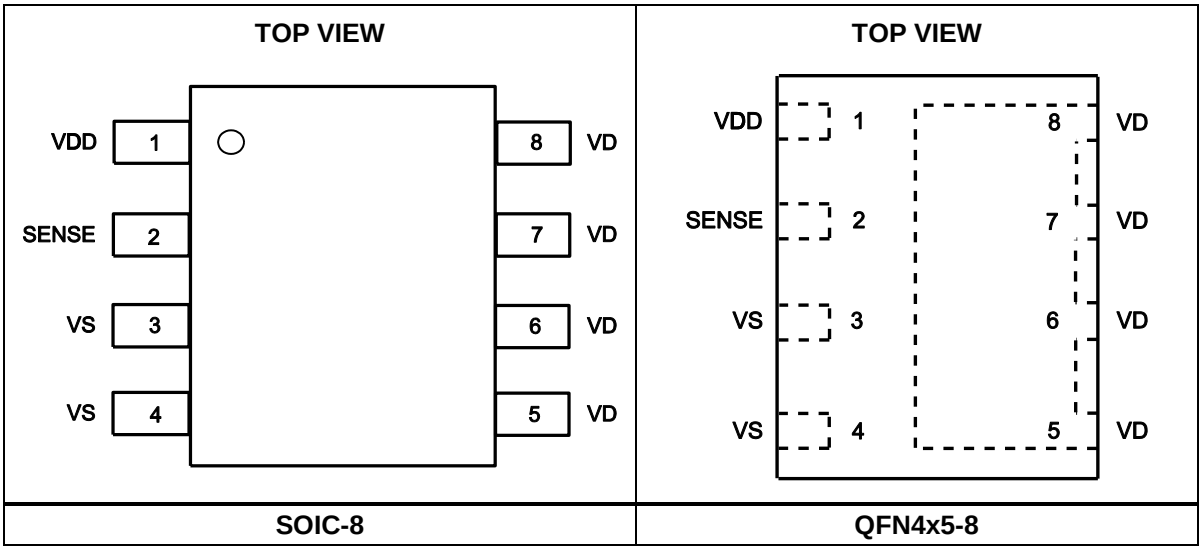
PACKAGE REFERENCE



SOIC-8	QFN4x5-8

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PIN FUNCTIONS

Pin # SOIC-8	Pin # QFN4x5-8	Name	Description
1	1	VDD	**Linear regulator output.** VDD is the supply of the MP9989.
2	2	SENSE	**MOSFET drain voltage sensing.** SENSE is also used as the linear regulator input.
3, 4	3, 4	VS	**MOSFET source.** VS is also used as a reference for VDD.
5, 6, 7, 8	5, 6, 7, 8	VD	**MOSFET drain.**

ABSOLUTE MAXIMUM RATINGS (2)

VDD to VS ..... -0.3V to +14V
VD to VS..... -1.5V to +100V
SENSE to VS..... -1V to +180V
Continuous drain current (T_C = 25°C)
SOIC-8 .....14.9A
QFN4x5-8.....28.1A
Continuous drain current (T_C = 100°C)
SOIC-8 .....9.42A
QFN4x5-8.....17.8A
Pulsed drain current (3)
SOIC-8 .....50A
QFN4x5-8.....94A
Maximum power dissipation (4)
SOIC-8 .....1.7W
QFN4x5-8 ..... 3.1W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature ..... -55°C to +150°C

ESD Rating

Human-body model (HBM) .....±1200V
Charged device model (CDM).....±2000V

Recommended Operation Conditions (5)

VDD to VS ..... 4.5V to 13V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

SOIC-8..... 70 ..... 32... °C/W
QFN4x5-8 ..... 40 ..... 9.... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) Repetitive rating: Pulse width = 100µs, duty cycle limited by maximum junction temperature.
4) T_A = +25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VDD = 6.7V, T_J = -40 to about +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	$V_{(BR)DSS}$	T_J = 25°C	100			V
VDD UVLO rising			4.0	4.2	4.4	V
VDD UVLO hysteresis			0.1	0.24	0.38	V
VDD maximum charging current	I_{VDD}	V_{DD} = 5.5V, SENSE = 30V		63		mA
Operating current	I_{CC}	f_{SW} = 100kHz		4	6	mA
Quiescent current	$I_{Q(VDD)}$	V_{DD} = 7V		110	135	µA
Control Circuitry Section						
Forward regulation voltage (VS-VD) (7)	V_{FWD}		25	40	55	mV
Turn-on threshold (VDS)			-115	-80	-57	mV
Turn-off threshold (VS-VD) (7)			-6	3	12	mV
Turn-on delay (8)	t_{D-ON}			20		ns
Turn-off delay (7)	t_{D-OFF}			25		ns
Turn-on blanking time	t_{B-ON}	C_{LOAD} = 2.2nF	0.8	1.2	1.55	µs
Turn-off blanking threshold (VDS)	V_{B-OFF}		2		3	V
Turn-off threshold during minimum on time (VDS)				1.8		V
Turn-on slew rate detection time (8)				30		ns
Power Switch Section						
Single pulse avalanche energy (9)	E_{AS}	V_{DD} = 50V, V_{GS} = 10V, L = 1.0mH, T_J = 25°C		20		mJ
Drain-source on state resistance	$R_{DS(ON)}$	I_D = 2A,T_J = 25°C		10	12.5	mΩ
Input capacitance	C_{ISS}	V_{DS} = 40V, V_{GS} = 0V, f = 1MHz		3850		pF
Output capacitance	C_{OSS}			614		pF
Reverse transfer capacitance	C_{RSS}			40		pF
Source-Drain Diode Characteristics						
Source-drain diode forward voltage	V_{SD}	I_S = 8A, V_{GS} = 0V		0.8	1.2	V
Reverse recovery time	t_{RR}	I_F = 10A, dI/dt = 100A/µs		78.8		ns
Diode reverse change	Q_{RR}			105.6		nC

Notes:

7) Guaranteed by characterization.
8) Guaranteed by design.
9) E_{AS} is tested at starting T_J = 25°C, L = 1mH, I_{AS} = 6.4A, V_{DD} = 50V, V_{GS} = 10V

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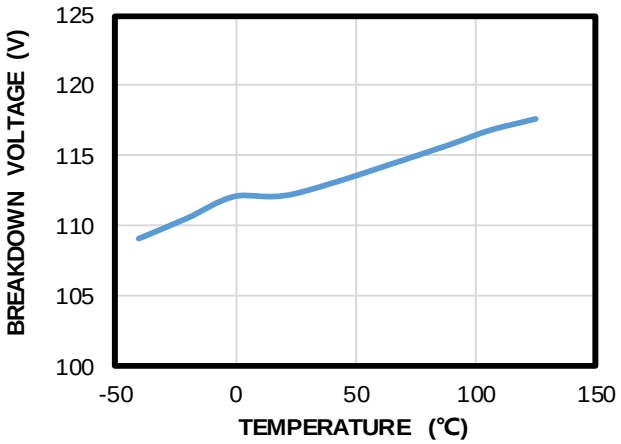
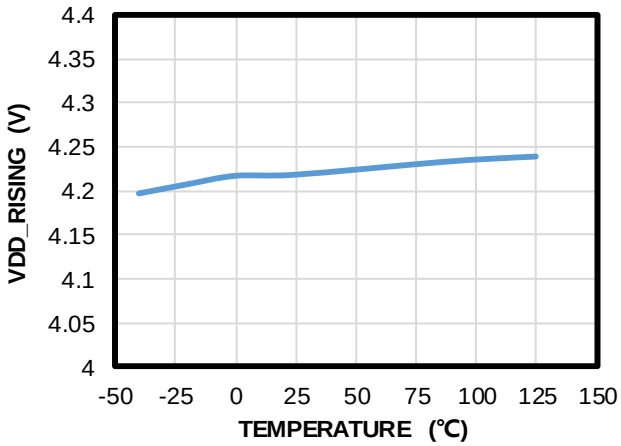
TYPICAL CHARACTERISTICS

VDD = 6.7V, unless otherwise noted.

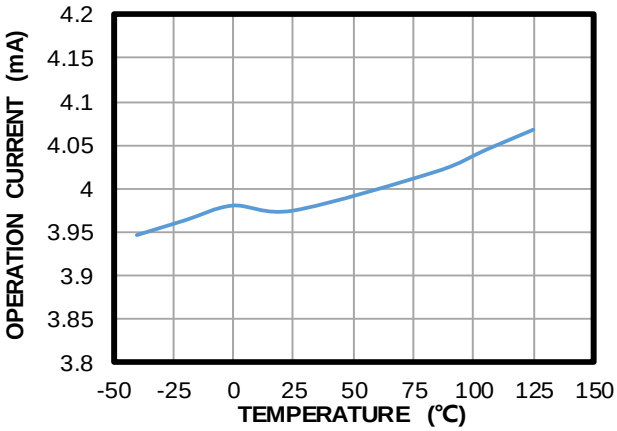
VD-VS Breakdown Voltage vs. Temperature



VDD Rising vs. Temperature

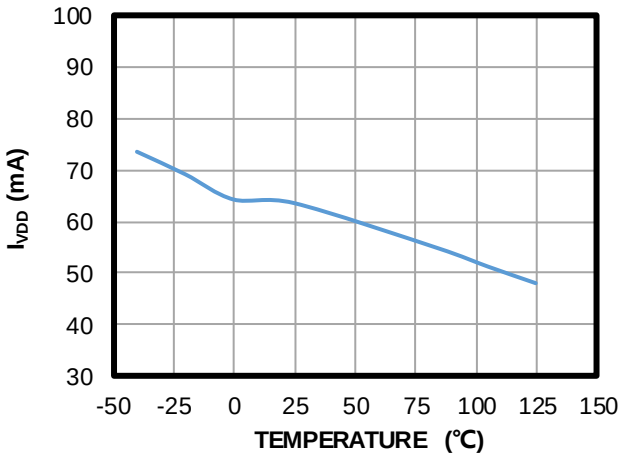


Operation Current vs. Temperature

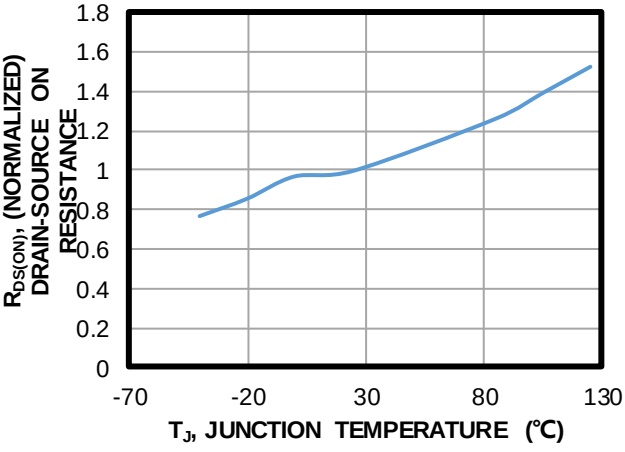


VDD Maximum Charging Current vs. Temperature

V_{DD} = 5.5V, SENSE = 30V



$R_{DS(ON)}$ vs. Temperature



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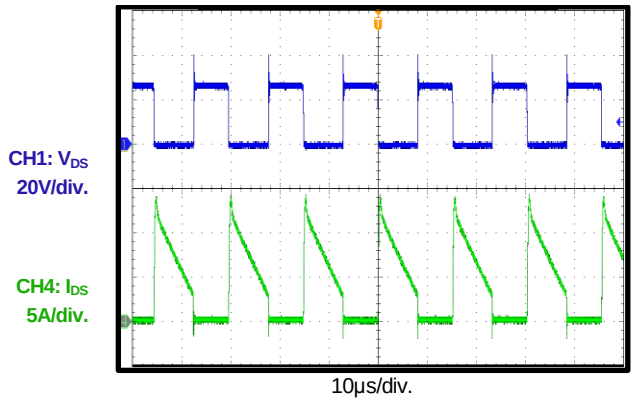
TYPICAL PERFORMANCE CHARACTERISTICS

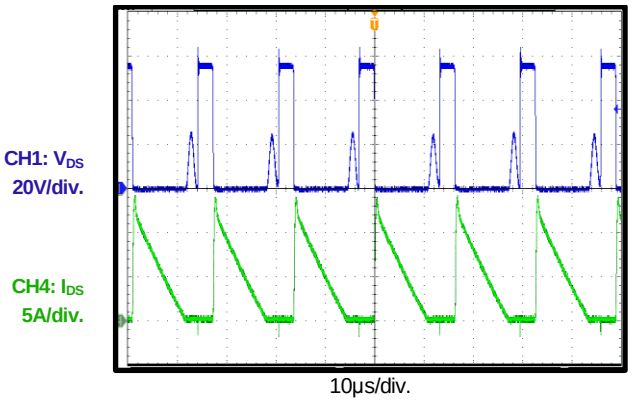
Operation in 48W Flyback Application

V_{IN} = 90V_{AC}, I_{OUT} = 4.0A



Operation in 48W Flyback Application

V_{IN} = 265V_{AC}, I_{OUT} = 4.0A



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FUNCTIONAL BLOCK DIAGRAM

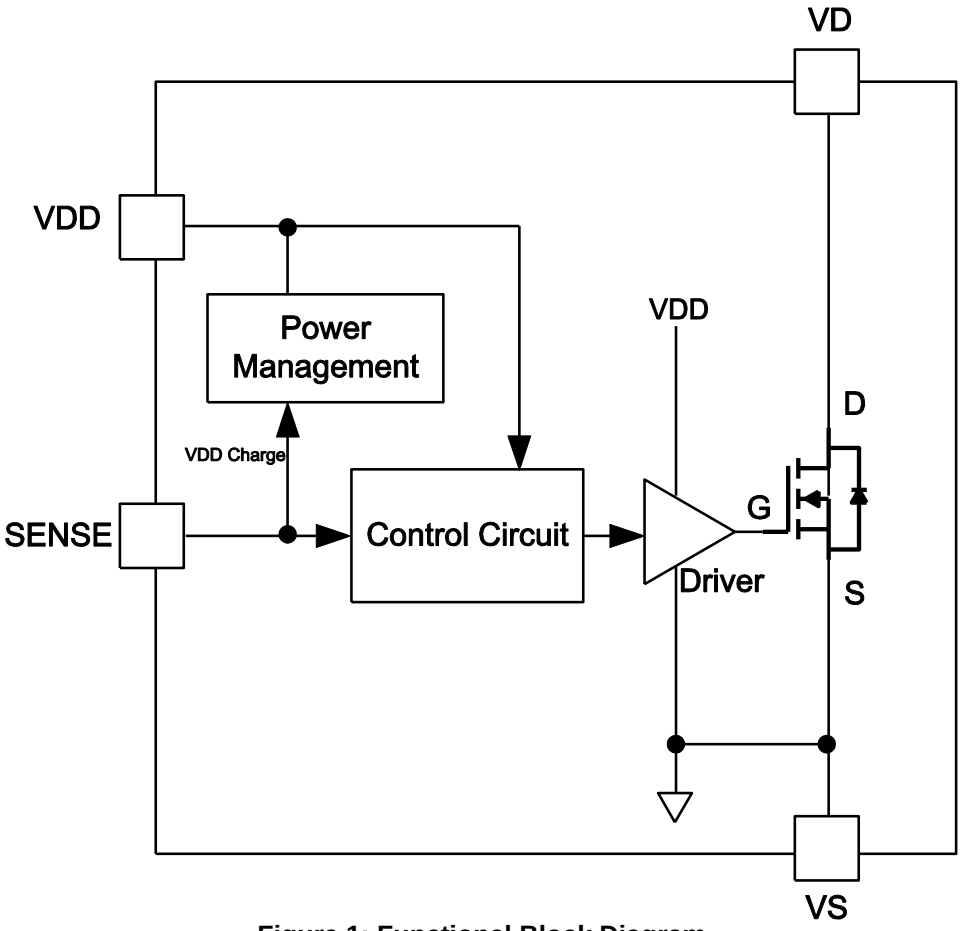

Figure 1: Functional Block Diagram

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OPERATION

The MP9989 supports operation in discontinuous conduction mode (DCM), continuous conduction mode (CCM), and quasi-resonant flyback converters. The control circuitry controls the gate in forward mode and turns the gate off when the synchronous rectification (SR) MOSFET current drops to zero.

VDD Generation

SENSE is the input for the linear regulator, the output of which is VDD. VDD supplies the MP9989, and is regulated at 6.7V.

When SENSE is under 4.7V, a 40mA current source from SENSE charges up VDD. When SENSE is above 4.7V, the linear regulator's maximum charging current is limited at I_{VDD} to charge the external capacitor at VDD.

Start-Up and Under-Voltage Lockout (UVLO)

When VDD rises above 4.2V, the MP9989 exits under-voltage lockout (UVLO) and is enabled. Once VDD drops below 4.0V, the MP9989 enters sleep mode and V_{GS} is kept low.

Turn-On Phase

When V_{DS} drops to ~2V, a turn-on timer begins. If V_{DS} reaches the -80mV turn-on threshold from 2V within the slew rate detection time (~30ns), the MOSFET is turned on after a turn-on delay t_{D-ON} (~20ns) (see Figure 2). If V_{DS} crosses -80mV after the timer ends, the gate voltage remains off. This turn-on timer prevents the MP9989 from falsely turning on due to ringing from DCM and quasi-resonant operations.

Turn-On Blanking

The control circuitry contains a blanking function. When the MOSFET turns on, the control circuit ensures that the on state lasts for a specific period of time. The turn-on blanking time is t_{B-ON} (~1.2µs) to prevent an accidental turn off due to ringing. However, if V_{DS} reaches 1.8V within the turn-on blanking time, V_{GS} is pulled low immediately.

Conduction Phase

When V_{DS} rises above the forward voltage drop, V_{FWD} (-40mV), according to the decrease of the switching current, the MP9989 lowers the gate voltage level to enlarge the on resistance of the synchronous MOSFET.

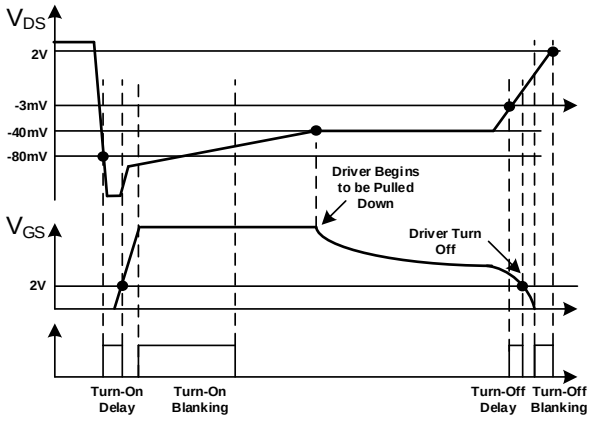

Figure 2: Turn-On/Turn-Off Timing Diagram

With this control scheme, V_{DS} is adjusted to be around V_{FWD} even when the current through the MOSFET is fairly low. This function keeps the driver voltage at a very low level when the synchronous MOSFET is turned off, which boosts the turn-off speed and is especially important to CCM operation.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold (-3mV), the gate voltage is pulled to zero after a short turn-off delay of t_{D-OFF} (about 25ns) (see Figure 2).

Turn-Off Blanking

After the gate driver (V_{GS}) is pulled to zero by V_{DS} reaching the turn-off threshold (-3mV), a turn-off blanking time is applied, during which the gate driver signal is latched off. The turn-off blanking is removed when V_{DS} rises above V_{B-OFF} (2V) (see Figure 2).

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APPLICATION INFORMATION

Slew Rate Detection Function

In DCM operations, the demagnetizing ringing may bring V_{DS} below 0V. If V_{DS} reaches the turn-on threshold during the ringing, SR controllers without the slew rate detection function may turn on the MOSFET by mistake. This not only increases power loss, but may also lead to shoot-through if the primary side MOSFET is turned on within the minimum on time.

Considering the slew rate of the ringing is always much less than when the primary MOSFET is completely turned off, this false turn-on situation can be prevented by the slew rate detection function. When the slew rate is less than the threshold, the IC does not turn on the gate even when V_{DS} reaches the turn-on threshold. For more details, see the Turn-On Phase section on page 8.

External Resistor on SENSE

Over-voltage conditions may lead to damage to the device, so there must be appropriate application design to guarantee safe operation, especially on the high voltage pin.

One common over-voltage condition is when the body diode of the SR MOSFET is turned on, as the forward voltage drop may exceed the negative rating on the SENSE pin. In this case, it is recommended to place an external resistor between SENSE and the MOSFET drain. In general, the resistance is recommended to be about 100Ω to 300Ω.

On the other hand, this resistor also cannot be too large, because it may compromise the VDD supply and slow down the slew rate on the V_{DS} detection. In general, it is not recommended to use a resistor greater than 300Ω, but for each use case, it should be checked based on the condition of VDD supply and the slew rate.

Typical System Implementations

Figure 3 and Figure 4 show the typical system IC implementation in low-side rectification and high-side rectification, respectively.

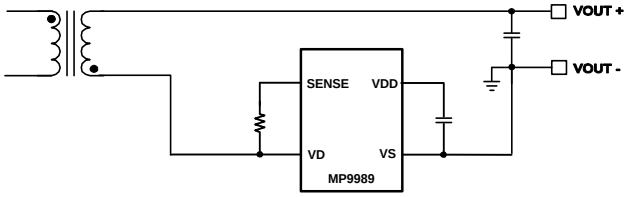

Figure 3: Low-Side Rectification

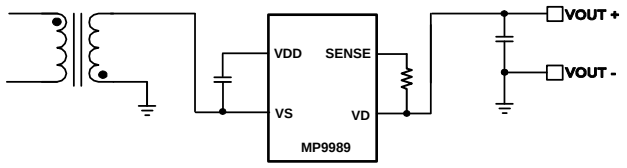

Figure 4: High-Side Rectification

Maximum Output Current

The allowed temperature rise of the MP9989 limits the maximum output current the device can handle. The temperature rise is determined by its own power loss. Generally, for a universal input adapter the recommended rated output current for MP9989 is 4A. For certain designs, the power loss of the MP9989 can be calculated, so the maximum output current can be deduced.

The power loss of the MP9989 can be separated into several parts: controller consumption, integrated MOSFET conduction loss, and so on. If the MP9989 works in continuous conduction mode (CCM), reverse-recovery loss of the integrated MOSFET must also be considered. Each part of the loss can be calculated based on Equation (1), Equation (2), and Equation (3):

$$P_{LOSS\_CONTROLLER} = V_{SENSE\_P} \times I_{DD} \quad (1)$$

$$P_{LOSS\_SR\_CONDUCTION} = f_{SW} \times \int_{0}^{t_{S\_ON}} V_{SR\_SD}(t) \times I_{SR\_SD}(t)dt \quad (2)$$

$$P_{LOSS\_SR\_RR} = \frac{1}{2} \times V_{DS} \times I_{RR} \times t_F \times f_{SW} \quad (3)$$

Where I_{DD} is the current of the MP9989, and V_{SENSE_P} is the corresponding plateau voltage in the SENSE pin when SR turns off. f_{SW} is the SR switching frequency, and t_{S_ON} is the SR on period, V_{SR_SD} is the voltage drop from the SR, and I_{SR_SD} is the current flowing from the SR. I_{RR}

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is the peak reverse current and t_F is the reverse current fall time.

The total loss of the MP9989 (P_{LOSS}) is the sum of the above losses. If a RC snubber is used, the power loss caused by this snubber must also be taken into consideration.

The junction and case temperature rises can be calculated with the thermal resistance of the junction-to-ambient (θ_{JA}) and junction-to-case (θ_{JC}). The junction temperature must be within ABS (typically 150°C). Calculate ΔT_{JA} and ΔT_{JC} with Equation (4) and Equation (5):

$$\Delta T_{JA} = P_{LOSS} \times \theta_{JA} \quad (4)$$

$$\Delta T_{JC} = P_{LOSS} \times \theta_{JC} \quad (5)$$

The thermal resistance can be reduced in one of several ways to lower the temperature: a thicker copper layer attached to VD and VS, additional vias for thermal dissipation, or heatsinks. The real maximum output current can be set combining the real tested data.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 5, Figure 6, Figure 7, and follow the guidelines below.

1. Connect SENSE pin to different position for an adjustable turn-off point of time during the fast transients in CCM. In general, the farther the junction point is from the VD, the earlier the SR turns off. (See Figure 5).
2. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other.

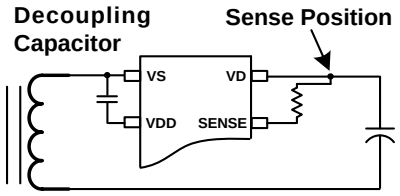

Figure 5: Voltage Sensing for VD/SENSE

3. Place a decoupling ceramic capacitor from VDD to VS close to the IC for adequate filtering.

Layout Example

Figure 6 and Figure 7 show the layout example for QFN4x5-8 package and SOIC-8 package in high-side application of flyback power supply, respectively. It is a single layer with a through-hole transformer. R2 and C2 are the RC snubber network for the internal MOSFET. The sensing loop (SENSE to the MOSFET drain) is optimized and kept separate from the power loop. The VDD decoupling capacitor (C1) is placed beside VDD.

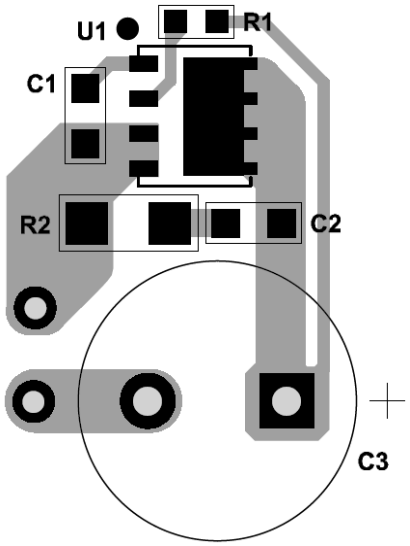

Figure 6: Layout Example for QFN4x5-8 package in Flyback High-Side Application

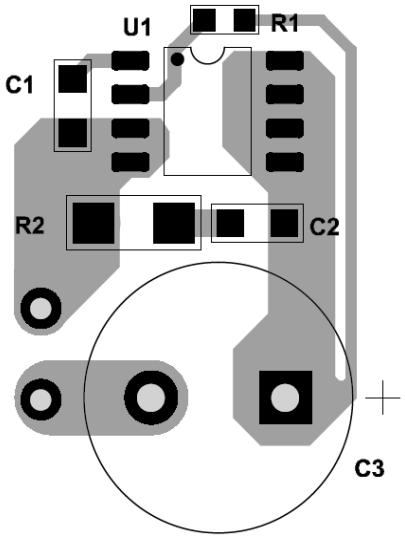

Figure 7: Layout Example for SOIC-8 package in Flyback High-Side Application

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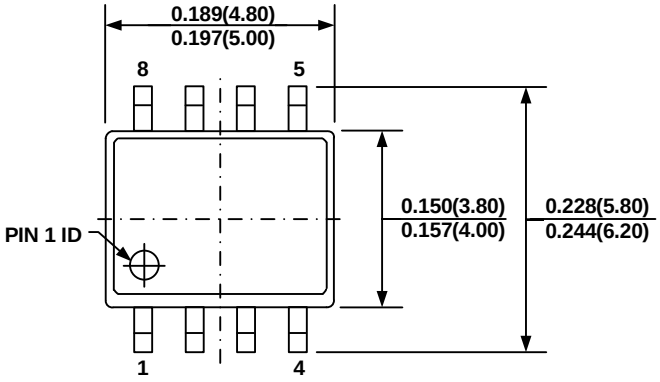
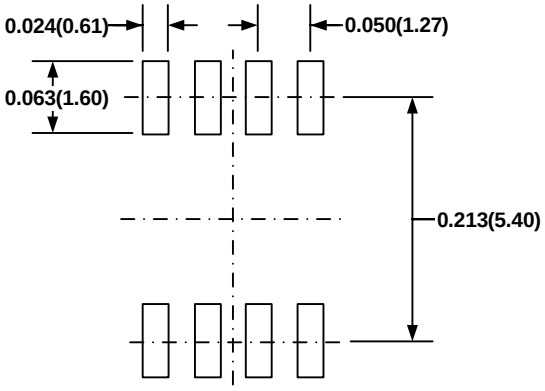
PACKAGE INFORMATION

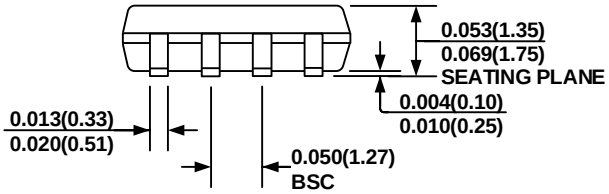
SOIC-8



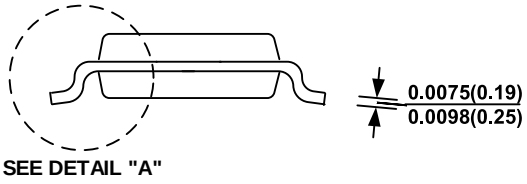
TOP VIEW



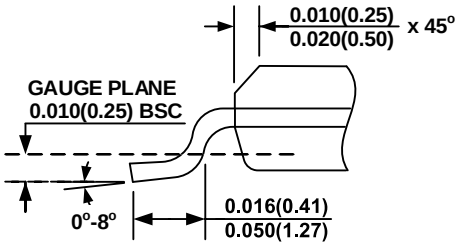
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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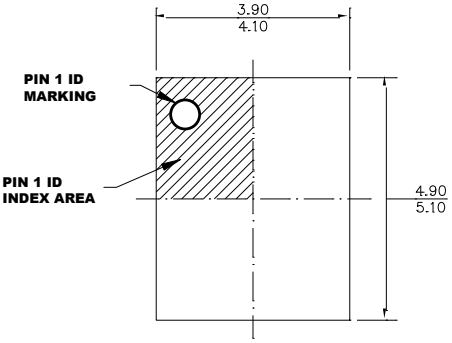
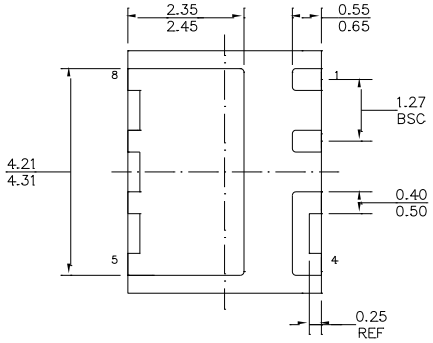
PACKAGE INFORMATION

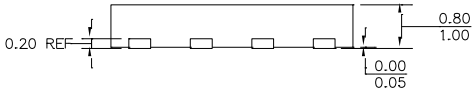
QFN4X5-8



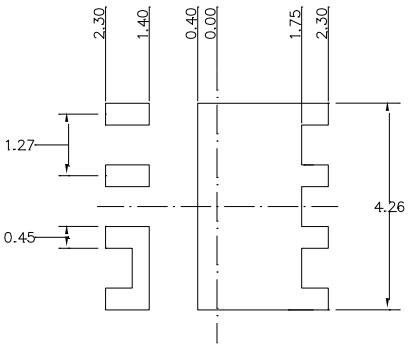
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220
5) DRAWING IS NOT TO SCALE.

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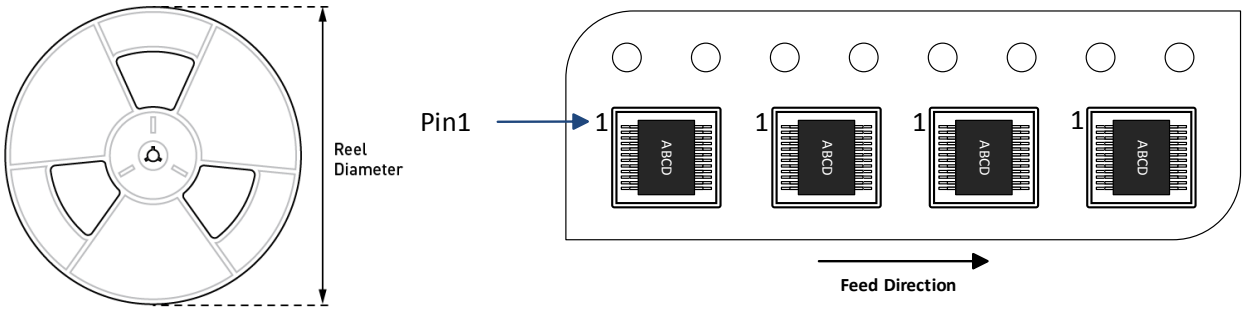
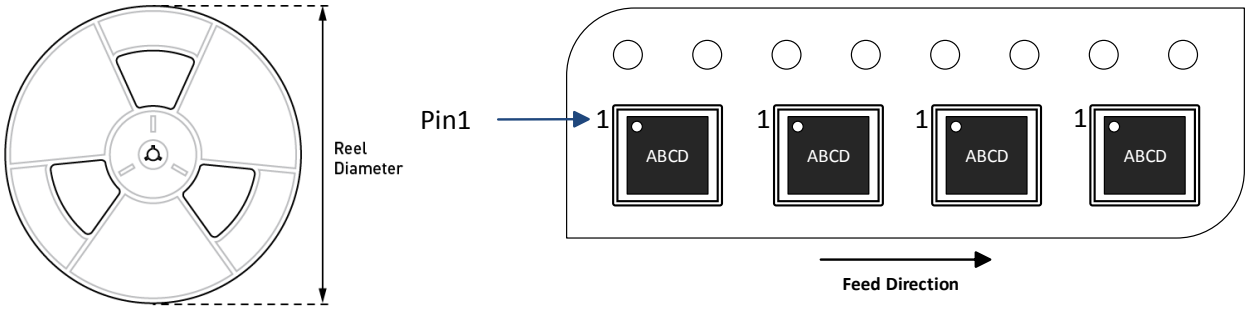
CARRIER INFORMATION

SOIC-8



Part Number	Package Description	Quantity/Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP9989GS-Z	SOIC-8	2500	100	N/A	13in	12mm	8mm

QFN4X5-8



Part Number	Package Description	Quantity/Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP9989GV-Z	QFN4x5-8	5000	N/A	N/A	13in	12mm	8mm

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.1	8/272020	Update ABS.	3
1.1	8/272020	Add sections for PCB layout.	11

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