# MP9840

## 36V, 3.5A, Low $I_Q$, Synchronous Step-Down Converter

The Future of Analog IC Technology

## DESCRIPTION

The MP9840 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves 3.5A of continuous output current with excellent load and line regulation over a wide 3.3V to 36V input supply range. The switching frequency can be programmed or synchronized to an external clock in the range of 350kHz to 2.5MHz. The synchronous operation and ultra-low 14μA sleep mode quiescent current provide high efficiency over the output current load range, allowing the MP9840 to be used in a variety of step-down applications in automotive input environments and battery-powered applications.

Peak-current-mode operation provides fast transient response and eases loop stabilization. The excellent low dropout performance allows the MP9840 to be used in high duty cycle applications.

Full protection features include over-current protection (OCP), short-circuit protection (SCP), and thermal shutdown. An open-drain power good (PG) signal indicates when the output is within 10% of its nominal voltage.

The MP9840 is available in a space-saving QFN-16 (3mmx4mm) package.

## FEATURES

- 2μA Low Shutdown Supply Current
- 14μA No-Load Quiescent Current
- Internal 125mΩ High-Side and 55mΩ Low-Side MOSFET
- 350kHz to 2.5MHz Programmable Switching Frequency
- Power Good (PG) Output
- External Soft Start (SS)
- 80ns Minimum On Time
- Selectable Forced CCM and AAM
- Hiccup Over-Current Protection (OCP)
- Available in a QFN-16 (3mmx4mm) Package

## APPLICATIONS

- Automotive Systems
- Industrial Power Systems

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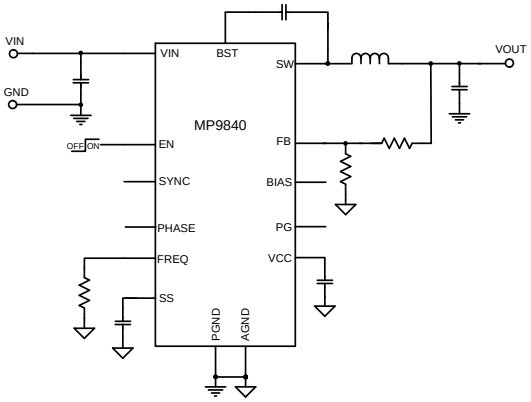
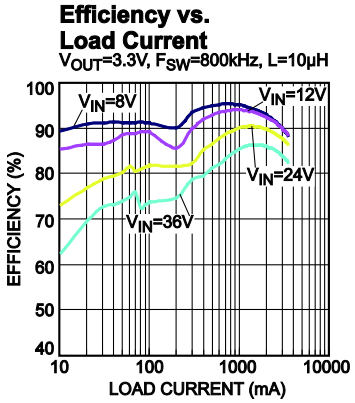
## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP9840GL | QFN-16 (3mmx4mm) | *See Below* |

* For Tape & Reel, add suffix –Z (e.g. MP9840GL–Z)

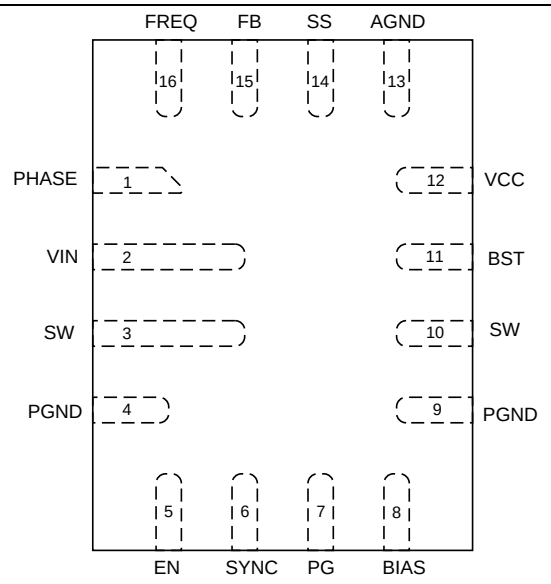
## TOP MARKING

MPYW
9840
LLL

MP: MPS prefix
Y: Year code
W: Week code
9840: First four digits of the part number
LLL: Lot number

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-16 (3mmx4mm)**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## ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage ($VIN_x$)..... -0.3V to 40V
Switch voltage ($V_{SWx}$)... -0.3V to $VIN_{(MAX)}$ + 0.3V
BST voltage ($V_{BSTx}$).....$V_{SW (MAX)}$ + 6.5V
EN voltage ($V_{ENx}$) ..... -0.3V to 40V
PG voltage..... -0.3V to 40V
BIAS voltage..... -0.3V to 20V
All other pins..... -0.3V to 6V
Continuous power dissipation ($T_A$ = +25°C) (2)
QFN-16 (3mmx4mm).....2.6W
Junction temperature.....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to 150°C

### *Recommended Operating Conditions*

Supply voltage (VIN)..... 3.3V to 36V
Operating junction temp. ($T_J$) ...-40°C to +125°C

### *Thermal Resistance* (3) $\theta_{JA}$ $\theta_{JC}$

QFN-16 (3mmx4mm) ..... 48..... 11 ... °C/W

**NOTES:**

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$(MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/ \theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**VIN = 12V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C (4), unless otherwise noted. Typical values are at $T_J$ = +25°C.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VIN quiescent current | $I_Q$ | $V_{FB}$ = 0.85V, no load, no switching, $T_J$ = +25°C | | 14 | 21 | µA |
| | | $V_{FB}$ = 0.85V, no load, no switching | | | 29 | |
| VIN shutdown current | $I_{SHDN}$ | $V_{EN}$ = 0V | | 2 | 6 | µA |
| VIN under-voltage lockout threshold rising | $INUV_{RISING}$ | | 2.4 | 2.8 | 3.2 | V |
| VIN under-voltage lockout threshold hysteresis | $INUV_{HYS}$ | | | 150 | | mV |
| EN rising threshold | $V_{EN_RISING}$ | | 0.9 | 1.05 | 1.2 | V |
| EN threshold hysteresis | $V_{EN_HYS}$ | | | 120 | | mV |
| Feedback reference voltage | $V_{REF}$ | | 784 | 800 | 816 | mV |
| | | $T_J$ = 25°C | 792 | 800 | 808 | mV |
| HS switch on resistance | $R_{ON_HS}$ | $V_{BST}$ - $V_{SW}$ = 5V | | 125 | 165 | mΩ |
| LS switch on resistance | $R_{ON_LS}$ | | | 55 | 85 | mΩ |
| Switching frequency | $F_{SW}$ | $R_{FREQ}$ = 180kΩ or from sync clock | 400 | 475 | 550 | kHz |
| | | $R_{FREQ}$ = 82kΩ or from sync clock | 850 | 1000 | 1150 | kHz |
| | | $R_{FREQ}$ = 27kΩ or from sync clock | 2250 | 2500 | 2750 | kHz |
| Minimum on time (5) | $T_{ON_MIN}$ | | | 80 | | ns |
| SYNC input low voltage | $V_{SYNC_LOW}$ | | | | 0.4 | V |
| SYNC input high voltage | $V_{SYNC_HIGH}$ | | 1.8 | | | V |
| Current limit | $I_{LIMIT_HS}$ | Duty cycle = 40% | 4.6 | 5.6 | 7.4 | A |
| Low-side valley current limit | $I_{LIMIT_LS}$ | $V_{OUT}$ = 3.3V, L = 4.7µH | 3.1 | 4.4 | 5.7 | A |
| ZCD current | $I_{ZCD}$ | | | 0.1 | | A |
| Reverse current limit | $I_{LIMIT_REVERSE}$ | | | 3 | | A |
| Switch leakage current | $I_{SW_LKG}$ | | | 0.01 | 1 | µA |
| Soft-start current | $I_{SS}$ | $V_{SS}$ = 0.8V | 5 | 10 | 15 | µA |
| VCC regulator | $V_{CC}$ | | | 5 | | V |
| VCC load regulation | | $I_{CC}$ = 5mA | | | 3.5 | % |
| Thermal shutdown (5) | $T_{SD}$ | | | 170 | | °C |
| Thermal shutdown hysteresis (5) | $T_{SD_HYS}$ | | | 20 | | °C |
| PG rising threshold ($V_{FB}/V_{REF}$) | $PG_{RISING}$ | $V_{FB}$ rising | 85 | 90 | 95 | % |
| | | $V_{FB}$ falling | 105 | 110 | 115 | |
| PG falling threshold ($V_{FB}/V_{REF}$) | $PG_{FALLING}$ | $V_{FB}$ falling | 79 | 84 | 89 | % |
| | | $V_{FB}$ rising | 113.5 | 118.5 | 123.5 | % |
| PG deglitch timer | $T_{PG_DEGLITCH}$ | PG from low to high | | 30 | | µs |
| | | PG from high to low | | 50 | | µs |
| PG output voltage low | $V_{PG_LOW}$ | $I_{SINK}$ = 2mA | | 0.2 | 0.4 | V |

**NOTE:**

4) Not tested in production and guaranteed by over-temperature correlation.
5) Not tested in production and guaranteed by design and characterization.


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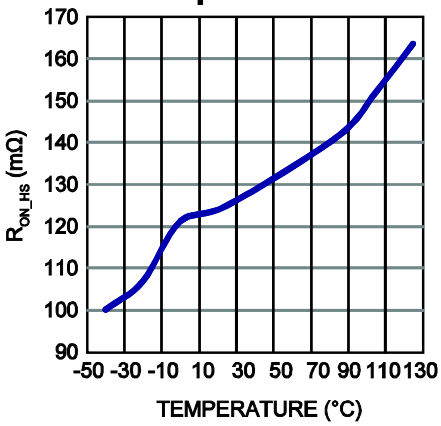
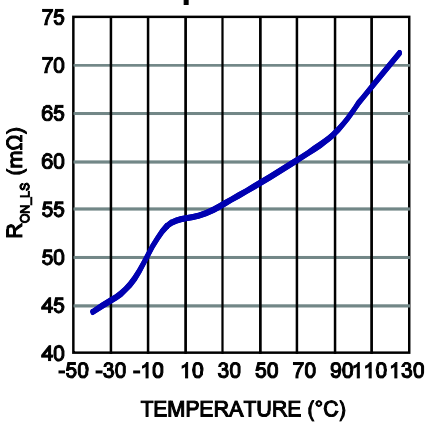
## TYPICAL CHARACTERISTICS

**VIN = 12V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

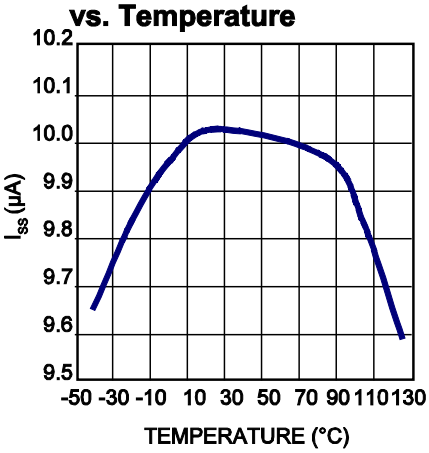
**HS-FET On Resistance vs. Temperature**



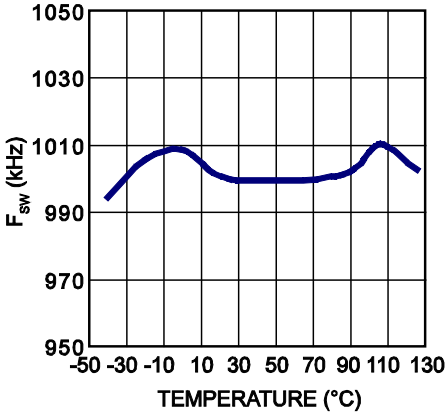

**LS-FET On Resistance vs. Temperature**



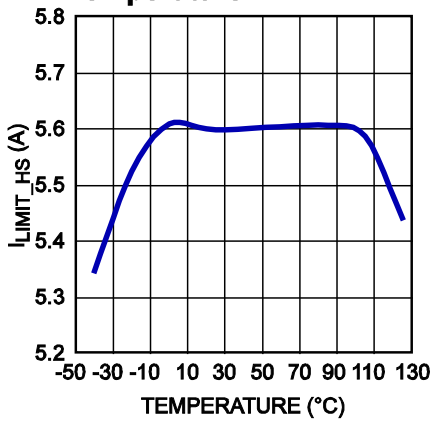

**Soft-Start Current vs. Temperature**



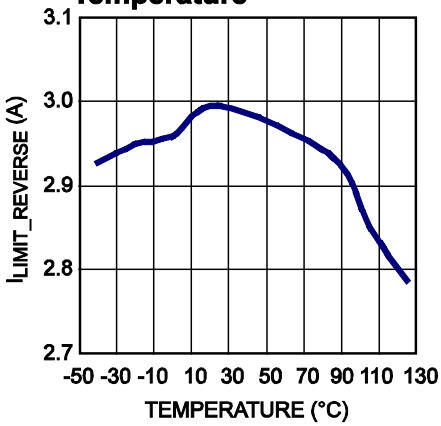

**Switching Frequency vs. Temperature**



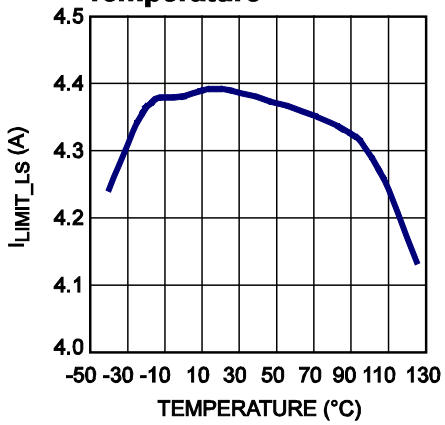

**Current Limit vs. Temperature**



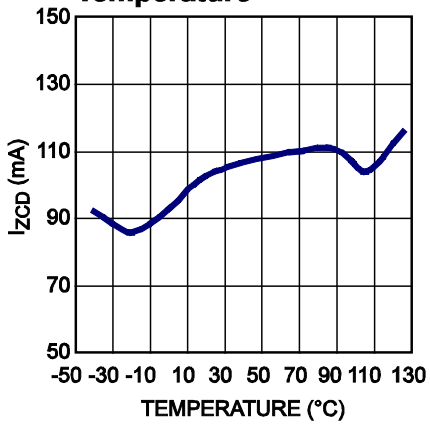

**Reverse Current Limit vs. Temperature**




**Valley Current Limit vs. Temperature**




**ZCD Current vs. Temperature**





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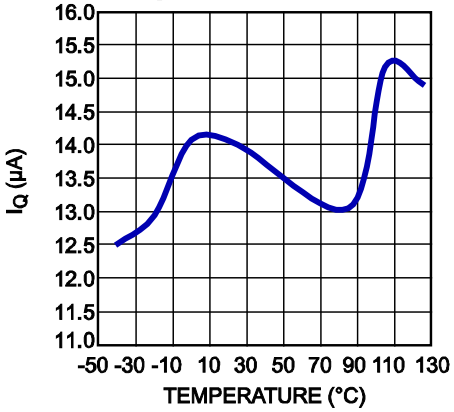
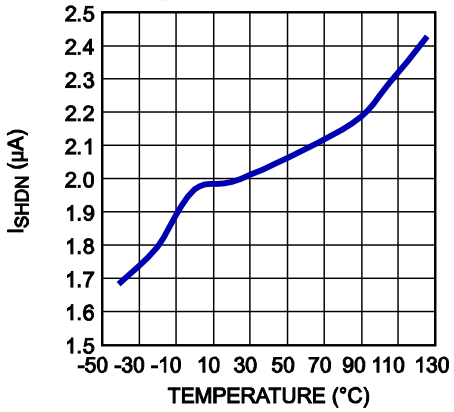
## TYPICAL CHARACTERISTICS *(continued)*

**VIN = 12V, $T_J$ = -40°C to +125°C, unless otherwise noted.**

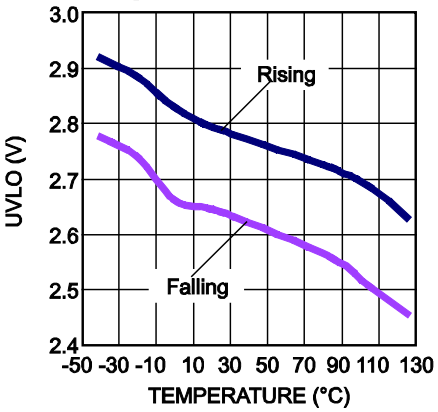
**Quiescent Current vs. Temperature**



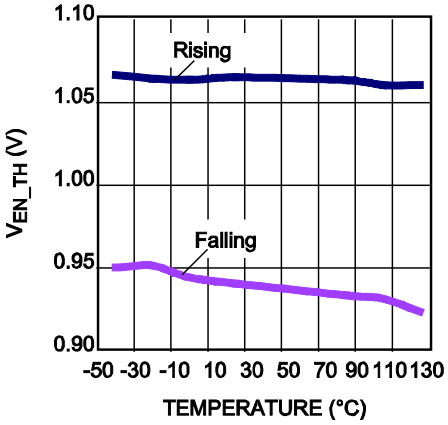

**Shutdown Current vs. Temperature**



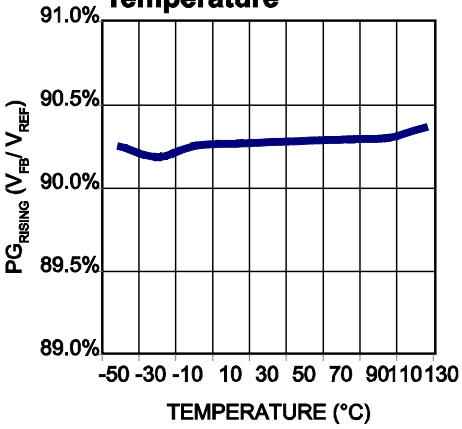

**VIN UVLO Threshold vs. Temperature**



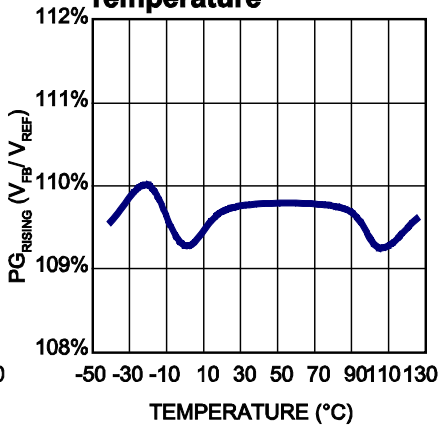

**EN Threshold vs. Temperature**



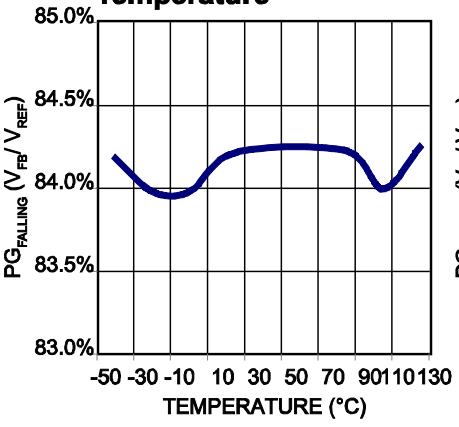

**PG Rising Threshold ($V_{FB}$ Rising) vs. Temperature**



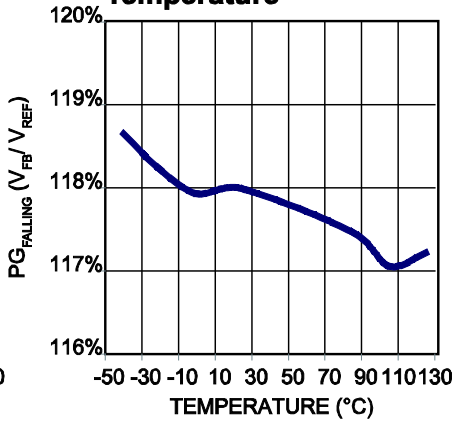

**PG Rising Threshold ($V_{FB}$ Falling) vs. Temperature**



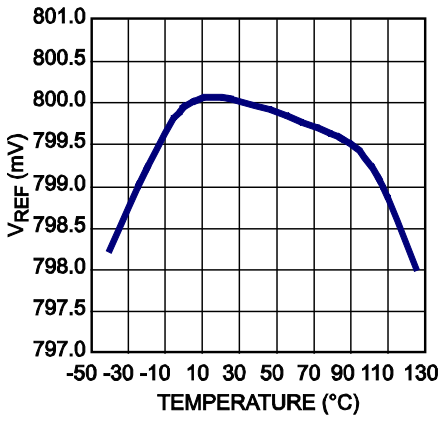

**PG Falling Threshold ($V_{FB}$ Falling) vs. Temperature**




**PG Falling Thershold ($V_{FB}$ Rising) vs. Temperature**




**Feedback Reference vs. Temperature**





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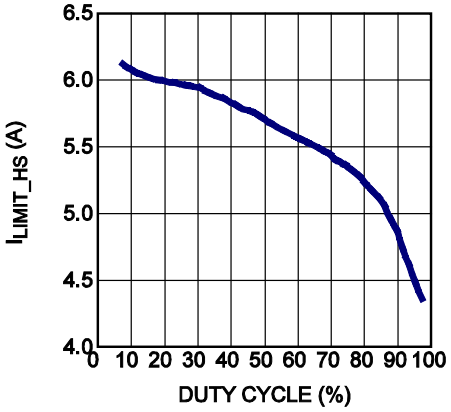
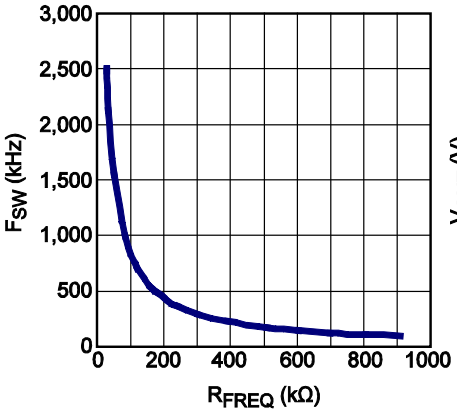
## TYPICAL PERFORMANCE CHARACTERISTICS

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

**Current Limit vs. Duty Cycle**



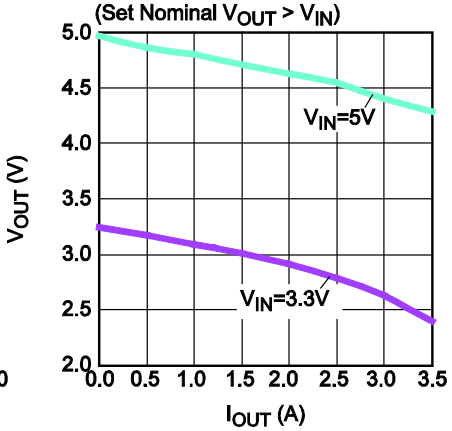

**$F_{SW}$ vs. $R_{FREQ}$**



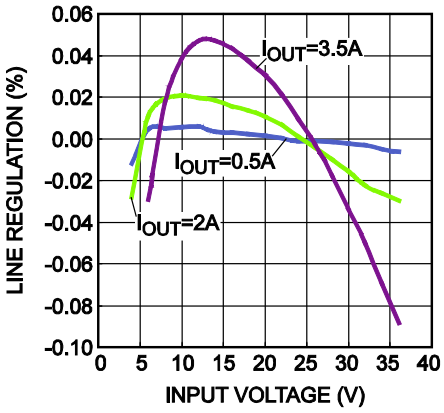

**Output Voltage vs. Load Current**

Dropout Performance

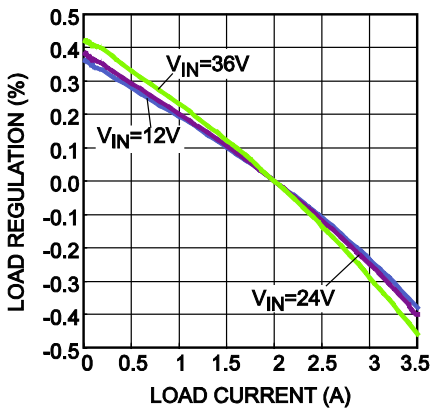
(Set Nominal $V_{OUT}$ > $V_{IN}$)




**Line Regulation**




**Load Regulation**





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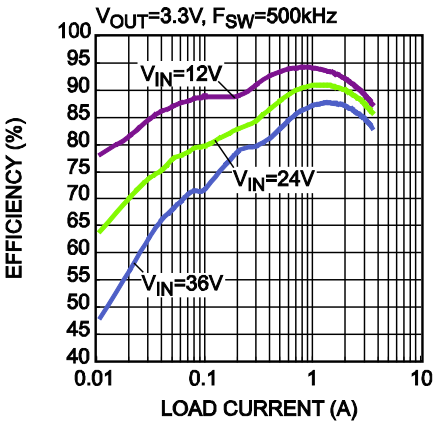
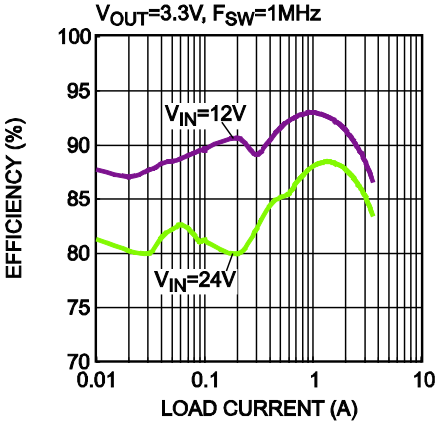
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

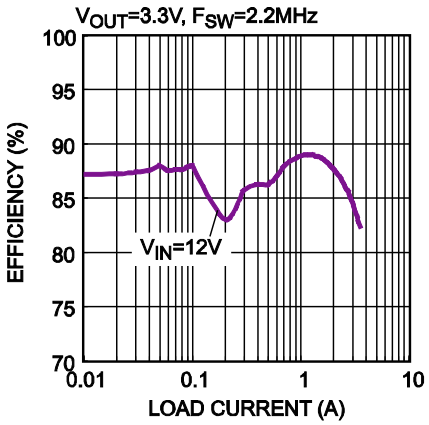
**Efficiency vs. Load Current**



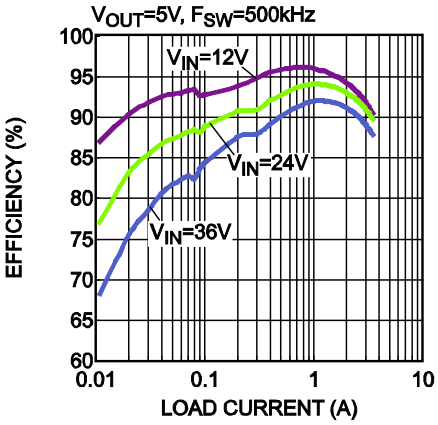

**Efficiency vs. Load Current**



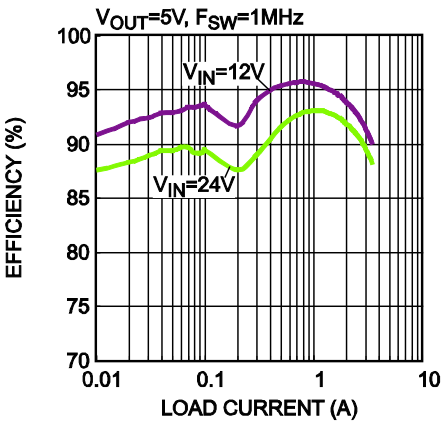

**Efficiency vs. Load Current**



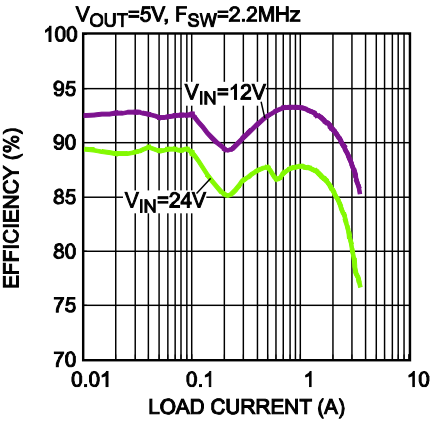

**Efficiency vs. Load Current**



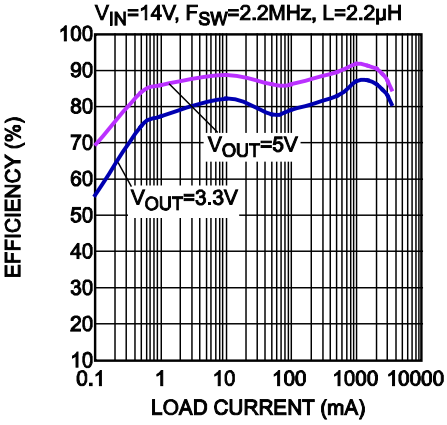

**Efficiency vs. Load Current**



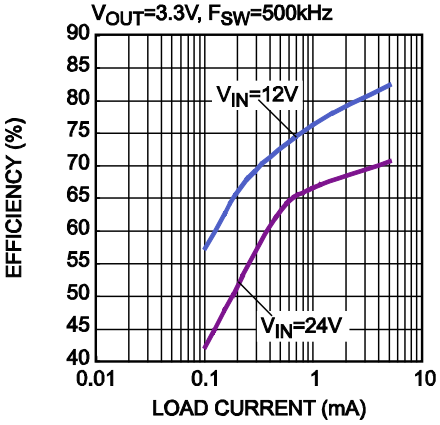

**Efficiency vs. Load Current**



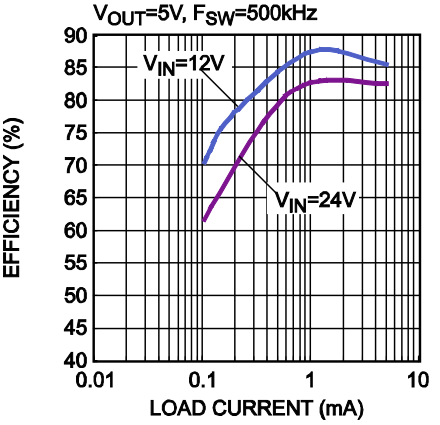

**Efficiency vs. Load Current**




**Efficiency vs. Load Current (Extreme Light Load)**




**Efficiency vs. Load Current (Extreme Light Load)**





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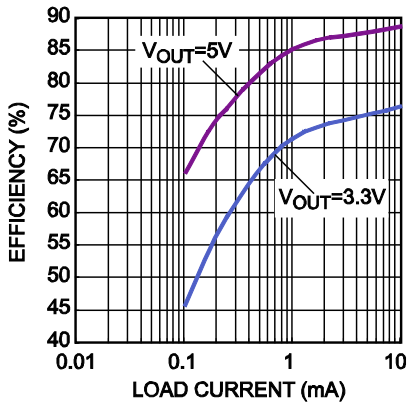
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

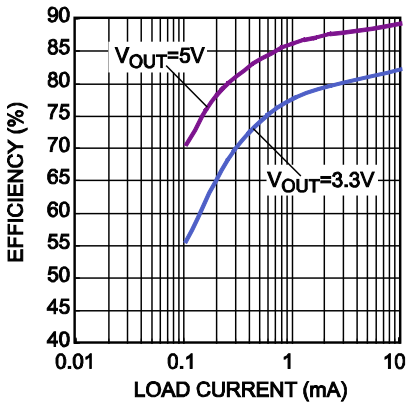
**Efficiency vs. Load Current (Extreme Light Load)**

$V_{IN}$=14V, $F_{SW}$=400kHz



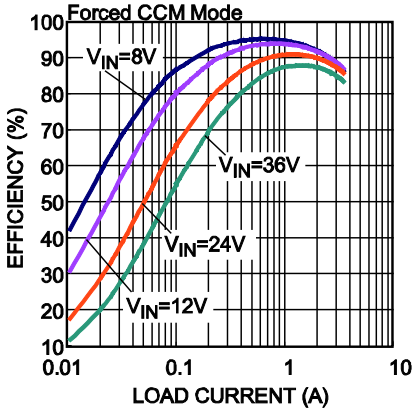

**Efficiency vs. Load Current (Extreme Light Load)**

$V_{IN}$=14V, $F_{SW}$=2.2MHz



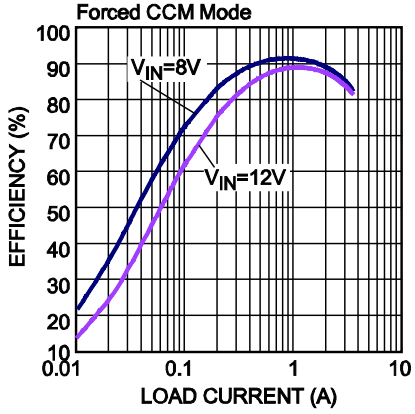

**Efficiency vs. Load Current**

$V_{OUT}$=3.3V, $F_{SW}$=500kHz, Forced CCM Mode



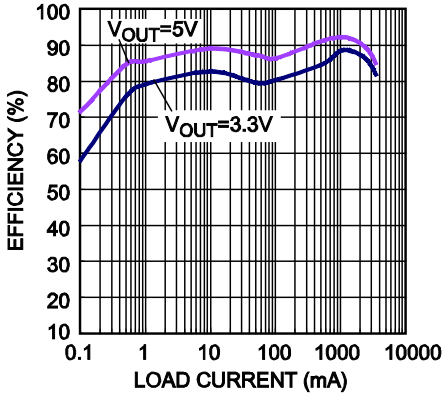

**Efficiency vs. Load Current**

$V_{OUT}$=3.3V, $F_{SW}$=2.2MHz, Forced CCM Mode



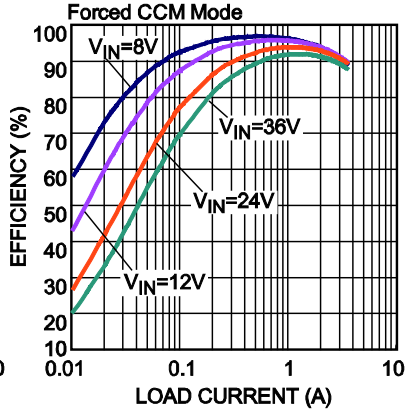

**Efficiency vs. Load Current**

$V_{IN}$=12V, $F_{SW}$=2.2MHz, L=2.2µH



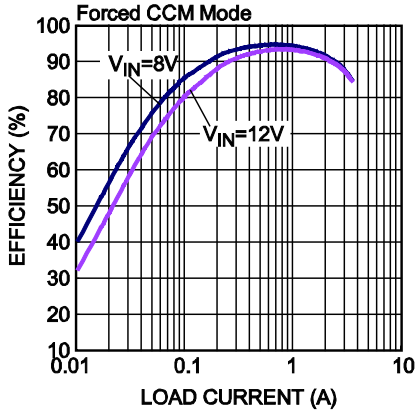

**Efficiency vs. Load Current**

$V_{OUT}$=5V, $F_{SW}$=500kHz, Forced CCM Mode



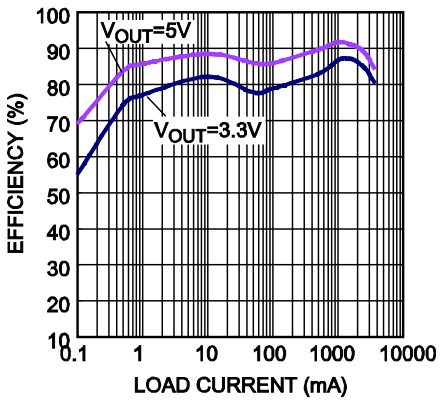

**Efficiency vs. Load Current**

$V_{OUT}$=5V, $F_{SW}$=2.2MHz, Forced CCM Mode



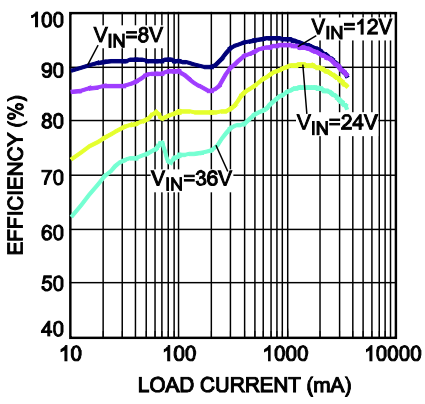

**Efficiency vs. Load Current**

$V_{IN}$=14V, $F_{SW}$=2.2MHz, L=2.2µH




**Efficiency vs. Load Current**

$V_{OUT}$=3.3V, $F_{SW}$=800kHz, L=10µH





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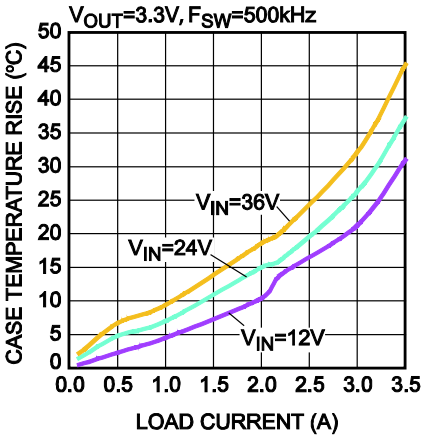
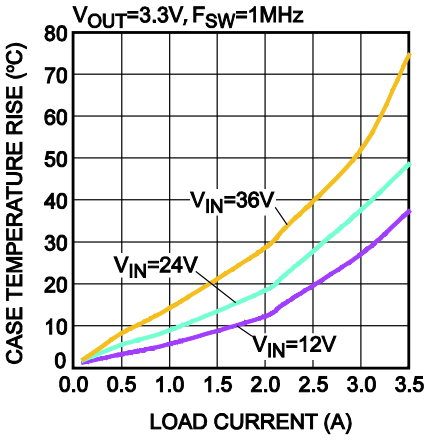
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

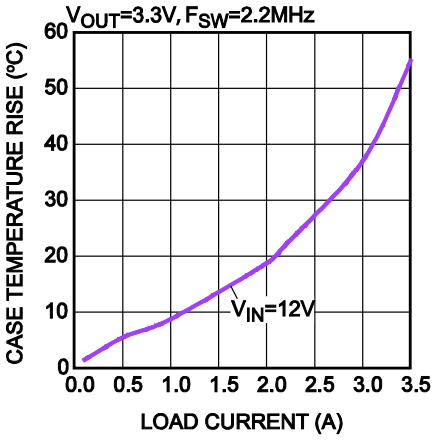
**Case Temperature Rise vs. Load Current**



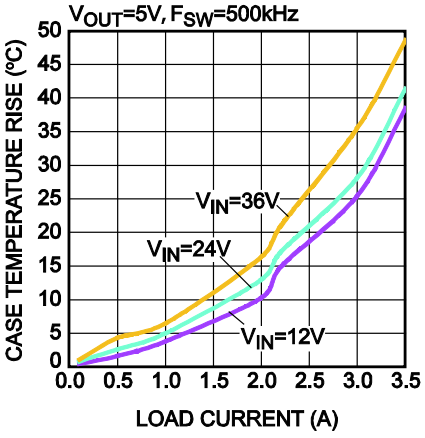

**Case Temperature Rise vs. Load Current**



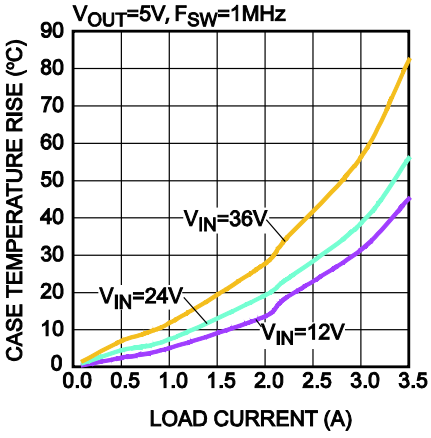

**Case Temperature Rise vs. Load Current**



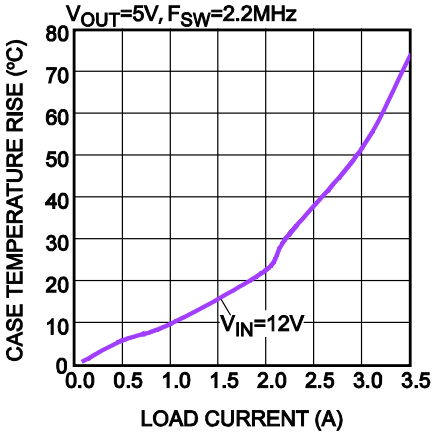

**Case Temperature Rise vs. Load Current**




**Case Temperature Rise vs. Load Current**




**Case Temperature Rise vs. Load Current**





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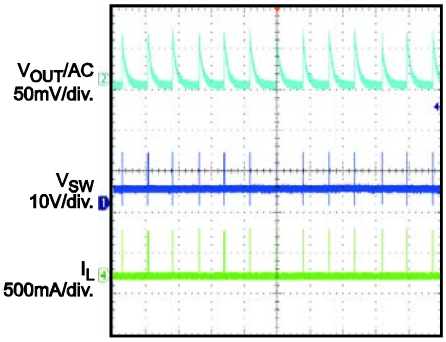
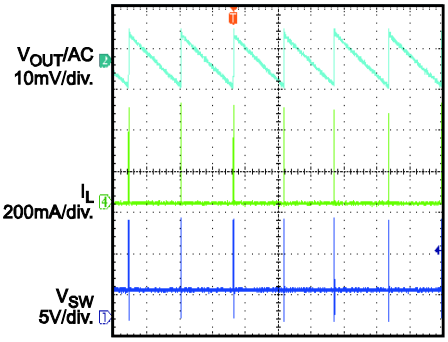
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

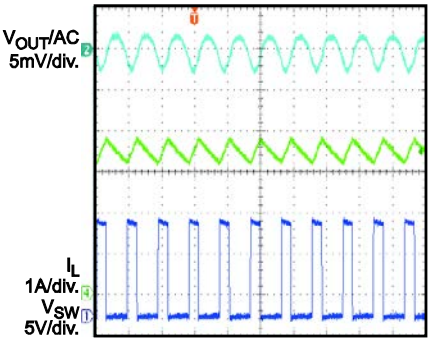
**Steady State**
$I_{OUT}$=0A, AAM Mode



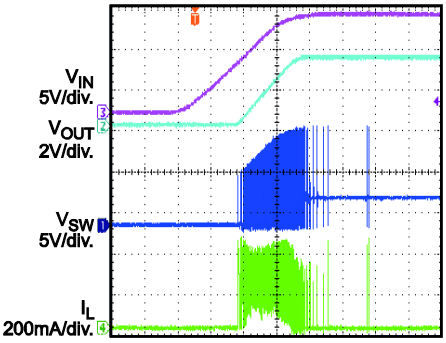

**Steady State**
$I_{OUT}$=1mA, AAM Mode



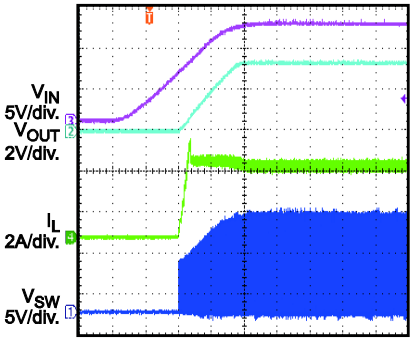

**Steady State**
$I_{OUT}$=3.5A



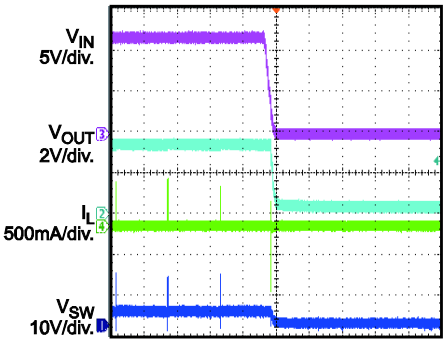

**Start-Up through VIN**
$I_{OUT}$=0A



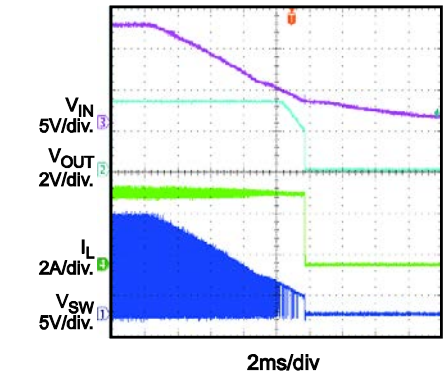

**Start-Up through VIN**
$I_{OUT}$=3.5A



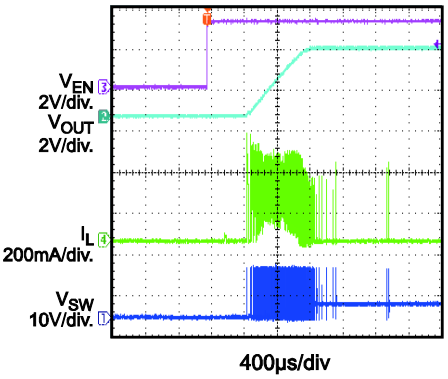

**Shutdown through VIN**
$I_{OUT}$=0A



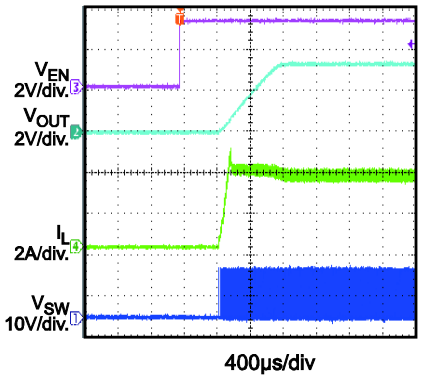

**Shutdown through VIN**
$I_{OUT}$=3.5A




**Start-Up through EN**
$I_{OUT}$=0A




**Start-Up through EN**
$I_{OUT}$=3.5A





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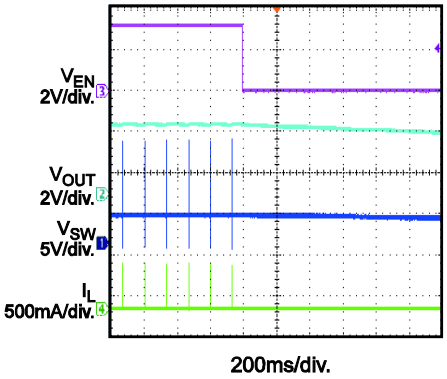
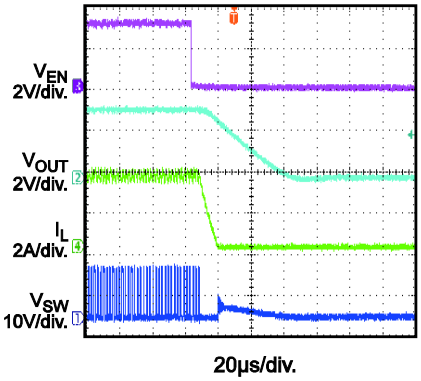
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

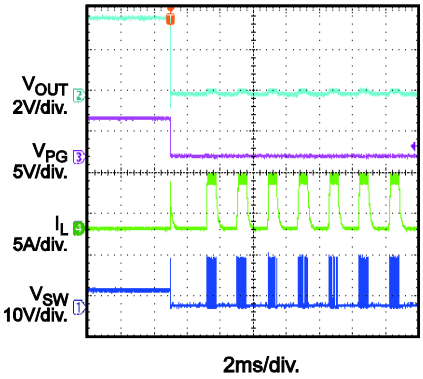
**Shutdown through EN**
$I_{OUT}$=0A



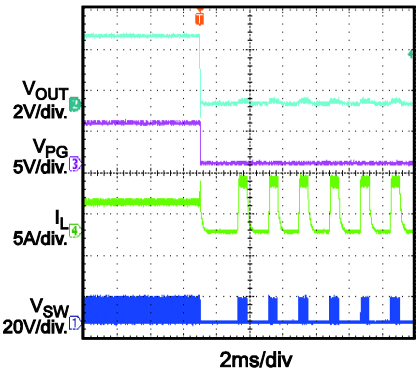

**Shutdown through EN**
$I_{OUT}$=3.5A



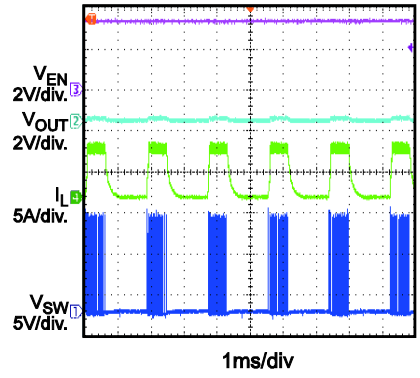

**SCP Entry**
$I_{OUT}$=0A to Short Circuit



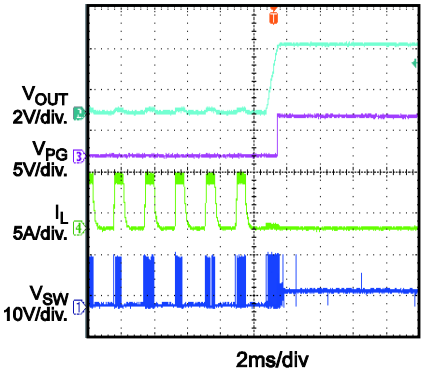

**SCP Entry**
$I_{OUT}$=3.5A to Short Circuit



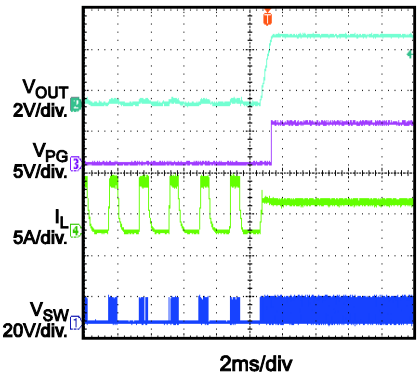

**SCP Steady State**



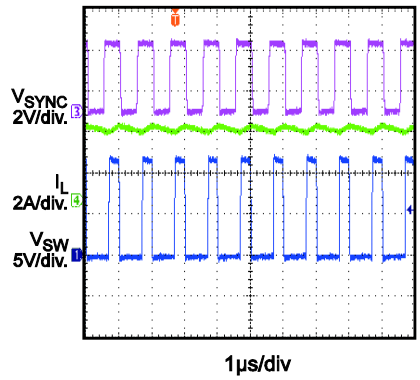

**SCP Recovery**
Short Circuit to $I_{OUT}$=0A



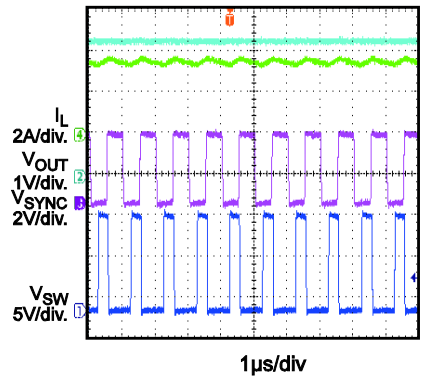

**SCP Recovery**
Short Circuit to $I_{OUT}$=3.5A




**SYNC Operation (In-Phase)**
Drive PHASE High, $I_{OUT}$=3.5A




**SYNC Operation (180° Out-of-Phase)**
Drive PHASE Low, $I_{OUT}$=3.5A





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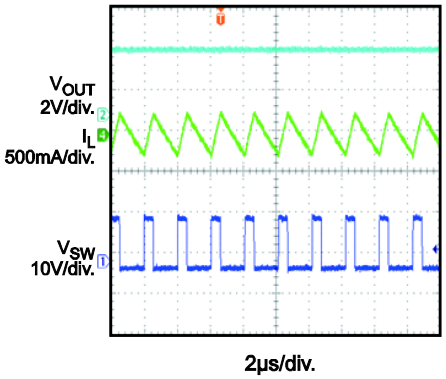
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

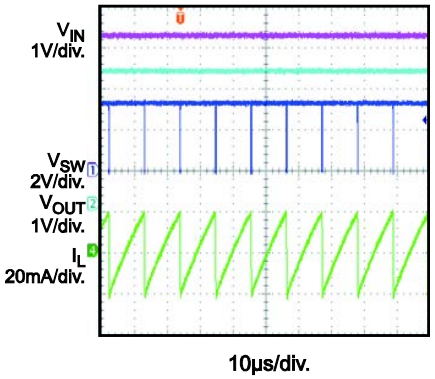
### Forced CCM Operation

$I_{OUT}$=0A, Forced CCM Mode



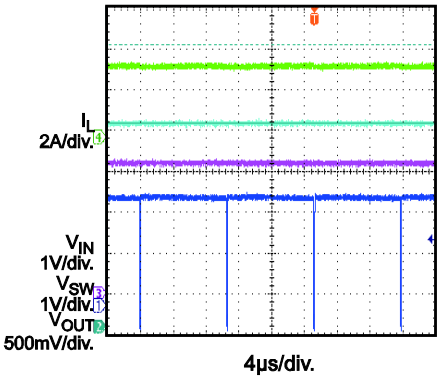

### Dropout Operation

$V_{IN}$=3.3V, $V_{OUT}$ Set to 3.3V, $I_{OUT}$=0A



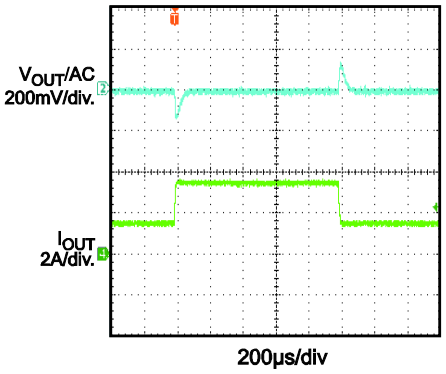

### Dropout Operation

$V_{IN}$=3.3V, $V_{OUT}$ Set to 3.3V, $I_{OUT}$=3.5A



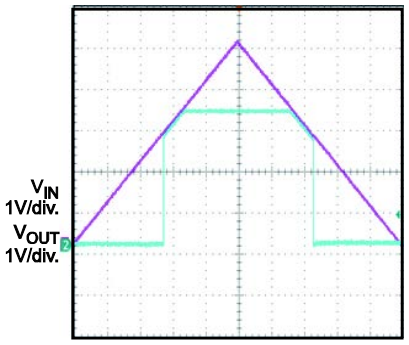

### Load Transient

$I_{OUT}$=1.5A<->3.5A, 1.6A/µs



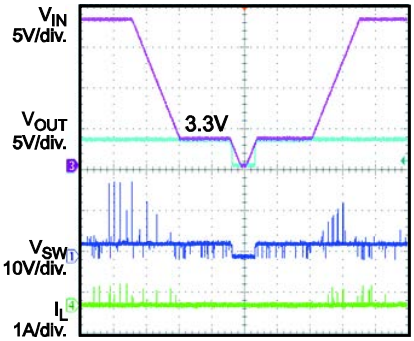

### VIN Ramp Up and Down

$I_{OUT}$=0.1A



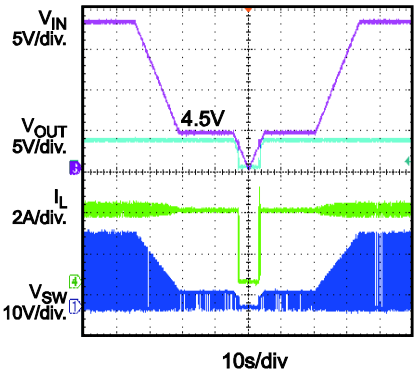

### VIN Ramp Down and Up

$I_{OUT}$=1mA



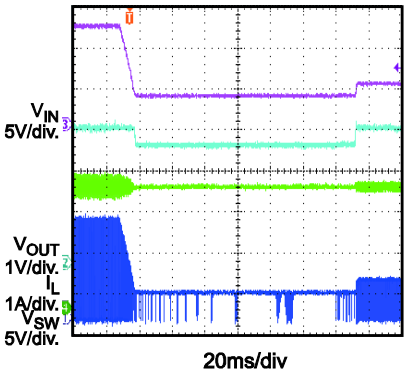

### VIN Ramp Down and Up

$I_{OUT}$=3.5A



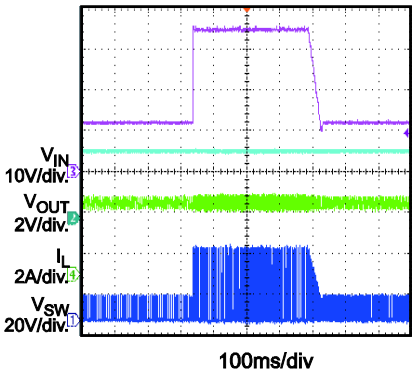

### Cold Crank

$V_{IN}$=12V->3.3V->5V, $I_{OUT}$=3.5A




### Load Dump

$V_{IN}$=12V<->36V, $I_{OUT}$=3.5A





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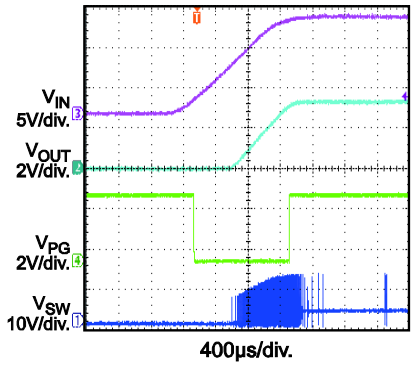
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**VIN = 12V, $V_{OUT}$ = 3.3V, L = 10µH, $F_{SW}$ = 500kHz, AAM, $T_A$ = +25°C, unless otherwise noted.**

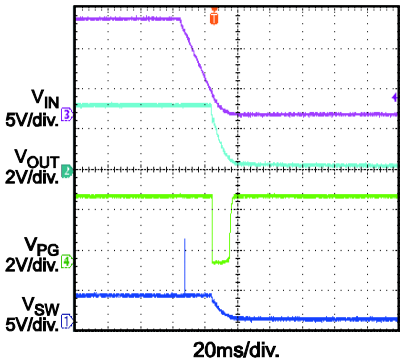
### PG in Start-Up through VIN

$I_{OUT}$ = 0A, PG is Pulled to 3.3V through 100k Resistor



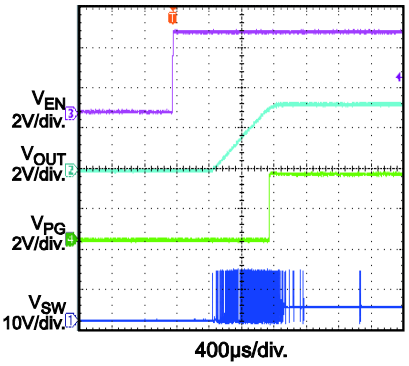

### PG in Shutdown through VIN

$I_{OUT}$ = 0A, PG is Pulled to 3.3V through 100k Resistor



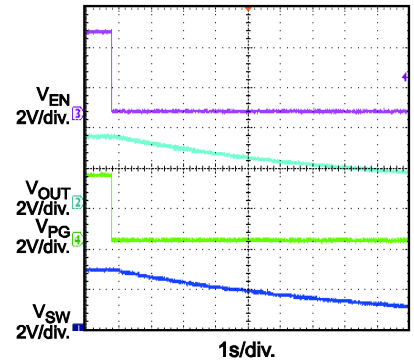

### PG in Start-Up through EN

$I_{OUT}$ = 0A, PG is Pulled to 3.3V through 100k Resistor



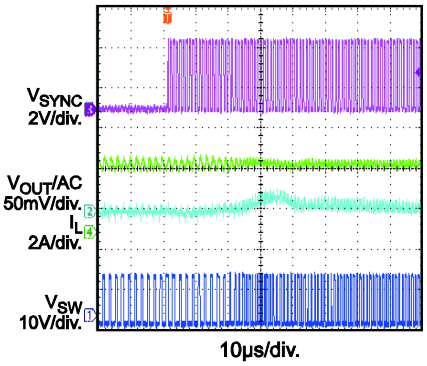

### PG in Shutdown through EN

$I_{OUT}$ = 0A, PG is Pulled to 3.3V through 100k Resistor



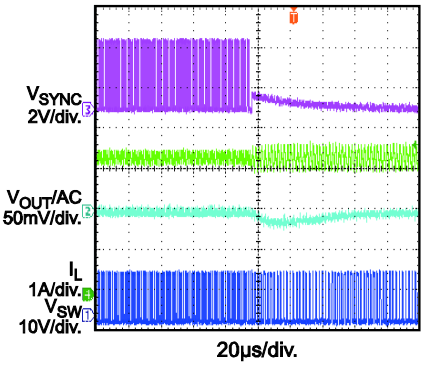

### Sync In Transient

$I_{OUT}$ = 3.5A, SYNC = 1MHz



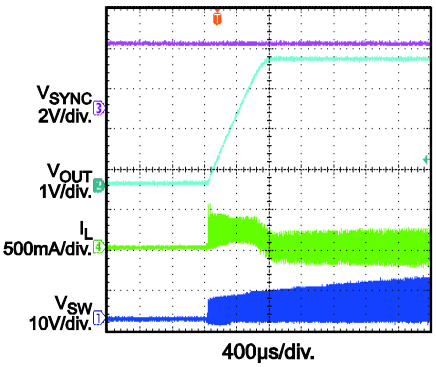

### Sync Out Transient

$I_{OUT}$ = 3.5A, SYNC = 1MHz




### Forced CCM Entry

$I_{OUT}$ = 0A, Pull Sync High before Startup





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## PIN FUNCTIONS

| Pin # QFN-16 (3mmx4mm) | Name | Description |
|---|---|---|
| 1 | PHASE | **Selectable in-phase or 180° out-of-phase of SYNC input.** Pull PHASE high to be in-phase. Pull PHASE low to be 180° out-of-phase. |
| 2 | VIN | **Input supply.** VIN supplies power to all of the internal control circuitries and the power switch connected to SW. Place a decoupling capacitor to ground close to VIN to minimize switching spikes. |
| 3, 10 | SW | **Switch node.** SW is the output of the internal power switch. |
| 4, 9 | PGND | **Power ground.** PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias. |
| 5 | EN | **Enable.** Pull EN below the specified threshold to shut the chip down. Pull EN above the specified threshold to enable the chip. |
| 6 | SYNC | **Synchronize.** Apply a 350kHz to 2.5MHz clock signal to SYNC to synchronize the internal oscillator frequency to the external clock. The external clock should be at least 250kHz larger than the $R_{FREQ}$ set frequency. SYNC can also be used to select forced CCM or AAM. Drive SYNC high before the chip starts up to choose forced CCM; drive SYNC low or leave SYNC floating to choose AAM. |
| 7 | PG | **Power good output.** The output of PG is an open drain. |
| 8 | BIAS | **Bias input.** Connect BIAS to an external power supply ($5V \leq V_{BIAS} \leq 18V$) to reduce power dissipation and increase efficiency. If not in use, float BIAS or connect BIAS to ground. |
| 11 | BST | **Bootstrap.** BST is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between BST and SW. |
| 12 | VCC | **Bias supply.** VCC supplies power to the internal control circuit and gate drivers. A decoupling capacitor (≥1μF) to ground is required close to VCC. |
| 13 | AGND | **Analog ground.** AGND is the reference ground of the logic circuit. |
| 14 | SS | **Soft-start input.** Place a capacitor from SS to AGND to set the soft-start period. The MP9840 sources 10μA from SS to the soft-start capacitor during start-up. As the SS voltage rises, the feedback threshold voltage increases to limit inrush current during start-up. |
| 15 | FB | **Feedback input.** Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.8V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces. |
| 16 | FREQ | **Switching frequency program.** Connect a resistor from FREQ to ground to set the switching frequency. |


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## BLOCK DIAGRAM

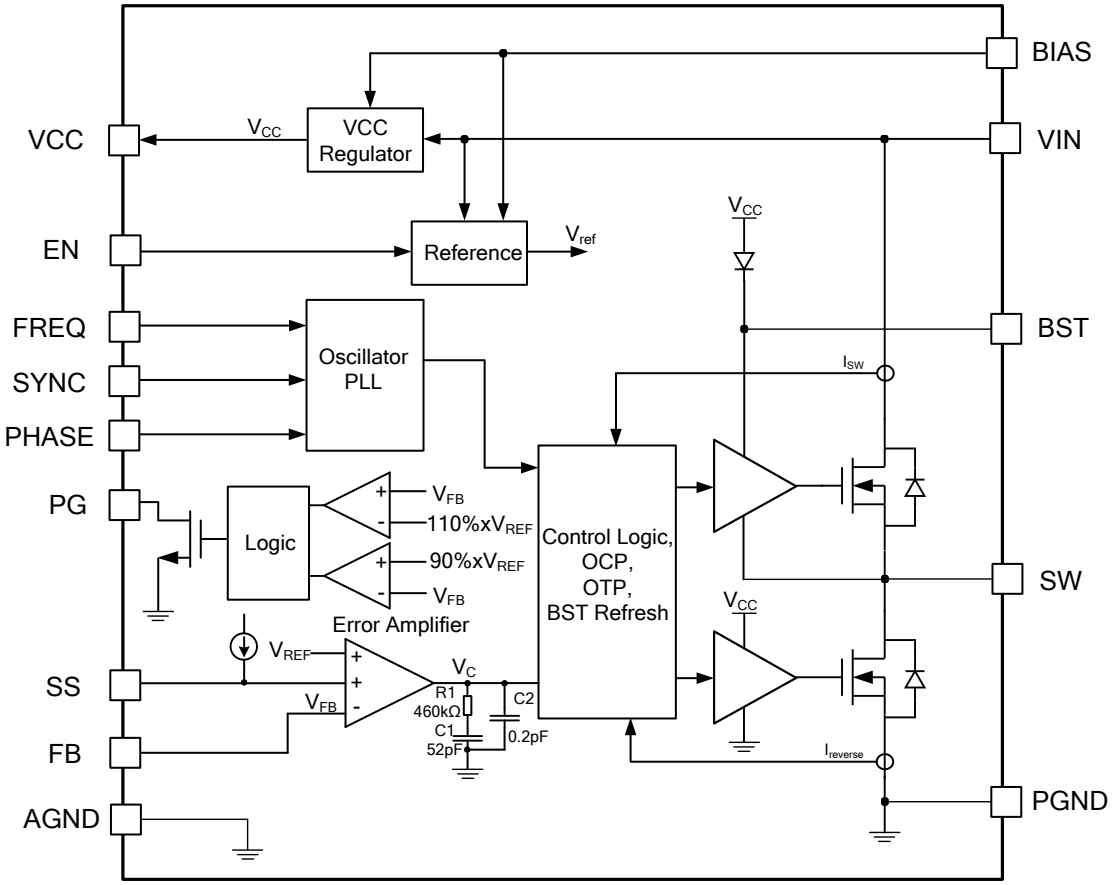


**Figure 1: Functional Block Diagram**


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## OPERATION

The MP9840 is a synchronous, step-down, switching regulator with integrated, internal, high-side and low-side power MOSFETs. The MP9840 provides 3.5A of highly efficient output current with current mode control.

The MP9840 features a wide input voltage range, switching frequency programmable from 350kHz to 2.5MHz, external soft start, and precision current limit. Its very low operational quiescent current makes it suitable for battery-powered applications.

### Pulse-Width Modulation (PWM) Control

At moderate-to-high output currents, the MP9840 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the rising edge of the clock, the high-side power MOSFET (HS-FET) is turned on and remains on until its current reaches the value set by the COMP voltage ($V_{COMP}$). If the current in the HS-FET does not reach $V_{COMP}$ in one PWM period, the HS-FET remains on, saving a turn-off operation.

When the high-side power switch is off, the low-side MOSFET (LS-FET) is turned on immediately and remains on until the next cycle begins.

For each turn-on and -off in a switching cycle, the HS-FET turns on and off with a minimum on and off time limit.

### Advanced Asynchronous Mode (AAM)

The MP9840 employs advanced asynchronous mode (AAM) functionality to optimize efficiency during light-load or no-load conditions. AAM can be enabled by connecting SYNC to a low level (<2V) before start-up; AAM can be disabled when connecting SYNC to a high level before start-up. SYNC can be used to synchronize switching again after start-up.

If continuous conduction mode (CCM) is enabled, the device is forced to work with a fixed frequency regardless of the output load current. The advantage of CCM is the controllable frequency and smaller output ripple, but it also has low efficiency at light load (see Figure 2).

If AAM is enabled, the MP9840 first enters non-synchronous operation for as long as the inductor current is approaching zero at light load. If the load is further decreased or is at no load, $V_{COMP}$ drops below the AAM voltage ($V_{AAM}$), making the MP9840 enter power-save mode (PSM). This puts the chip into sleep mode, which consumes very low quiescent current to further improve light-load efficiency.

In PSM, the internal clock is reset whenever $V_{COMP}$ crosses over $V_{AAM}$, and the crossover time is taken as the benchmark of the next clock. When the load increases, and the DC value of $V_{COMP}$ is higher than $V_{AAM}$, the operation mode is discontinuous conduction mode (DCM) or CCM, which have a constant switching frequency.

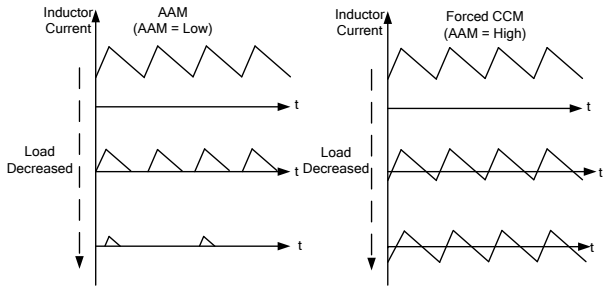


**Figure 2: AAM and Forced CCM**

### Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage with the internal reference (0.8V) and outputs a current proportional to the difference between the two. This output current is used to charge or discharge the internal compensation network to form $V_{COMP}$, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

### Bootstrap Charging

The bootstrap capacitor (0.1µF to 1µF) is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW nodes is lower than its regulation, a PMOS pass transistor connected from VIN to BST is turned on. The charging current path is from VIN to BST to SW. An external circuit should provide enough voltage headroom to facilitate charging.


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When the HS-FET is on, VIN is about equal to SW, so the bootstrap capacitor cannot be charged.

At a higher duty cycle operation condition, the time period available to the bootstrap charging is less, so the bootstrap capacitor may not be charged sufficiently. In case the external circuit does not have sufficient voltage or time to charge the bootstrap capacitor, extra external circuitry can be used to ensure that the bootstrap voltage is in the normal operation region.

### Low Dropout Operation (BST Refresh)

To improve dropout, the MP9840 is designed to operate at close to 100% duty cycle for as long as the BST to SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET is turned off using an under-voltage lockout (UVLO) circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. In DCM or PSM, the LS-FET is forced on to refresh the BST voltage.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor, making the effective duty cycle of the switching regulator high.

The effective duty cycle during the dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode and printed circuit board resistance.

### Internal Regulator

Most of the internal circuitry is powered on by the 2.6V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 3V, the output of the regulator is in full regulation. When VIN is lower than 3V, the output degrades.

For better thermal performance, connect BIAS to an external 5V source. VCC and the internal circuit are powered by BIAS. Since there is an internal diode between BIAS and the internal circuit, float BIAS or connect BIAS to GND if it is not being used.

### Enable (EN) Control

EN is a digital control pin that turns the regulator on and off by either the external logic H/L signal or programming the VIN UVLO (see Figure 3). When EN is pulled below its threshold voltage, the MP9840 is put into the lowest shutdown current mode. Forcing EN above the EN threshold voltage turns the MP9840 on. With a high enough VIN, the MP9840 can be enabled and disabled by EN. Do not float EN.

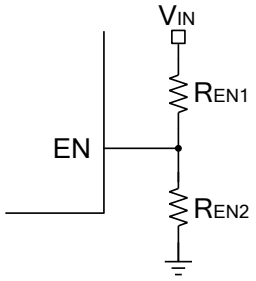


**Figure 3: Enable Divider Circuit**

### Programmable Frequency (FREQ)

The MP9840 oscillating frequency is programmed either by an external resistor ($R_{FREQ}$) from FREQ to ground or by a logic level SYNC signal. The value of $R_{FREQ}$ can be calculated with Equation (1):

$$R_{FREQ}(k\Omega) = \frac{170000}{f_s^{1.11}(kHz)} \quad (1)$$

The chip can be synchronized to an external clock ranging from 350kHz up to 2.5MHz through FREQ/SYNC.

### SYNC and PHASE

The internal oscillator frequency can be synchronized to an external clock ranging from 350kHz up to 2.5MHz through SYNC. The external clock should be at least 250kHz larger than the $R_{FREQ}$ set frequency. Ensure that the high amplitude of the SYNC clock is higher than 1.8V and the low amplitude is lower than 0.4V. There is no pulse width requirement, but there is always parasitic capacitance of the pad, so if the pulse width is too short, a clear rising and falling edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in application.


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PHASE is used when two or more MP9840 devices are in parallel with the same SYNC clock. Pulling PHASE high forces the MP9840 to operate in-phase of the SYNC clock. Pulling PHASE low forces the device to be 180° out-of-phase of the SYNC clock. By setting different voltages for PHASE, two devices can operate 180° out-of-phase to reduce the total input current ripple, so a smaller input bypass capacitor can be used (see Figure 4). The PHASE rising threshold is about 2.5V with a 400mV hysteresis.

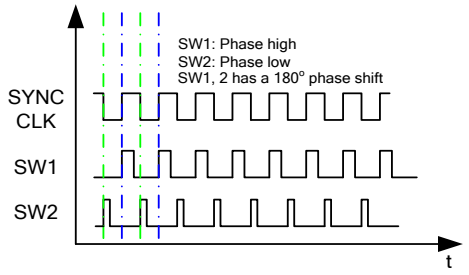


**Figure 4: In-Phase and 180° Out-of-Phase**

### Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the soft-start period begins, an internal current source charges the external soft-start capacitor. When the soft-start voltage (SS) is lower than the internal reference (REF), SS overrides REF, so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. $C_{SS}$ can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (2)$$

Where $C_{SS}$ is the external SS capacitor, $V_{REF}$ is 0.8V, and $I_{SS}$ is the internal 10μA SS charge current.

SS can be used for tracking and sequencing.

### Pre-Bias Start-Up

During start-up, if FB is greater than SS - 150mV, which means the output has a pre-bias voltage, then neither the HS-FET nor LS-FET turn on until SS is higher than FB.

### Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from running away thermally. When the silicon die temperature is higher than its upper threshold, the power MOSFETs are shut down. When the temperature is lower than its lower threshold, thermal shutdown is removed and the chip is enabled again.

### Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current sense MOSFET. The current is then fed to the high-speed current comparator for current-mode control purposes. The current comparator takes this sensed current as one of its inputs. When the HS-FET is turned on, the comparator is first blanked until the end of the turn-on transition to avoid noise. Then the comparator compares the power switch current with $V_{COMP}$. When the sensed current is higher than $V_{COMP}$, the comparator outputs low to turn off the HS-FET. The maximum current of the internal power MOSFET is limited cycle-by-cycle internally.

### Hiccup Protection

When the output is shorted to ground, causing the output voltage to drop below 55% of its nominal output, the IC is shut down momentarily and begins discharging the soft-start capacitor. The IC restarts with a full soft start when the soft-start capacitor is fully discharged. This hiccup process is repeated until the fault is removed.

### Start-Up and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the rest of the circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50μs to blank any start-up glitches. When the soft-start block is enabled, the SS output is held low to ensure that the rest of the circuitries are ready before slowly ramping up.


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Three events can shut down the chip: EN low, VIN low, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. $V_{COMP}$ and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

**Power Good (PG) Output**

The MP9840 includes an open-drain power good (PG) output that indicates whether the regulator output is within ±10% of its nominal output range. When the output voltage moves outside of this range, the PG output is pulled to ground.


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# APPLICATION INFORMATION

## Setting the Output Voltage

The external resistor divider connected to FB sets the output voltage (see Figure 5).

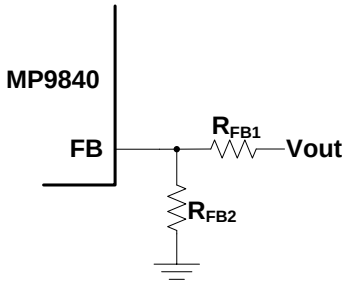


**Figure 5: Feedback Network**

Choose $R_{FB1}$ to be around 40kΩ. $R_{FB2}$ can then be calculated with Equation (3):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.8V} - 1} \quad (3)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

**Table 1: Resistor Selection for Common Output Voltages**

| $V_{OUT}$ (V) | $R_{FB1}$ (kΩ) | $R_{FB2}$ (kΩ) |
|---|---|---|
| 3.3 | 41.2 (1%) | 13 (1%) |
| 5 | 68.1 (1%) | 13 (1%) |

## Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can then be calculated with Equation (4):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where $\Delta I_L$ is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (5):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

## Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower-value capacitor (e.g.: 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since $C_{IN}$ absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g.: 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.


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The input voltage ripple caused by the capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

### Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

Where L is the inductor value, and $R_{ESR}$ is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP9840 can be optimized for a wide range of capacitance and ESR values.

### VIN UVLO Setting

The MP9840 has an internal, fixed, UVLO threshold. The rising threshold is 2.8V, while the falling threshold is about 2.65V. For applications that require a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 6).

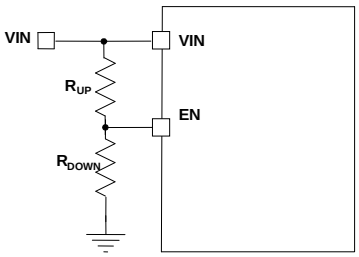


**Figure 6: Adjustable UVLO Using EN Divider**

The UVLO threshold can be calculated with Equation (12) and Equation (13):

$$INUV_{RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_RISING} \quad (12)$$

$$INUV_{FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_FALLING} \quad (13)$$

Where $V_{EN_RISING}$ is 1.05V, and $V_{EN_FALLING}$ is 0.93V.

### External BST Diode and Resistor

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external bootstrap diode. VCC or $V_{OUT}$ is recommended to be the power supply in the circuit (see Figure 7).

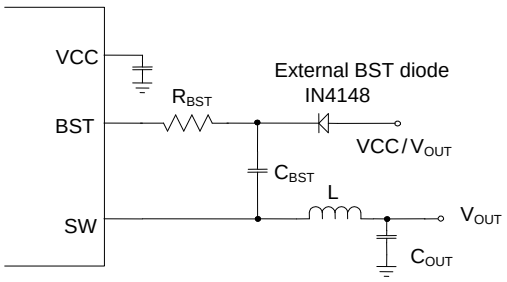


**Figure 7: Optional External Bootstrap Diode to Enhance Efficiency**

The recommended external BST diode is IN4148, and the recommended BST capacitor value is 0.1μF to 1μF.

A resistor in series with the BST capacitor ($R_{BST}$) can reduce the SW rising rate and voltage spikes. This helps enhance EMI performance and reduce the voltage stress at a high VIN. A higher resistance is better for SW spike reduction but compromises efficiency. To make a tradeoff between EMI and efficiency, a ≤20Ω $R_{BST}$ is recommended.


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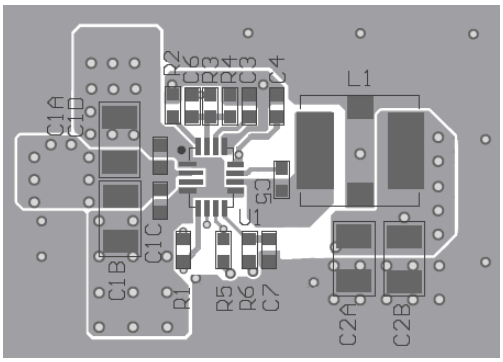
## PCB Layout Guidelines [6]

Efficient PCB layout, is critical for stable operation, especially for the input capacitor placement. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 8 and follow the guidelines below.

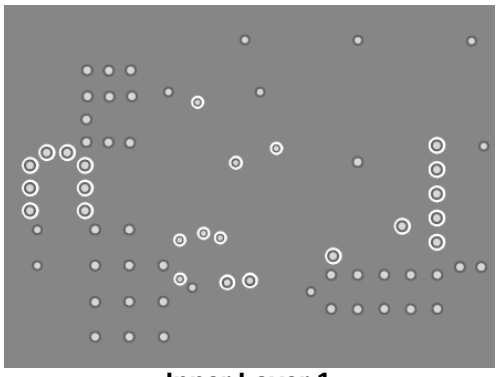
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect to PGND directly.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitors, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas such as FB.
9. Place the feedback resistors close to the chip to ensure that the trace connecting to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

**NOTE:**

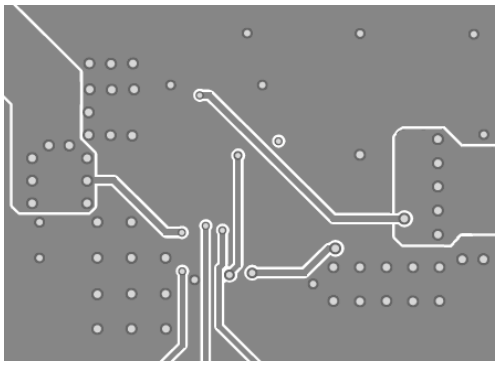
6) The recommended PCB layout is based on Figure 9.



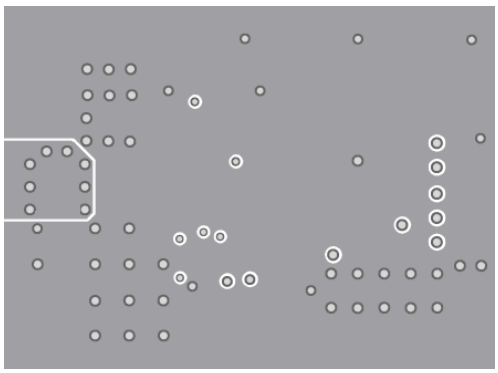

**Top Layer**



**Inner Layer 1**



**Inner Layer 2**



**Bottom Layer**

**Figure 8: Recommended PCB Layout**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# TYPICAL APPLICATION CIRCUITS

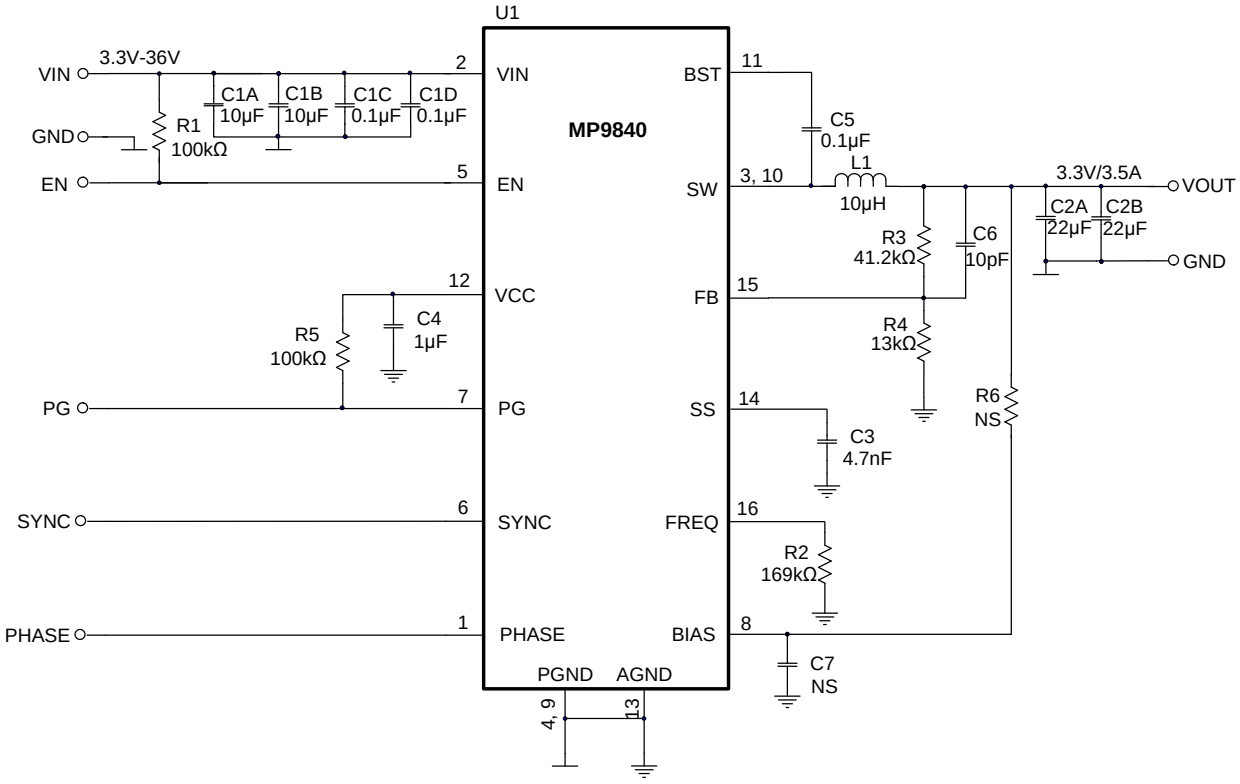


**Figure 9: $V_{OUT}$ = 3.3V, $F_{SW}$ = 500kHz**

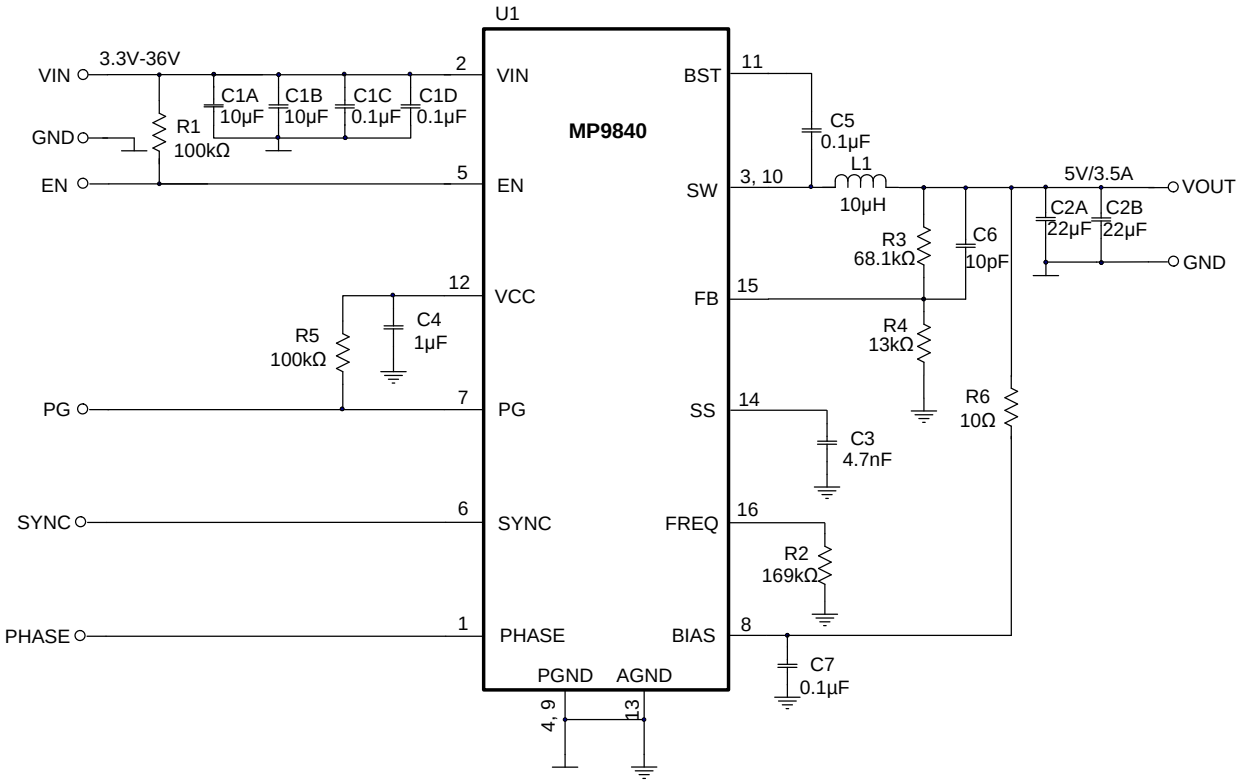


**Figure 10: $V_{OUT}$ = 5V, $F_{SW}$ = 500kHz**


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## TYPICAL APPLICATION CIRCUITS *(continued)*

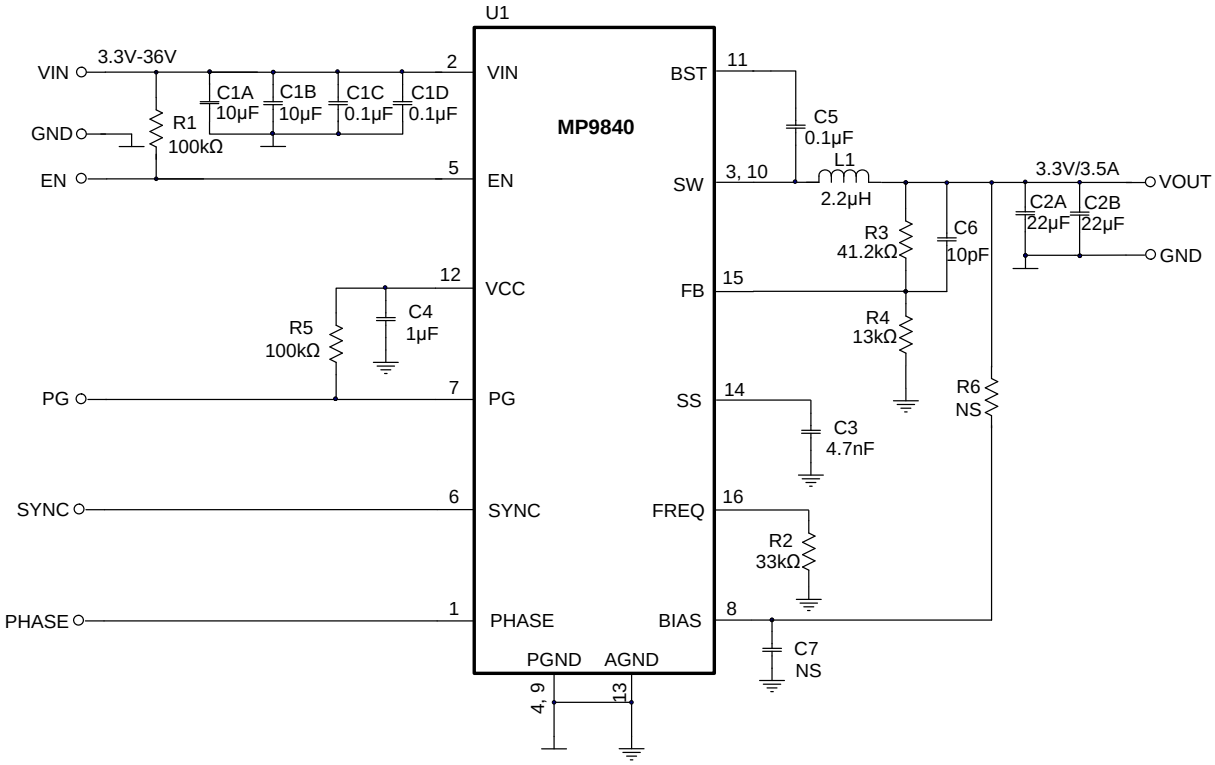


**Figure 11: $V_{OUT}$ = 3.3V, $F_{SW}$ = 2.2MHz**

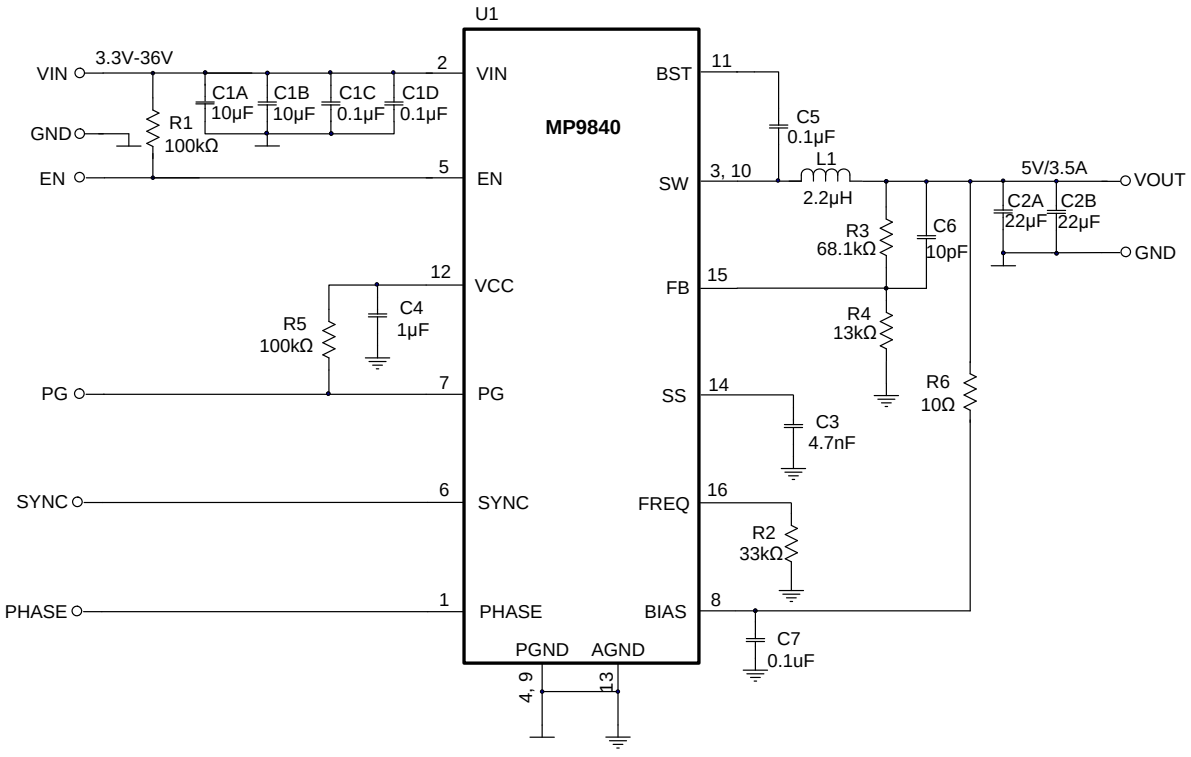


**Figure 12: $V_{OUT}$ = 5V, $F_{SW}$ = 2.2MHz**


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## TYPICAL APPLICATION CIRCUITS *(continued)*

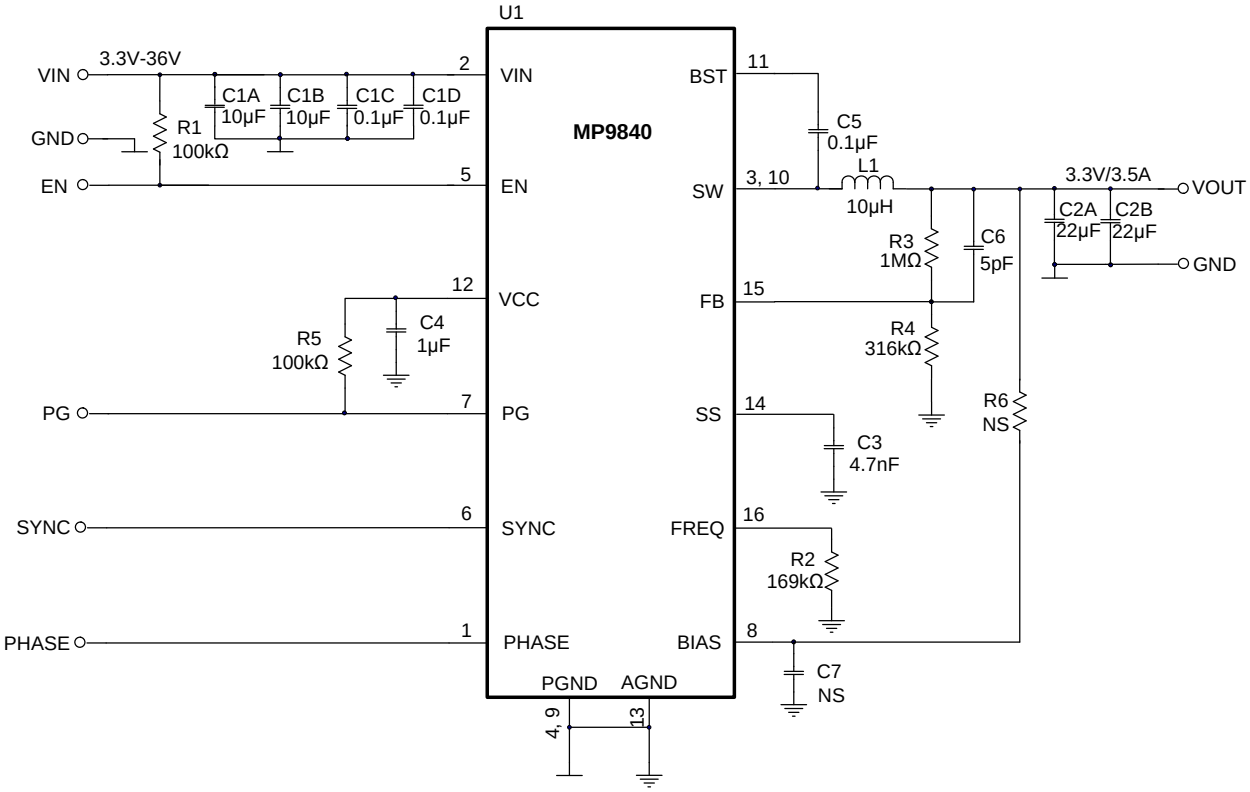


**Figure 13: $V_{OUT}$ = 3.3V, $F_{SW}$ = 500kHz for Big FB Resistor Divider Application**

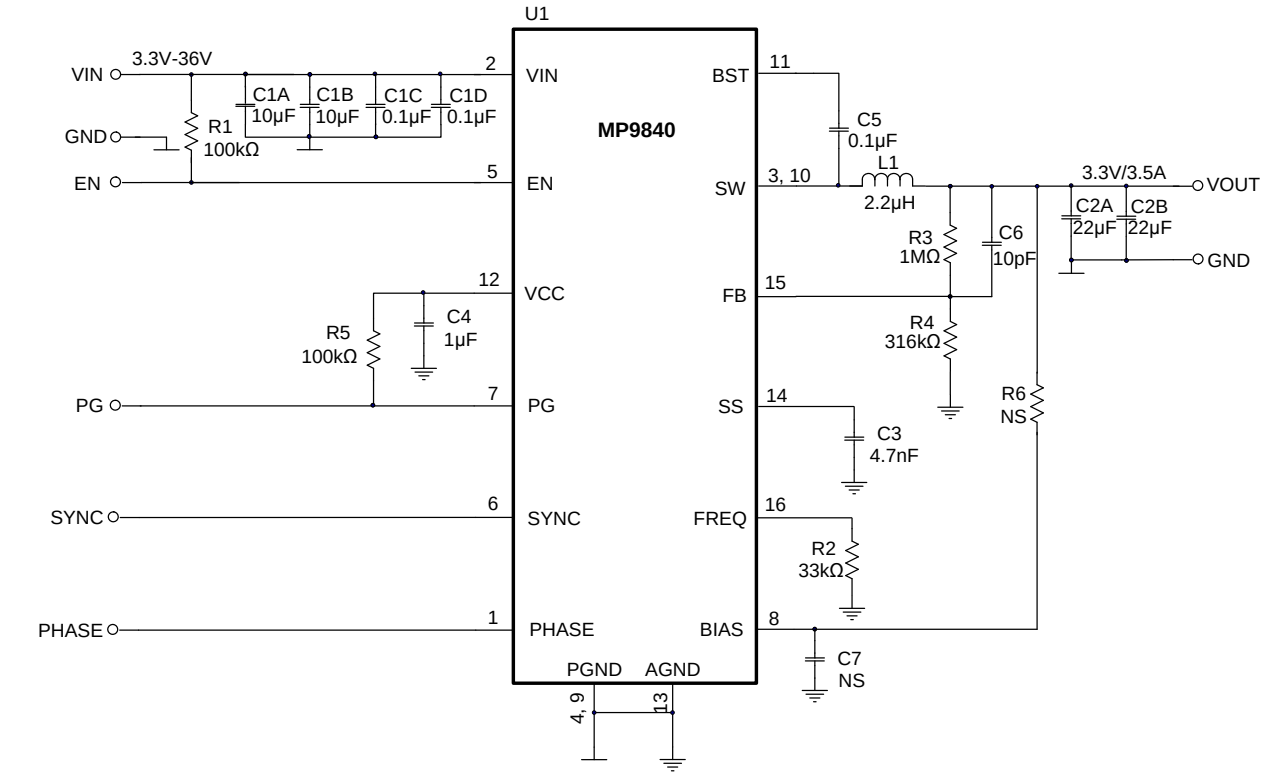


**Figure 14: $V_{OUT}$ = 3.3V, $F_{SW}$ = 2.2MHz for Big FB Resistor Divider Application**


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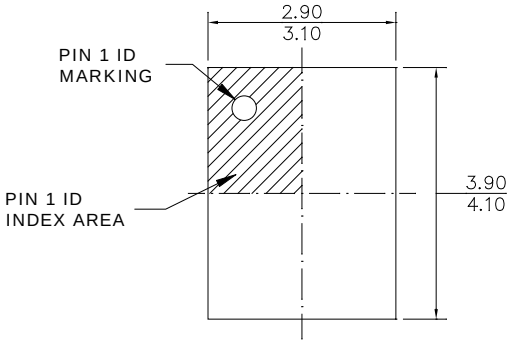
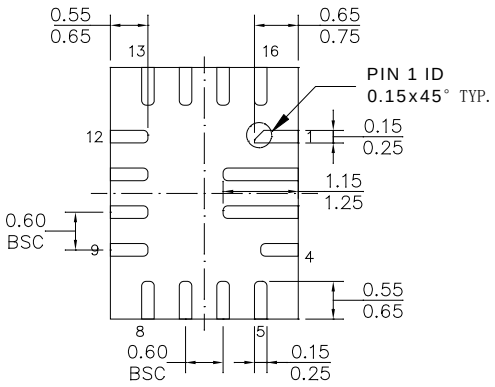
# PACKAGE INFORMATION

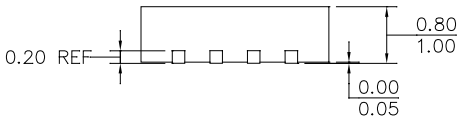
## QFN-16 (3mmx4mm)



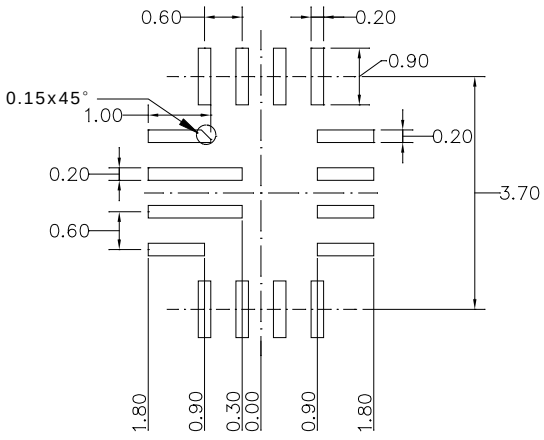

TOP VIEW




BOTTOM VIEW




SIDE VIEW




RECOMMENDED LAND PATTERN

NOTE:

**1) ALL DIMENSIONS ARE IN MILLIMETERS.**
**2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.**
**3) JEDEC REFERENCE IS MO-220.**
**4) DRAWING IS NOT TO SCALE.**

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