

DESCRIPTION

The MP8902 is a low-noise, low-dropout linear regulator. It operates from 2.7V to 6.5V input voltage, and regulates the output voltage with 2% accuracy at 2.5V, 3.3V, or from 1.25V to 5V.

The MP8902 can supply up to 250mA of load current. The MP8902 features thermal overload protection. It is available in a 2mm x 2mm 8-pin QFN package.

FIXED VOLTAGE PART NUMBERS

Part Number	Output Voltage
MP8902DG-2.5	2.5V
MP8902DG-3.3	3.3V

FEATURES

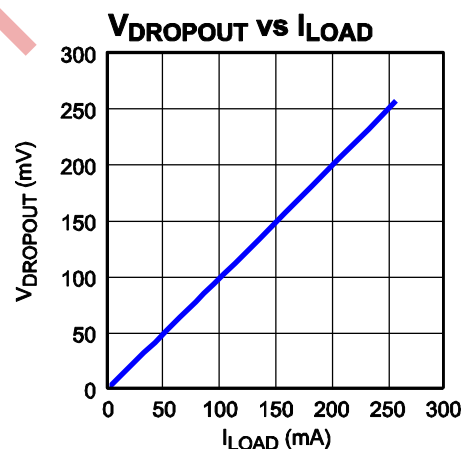
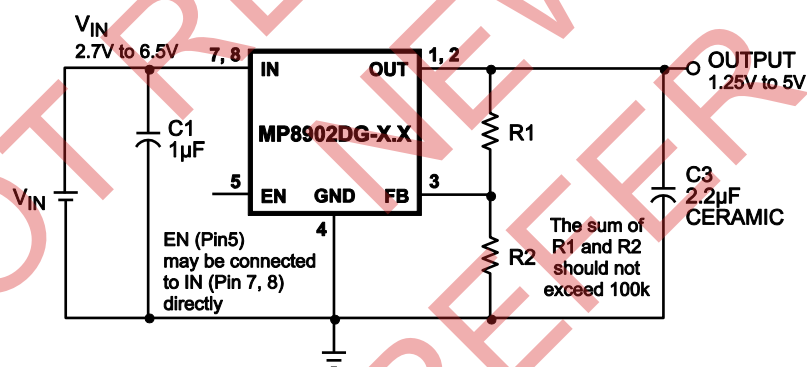
- Low 250mV Dropout at 250mA Output
- 2% Accurate Output Voltage
- Fixed Output Voltage Options of 2.5V or 3.3V
- Adjustable Output Voltage Option from 1.25V to 5V using an External Resistor Divider
- Up to 6.5V Input Voltage
- High PSRR
 - 70dB at 1kHz
 - 30dB at 1MHz
- Better Than 0.001%/mA Load Regulation
- Stable With Low-ESR Output Capacitor
- Low 125µA Ground Current
- Internal Thermal Protection

APPLICATIONS

- 802.11 PC Cards
- Mobile Handset PLL Power
- Audio Codec Power

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP8902DG–2.5	QFN8 (2x2)		–40°C to +85°C
Part Number**	Package	Top Marking	Temperature
MP8902DG–3.3	QFN8 (2x2)		–40°C to +85°C

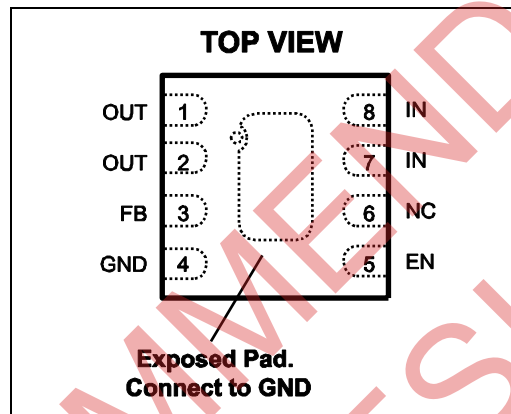
* For Tape & Reel, add suffix –Z (e.g. MP8902DG–2.5–Z).

For RoHS compliant packaging, add suffix –LF (e.g. MP8902DG–2.5–LF–Z)

** For Tape & Reel, add suffix –Z (e.g. MP8902DG–3.3–Z).

For RoHS compliant packaging, add suffix –LF (e.g. MP8902DG–3.3–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN Supply Voltage	–0.3V to +7.0V
FB Voltage	–0.3V to $V_{OUT} + 0.3V$
All Other Pins	–0.3V to +6V
Continuous Power Dissipation ($T_A = +25^\circ C$) ⁽²⁾	1.6W
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	–65°C to +150°C

Recommended Operating Conditions ⁽³⁾

Input Voltage	2.7V to 6.5V
Output Voltage	1.25V to 5V
Load Current	250mA Maximum
Operating Temperature	–40°C to +85°C

Thermal Resistance ⁽⁴⁾

QFN8 (2x2)	θ_{JA} 80	θ_{JC} 16	°C/W
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Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) – T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS
 $V_{IN} = 5V$, $T_A = +25^\circ C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ ⁽⁵⁾	Max	Units
Operating Voltage		$I_{OUT} = 1mA$	2.7		6.5	V
Output Voltage Accuracy		$I_{OUT} = 1mA$, $V_{OUT} = 1.25V$ to $5V$	2.0	± 1.0	2.0	%
Ground Pin Current		$I_{OUT} = 1mA$ – $250mA$		125	155	μA
Shutdown Current		$V_{EN} = 0V$, $V_{IN} = 5V$		0.1	1	μA
FB Regulation Voltage			1.197	1.222	1.246	V
		$-40^\circ C \leq T_A \leq +85^\circ C$	1.194	1.222	1.249	
Dropout Voltage ⁽⁶⁾		$I_{OUT} = 250mA$	$V_{OUT} = 3V$	230		mV
			$V_{OUT} = 4V$	190		
Line Regulation		$I_{OUT} = 1mA$, $V_{IN} = (V_{OUT} + 0.5V)$ to $6.5V$ ⁽⁷⁾		0.005	0.08	%/V
Load Regulation		$I_{OUT} = 1mA$ to $250mA$, $V_{IN} = V_{OUT} + 0.5V$ ⁽⁷⁾		0.001	0.02	%/mA
PSRR		$V_{IN} > V_{OUT} + 0.5V$, $C_{OUT} = 2.2\mu F$, $V_{IN(AC)} = 100mV$, $f = 1kHz$		70		dB
		$V_{IN} > V_{OUT} + 0.5V$, $C_{OUT} = 2.2\mu F$, $V_{IN(AC)} = 100mV$, $f = 1MHz$		30		dB
Output Voltage Noise		$f = 1kHz$, $C_{FB} > 0.1\mu F$, $I_{OUT} = 1mA$		300		nV/\sqrt{Hz}
EN Input High Voltage					1.5	V
EN Input Low Voltage			0.4			V
EN Input Bias Current		$V_{EN} = 0V$, $5V$		0.01	1	μA
Thermal Protection				155		$^\circ C$
Thermal Protection Hysteresis				30		$^\circ C$

Notes:

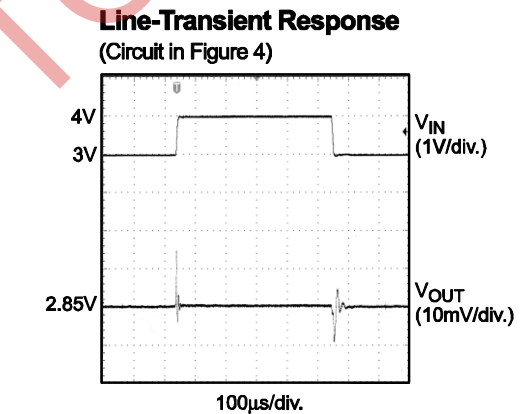
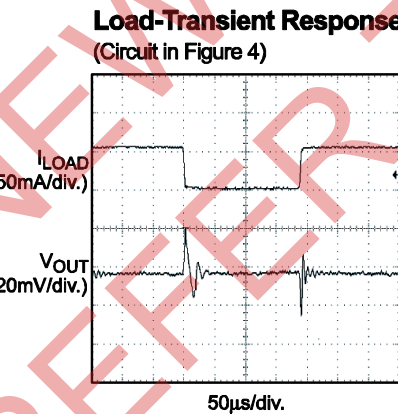
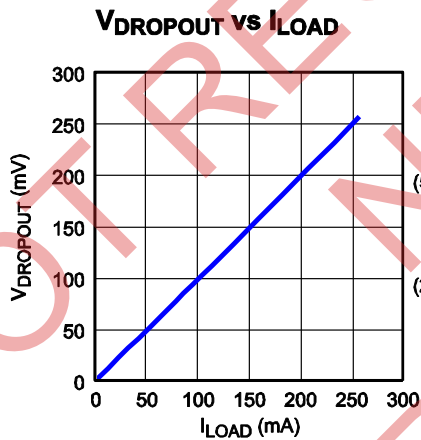
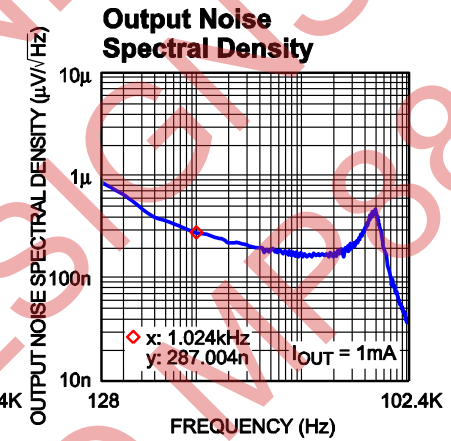
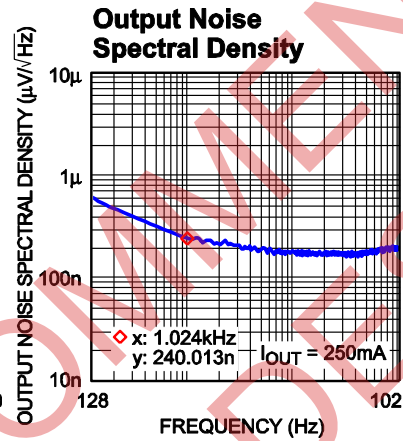
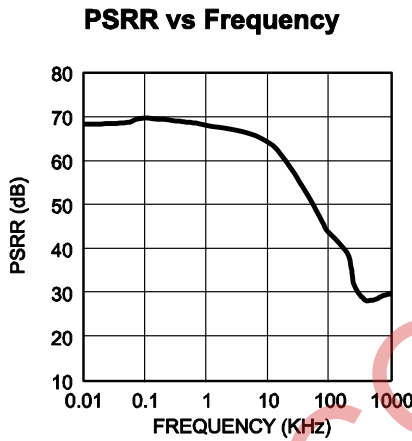
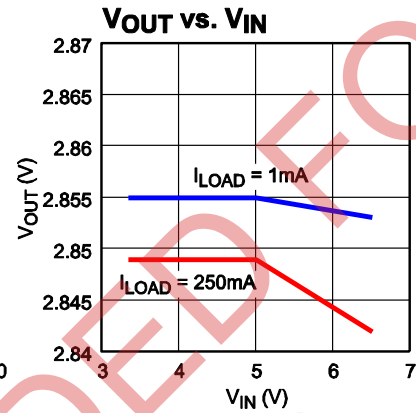
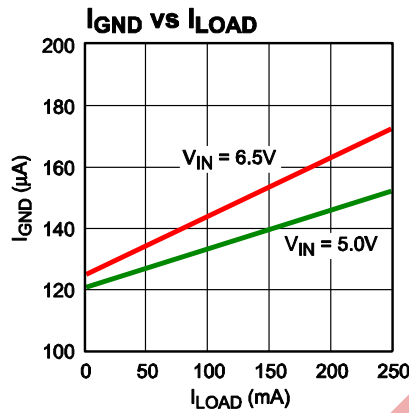
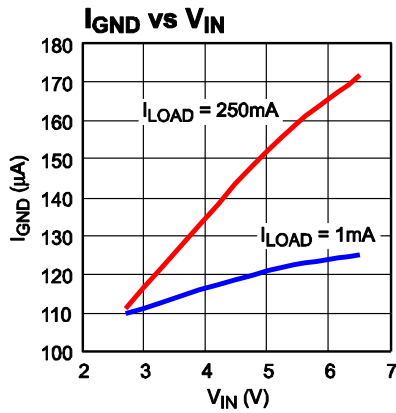
5) Parameter is guaranteed by design, not production tested.

6) Dropout Voltage is defined as the input to output differential when the output voltage drops 1% below its normal value.

 7) $V_{IN} = 2.7V$ for $V_{OUT} = 1.25V$ to $2.2V$

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 4.5V$, $V_{OUT} = 2.85V$, $C1 = 1\mu F$, $C2 = 0.1\mu F$, $C3 = 2.2\mu F$, $T_A = +25^\circ C$ unless otherwise noted.



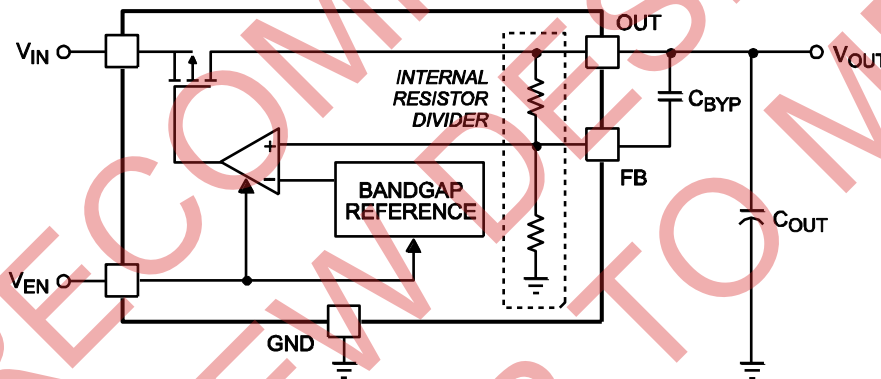
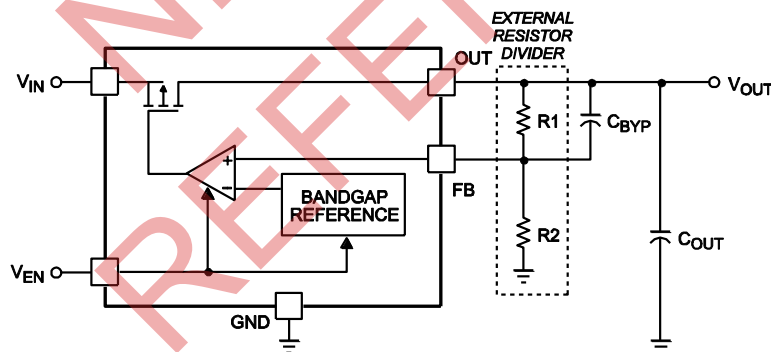
PIN FUNCTIONS

Pin #	Name	Description
1, 2	OUT	Regulator Output. OUT is the output of the linear regulator. Bypass OUT to GND with a 1µF or greater capacitor.
3	FB	Feedback Input. Connect a resistive voltage divider from OUT to FB to set the output voltage. OUT feedback threshold is 1.222V.
4	GND, Exposed Pad	The exposed pad and GND pin must be connected to the same ground plane.
5	EN	Enable Input. Drive EN high to turn on the MP8902, drive EN low to turn it off. For automatic startup, connect EN to IN.
6	NC	No Connect.
7, 8	IN	Power Source Input. IN supplies the internal power to the MP8902 and is the source of the pass transistor. Bypass IN to GND with a 1µF or greater capacitor.

OPERATION

The MP8902 is a low-current, low-noise, high-PSRR, low-dropout, linear regulator. It is intended for use in devices that require very low noise power supplies and high-PSRR such as PLL VCO supplies for mobile handsets and 802.11 PC Cards, as well as audio codecs and

microphones. The MP8902 uses a PMOS pass element and features internal thermal shutdown. As shown in Figures 1 and 2, optional feed-forward capacitor C_{BYP} may be added between FB and OUT pins for an improved transient response.


Figure 1—Ultra-Low-Noise Fixed Output Regulator

Figure 2—Ultra-Low-Noise Adjustable Regulator: $V_{OUT} = V_{FB}(1+(R1/R2))$

APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

The fixed output voltage of the MP8902DG is set to 2.5V or 3.3V, depending on the internal resistor divider (Figure 1). You can also adjust the output voltage by using an external resistor divider (R1 and R2 in Figure 2). However, the sum of R1 and R2 should not exceed 100kΩ to minimize the impact of the internal resistor divider. For accurate output-voltage setting, it is suggested to use 10kΩ (±1%) for the low-side resistor R2 of the voltage divider, the high side resistor R1 can be determined by the equation:

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right)$$

Where V_{FB} is the OUT feedback threshold voltage equal to 1.222V.

Example: For 2.5V Output

$$R1 = \frac{2.5V - 1.222V}{\left(\frac{1.222V}{10k\Omega} \right)} = 10.41k\Omega$$

You can select a standard 10.5kΩ (±1%) resistor for R1.

The following table lists the selected R1 values for some typical output voltages:

Table 1—Adjustable Output Voltage R1 Values

V _{OUT} (V)	R1 (Ω)
1.25	232
1.5	2.26k
1.8	4.75k
2	6.34k
2.5	10.5k
2.8	13k
3	14.7k
3.3	16.9k
4	22.6k
5	30.9k

In Figures 3 and 4, C2 is added for an improved transient response.

TYPICAL APPLICATION CIRCUIT

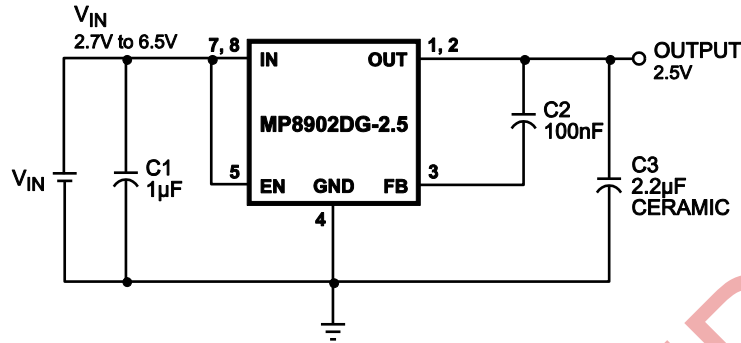


Figure 3—Typical Application Circuit (Fixed)

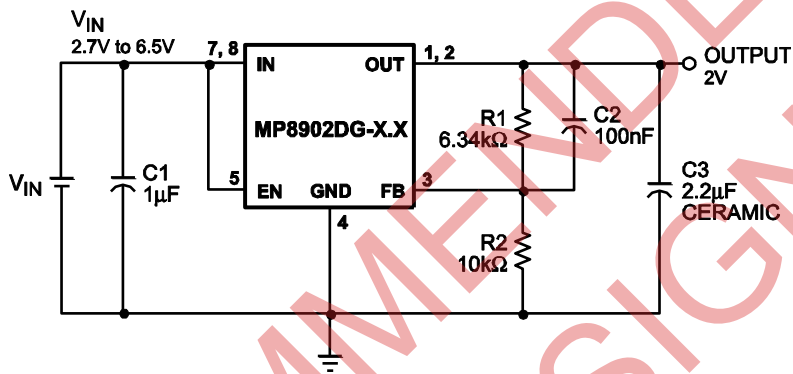
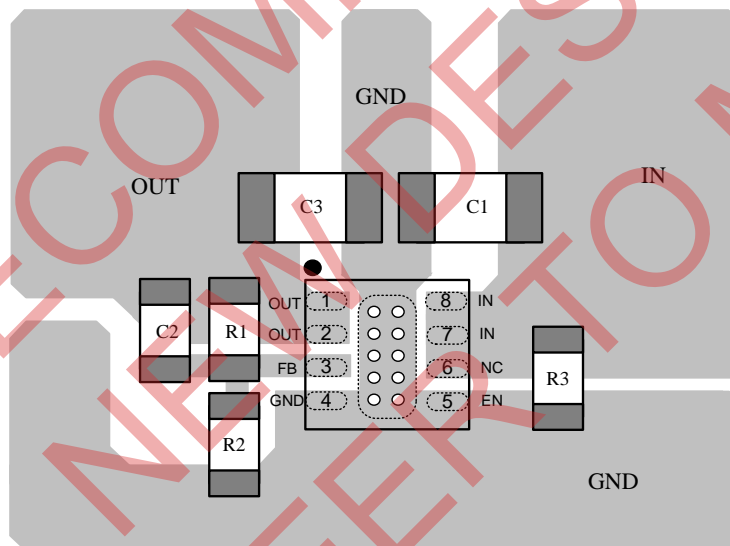
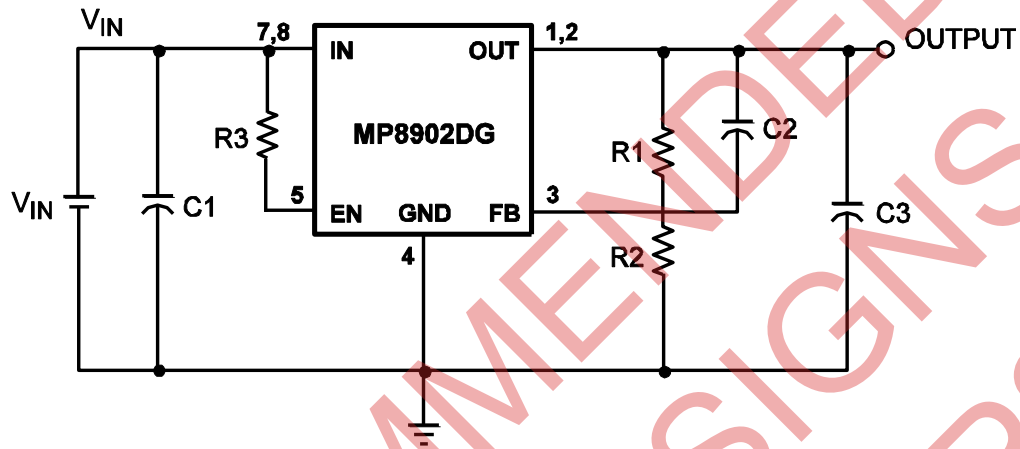


Figure 4—Typical Application Circuit (Adjustable)

PCB layout guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take figure 5 for reference.

- 1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
- 2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 3) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

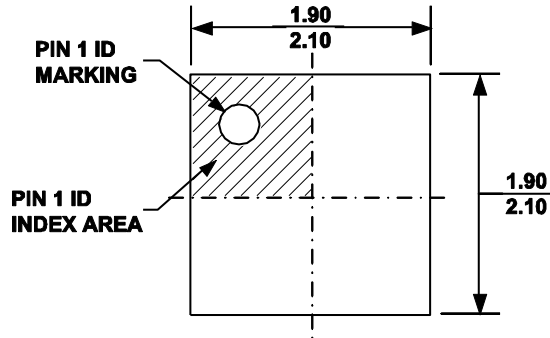


Top Layer

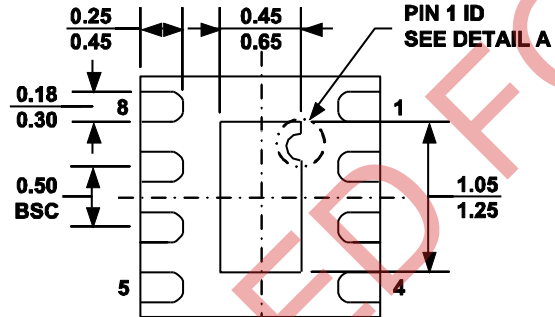
Figure 5—PCB Layout

PACKAGE INFORMATION

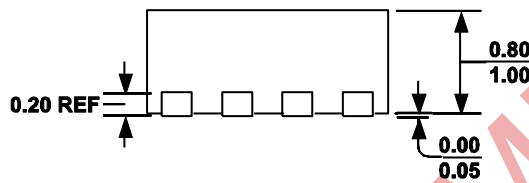
2x2 QFN8



TOP VIEW



BOTTOM VIEW

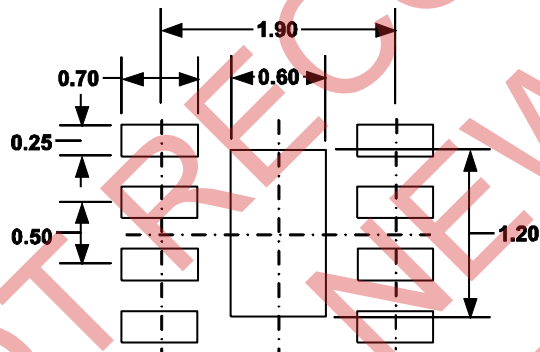


SIDE VIEW

 PIN 1 ID OPTION A
R0.20 TYP.

 PIN 1 ID OPTION B
R0.20 TYP.


DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VCCD-3.
- 5) DRAWING IS NOT TO SCALE.

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