MP8869N

18V, 12A, High-Efficiency, Wide-Input, Synchronous, Step-Down Converter with Integrated Telemetry via I²C Interface

DESCRIPTION

The MP8869N is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. The MP8869N offers a fully integrated solution that achieves up to 12A of continuous current and 15A of peak output current (I_{OUT}), with excellent load and line regulation across a wide input supply range.

The output voltage (V_{OUT}) level can be controlled on-the-fly via the I²C serial interface. The reference voltage (V_{REF}) range can be adjusted from 0.6V to 1.108V in 4mV steps. The voltage slew rate, frequency, current limit, hiccup/latch-off protection, enable, and power-saving mode are also adjustable via the I²C interface.

Constant-on-time (COT) control operation provides fast transient response. An open-drain power good (PG) pin indicates whether V_{OUT} is within the nominal range. Full protection features include over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8869N is available in a QFN-14 (3mmx4mm) package.

FEATURES

- Output Voltage (V_{OUT}) Adjustable Up to 5.5V using the FB Pin
- Wide 2.85V to 18V Operating Input Voltage (V_{IN}) Range
- 12A Continuous/15A Peak Output Current (I_{OUT})
- 1% Internal Reference Accuracy
- I²C-Configurable Reference Voltage (V_{REF}) Range from 0.6V to 1.108V in 4mV Steps with Slew Rate Control
- 5% Accuracy V_{OUT} and I_{OUT} Monitoring via the I²C
- Selectable PFM/PWM Mode, Adjustable Frequency and Current Limit via the I²C
- Four Different Selectable I²C Addresses
- External Soft Start (SS)
- Open-Drain Power Good (PG) Indication
- Output Over-Voltage Protection (OVP), Hiccup/Latch-Off Over-Current Protection (OCP)
- Available in a QFN-14 (3mmx4mm) Package

APPLICATIONS

- Solid-State Drives (SSDs)
- Flat-Panel Televisions and Monitors
- Digital Set-Top Boxes
- Distributed Power Systems
- Networking/Servers

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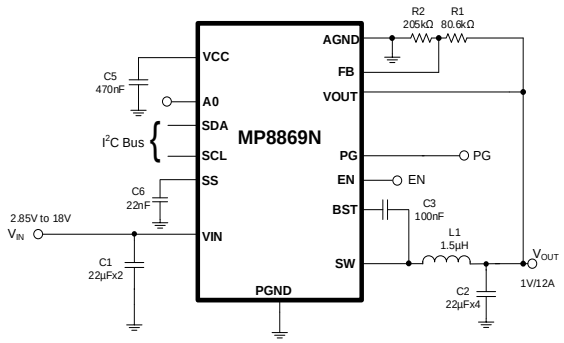
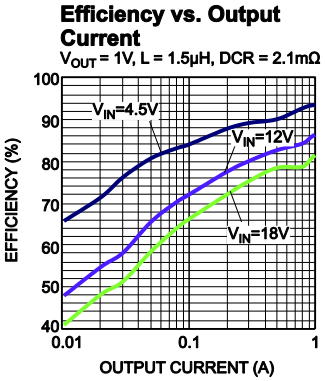
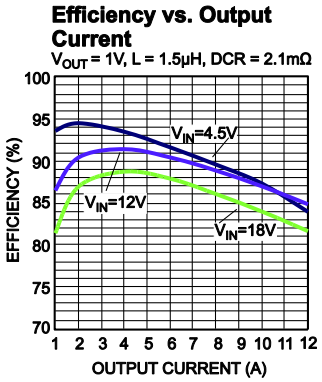
TYPICAL APPLICATION







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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP8869NGL*	QFN-14 (3mmx4mm)	*See Below*	1
EVKT-8869N	Evaluation kit		

* For Tape & Reel, add suffix -Z (e.g. MP8869NGL-Z).

TOP MARKING

MPYW
8869
NLLL

MP: Product code of MP8869NGL
Y: Year code
W: Lot number
8869N: First five digits of the part number
LLL: Lot number

EVALUATION KIT (EVKT-8869N)

The EVKT-8869N evaluation kit contents include (items can be ordered separately):

#	Part Number	Item	Quantity
1	EV8869N-L-00A	MP8869NGL evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order directly from MonolithicPower.com or our distributors.

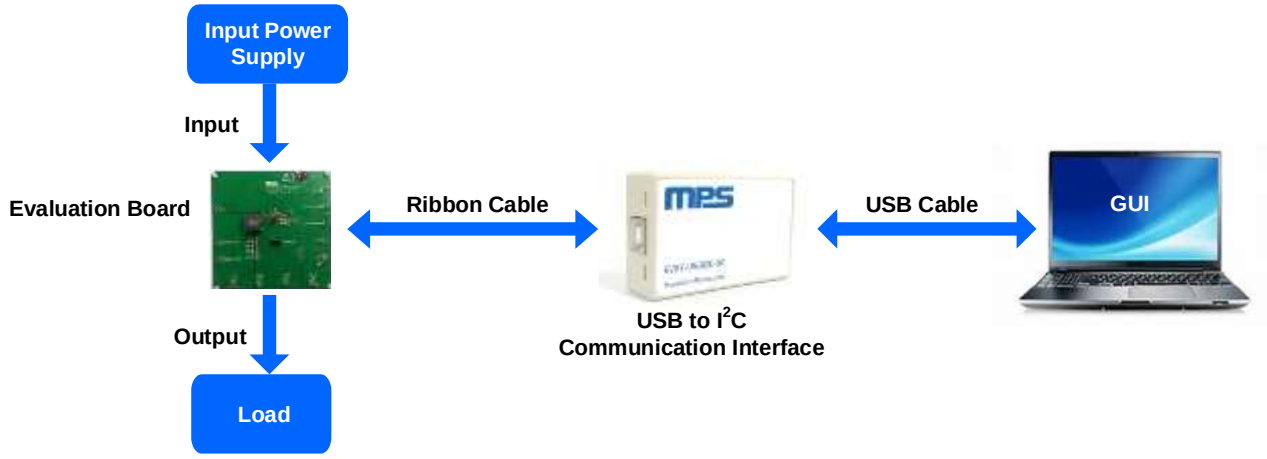

Figure 1: EVKT-8869N Evaluation Kit Set-Up

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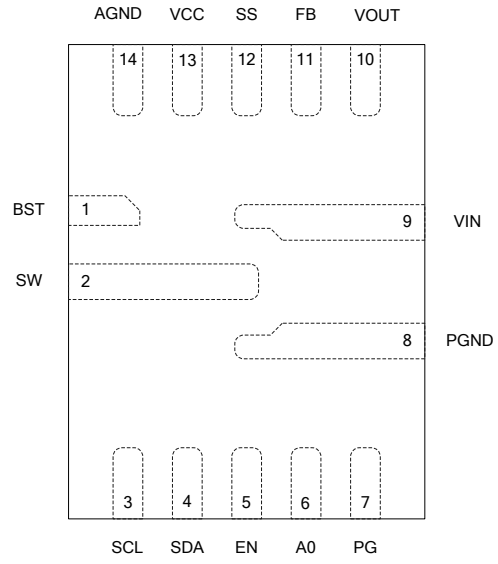
PACKAGE REFERENCE



QFN-14 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** Place a capacitor is between SW and BST to form a floating supply across the high-side MOSFTE (HS-FET) driver.
2	SW	**Switch output.** Connect the SW pin to the PCB's SW connector using a wide PCB trace.
3	SCL	**I²C serial clock.**
4	SDA	**I²C serial data.**
5	EN	**Enable.** Drive EN high to enable the MP8869N. EN has a 1.5MΩ internal pull-down resistor to GND. EN is a high-voltage pin, so it can be connected to directly VIN for automatic start-up.
6	A0	**I²C address set-up.** Connect a resistor divider from VCC to A0 to set different I²C addresses.
7	PG	**Power good (PG) indication.** PG is an open-drain structure. PG is de-asserted if the output voltage (V_{OUT}) goes out of the regulation window.
8	PGND	**System power ground.** PGND is the reference ground of the regulated V_{OUT}. PGND requires special consideration during PCB layout. Connect PGND to the ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8869N operates from a 2.85V to 18V input rail. Decouple the input rail with a ceramic capacitor. Connect VIN to the positive power terminal using a wide PCB trace.
10	VOUT	**Output voltage sense.** Connect VOUT to the positive load terminal.
11	FB	**Feedback.** To set V_{OUT}, connect FB to the tap of an external resistor divider between the output and GND.
12	SS	**Soft-start (SS) set-up.** Connect a capacitor from SS to ground to set the soft-start time (t_{SS}).
13	VCC	**Internal low-dropout (LDO) regulator output.** Decouple VCC with a 0.47µF capacitor.
14	AGND	**Signal ground.** If AGND is not connected to PGND internally, ensure that AGND is connected to PGND during PCB layout.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +19V
V_{SW} .....-0.6V (-7V for <10ns) to .....V_{IN} + 0.7V (25V for <25ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} 18V
V_{OUT} 7V
All other pins .....-0.3V to 4V
Continuous power dissipation……(T_A = 25°C) (2)
QFN-14 (3mmx4mm) 2.5W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.85V to 18V
Output voltage (V_{OUT}) .....0.6V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-14 (3mmx4mm)	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (5), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V		2.1	4	μA
Quiescent supply current	I_Q	No switching, PFM mode, FB = 105% x V_{REF}		420	600	μA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST} - V_{SW} = 3.3V		15		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 3.3V		4.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V, T_J = 25°C			1	μA
Low-side (LS) valley current limit	I_{LIMIT_L}	Adjustable via the I²C		14		A
LS negative current limit	I_{LIMIT_LN}	In forced pulse-width modulation (PWM) mode or an over-voltage protection (OVP) state		-5		A
LS zero-current detection (ZCD) threshold	I_{ZCD}	T_J = 25°C		200		mA
Switching frequency	f_{SW1}	V_{IN} = 12V, V_{OUT} = 1V	400	500	600	kHz
	f_{SW2}	V_{IN} = 12V, V_{OUT} = 5V	400	500	600	kHz
Minimum off time (6)	t_{OFF_MIN}			185		ns
Minimum on time (6)	t_{ON_MIN}	V_{OUT} = 0.6V		50		ns
Reference voltage	V_{REF}	T_J = 25°C	-1%	720	+1%	mV
		-40°C < T_J < +125°C (5)	-1.5%	720	+1.5%	
Feedback (FB) current	I_{FB}	V_{FB} = 740mV		10	50	nA
A0 voltage threshold 1	V_{ADD_1}	Set I²C address 61h			0.24	V_{CC}
A0 voltage threshold 2	V_{ADD_2}	Set I²C address 63h	0.28		0.49	V_{CC}
A0 voltage threshold 3	V_{ADD_3}	Set I²C address 65h	0.53		0.72	V_{CC}
A0 voltage threshold 4	V_{ADD_4}	Set I²C address 67h	0.77			V_{CC}
A0-to-GND pull-down resistor	R_{A0_PD}			2		MΩ
EN rising threshold	V_{EN_RISING}		1.1	1.2	1.3	V
EN threshold hysteresis	V_{EN_HYS}			110		mV
EN to GND pull-down resistor	R_{EN}			1.5		MΩ
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UV_TH_R}$		2.45	2.65	2.85	V
V_{IN} UVLO falling threshold	$V_{IN_UV_TH_F}$		2.3	2.5	2.7	V
Power good (PG) under-voltage (UV) rising threshold	PGV_{TH-HI}	Good	0.86	0.9	0.94	V_{OUT}
PG UV falling threshold	PGV_{TH-LO}	Fault	0.81	0.85	0.89	V_{OUT}
PG over-voltage (OV) rising threshold	PGV_{TH-HI}	Fault	1.11	1.15	1.19	V_{OUT}
PG OV falling threshold	PGV_{TH-LO}	Good	1.01	1.05	1.09	V_{OUT}
PG deglitch time	t_{PG_D}	I²C configurable		30		μs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (5), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over-voltage protection (OVP) rising threshold	V_{OVP_RISING}	FB	121%	125%	129%	V_{REF}
OVP falling threshold	$V_{OVP_FALLING}$	FB	106%	110%	114%	V_{REF}
OVP delay	t_{OVP}			3.7		µs
Output pin absolute OV	V_{OVP2}		6	6.5	7	V
Under-voltage protection (UVP) threshold	$V_{FB_UV_TH}$	Hiccup entry	55%	60%	65%	V_{REF}
UVP delay (6)	t_{UVP}			10		µs
Soft-start current	I_{SS}		5	7	9	µA
VCC voltage	V_{CC}			3.5		V
VCC load regulation	V_{CC_REG}	I_{CC} = 20mA			3	%
Thermal shutdown (6)	T_{TSD}			160		°C
Thermal hysteresis (6)	T_{TSD_HYS}			20		°C

Notes:

5) Not tested in production and guaranteed by over-temperature correlation.
6) Guaranteed by characterization testing.

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I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	+0.3 x V_{CC}	-0.5	+0.3 x V_{CC}	V
High-level input voltage	V_{IH}		0.7 x V_{CC}	V_{CC} + 0.5	0.7 x V_{CC}	V_{CC} + 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{CC} > 2V	0.05 x V_{CC}	-	0.05 x V_{CC}	-	V
		V_{CC} < 2V	0.1 x V_{CC}	-	0.1 x V_{CC}	-	
Low-level output voltage (open drain) at 3mA sink current	V_{OUT_L}	V_{CC} > 2V	0	0.4	0	0.4	V
		V_{CC} < 2V	0	0.2 x V_{CC}	0	0.2 x V_{CC}	
Low-level output current	I_{OUT_L}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{ONL}	V_{OUT_L} level at a 3mA sink current, I_{OUT_L} = 3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{ONH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{CC} level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{CS}	SCLH output levels between 0.3 x V_{CC} and 0.7 x V_{CC}	2	6	2	6	mA
SCLH or SCL signal rise time	t_{RCL}	Output rise time (current source enabled) with a 3mA external pull-up current source					
		10pF to 100pF capacitive load	10	40			ns
		400pF capacitive load	20	80			ns
SCLH or SCL signal fall time	t_{FCL}	Output fall time (current source enabled) with aa 3mA external pull-up current source					
		10pF to 100pF capacitive load	10	40			ns
		400pF capacitive load	20	80	20	250	ns
SDAH signal rise time	t_{RDA}	10pF to 100pF capacitive load	10	80	-	-	ns
		400pF capacitive load	20	160	20	250	ns
SDAH signal fall time	t_{FDA}	10pF to 100pF capacitive load	10	80	-	-	ns
		400pF capacitive load	20	160	20	250	ns

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I/O LEVEL CHARACTERISTICS *(continued)*

Parameter	Symbol	Condition	HS Mode		LS Mode		Units
			Min	Max	Min	Max	
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O pin	I_{IN}	V_{IN} between 0.1 x V_{CC} and 0.9 x V_{CC}	-	10	-10	+10	µA
Capacitance for each I/O pin	C_{IN}		-	10	-	10	pF

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I²C PORT SIGNAL CHARACTERISTICS

Parameter	Symbol	Condition	C_B = 100pF		C_B = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$t_{SU;STA}$		160	-	600	-	ns
Hold time for a repeated start condition	$t_{HD;STA}$		160	-	600	-	ns
SCL clock low period	t_{LOW}		160	-	1300	-	ns
SCL clock high period	t_{HIGH}		60	-	600	-	ns
Data set-up time	$t_{SU:DAT}$		10	-	100	-	ns
Data hold time	$t_{HD;DAT}$		0	70	0	-	ns
SCLH signal rise time	t_{R_CL}		10	40	20 x (0.1 x C_B)	300	ns
SCLH signal rise time after a repeated start condition and after an acknowledge bit	t_{R_CL1}		10	80	20 x (0.1 x C_B)	300	ns
SCLH signal fall time	t_{F_CL}		10	40	20 x (0.1 x C_B)	300	ns
SDAH signal rise time	t_{R_DA}		10	80	20 x (0.1 x C_B)	300	ns
SDAH signal fall time	t_{F_DA}		10	80	20 x (0.1 x C_B)	300	ns
Set-up time for a stop condition	$t_{SU;STO}$		160	-	600	-	ns
Bus free time between a stop and start condition	t_{BUF}		160	-	1300	-	ns
Data valid time	$t_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$t_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_B	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF
Low-level noise margin	C_{NL}	For each connected device	-	0.1 x V_{CC} (7)	0.1 x V_{CC} (7)	-	V
High-level noise margin	V_{NH}	For each connected device	-	0.2 x V_{CC} (7)	0.2 x V_{CC} (7)	-	V

Note:

7) V_{CC} is the I²C bus voltage. It ranges from 1.8V to 3.6V, and is used for 1.8V, 2.5V, and 3.3V bus voltages.

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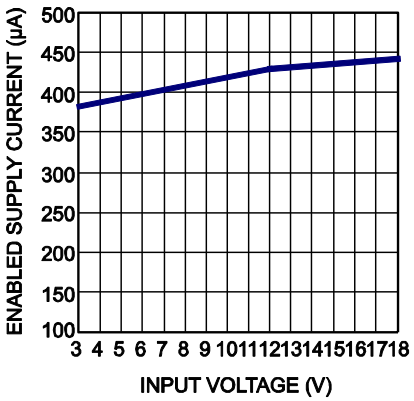
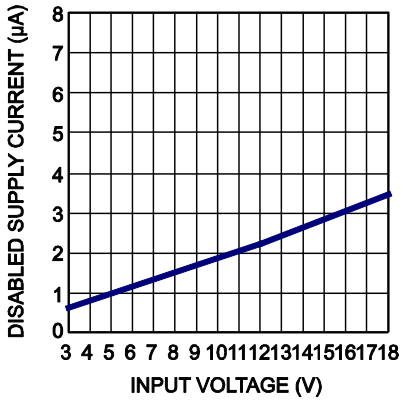
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

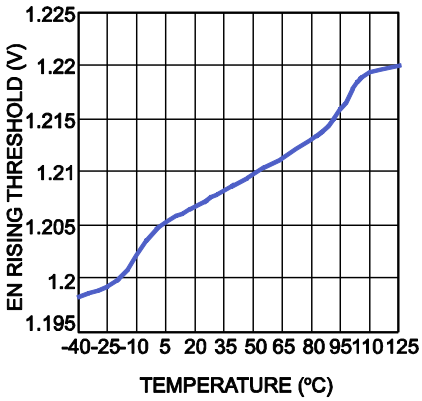
Enabled Supply Current vs. Input Voltage



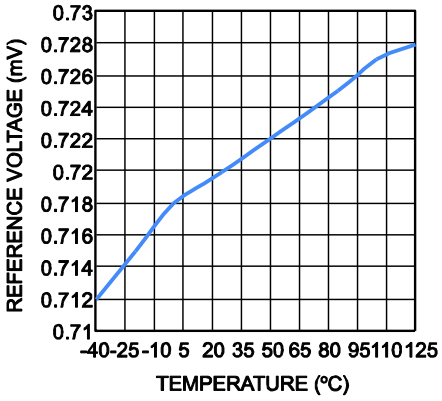
Disabled Supply Current vs. Input Voltage



EN Rising Threshold vs. Temperature

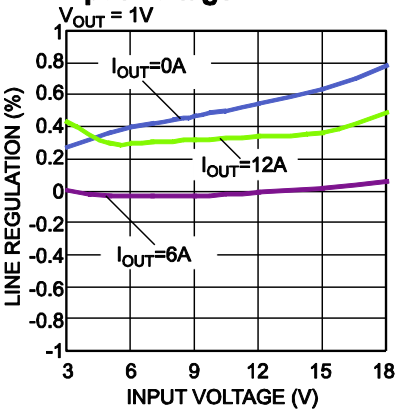


Reference Voltage vs. Temperature



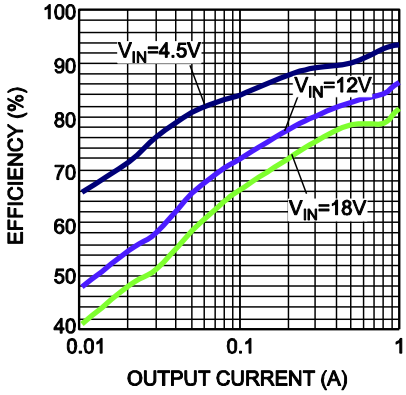
Line Regulation vs. Input Voltage

V_{OUT} = 1V



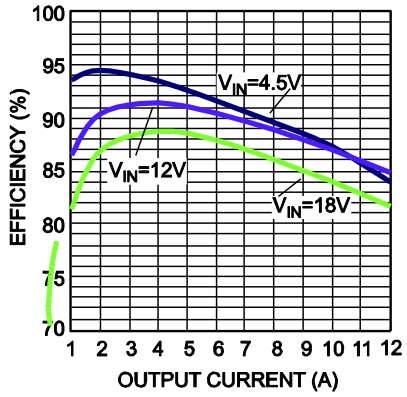
Efficiency vs. Output Current

V_{OUT} = 1V, L = 1.5µH, DCR = 2.1mΩ



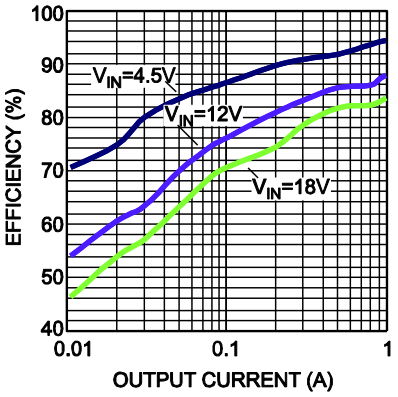
Efficiency vs. Output Current

V_{OUT} = 1V, L = 1.5µH, DCR = 2.1mΩ



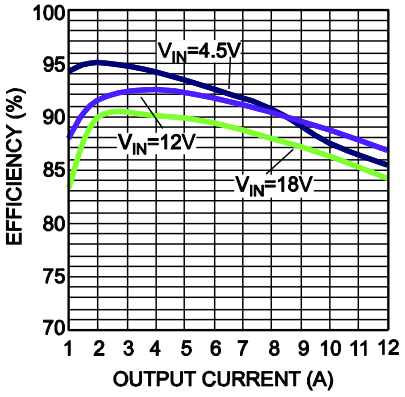
Efficiency vs. Output Current

V_{OUT} = 1.2V, L = 1.5µH, DCR = 2.1mΩ



Efficiency vs. Output Current

V_{OUT} = 1.2V, L = 1.5µH, DCR = 2.1mΩ



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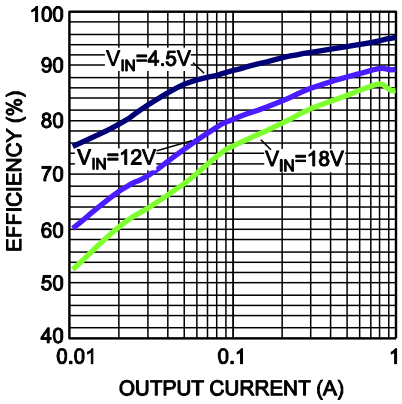
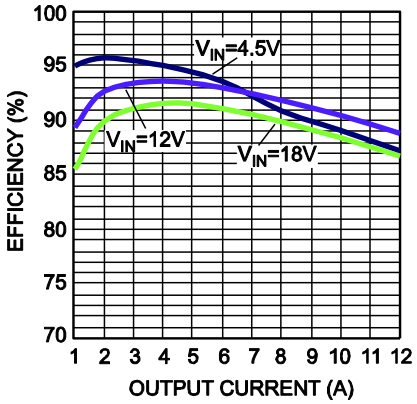
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

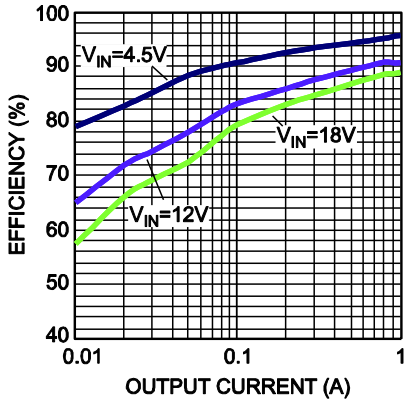
Efficiency vs. Output Current
V_{OUT} = 1.5V, L = 1.5µH, DCR = 2.1mΩ



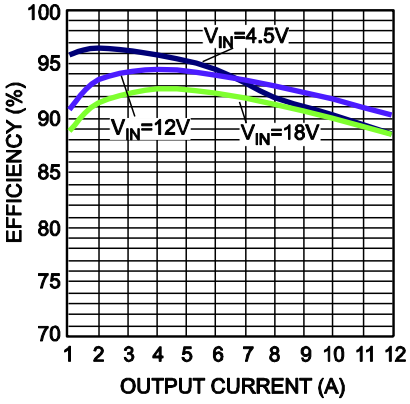
Efficiency vs. Output Current
V_{OUT} = 1.5V, L = 1.5µH, DCR = 2.1mΩ



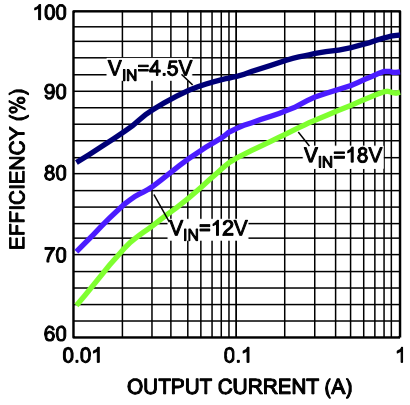
Efficiency vs. Output Current
V_{OUT} = 1.8V, L = 1.5µH, DCR = 2.1mΩ



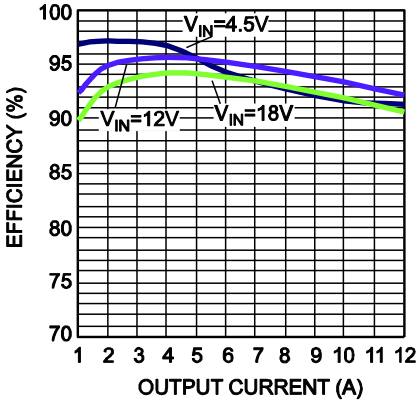
Efficiency vs. Output Current
V_{OUT} = 1.8V, L = 1.5µH, DCR = 2.1mΩ



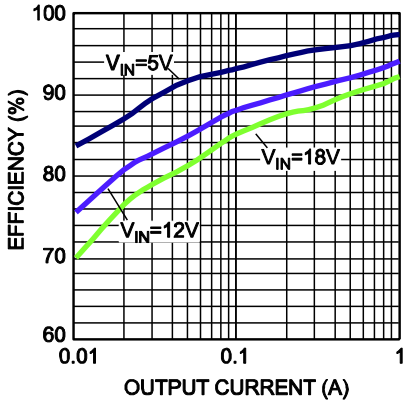
Efficiency vs. Output Current
V_{OUT} = 2.5V, L = 2.2µH, DCR = 3mΩ



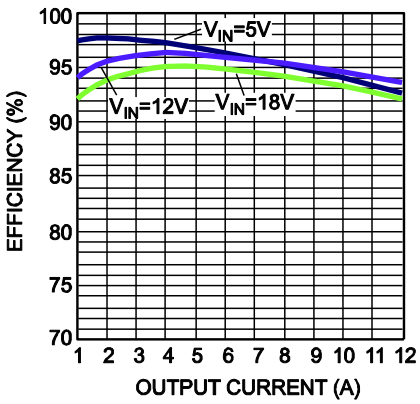
Efficiency vs. Output Current
V_{OUT} = 2.5V, L = 2.2µH, DCR = 3mΩ



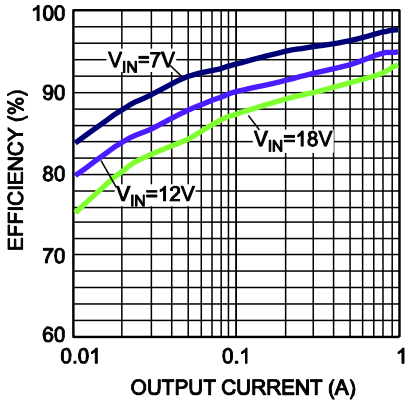
Efficiency vs. Output Current
V_{OUT} = 3.3V, L = 2.2µH, DCR = 3mΩ



Efficiency vs. Output Current
V_{OUT} = 3.3V, L = 2.2µH, DCR = 3mΩ



Efficiency vs. Output Current
V_{OUT} = 5V, L = 3.3µH, DCR = 4.4mΩ



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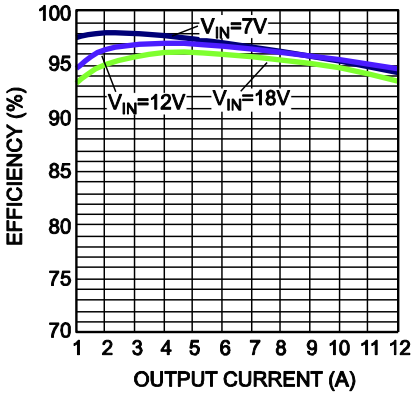
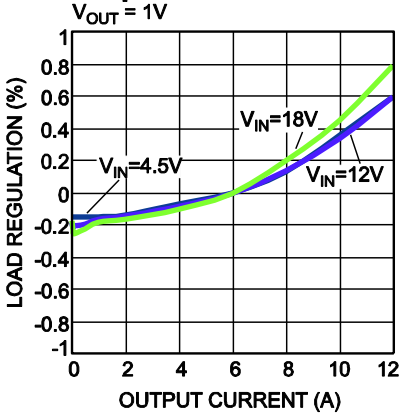
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

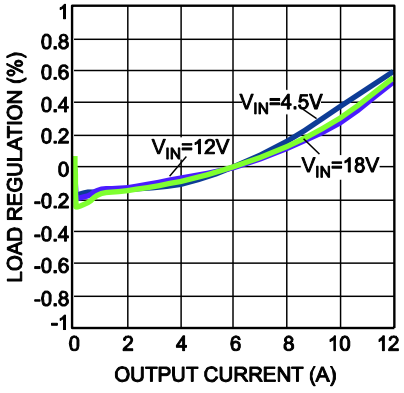
Efficiency vs. Output Current
V_{OUT} = 5V, L = 3.3µH, DCR = 4.4mΩ



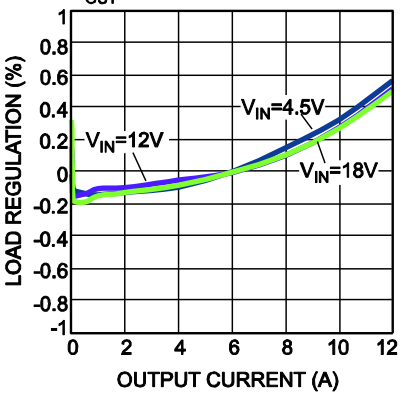
Load Regulation vs. Output Current
V_{OUT} = 1V



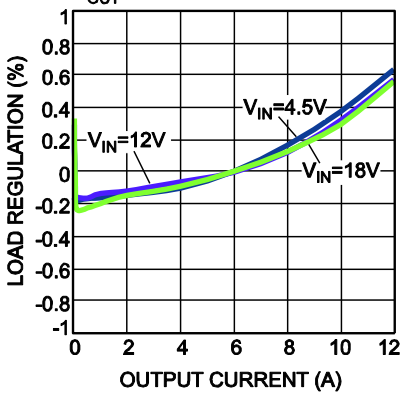
Load Regulation vs. Output Current
V_{OUT} = 1.2V



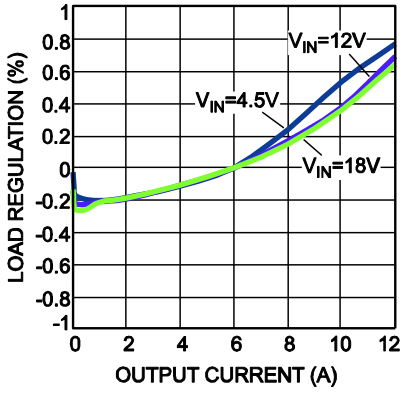
Load Regulation vs. Output Current
V_{OUT} = 1.5V



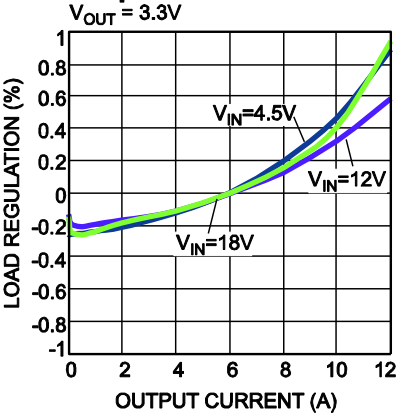
Load Regulation vs. Output Current
V_{OUT} = 1.8V



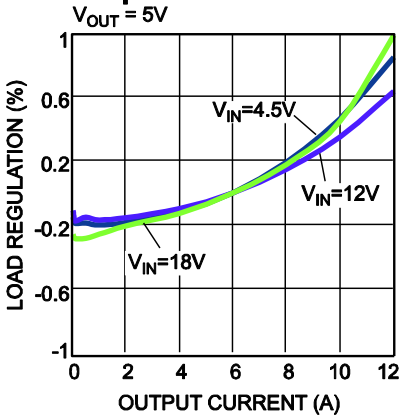
Load Regulation vs. Output Current
V_{OUT} = 2.5V



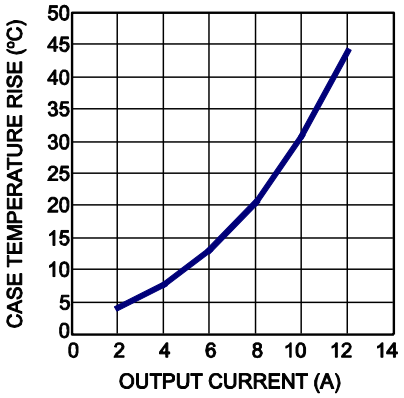
Load Regulation vs. Output Current
V_{OUT} = 3.3V



Load Regulation vs. Output Current
V_{OUT} = 5V



Case Temperature Rise vs. Output Current



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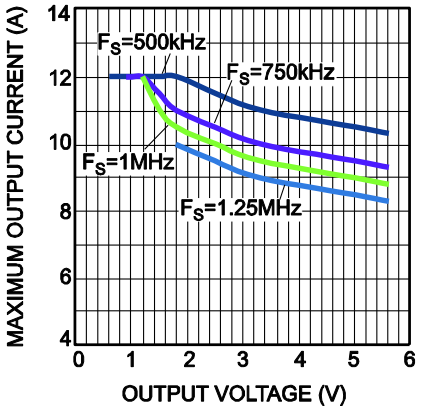
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

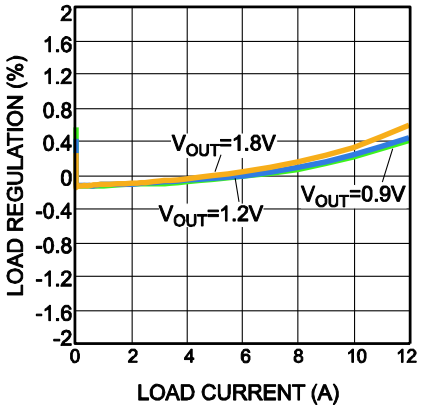
Maximum Output Current vs. Output Voltage

V_{IN} = 12V, 4-layer PCB (8.5cmx8.5cm)



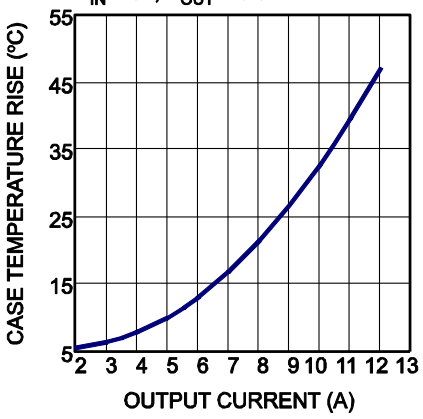
Load Regulation

V_{IN} = 3V, V_{OUT} = 0.9V



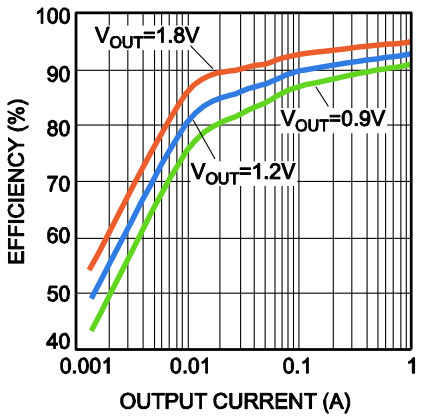
Case Temperature Rise vs. Output Current

V_{IN} = 3V, V_{OUT} = 0.9V



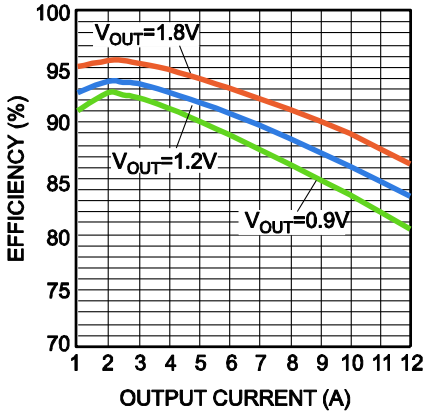
Efficiency

V_{IN} = 3V, V_{OUT} = 0.9V



Efficiency

V_{IN} = 3V, V_{OUT} = 0.9V



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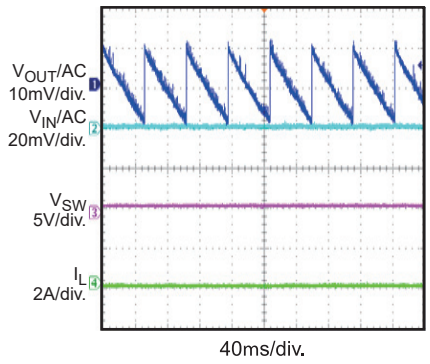
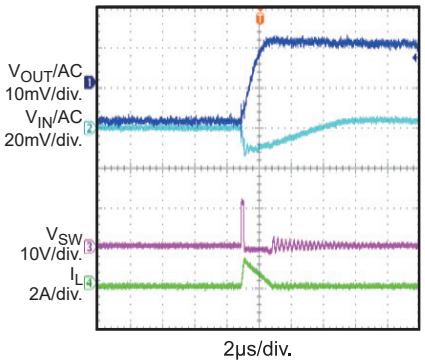
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

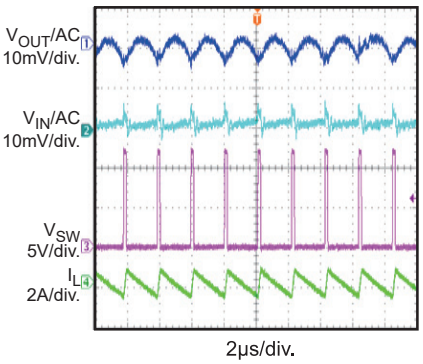
Input/Output Ripple
I_{OUT} = 0A



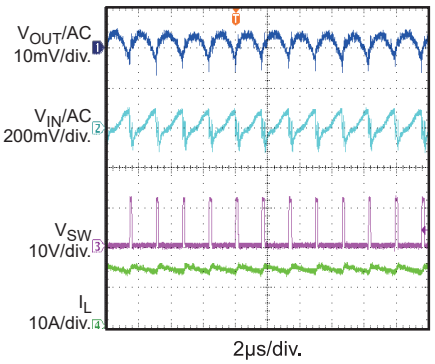
Input/Output Ripple
I_{OUT} = 0A



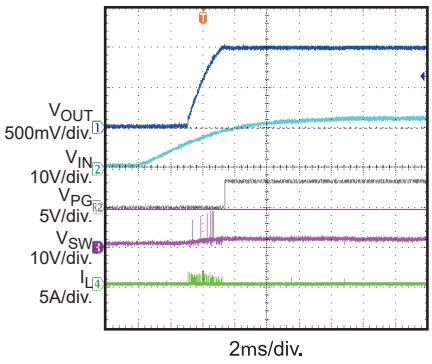
Input/Output Ripple
I_{OUT} = 0A, Forced PWM Mode



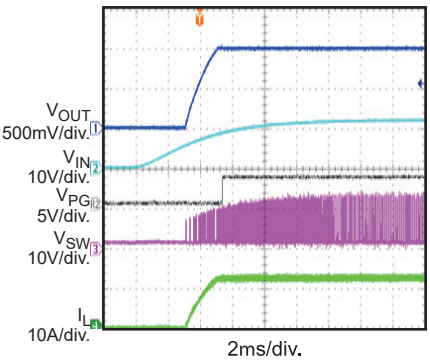
Input/Output Ripple
I_{OUT} = 12A



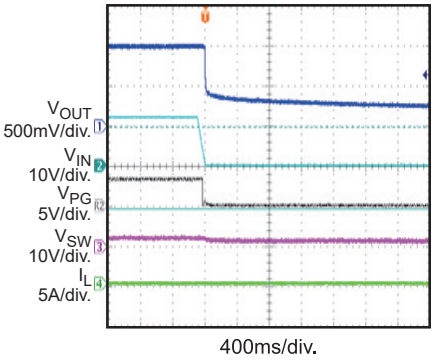
Start-Up through Input Voltage
I_{OUT} = 0A



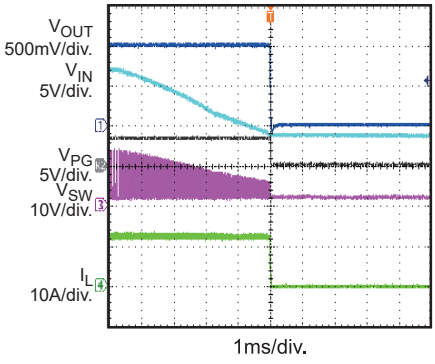
Start-Up through Input Voltage
I_{OUT} = 12A



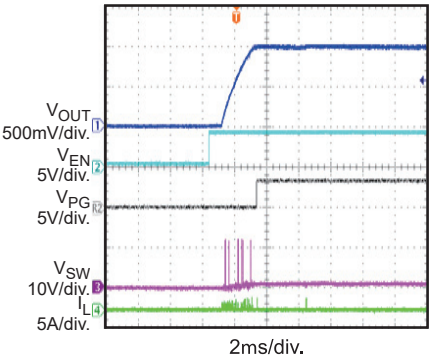
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 12A



Start-Up through EN
I_{OUT} = 0A



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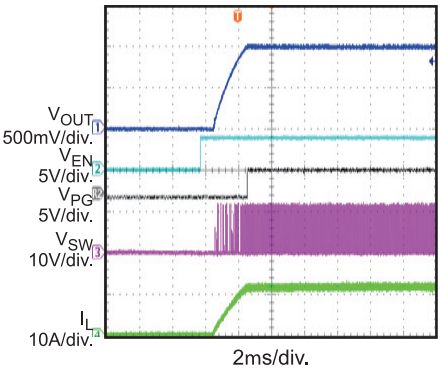
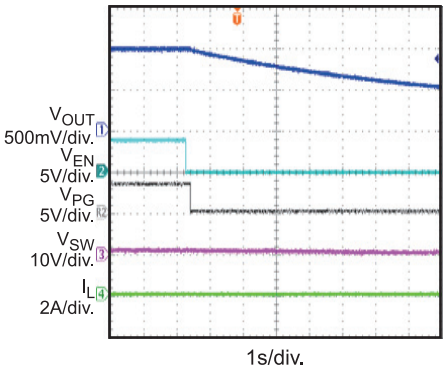
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

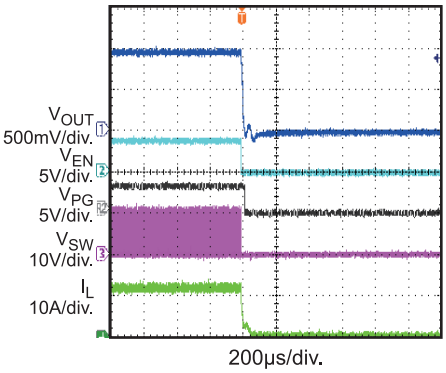
Start-Up through EN
I_{OUT} = 12A



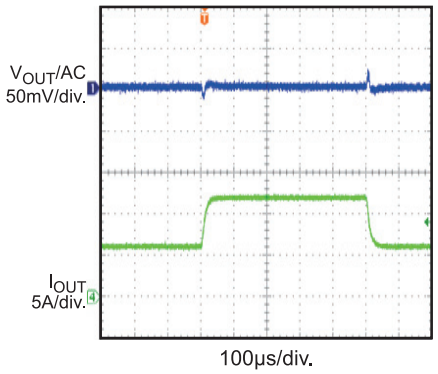
Shutdown through EN
I_{OUT} = 0A



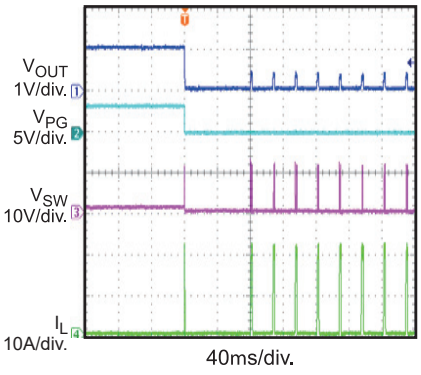
Shutdown through EN
I_{OUT} = 12A



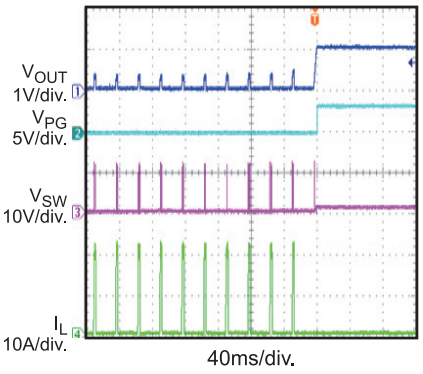
Load Transient
I_{OUT} = 6A-12A



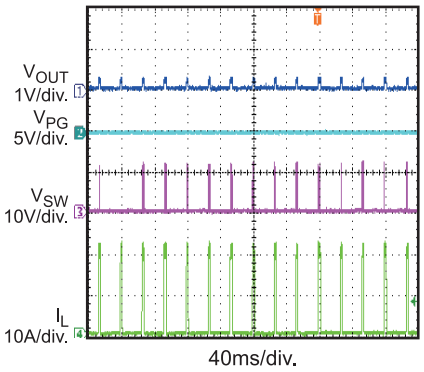
Short-Circuit Protection Entry
I_{OUT} = 0A



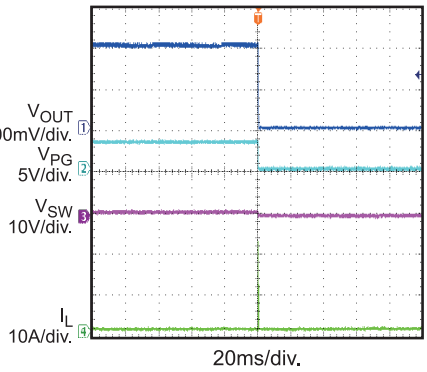
Short-Circuit Protection Recovery
I_{OUT} = 0A



Short-Circuit Protection Steady State
Short Output to GND



Short-Circuit Protection Entry, Latch Off Mode
I_{OUT}=0A



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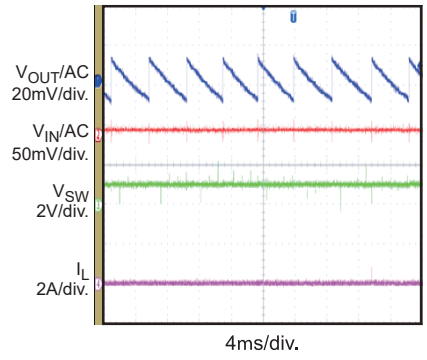
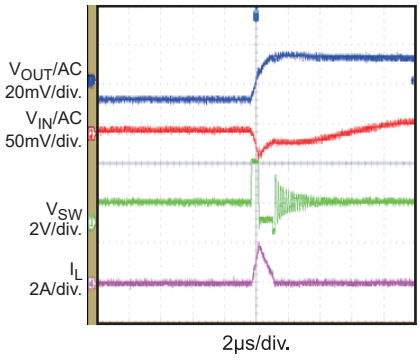
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 3V, V_{OUT} = 0.9V, L = 0.47µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

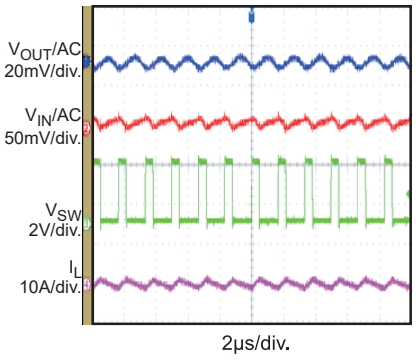
Input/Output Ripple
I_{OUT} = 0A



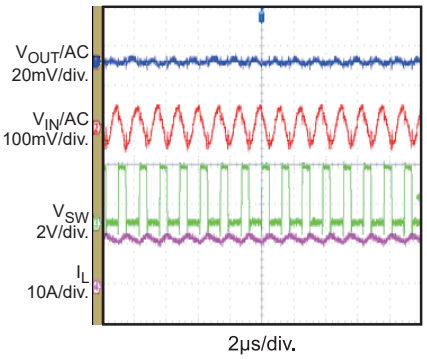
Input/Output Ripple
I_{OUT} = 0A



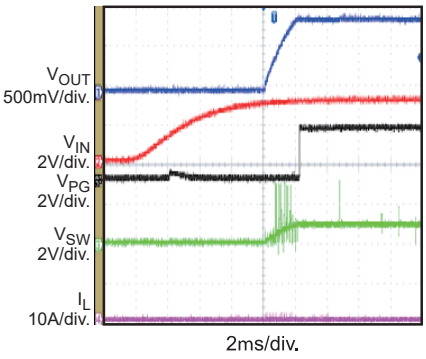
Input/Output Ripple
I_{OUT} = 0A, Forced PWM Mode



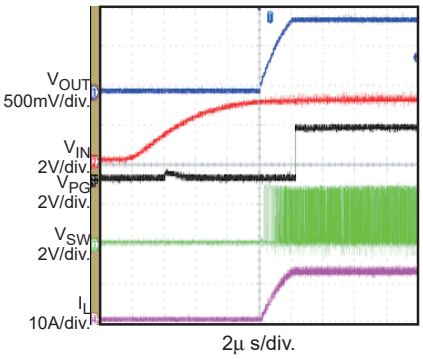
Input/Output Ripple
I_{OUT} = 12A



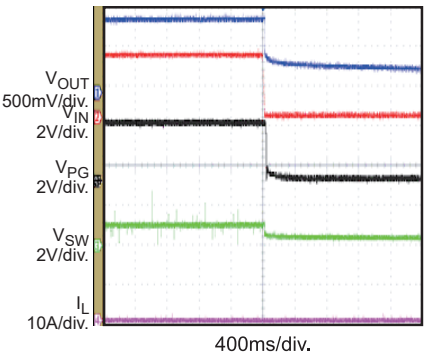
Start-Up through Input Voltage
I_{OUT} = 0A



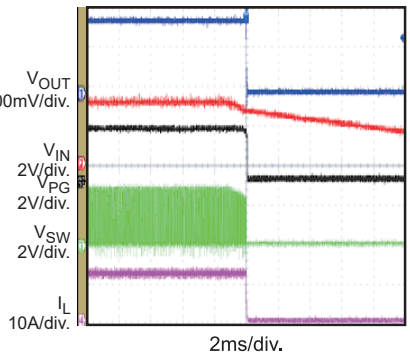
Start-Up through Input Voltage
I_{OUT} = 12A



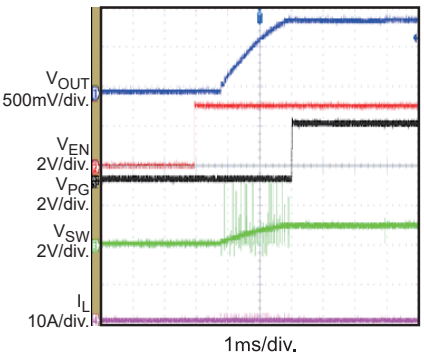
Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 12A



Start-Up through EN
I_{OUT} = 0A



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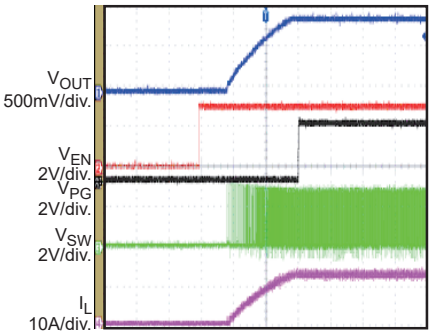
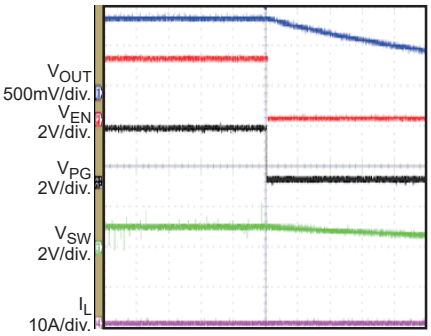
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board, V_{IN} = 3V, V_{OUT} = 0.9V, L = 0.47µH, f_{SW} = 500kHz, auto-PFM/PWM mode, T_A = 25°C, unless otherwise noted.

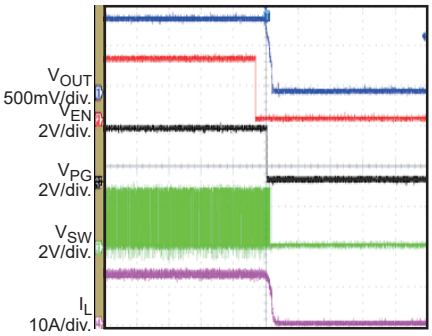
Start-Up through EN
I_{OUT} = 12A



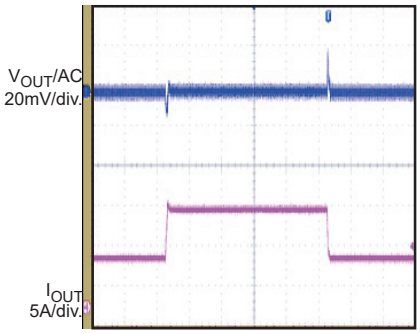
Shutdown through EN
I_{OUT} = 0A



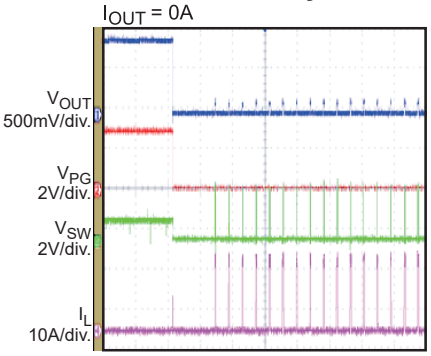
Shutdown through EN
I_{OUT} = 12A



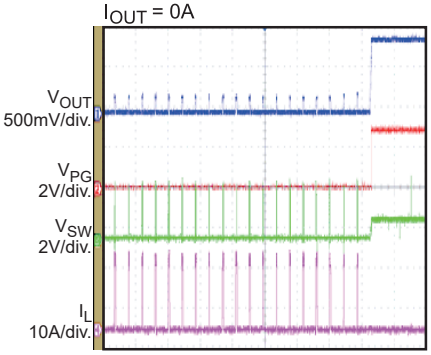
Load Transient
I_{OUT} = 6A-12A



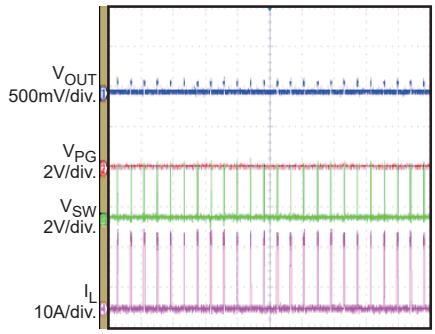
Short-Circuit Protection Entry
I_{OUT} = 0A



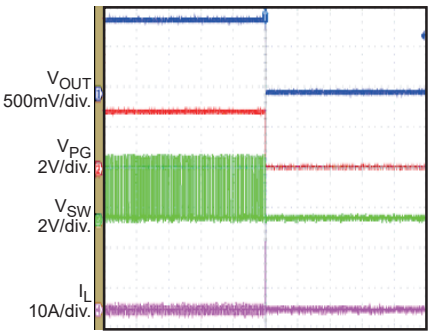
Short-Circuit Protection Recovery
I_{OUT} = 0A



Short-Circuit Protection Steady State
Short Output to GND



Short-Circuit Protection Entry, Latch Off Mode
I_{OUT}=0A



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FUNCTIONAL BLOCK DIAGRAM

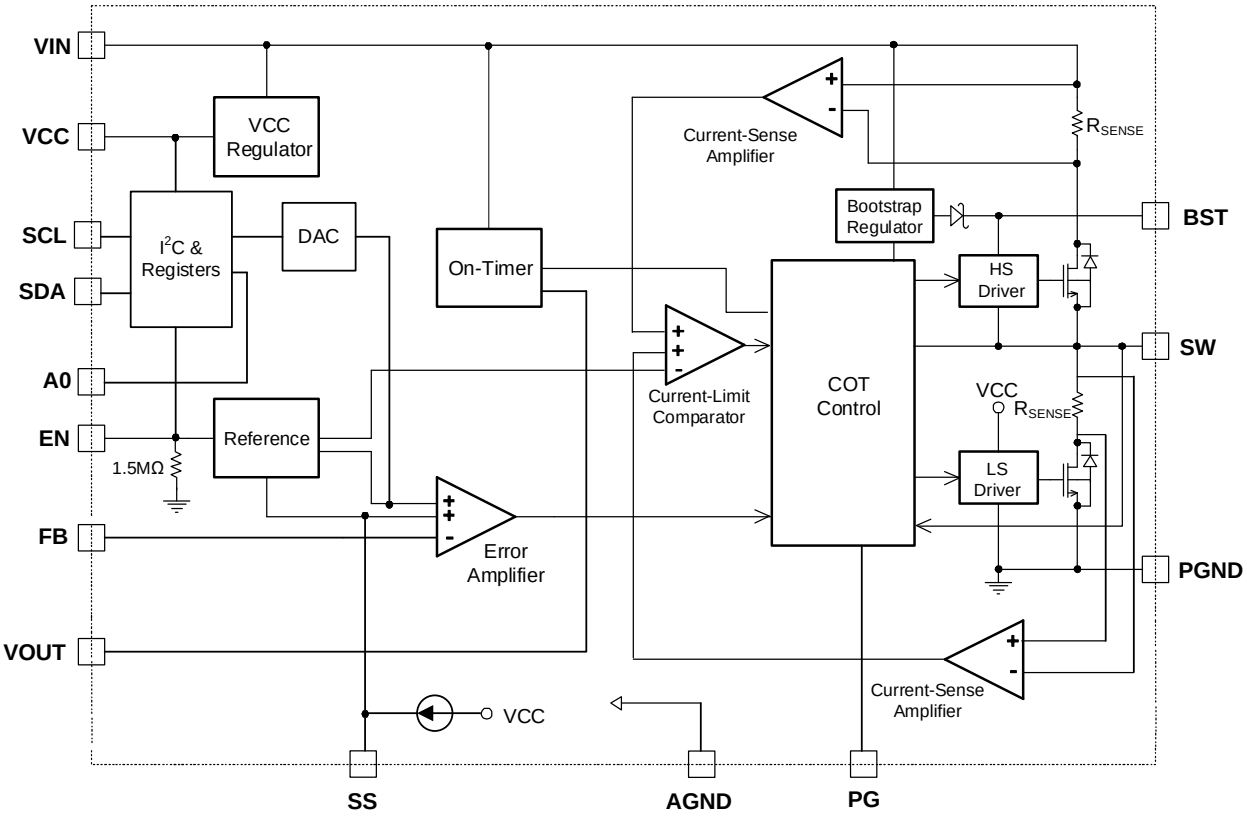

Figure 2: Functional Block Diagram

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OPERATION

Pulse-Width Modulation (PWM) Operation

The MP8869N is a fully integrated, synchronous, rectified, step-down, switch-mode converter. The MP8869N uses constant-on-time (COT) control to provide fast transient response and ease loop stabilization. Figure 3 shows the simplified ramp compensation block.

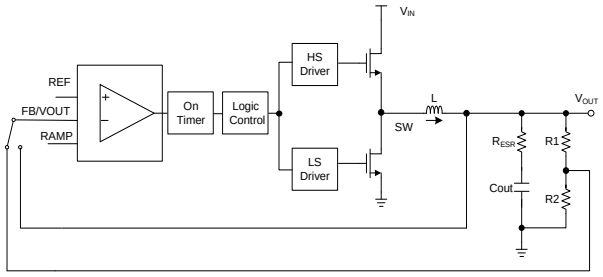

Figure 3: Simplified Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on whenever the ramp voltage (V_{RAMP}) is below the error amplifier (EA) output voltage (V_{EAO}), which indicates an insufficient output voltage (V_{OUT}). The on time is determined by both V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the entire V_{IN} range.

After the on time elapses, the HS-FET turns off. By cycling the HS-FET on and off, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss.

Shoot-through occurs when both the HS-FET and LS-FET are on at the same time, causing a dead short between input and GND, which dramatically reduces efficiency. The MP8869N prevents shoot-through by generating a dead time (DT) internally between the HS-FET off period and the LS-FET on period, and vice versa. The MP8869N enters either heavy-load operation or light-load operation, depending on the amplitude of the output current (I_{OUT}).

Switching Frequency

The MP8869N uses COT control, and there is no dedicated oscillator in the IC. V_{IN} is fed into the one-shot on-timer through the internal frequency resistor. The duty ratio is V_{OUT} / V_{IN}, and f_{SW} is fairly constant across the entire V_{IN} range.

The MP8869N's f_{SW} can be adjusted by setting bits D[5:4] in register 02 via I^2C communication. When V_{OUT} is low and V_{IN} is high, the switching on time may be limited by the internal minimum on time limit, and f_{SW} decreases. Table 1 shows the maximum f_{SW} vs. V_{OUT} when V_{IN} = 12V and when V_{IN} = 5V.

Table 1: Maximum Frequency vs. Output Voltage

V_{OUT} (V)	Maximum Frequency	
	V_{IN} = 12V	V_{IN} = 5V
5	1.25MHz	/
3.3	1.25MHz	1.25MHz
2.5	1.25MHz	1.25MHz
1.8	1.25MHz	1.25MHz
1.5	1.25MHz	1.25MHz
1.2	1MHz	1.25MHz
1	750kHz	1.25MHz
0.9	750kHz	1.25MHz
0.6	500kHz	1.25MHz

Forced Pulse-Width Modulation (PWM) Operation

When the MP8869N works in forced pulse-width modulation (PWM) mode, the IC enters continuous conduction mode (CCM), in which the HS-FET and LS-FET repeat the on/off operation, even if the inductor current is 0A or a negative value. f_{SW} remains fairly constant (see Figure 4).

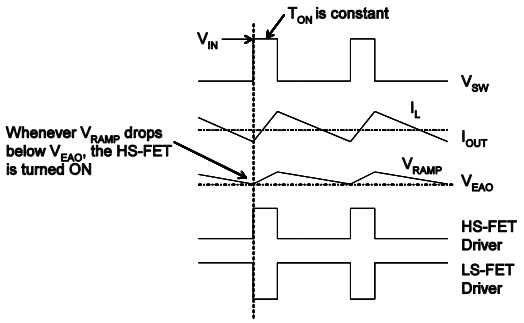

Figure 4: Forced PWM Operation

Light-Load Operation

When the MP8869N works in auto-PWM, automatic pulse-frequency modulation (PFM) mode, or light-load operation, the MP8869N reduces f_{SW} automatically to maintain high efficiency, and the inductor current drops almost to 0A. When the inductor current reaches 0A, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 5 on page 21).

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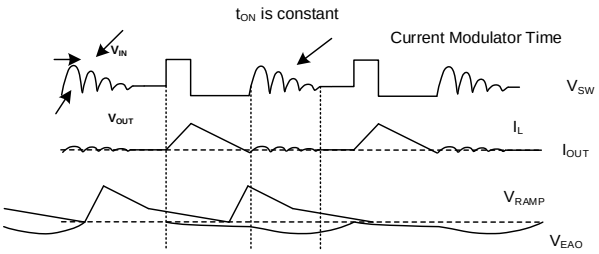

Figure 5: Light-Load Operation

The output capacitors discharge slowly to GND through R1 and R2. This operation improves device efficiency greatly when I_{OUT} is low.

Light-load operation is also called skip mode, since the HS-FET does not turn on as frequently as it does during heavy-load condition. The frequency at which the HS-FET turns on is a function of I_{OUT}. As I_{OUT} increases, the current modulator regulation period becomes shorter, the HS-FET turns on more frequently, and f_{SW} increases. I_{OUT} reaches its critical level when the current modulator time is zero, and can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The MP8869N reverts to PWM mode once I_{OUT} exceeds its critical level. f_{SW} then remains fairly constant across the entire I_{OUT} range.

The MP8869N can operate in PFM mode under light loads to improve efficiency (low-power mode). The MP8869N can also operate in forced PWM mode under any load condition. This mode is selectable via the I²C. To enable low-power mode, set the MODE bit to 0. To disable low-power mode and make the converter will work in forced PWM mode, set the MODE bit to 1. The MODE bit is set to 0 (PFM) by default.

Operating without an External Ramp

The traditional COT control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to be an effective current-sense resistor. Ceramic capacitors cannot typically be used as output capacitor. The MP8869N has built-in, internal ramp compensation to ensure that the system is stable, even without the help of the output capacitor's ESR. The pure ceramic capacitor solution can significantly reduce the output ripple, total BOM cost, and board area.

VCC Regulator

A 3.5V internal regulator powers most of the internal circuitries. A 470nF decoupling capacitor is required to stabilize the regulator and reduce ripple. This regulator takes the V_{IN} input and operates across the full V_{IN} range. After EN is pulled high and V_{IN} exceeds 3.5V, the output of the regulator is in full regulation. When V_{IN} falls below 3.5V, V_{OUT} decreases and follows V_{IN}. A 0.47µF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier (EA) compares the FB voltage (V_{FB}) to the internal reference voltage (V_{REF}) and outputs a PWM signal. V_{REF} can to be between 0.6V and 1.108V via the I²C. The optimized internal ramp compensation minimizes the external component count and simplifies control loop design.

Enable (EN)

EN is a digital control pin that turns the regulator, including the I²C block, on and off. Drive EN high to turn the regulator on; drive EN low to turn it off. An internal 1.5MΩ resistor is connected from EN to ground. EN can operate with an 18V V_{IN}, which allows EN to be connected directly to VIN for automatic start-up. When the external EN is high, set the EN bit in register 01 to 0 to stop the HS-FET and LS-FET from switching. The MP8869N resumes switching when the EN bit is set to 1.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8869N UVLO comparator monitors the VCC regulator's V_{IN} and V_{OUT}. The MP8869N is active when these voltages exceed the UVLO rising threshold.

Soft Start (SS) and Pre-Biased Start-Up

Soft start (SS) prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to V_{CC}. When SS is below V_{REF}, the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

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The typical soft-start time (t_{SS}) can be estimated with Equation (2):

$$t_{ss}(ms) = \frac{V_{ref}(V) \times C_{ss}(nF)}{7\mu A} \quad (2)$$

Where V_{REF} is the reference voltage.

If the MP8869N's output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the HS-FET and LS-FET until the voltage on the internal SS capacitor exceeds the sensed V_{FB}.

The MP8869N also provides a selectable soft shutdown function, which defines the output discharge behavior after an EN shutdown. By default, the output is not controlled after EN shutdown. If setting the soft shutdown control bit D[3] to 1 in register 02 via the I^2C, the output is discharged linearly to zero in a quarter of t_{SS}.

Over-Current Protection (OCP)

The MP8869N has default, hiccup, cycle-by-cycle, over-current (OC) limiting control. The current-limit circuit employs both a high-side current limit and a low-side valley current-sensing algorithm. The MP8869N uses the LS-FET's $R_{DS(ON)}$ as a current-sensing element for the valley current limit. If the magnitude of the high-side current-sense signal exceeds the current-limit threshold, then the PWM on pulse is terminated and the LS-FET turns on. Afterward, the inductor current is monitored by the voltage between GND and SW. GND is used as the positive current-sensing node, so GND should be connected to the bottom MOSFET's source terminal. PWM cannot initiate a new cycle before the inductor current falls to the valley threshold.

After the cycle-by-cycle OC limit occurs, V_{OUT} drops until it falls below the under-voltage (UV) threshold (typically 60% below V_{REF}). Once UV is triggered, the MP8869N enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. Once the OC condition is removed, the MP8869N exits hiccup mode and resumes normal operation.

Short the output to ground first, then start up the part. The MP8869N's I^2C is disabled in this condition. Once the short circuit is removed, the I^2C resumes normal operation. If the hiccup OCP bit D[1] in register 01 is set to 0, then a latch-off occurs if OCP and FB under-voltage protection (UVP) are triggered.

Power Good (PG)

The power good (PG) pin indicates whether V_{OUT} is within the normal range compared to the internal V_{REF}. PG is an open-drain structure. An external pull-up supply is required. During start-up, the PG output is pulled low. This indicates to the system to remain off and keep the output load to a minimum, which helps reduce in-rush current at start-up.

When V_{OUT} is above 90% and below 115% of the internal V_{REF} and soft start is complete, then the PG signal is pulled high. When V_{OUT} is below 85% of V_{REF} after soft start completes, the PG signal remains low. When V_{OUT} exceeds 115% of the internal V_{REF}, PG goes low. The PG signal rises back to high after V_{OUT} drops below 105% of the internal V_{REF}.

PG implements an adjustable deglitch time via the I^2C whenever V_{OUT} crosses the under-voltage (UV) and over-voltage (OV) rising and falling thresholds. This guarantees the correct indication when V_{OUT} is scaled via the I^2C.

If EN UVLO, input UVLO, OCP, or over-temperature protection (OTP) are triggered, the PG output is pulled low immediately.

Input Over-Voltage Protection (V_{IN} OVP)

The MP8869N monitors V_{IN} to detect an input OV event. This function is active only when the output is in OV or a soft shutdown condition. When the output is in OVP or soft shutdown is enabled, output discharge is enabled to charge V_{IN} high. When V_{IN} exceeds the input OVP threshold, both the HS-FET and LS-FET stop switching.

Output Over-Voltage Protection (OVP)

The MP8869N monitors both V_{FB} and V_{OUT} to detect an OV event. When V_{FB} exceeds 125% of V_{REF}, an internal comparator monitors V_{FB}, and the controller enters dynamic regulation mode.

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V_{IN} may be charged up during this time. If input OVP is triggered, the IC stops switching. If OVP mode is set to auto-retry via the I²C, then the IC begins switching once V_{IN} drops below the V_{IN} OVP recovery threshold. Otherwise, the MP8869N latches off. OVP auto-retry mode and latch-off mode occur only if soft start has completed.

Dynamic regulation mode can be operated by turning on the LS-FET until the low-side negative current limit is triggered. Then the body diode of the HS-FET freewheels the current.

The output power (P_{OUT}) charges the input, which may trigger V_{IN} OVP. In V_{IN} OVP, neither the HS-FET or LS-FET turn on and V_{IN} continues charging. If the output is still OV and V_{IN} drops below the V_{IN} OVP threshold, this operation repeats. If V_{OUT} is below 110% of the internal V_{REF}, then the device exits output OVP.

Output Absolute Over-Voltage Protection (OVP_ABS)

The MP8869N's V_{OUT} can be adjusted by V_{REF} and the external resistor dividers. However, V_{OUT} must be set below the absolute OVP threshold (typically 6.5V).

The MP8869N monitors V_{OUT} to detect absolute OVP. When V_{OUT} exceeds 6.5V, the controller enters dynamic regulation mode if the OVP retry bit in register 01 is set to 1. Otherwise, the MP8869N latches off when output OVP and input OVP are both triggered. Absolute OVP works once both V_{IN} and EN exceed their rising thresholds. This means that this function can work even during soft start.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. Once the temperature falls below its lower threshold (typically 140°C), the chip is enabled again.

The D[1] and D[2] bits in register 06 provide more information about the IC silicon temperature.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor (C_{BST}) powers the floating MOSFET driver. This floating driver has its own UVLO protection. This UVLO rising threshold is 2.4V, with a 150mV hysteresis. The C_{BST} voltage is internally regulated by VIN through D1, M1, C4, L1, and C2 (see Figure 6). If V_{BST} - V_{SW} exceeds 3.3V, then U1 regulates M1 to maintain a 3.3V BST voltage across C4.

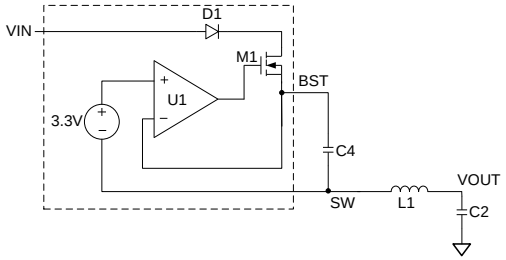

Figure 6: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If V_{IN}, V_{CC}, and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, V_{IN} low, V_{CC} low, thermal shutdown, OVP latch-off, and OCP latch-off. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{EAO} and the internal supply rail are then pulled down.

I²C Control and Default Output Voltage

When the MP8869N is enabled, V_{OUT} is determined by the FB resistors with a programmed t_{SS}. After that, the I²C bus can communicate with the master. If the chip does not receive a continuous I²C communication signal, it can work well through FB and perform behavior similar to a traditional non-I²C part. V_{OUT} is determined by the resistor dividers R1, R2, and V_{REF}. V_{OUT} can be calculated using Equation (3):

$$V_{OUT} = V_{REF} \times (\frac{R1+R2}{R2}) \quad (3)$$

Note that V_{OUT} cannot be set above the absolute OVP threshold (typically 6.5V).

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I²C Slave Address

To support multiple devices used on the same I²C bus, A0 can be used to select four different addresses. A resistor divider from VCC to GND can achieve an accurate V_{REF}. Connect A0 to V_{REF} to set a different I²C slave address (see Figure 7).

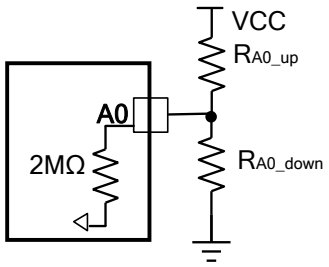

Figure 7: I²C Slave Address Selection Set-Up

The internal circuit changes the I²C address accordingly. When the master sends an 8-bit address value, the 7-bit I²C address should be followed by 0 or 1 to indicate a write or read operation, respectively. Table 2 shows the recommended I²C address selection by the A0 voltage.

Table 2: Recommended I²C Slave Address Selection by A0 Resistor Divider

A0 Upper Resistor R_{A0_UP} (kΩ)	A0 Lower Resistor R_{A0_DOWN} (kΩ)	I²C Slave Address	
		Binary	Hex
Not connected	Not connected	110 0001	61h
500	300	110 0011	63h
300	500	110 0101	65h
100	Not connected	110 0111	67h

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I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MP8869N interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The transition slew rate, V_{OUT}, and other parameters can be instantaneously controlled via the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The data line's high or low state can only change when the clock signal on the SCL line is low (see Figure 8).

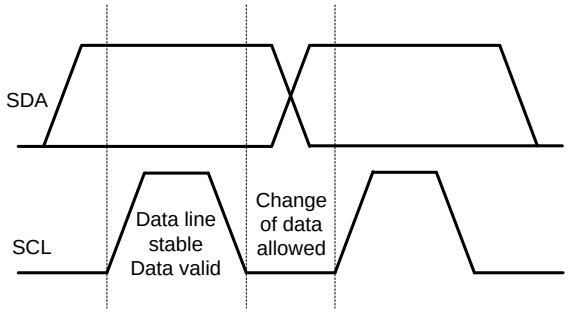

Figure 8: Bit Transfer on the I²C Bus

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of an I²C transfer. A start command is defined as the SDA signal transitioning from high to low while the SCL is high. A stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

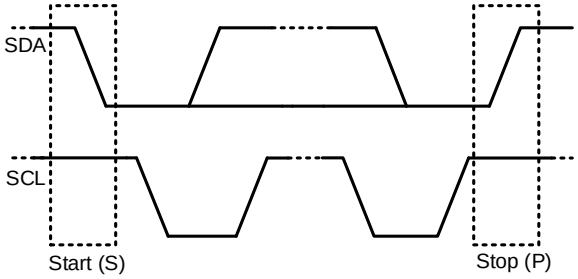

Figure 9: Start and Stop Commands

Start and stop commands are always generated by the master. The bus is considered busy after a start command is sent, and is considered to be free again after a minimum of 4.7μs after a stop command is sent. The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. Start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains at stable low during the high period of this clock pulse.

Figure 10 shows the format that data transfers follow. After a start command, a slave address is sent. This address is 7 bits long, followed by an 8th bit data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

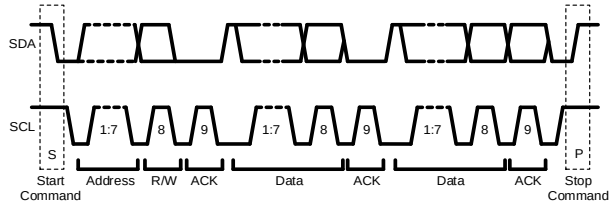

Figure 10: Complete Data Transfer

The MP8869N requires a start command, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MP8869N acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8869N. The MP8869N performs an update on the falling edge of the LSB byte.

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I²C WRITE AND READ SEQUENCE EXAMPLE

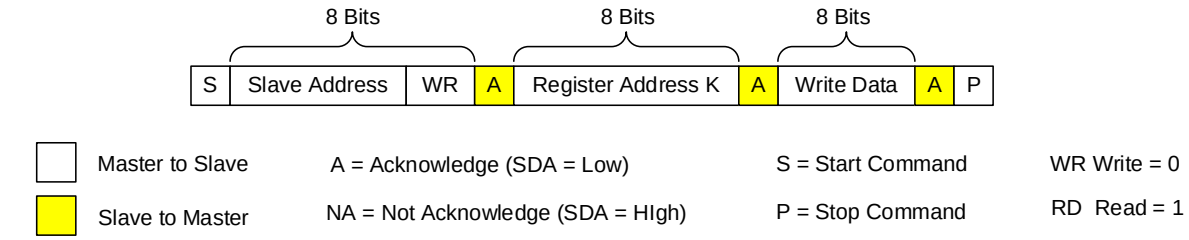

Figure 11: I²C Single-Register Write Example

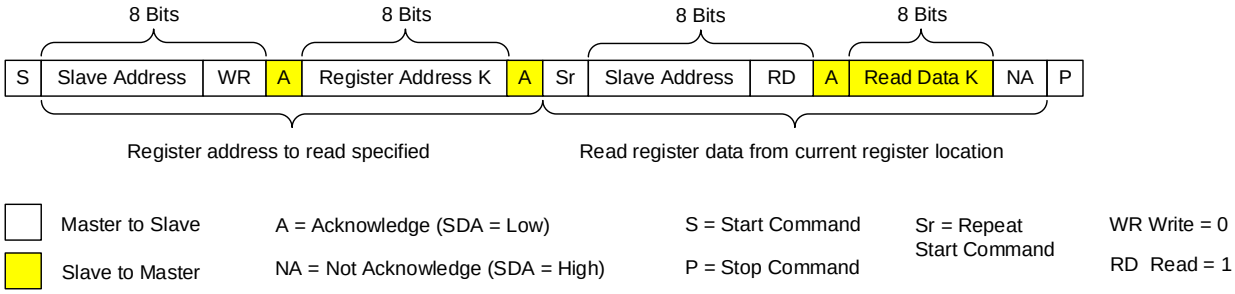

Figure 12: I²C Single-Register Read Example

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REGISTER DESCRIPTION

Register Map

The MP8869N contains 7 write or read registers. Register 00 is the feedback reference voltage (V_{REF}) selection register. Register 01 is the first system control register, and can be used to set the slew rate, hiccup OCP, etc. Register 02 is the second system control register, and can be used to set f_{SW}, the current limit, etc.

Register 03 and register 04 are I_{OUT} and V_{OUT} indication registers. Register 05 is the IC ID register. Register 06 is the IC status indication register, and can be used to check if the IC is in OCP, over-temperature protection (OTP) status, etc. The register map is shown below.

Add	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	RESERVED	FEEDBACK_REFERENCE						
01	SYSCNTL REG1	R/W	EN	GO_ BIT	SLEW_RATE			RETRY _OVP	HICCUP _OCP	MODE
02	SYSCNTL REG2	R/W	PG_DEGLITCH_ TIME		SWITCHING_ FREQUENCY		SOFT_ SHUT DOWN	CURRENT_LIMIT_ADJUST		
03	OUTPUT_ CURRENT	R	OUTPUT_CURRENT							
04	OUTPUT_ VOLTAGE	R	OUTPUT_VOLTAGE							
05	ID1	R	VENDOR_ID				DIE_ID			
06	STATUS	R	RESERVED				OC	OTEW	OT	PG

1) Reg00 VSEL

Register 00 is the V_{REF} selection register. The MP8869N's default V_{REF} is 0.72V, so the MP8869N's default V_{OUT} is determined by the FB resistor divider and 0.72V default V_{REF} after power start-up or EN start-up. V_{REF} is adjustable from 0.6V to 1.108V. Before adjusting V_{REF}, GO_BIT in register 01 should be set to 1, and then V_{REF} can be adjusted by the lower 7 bits of register 00.

Once V_{REF} has been set, GO_BIT auto-resets to 0 to prevent false V_{OUT} scaling. GO_BIT should be set to 1 before adjusting V_{REF} via the I^2C.

Table 3 on page 28 shows the V_{REF} selection chart from 0.6V to 1.108V via the I^2C.

Name	Bits	Default	Description
RESERVED	D[7]	0	Reserved for future use.
FEEDBACK_ REFERENCE	D[6:0]	001 1110	These bits set V_{REF} from 0.6V to 1.108V (see Table 3 on page 28). The default value is 0.72V.

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Table 3: Feedback Reference Voltage Selection Chart

D[6:0]	V_{REF} (V)	D[6:0]	V_{REF} (V)	D[6:0]	V_{REF} (V)	D[6:0]	V_{REF} (V)
000 0000	0.6	010 0000	0.728	100 0000	0.856	110 0000	0.984
000 0001	0.604	010 0001	0.732	100 0001	0.86	110 0001	0.988
000 0010	0.608	010 0010	0.736	100 0010	0.864	110 0010	0.992
000 0011	0.612	010 0011	0.74	100 0011	0.868	110 0011	0.996
000 0100	0.616	010 0100	0.744	100 0100	0.872	110 0100	1
000 0101	0.62	010 0101	0.748	100 0101	0.876	110 0101	1.004
000 0110	0.624	010 0110	0.752	100 0110	0.88	110 0110	1.008
000 0111	0.628	010 0111	0.756	100 0111	0.884	110 0111	1.012
000 1000	0.632	010 1000	0.76	100 1000	0.888	110 1000	1.016
000 1001	0.636	010 1001	0.764	100 1001	0.892	110 1001	1.02
000 1010	0.64	010 1010	0.768	100 1010	0.896	110 1010	1.024
000 1011	0.644	010 1011	0.772	100 1011	0.9	110 1011	1.028
000 1100	0.648	010 1100	0.776	100 1100	0.904	110 1100	1.032
000 1101	0.652	010 1101	0.78	100 1101	0.908	110 1101	1.036
000 1110	0.656	010 1110	0.784	100 1110	0.912	110 1110	1.04
000 1111	0.66	010 1111	0.788	100 1111	0.916	110 1111	1.044
001 0000	0.664	011 0000	0.792	101 0000	0.92	111 0000	1.048
001 0001	0.668	011 0001	0.796	101 0001	0.924	111 0001	1.052
001 0010	0.672	011 0010	0.8	101 0010	0.928	111 0010	1.056
001 0011	0.676	011 0011	0.804	101 0011	0.932	111 0011	1.06
001 0100	0.68	011 0100	0.808	101 0100	0.936	111 0100	1.064
001 0101	0.684	011 0101	0.812	101 0101	0.94	111 0101	1.068
001 0110	0.688	011 0110	0.816	101 0110	0.944	111 0110	1.072
001 0111	0.692	011 0111	0.82	101 0111	0.948	111 0111	1.076
001 1000	0.696	011 1000	0.824	101 1000	0.952	111 1000	1.08
001 1001	0.7	011 1001	0.828	101 1001	0.956	111 1001	1.084
001 1010	0.704	011 1010	0.832	101 1010	0.96	111 1010	1.088
001 1011	0.708	011 1011	0.836	101 1011	0.964	111 1011	1.092
001 1100	0.712	011 1100	0.84	101 1100	0.968	111 1100	1.096
001 1101	0.716	011 1101	0.844	101 1101	0.972	111 1101	1.1
001 1110	0.72	011 1110	0.848	101 1110	0.976	111 1110	1.104
001 1111	0.724	011 1111	0.852	101 1111	0.98	111 1111	1.108

2) Reg01 SYSCNTLREG1

Register 01 is the first system control register.

The highest bit, EN, can be used to turn the part on and off when the external EN pin is high. When the external EN pin is high, the MP8869N shuts down by setting the EN bit to 0, and then the HS-FET and LS-FET stop switching. Set the EN bit to 1 again for the MP8869N to resume switching. When the external EN pin is low, the converter is off and the I^2C shuts down.

Set GO_BIT to 1 to enable the I^2C to write the V_{REF} value. Once the command is finished, GO_BIT auto-resets to 0 to prevent false V_{OUT} scaling.

The IC switches to forced PWM mode when GO_BIT is set to 1 to achieve a smooth output waveform during output dynamic scaling. Once the output scaling is complete, GO_BIT resets to 0 automatically, and the IC operation mode switches to the original mode set by the MODE bit.

The 3-bit slew rate D[5:3] is used for slew rate selection during V_{OUT} dynamic scaling. A proper slew rate reduces the inrush current, as well as voltage overshoot and undershoot. Eight different slew rate levels can be selected.

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The RETRY_OVP bit defines the protection mode when OVP is triggered. When RETRY_OVP is set to 1, the part enters auto-recovery once the OVP condition is removed. When RETRY_OVP is set to 0, the MP8869N latches off if output OVP occurs, and remains off until VIN or EN are toggled.

The HICCUP_OCP bit defines the OCP mode. When HICCUP_OCP is set to 1, the MP8869N enters hiccup mode if OCP and UVP are both triggered. When HICCUP_OCP is set to 0, the MP8869N latches off if OCP and UVP are both triggered.

The lowest bit, MODE, selects forced PWM or auto-PFM/PWM mode under light-load conditions. When MODE is set to 0, auto-PFM/PWM mode is enabled under light-load conditions. When MODE is set to 1, forced PWM mode is enabled under light-load conditions.

<table>
<tr><th>Name</th><th>Bits</th><th>Default</th><th>Description</th></tr>
<tr><td>EN</td><td>D[7]</td><td>1</td><td>This bit turns the part on and off via the I²C. When the external EN pin is low, the converter is off and the I²C shuts down. When the external EN pin is high, the EN bit takes over. The default is 1.</td></tr>
<tr><td>GO_BIT</td><td>D[6]</td><td>0</td><td>Enables the I²C to write the V_{REF} value. Set GO_BIT = 1 to enable the I²C authority to write V_{REF}. When the command is finished, GO_BIT auto-resets to 0 to prevent false V_{OUT} scaling.

Voltage scaling examples:
1) Set GO_BIT = 1.
2) Write register 00 to set V_{REF}.
3) Read back the GO_BIT value to see if V_{OUT} scaling is finished. If GO_BIT = 0, V_{OUT} scaling is done. Otherwise, V_{REF} is still being adjusted.
4) Set GO_BIT = 1 if V_{OUT} scaling is required a second time.
5) Write register 00 to set V_{REF}.</td></tr>
<tr><td>SLEW_RATE</td><td>D[5:3]</td><td>100</td><td>The slew rate during I²C-controlled voltage adjustment is determined by these 3 bits. V_{OUT} changes linearly from the previous voltage to the new set voltage with a slew rate (see the table below). This helps significantly reduce inrush current, voltage overshoot, and voltage undershoot.
<table>
<tr><th>D[5:3]</th><th>Slew Rate</th><th>D[5:3]</th><th>Slew Rate</th></tr>
<tr><td>000</td><td>16mV/µs</td><td>100</td><td>2mV/µs</td></tr>
<tr><td>001</td><td>12mV/µs</td><td>101</td><td>1mV/µs</td></tr>
<tr><td>010</td><td>8mV/µs</td><td>110</td><td>0.5mV/µs</td></tr>
<tr><td>011</td><td>4mV/µs</td><td>111</td><td>0.25mV/µs</td></tr>
</table></td></tr>
<tr><td>RETRY_OVP</td><td>D[2]</td><td>1</td><td>This bit selects the FB or V_{REF} over-voltage protection (OVP) mode.

1: The part auto-recovers when OVP is removed
0: The part latches off if output OVP and V_{IN} OVP are both triggered, and remains off until V_{IN} or EN is power reset</td></tr>
<tr><td>HICCUP_OCP</td><td>D[1]</td><td>1</td><td>This bit selects the over-current protection (OCP) mode.

1: Hiccup mode OCP
0: Latch-off OCP</td></tr>
<tr><td>MODE</td><td>D[0]</td><td>0</td><td>Set this bit to 0 to enable PFM mode. Set it to 1 to disable auto-PFM/PWM mode. The default is auto-PFM/PWM mode for light loads.</td></tr>
</table>

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3) Reg02 SYSCNTLREG2

Register 02 is the second system control register.

The highest 2 bits of the PG deglitch time (D[7:6]) define the PG signal rising and falling edge delay times. When output OVP or UVP is triggered, the PG signal goes low or high after a set delay time. Four levels of PG delay time can be programmed via the I²C for different conditions.

Bits (D[5:4]) select the switching frequency (f_{SW}). The MP8869N supports up to 1.25MHz of f_{SW} by setting these 2 bits to 11. The MP8869N's maximum f_{SW} is limited by internal minimum on time (see Table 1 on page 20).

Name	Bits	Default	Description
PG_ DEGLITCH_ TIME	D[7:6]	11	These bits set the power good (PG) signal rising and falling edge delay times. When V_{FB} or V_{OUT} is outside of its regulation window, the PG comparator is triggered, but there is a delay time before the PG signal can go high or low.
			D[7:6] / PG Deglitch / D[7:6] / PG Deglitch 00 / <1µs / 10 / 12µs 01 / 6µs / 11 / 30µs
SWITCHING _FREQ UENCY	D[5:4]	00	These bits set the switching frequency (f_{SW}). There is no dedicated frequency oscillator inside the part. f_{SW} remains fairly constant by controlling t_{ON}.
			D[5:4] / Frequency / D[5:4] / Frequency 00 / 500kHz / 10 / 1MHz 01 / 750kHz / 11 / 1.25MHz
SOFT_SHUT DOWN	D[3]	0	This bit defines the V_{OUT} discharge behavior after EN shutdown. 0: V_{OUT} is not controlled after EN shutdown 1: V_{OUT} is discharged linearly to 0V with the set soft shutdown time
CURRENT_ LIMIT_ ADJUST	D[2:0]	001	These bits set the valley current limit.
			D[2:0] / Valley Current Limit (A) / D[2:0] / Valley Current Limit (A) 000 / 16 / 100 / 8.5 001 / 14 / 101 / 7 010 / 12 / 110 / 6 011 / 10 / 111 / 5

The SOFT_SHUTDOWN bit determines the V_{OUT} discharge behavior after EN shutdown. When SOFT_SHUTDOWN is set to 0, V_{OUT} is not controlled after EN shutdown. When SOFT_SHUTDOWN is set to 1, V_{OUT} is discharged linearly to 0V with the set soft shutdown time.

The lowest 3 bits, CURRENT_LIMIT_ADJUST D[2:0], select the peak and valley current limits. Eight current limit levels can be selected for different application conditions.

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4) Reg03 OUTPUT_CURRENT

Register 03 is the I_{OUT} indication register. After the MP8869N starts up, the DC I_{OUT} information can be read via the I^2C.

When the inductor current is in discontinuous conduction mode (DCM), the I_{OUT} sense is not very accurate. The MODE bit can be set to 1 (PWM mode) for good current-sensing accuracy under light-load conditions.

When the inductor current enters continuous conduction mode (CCM), the I_{OUT} sense accuracy is excellent (typical accuracy is 5% when I_{OUT} is above 2A).

Table 4 shows the I_{OUT} chart from 0A to 12.75A.

Name	Bits	Default	Description
OUTPUT_CURRENT	D[7:0]	0000 0000	I_{OUT} monitor bits. Table 4 shows the I_{OUT} chart.

Table 4: Output Current Chart

D[7:0]	I_{OUT} (A)	D[7:0]	I_{OUT} (A)	D[7:0]	I_{OUT} (A)	D[7:0]	I_{OUT} (A)	D[7:0]	I_{OUT} (A)	D[7:0]	I_{OUT} (A)
0000 0000	0	0010 1011	2.15	0101 0110	4.3	1000 0001	6.45	1010 1100	8.6	1101 0111	10.75
0000 0001	0.05	0010 1100	2.2	0101 0111	4.35	1000 0010	6.5	1010 1101	8.65	1101 1000	10.8
0000 0010	0.1	0010 1101	2.25	0101 1000	4.4	1000 0011	6.55	1010 1110	8.7	1101 1001	10.85
0000 0011	0.15	0010 1110	2.3	0101 1001	4.45	1000 0100	6.6	1010 1111	8.75	1101 1010	10.9
0000 0100	0.2	0010 1111	2.35	0101 1010	4.5	1000 0101	6.65	1011 0000	8.8	1101 1011	10.95
0000 0101	0.25	0011 0000	2.4	0101 1011	4.55	1000 0110	6.7	1011 0001	8.85	1101 1100	11
0000 0110	0.3	0011 0001	2.45	0101 1100	4.6	1000 0111	6.75	1011 0010	8.9	1101 1101	11.05
0000 0111	0.35	0011 0010	2.5	0101 1101	4.65	1000 1000	6.8	1011 0011	8.95	1101 1110	11.1
0000 1000	0.4	0011 0011	2.55	0101 1110	4.7	1000 1001	6.85	1011 0100	9	1101 1111	11.15
0000 1001	0.45	0011 0100	2.6	0101 1111	4.75	1000 1010	6.9	1011 0101	9.05	1110 0000	11.2
0000 1010	0.5	0011 0101	2.65	0110 0000	4.8	1000 1011	6.95	1011 0110	9.1	1110 0001	11.25
0000 1011	0.55	0011 0110	2.7	0110 0001	4.85	1000 1100	7	1011 0111	9.15	1110 0010	11.3
0000 1100	0.6	0011 0111	2.75	0110 0010	4.9	1000 1101	7.05	1011 1000	9.2	1110 0011	11.35
0000 1101	0.65	0011 1000	2.8	0110 0011	4.95	1000 1110	7.1	1011 1001	9.25	1110 0100	11.4
0000 1110	0.7	0011 1001	2.85	0110 0100	5	1000 1111	7.15	1011 1010	9.3	1110 0101	11.45
0000 1111	0.75	0011 1010	2.9	0110 0101	5.05	1001 0000	7.2	1011 1011	9.35	1110 0110	11.5
0001 0000	0.8	0011 1011	2.95	0110 0110	5.1	1001 0001	7.25	1011 1100	9.4	1110 0111	11.55
0001 0001	0.85	0011 1100	3	0110 0111	5.15	1001 0010	7.3	1011 1101	9.45	1110 1000	11.6
0001 0010	0.9	0011 1101	3.05	0110 1000	5.2	1001 0011	7.35	1011 1110	9.5	1110 1001	11.65
0001 0011	0.95	0011 1110	3.1	0110 1001	5.25	1001 0100	7.4	1011 1111	9.55	1110 1010	11.7
0001 0100	1	0011 1111	3.15	0110 1010	5.3	1001 0101	7.45	1100 0000	9.6	1110 1011	11.75
0001 0101	1.05	0100 0000	3.2	0110 1011	5.35	1001 0110	7.5	1100 0001	9.65	1110 1100	11.8
0001 0110	1.1	0100 0001	3.25	0110 1100	5.4	1001 0111	7.55	1100 0010	9.7	1110 1101	11.85
0001 0111	1.15	0100 0010	3.3	0110 1101	5.45	1001 1000	7.6	1100 0011	9.75	1110 1110	11.9
0001 1000	1.2	0100 0011	3.35	0110 1110	5.5	1001 1001	7.65	1100 0100	9.8	1110 1111	11.95
0001 1001	1.25	0100 0100	3.4	0110 1111	5.55	1001 1010	7.7	1100 0101	9.85	1111 0000	12
0001 1010	1.3	0100 0101	3.45	0111 0000	5.6	1001 1011	7.75	1100 0110	9.9	1111 0001	12.05
0001 1011	1.35	0100 0110	3.5	0111 0001	5.65	1001 1100	7.8	1100 0111	9.95	1111 0010	12.1
0001 1100	1.4	0100 0111	3.55	0111 0010	5.7	1001 1101	7.85	1100 1000	10	1111 0011	12.15
0001 1101	1.45	0100 1000	3.6	0111 0011	5.75	1001 1110	7.9	1100 1001	10.05	1111 0100	12.2
0001 1110	1.5	0100 1001	3.65	0111 0100	5.8	1001 1111	7.95	1100 1010	10.1	1111 0101	12.25
0001 1111	1.55	0100 1010	3.7	0111 0101	5.85	1010 0000	8	1100 1011	10.15	1111 0110	12.3
0010 0000	1.6	0100 1011	3.75	0111 0110	5.9	1010 0001	8.05	1100 1100	10.2	1111 0111	12.35
0010 0001	1.65	0100 1100	3.8	0111 0111	5.95	1010 0010	8.1	1100 1101	10.25	1111 1000	12.4
0010 0010	1.7	0100 1101	3.85	0111 1000	6	1010 0011	8.15	1100 1110	10.3	1111 1001	12.45
0010 0011	1.75	0100 1110	3.9	0111 1001	6.05	1010 0100	8.2	1100 1111	10.35	1111 1010	12.5
0010 0100	1.8	0100 1111	3.95	0111 1010	6.1	1010 0101	8.25	1101 0000	10.4	1111 1011	12.55
0010 0101	1.85	0101 0000	4	0111 1011	6.15	1010 0110	8.3	1101 0001	10.45	1111 1100	12.6
0010 0110	1.9	0101 0001	4.05	0111 1100	6.2	1010 0111	8.35	1101 0010	10.5	1111 1101	12.65
0010 0111	1.95	0101 0010	4.1	0111 1101	6.25	1010 1000	8.4	1101 0011	10.55	1111 1110	12.7
0010 1000	2	0101 0011	4.15	0111 1110	6.3	1010 1001	8.45	1101 0100	10.6	1111 1111	12.75
0010 1001	2.05	0101 0100	4.2	0111 1111	6.35	1010 1010	8.5	1101 0101	10.65		
0010 1010	2.1	0101 0101	4.25	1000 0000	6.4	1010 1011	8.55	1101 0110	10.7		

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5) Reg04 OUTPUT_VOLTAGE

Register 04 is the V_{OUT} indication register. After the part starts up, V_{OUT} can be read via the I^2C. Under light loads, if the MODE bit is set to 0, the MP8869N works in PFM mode. Under extremely light loads or no load, the analog-to-digital converter (ADC) only works when the first pulse comes, and then the MP8869N refreshes the V_{OUT} register before entering sleep mode.

When the part is operating at extremely light loads or no load, the sensed V_{OUT} is the maximum value, not the average V_{OUT}, meaning that the sensed I^2C voltage is above the set point. When there is a greater load, sense accuracy is improved. The MODE bit can be set to 1 (PWM mode) for good voltage-sense accuracy under light-load conditions. Table 5 shows the V_{OUT} chart from 0.5V to 5.643V.

Name	Bits	Default	Description
OUTPUT_VOLTAGE	D[7:0]	0000 0000	V_{OUT} monitor bits. Table 5 shows the V_{OUT} chart.

Table 5: Output Voltage Chart

D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)	D[7:0]	V_{OUT} (V)
0000 0000	0.500	0010 1011	1.367	0101 0110	2.235	1000 0001	3.102	1010 1100	3.969	1101 0111	4.837
0000 0001	0.520	0010 1100	1.387	0101 0111	2.255	1000 0010	3.122	1010 1101	3.989	1101 1000	4.857
0000 0010	0.540	0010 1101	1.408	0101 1000	2.275	1000 0011	3.142	1010 1110	4.010	1101 1001	4.877
0000 0011	0.561	0010 1110	1.428	0101 1001	2.295	1000 0100	3.162	1010 1111	4.030	1101 1010	4.897
0000 0100	0.581	0010 1111	1.448	0101 1010	2.315	1000 0101	3.183	1011 0000	4.050	1101 1011	4.917
0000 0101	0.601	0011 0000	1.468	0101 1011	2.335	1000 0110	3.203	1011 0001	4.070	1101 1100	4.937
0000 0110	0.621	0011 0001	1.488	0101 1100	2.356	1000 0111	3.223	1011 0010	4.090	1101 1101	4.958
0000 0111	0.641	0011 0010	1.509	0101 1101	2.376	1000 1000	3.243	1011 0011	4.110	1101 1110	4.978
0000 1000	0.661	0011 0011	1.529	0101 1110	2.396	1000 1001	3.263	1011 0100	4.131	1101 1111	4.998
0000 1001	0.682	0011 0100	1.549	0101 1111	2.416	1000 1010	3.283	1011 0101	4.151	1110 0000	5.018
0000 1010	0.702	0011 0101	1.569	0110 0000	2.436	1000 1011	3.304	1011 0110	4.171	1110 0001	5.038
0000 1011	0.722	0011 0110	1.589	0110 0001	2.456	1000 1100	3.324	1011 0111	4.191	1110 0010	5.058
0000 1100	0.742	0011 0111	1.609	0110 0010	2.477	1000 1101	3.344	1011 1000	4.211	1110 0011	5.079
0000 1101	0.762	0011 1000	1.630	0110 0011	2.497	1000 1110	3.364	1011 1001	4.231	1110 0100	5.099
0000 1110	0.782	0011 1001	1.650	0110 0100	2.517	1000 1111	3.384	1011 1010	4.252	1110 0101	5.119
0000 1111	0.803	0011 1010	1.670	0110 0101	2.537	1001 0000	3.404	1011 1011	4.272	1110 0110	5.139
0001 0000	0.823	0011 1011	1.690	0110 0110	2.557	1001 0001	3.425	1011 1100	4.292	1110 0111	5.159
0001 0001	0.843	0011 1100	1.710	0110 0111	2.578	1001 0010	3.445	1011 1101	4.312	1110 1000	5.179
0001 0010	0.863	0011 1101	1.730	0110 1000	2.598	1001 0011	3.465	1011 1110	4.332	1110 1001	5.200
0001 0011	0.883	0011 1110	1.751	0110 1001	2.618	1001 0100	3.485	1011 1111	4.352	1110 1010	5.220
0001 0100	0.903	0011 1111	1.771	0110 1010	2.638	1001 0101	3.505	1100 0000	4.373	1110 1011	5.240
0001 0101	0.924	0100 0000	1.791	0110 1011	2.658	1001 0110	3.526	1100 0001	4.393	1110 1100	5.260
0001 0110	0.944	0100 0001	1.811	0110 1100	2.678	1001 0111	3.546	1100 0010	4.413	1110 1101	5.280
0001 0111	0.964	0100 0010	1.831	0110 1101	2.699	1001 1000	3.566	1100 0011	4.433	1110 1110	5.300
0001 1000	0.984	0100 0011	1.851	0110 1110	2.719	1001 1001	3.586	1100 0100	4.453	1110 1111	5.321
0001 1001	1.004	0100 0100	1.872	0110 1111	2.739	1001 1010	3.606	1100 0101	4.473	1111 0000	5.341
0001 1010	1.024	0100 0101	1.892	0111 0000	2.759	1001 1011	3.626	1100 0110	4.494	1111 0001	5.361
0001 1011	1.045	0100 0110	1.912	0111 0001	2.779	1001 1100	3.647	1100 0111	4.514	1111 0010	5.381
0001 1100	1.065	0100 0111	1.932	0111 0010	2.799	1001 1101	3.667	1100 1000	4.534	1111 0011	5.401
0001 1101	1.085	0100 1000	1.952	0111 0011	2.820	1001 1110	3.687	1100 1001	4.554	1111 0100	5.421
0001 1110	1.105	0100 1001	1.972	0111 0100	2.840	1001 1111	3.707	1100 1010	4.574	1111 0101	5.442
0001 1111	1.125	0100 1010	1.993	0111 0101	2.860	1010 0000	3.727	1100 1011	4.595	1111 0110	5.462
0010 0000	1.145	0100 1011	2.013	0111 0110	2.880	1010 0001	3.747	1100 1100	4.615	1111 0111	5.482
0010 0001	1.166	0100 1100	2.033	0111 0111	2.900	1010 0010	3.768	1100 1101	4.635	1111 1000	5.502
0010 0010	1.186	0100 1101	2.053	0111 1000	2.920	1010 0011	3.788	1100 1110	4.655	1111 1001	5.522
0010 0011	1.206	0100 1110	2.073	0111 1001	2.941	1010 0100	3.808	1100 1111	4.675	1111 1010	5.543
0010 0100	1.226	0100 1111	2.093	0111 1010	2.961	1010 0101	3.828	1101 0000	4.695	1111 1011	5.563
0010 0101	1.246	0101 0000	2.114	0111 1011	2.981	1010 0110	3.848	1101 0001	4.716	1111 1100	5.583
0010 0110	1.266	0101 0001	2.134	0111 1100	3.001	1010 0111	3.868	1101 0010	4.736	1111 1101	5.603
0010 0111	1.287	0101 0010	2.154	0111 1101	3.021	1010 1000	3.889	1101 0011	4.756	1111 1110	5.623
0010 1000	1.307	0101 0011	2.174	0111 1110	3.041	1010 1001	3.909	1101 0100	4.776	1111 1111	5.643
0010 1001	1.327	0101 0100	2.194	0111 1111	3.062	1010 1010	3.929	1101 0101	4.796		
0010 1010	1.347	0101 0101	2.214	1000 0000	3.082	1010 1011	3.949	1101 0110	4.816		

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5) Reg06 ID1

Register 05 is the IC information indication register. The highest 4 bits, VENDOR_ID D[7:4], are set to 1000 internally.

The lowest 4 bits, IC_REVISION_ID D[3:0], indicate the IC revision information.

Name	Bits	Description
VENDOR_ID	D[7:4]	1000.
IC_REVISION_ID	D[3:0]	IC revision.

7) Reg06 STATUS

Register 06 is a fault condition indication register. The highest 4 bits, D[7:4], are reserved for future use.

The OC bit indicates whether there is an output over-current (OC) condition. When this bit is set to 1, the IC is in hiccup mode or OC latch-off.

The OTEW bit is the die temperature early warning indication. When this bit is set to 1, the IC die temperature is above 120°C.

The PG bit is the output power good indication. When the bit is set to 1, V_{OUT} is normal.

Name	Bits	Description
RESERVED	D[7:4]	Reserved for future use.
OC	D[3]	Output over-current (OC) indication. When this bit is high, the IC is in hiccup mode or OC latch-off.
OTEW	D[2]	Die temperature early warning bit. When the bit is high, the die temperature is above 120°C.
OT	D[1]	Over-temperature (OT) indication. When this bit is high, the IC is in thermal shutdown.
PG	D[0]	Output power good (PG) indication. When the bit is high, V_{OUT} is normal. This means V_{OUT} is above 95% and below 115% of V_{REF}. PG compares V_{FB} / V_{OUT} with V_{REF}.

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APPLICATION INFORMATION

Setting the Output Voltage in an FB Control Loop

The MP8869N can be controlled by the FB loop. V_{OUT} can be set by the external resistor dividers. The FB loop reference voltage is a default value (0.72V), and can be configured by the I²C. The MP8869N's V_{OUT} must be below the absolute OVP threshold (typically 6.5V).

Figure 13 shows the FB loop network.

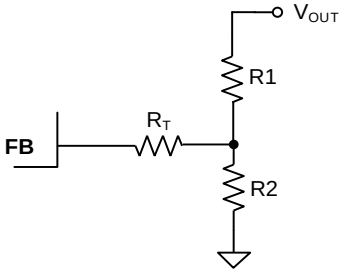

Figure 13: FB Loop Network

Calculate R1 and R2 with Equation (4):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.72V} - 1} \quad (4)$$

Table 6 lists the recommended feedback resistors value for common output voltages.

Table 6: Resistor Selection for Common Output Voltages (8)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (μH)
1.0	80.6	205	10	1.5
1.2	80.6	121	10	1.5
1.5	80.6	74.4	10	1.5
1.8	80.6	53.6	10	1.5
2.5	80.6	32.4	10	2.2
3.3	80.6	22.6	10	2.2
5	80.6	13.7	10	3.3

Note:

8) The recommended parameters are based on a 12V V_{IN} and a 22μF x 4 output capacitor. Different V_{IN} and output capacitor values may affect the selection of R1 and R2. For other components' parameters, see the Typical Application Circuits section on page 38.

Output Voltage Dynamic Scaling

V_{OUT} dynamic scaling can only be done via the I²C. Refer to Figure 14 and follow the steps below:

1) Write GO_BIT (Reg01, D[6]) to 1.
2) Write Reg00 to set V_{REF} (Reg00 [6:0]) simultaneously. When the command is complete, GO_BIT auto-resets to 0 to prevent false V_{OUT} scaling.

Repeat the above two steps if V_{OUT} must be changed to a different voltage.

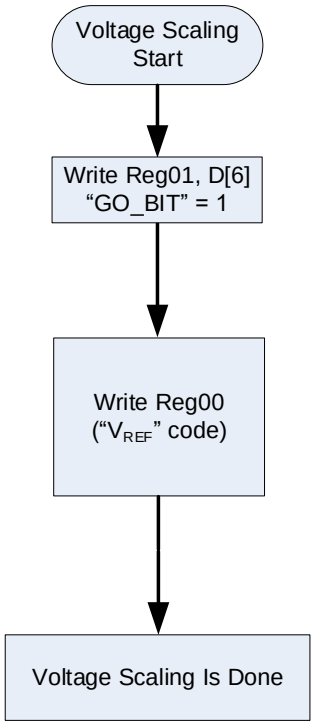

Figure 14: V_{OUT} Dynamic Scaling Flowchart

Selecting the Inductor

It is recommended to use a 0.47μH to 5μH inductor with a DC current rating at least 25% greater than the maximum load current for most applications. For the highest efficiency, use an inductor with a DC resistance less than 5mΩ. For most designs, the inductance (L_1) can be calculated with Equation (5):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

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Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current ($I_{L(MAX)}$) can be calculated with Equation (6):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to use two 22µF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor (I_{C1}) can be estimated with Equation (7):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (8):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input.

Estimate the input voltage ripple (ΔV_{IN}) caused by the capacitance with Equation (9):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (10)$$

Where L_1 is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8869N can be optimized for a wide range of capacitances and ESR values.

Selecting the Bootstrap Capacitor and Resistor

The bootstrap capacitor (C_{BST}) powers the floating MOSFET driver. It is recommended to use 0.1µF ceramic capacitor.

C_{BST} is typically recommended to be between 0 and 10Ω. The BST resistor determines the turn-on speed of the HS-FET. For designs in which the VCC decoupling capacitor layout cannot be optimized and follow the recommended layout, a 10Ω BST resistor is recommended to be used in series with C_{BST}.

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External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- V_{OUT} is 5V or 3.3V
- The duty cycle is high (>50%)

In these cases, add an external BST diode from VCC to BST (see Figure 15).

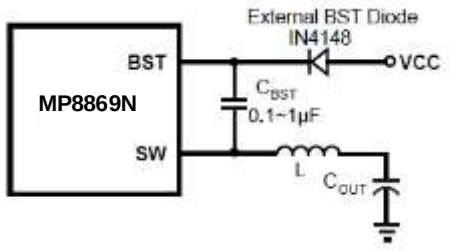

Figure 15: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended C_{BST} value is 0.1µF to 1µF.

Connect VCC to VIN at a Low Input Voltage

VCC can be connected to directly VIN when V_{IN} is below 3.5V. This helps improve the MP8869N's low V_{IN} efficiency. To use this application set-up, the V_{IN} spike voltage must be limited below 4V, otherwise VCC may be damaged.

Design Example

Table 7 shows a design example following the application guidelines for the specifications below.

Table 7: Design Example

V_{IN}	5V
V_{OUT}	1.8V
I_O	12A

For the detailed application schematics, see Figure 17 through Figure 23 on pages 38–40. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 11. For more device applications, refer to the related evaluation board datasheets.

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PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 16 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SW) as close as possible to the device with short, direct, and wide traces.
2. Keep the VIN and PGND pads connected with large copper planes.
3. Use at least 2 layers for the VIN and PGND trace to achieve better thermal performance.
4. Add several vias close to the VIN and PGND pads to help with thermal dissipation.
5. Place the input capacitors as close to VIN and PGND as possible.
6. Place the decoupling capacitor as close to VCC and PGND as possible.
7. Place the external feedback resistors next to FB.
8. Ensure that there is no via on the FB trace.
9. Keep the switching node (SW) short and away from the feedback network.
10. Keep the BST voltage path (BST, C3, and SW) as short as possible.

Note:

9) The recommended layout is based on the Typical Application Circuits section on page 38.

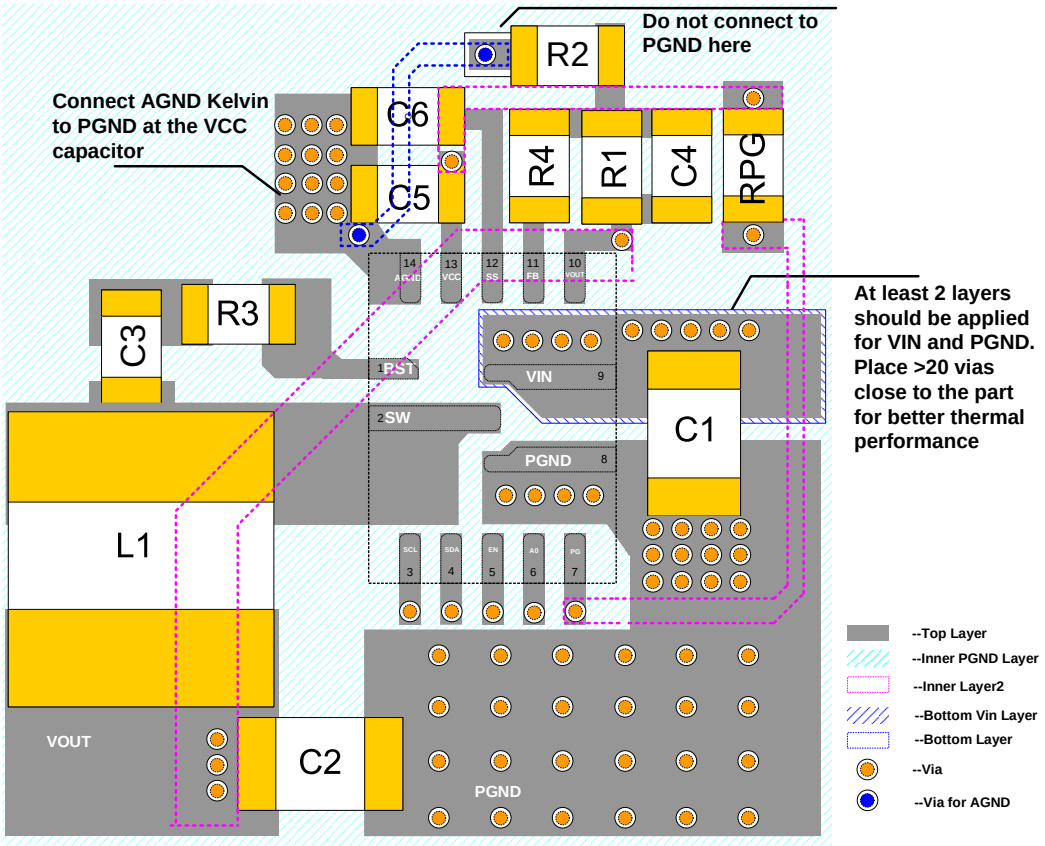

Figure 16: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS (10)

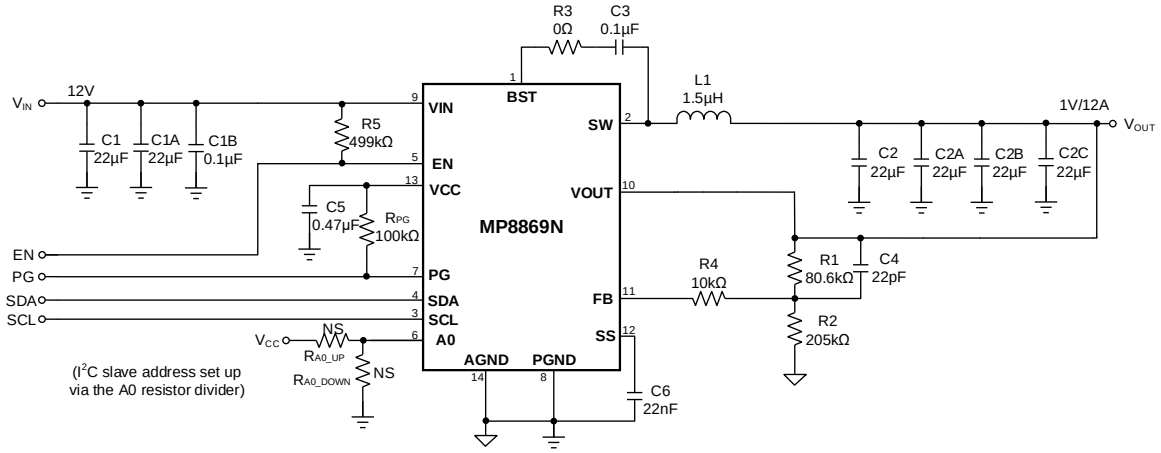

Figure 17: V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A

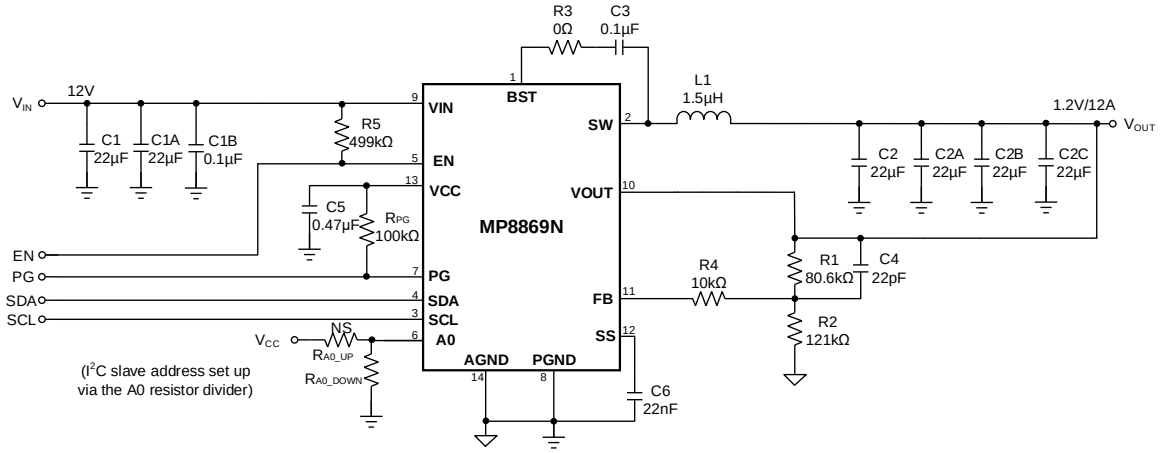

Figure 18: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 12A

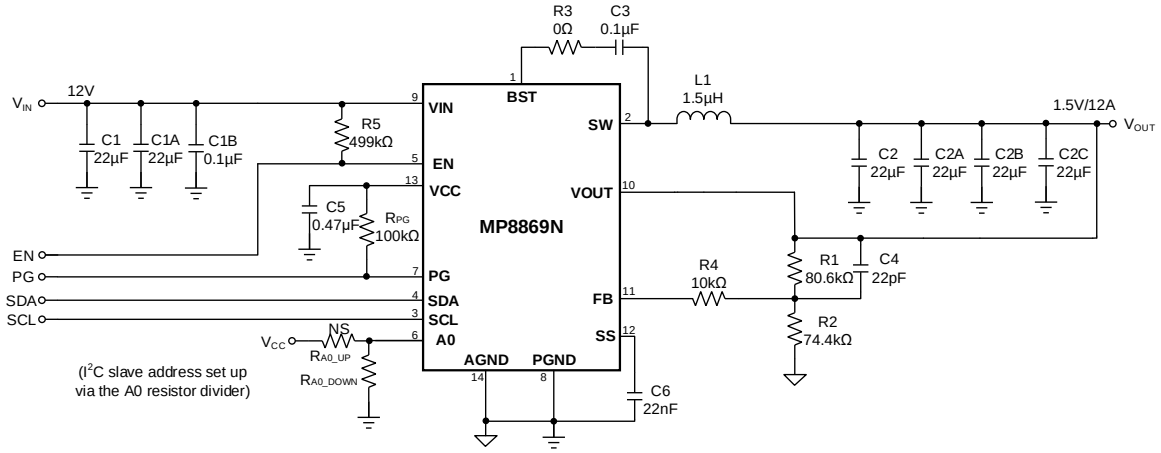

Figure 19: V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A

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TYPICAL APPLICATION CIRCUITS *(continued)*

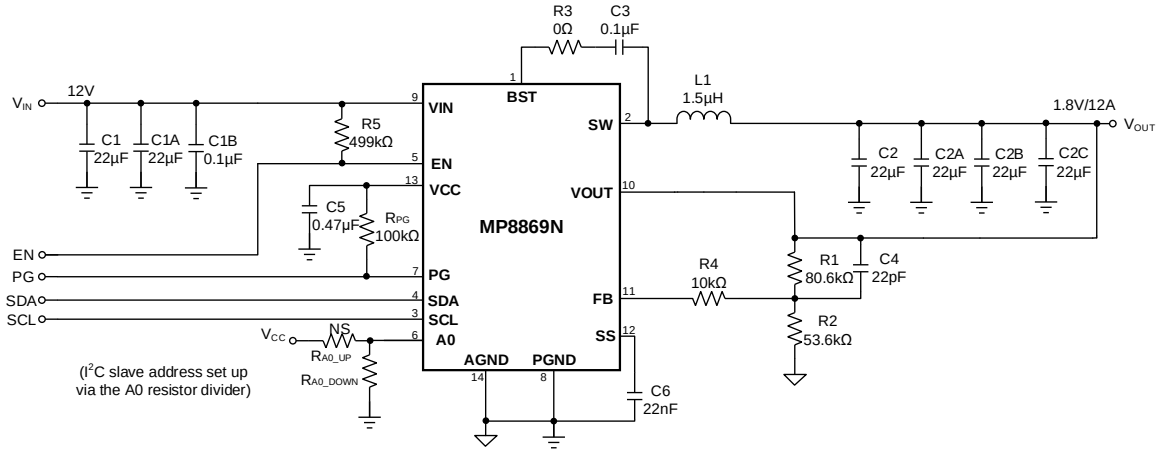

Figure 20: V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 12A

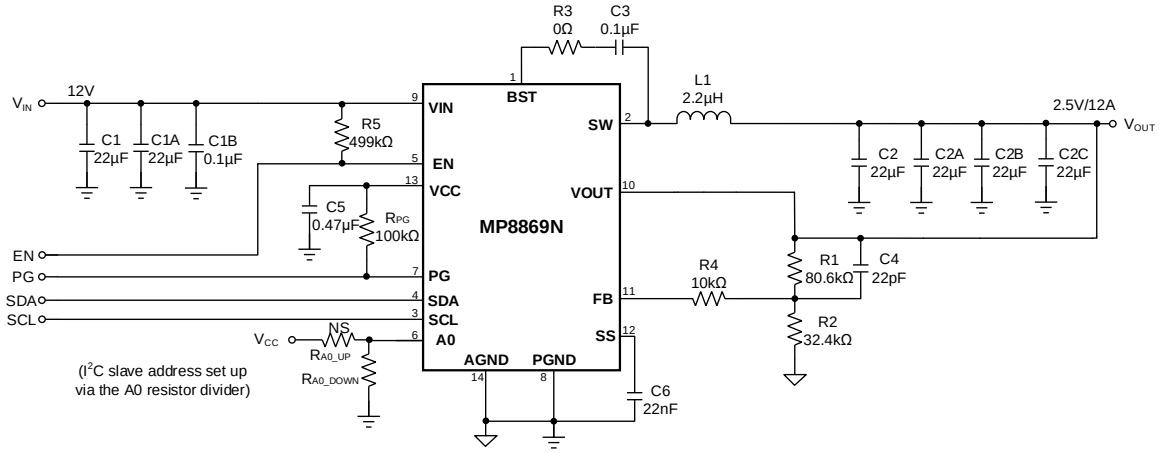

Figure 21: V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 12A

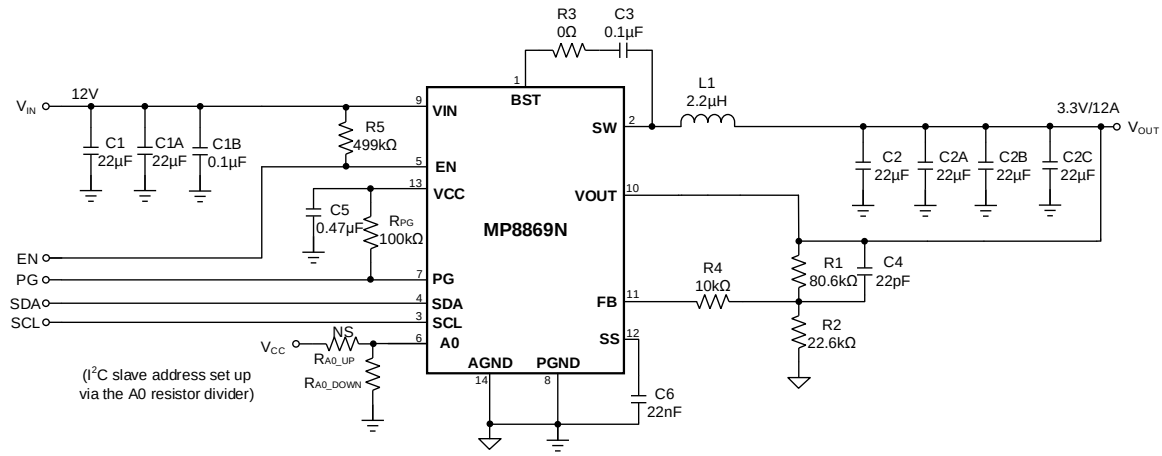

Figure 22: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 12A

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TYPICAL APPLICATION CIRCUITS *(continued)*

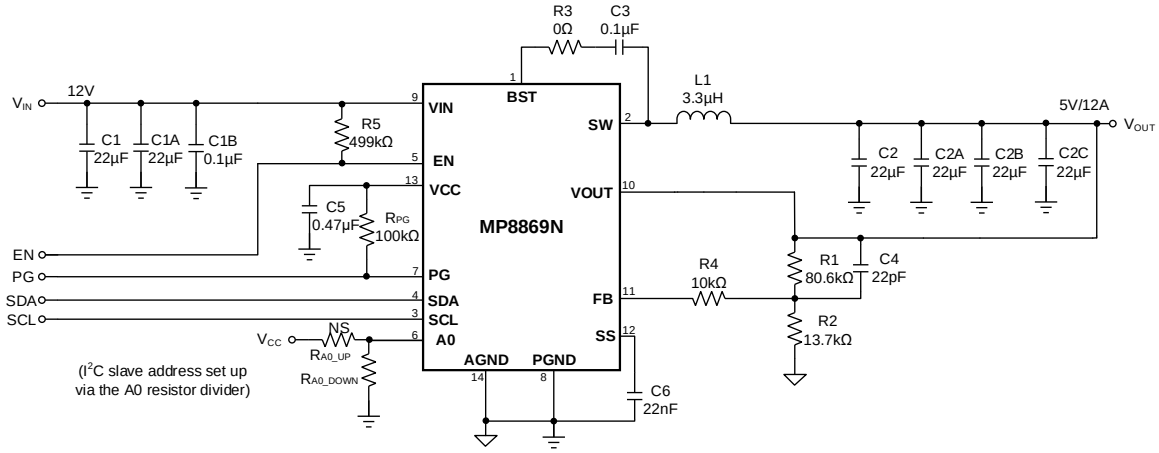

Figure 23: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 12A

Note:

10) All circuits are based on a 0.72V default V_{REF}. The MP8869N's V_{OUT} can be adjusted via V_{REF} and the external resistor dividers. However, V_{OUT} must be set below the absolute OVP threshold (typically 6.5V).

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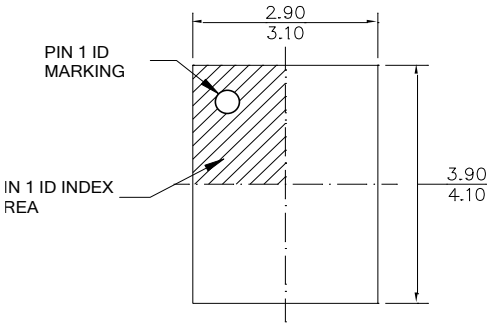
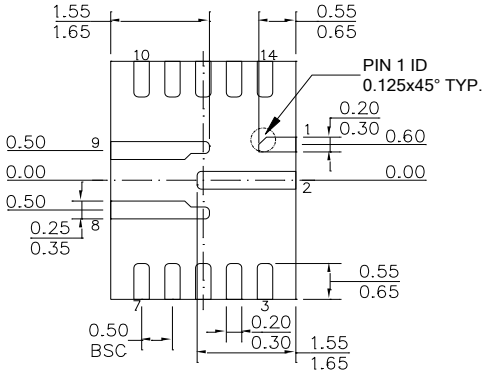
PACKAGE INFORMATION

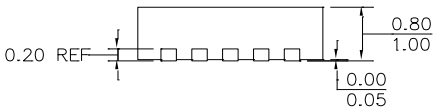
QFN-14 (3mmx4mm)



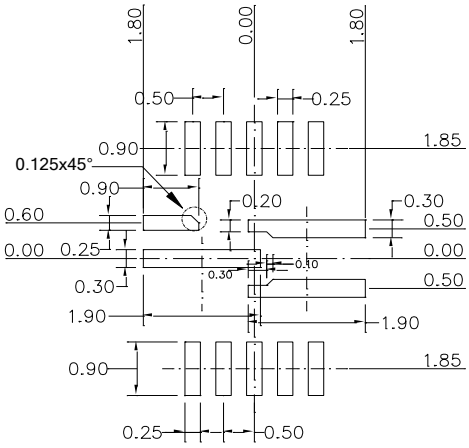
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMET MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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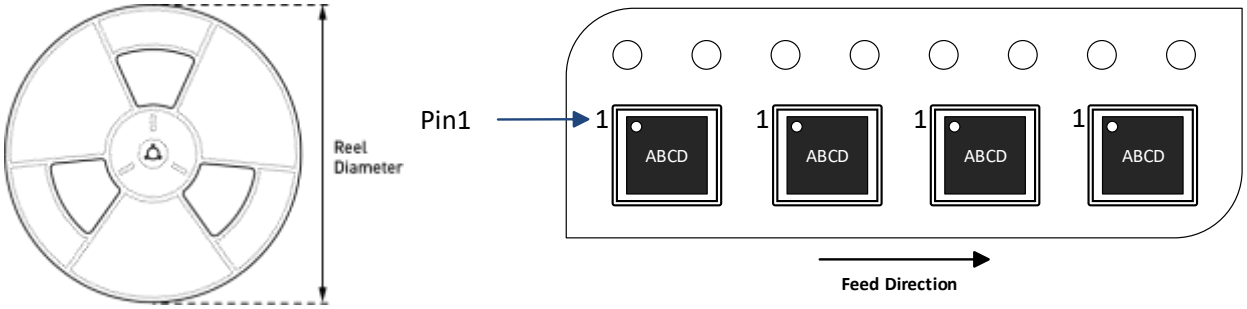
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8869NGL-Z	QFN-14 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2022	Initial Release	-

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