MP8867

High-Efficiency, 8A, 17V, Synchronous Step-Down Converter with I²C Interface

The Future of Analog IC Technology

DESCRIPTION

The MP8867 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. It achieves an 8A output current with excellent load and line regulation over a wide input supply range.

The reference voltage level is controlled by the I²C serial interface with an adjustable reference voltage ranging from 0.6V to 1.87V in 10mV steps. The voltage scaling slew rate, the switching frequency, enable/sync, and power save mode are all selectable through the I_2C interface.

Current-mode operation provides a fast transient response and eases loop stabilization. EN/SYNC supports external clock synchronization, and an open-drain power good indicates when the output voltage is in the nominal range. Full protection features include over-voltage protection (OVP), hiccup over-current protection (OCP), and thermal shutdown.

The MP8867 requires a minimal number of readily available, standard, external components and is available in a QFN-14 (3x4mm) package.

FEATURES

- Wide 4.5V to 17V Operating Input Range
- 1% Internal Reference Accuracy
- I²C Programmable Reference Output Voltage
- Reference Voltage Range from 0.6V to 1.87V in 10mV Steps with Slew Rate Control
- I²C Selectable Switching Frequency
- 200kHz to 2MHz Synchronized External Clock
- OTP and OCP Hiccup Indication via I²C
- Selectable PSM and FS through I²C
- Programmable Soft-Start Time
- Open-Drain Power Good Indicator
- Small 3x4mm QFN-14 Package

APPLICATIONS

- FPGA-Based Systems
- ASIC Supplies
- Distributed Power Systems

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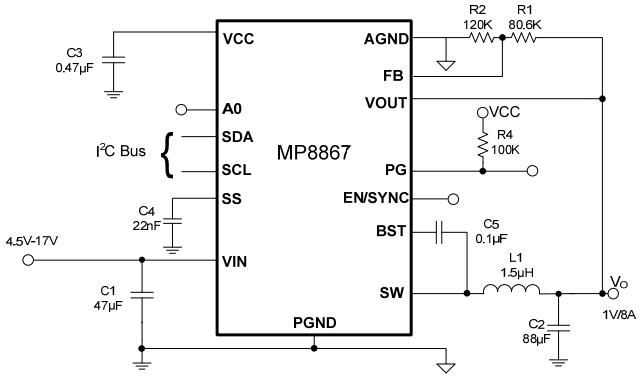
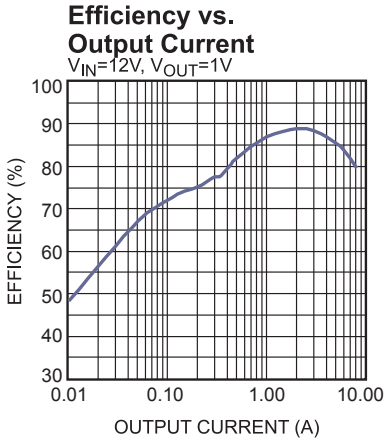
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8867GLE	QFN-14 (3mmx4mm)	*See Below*

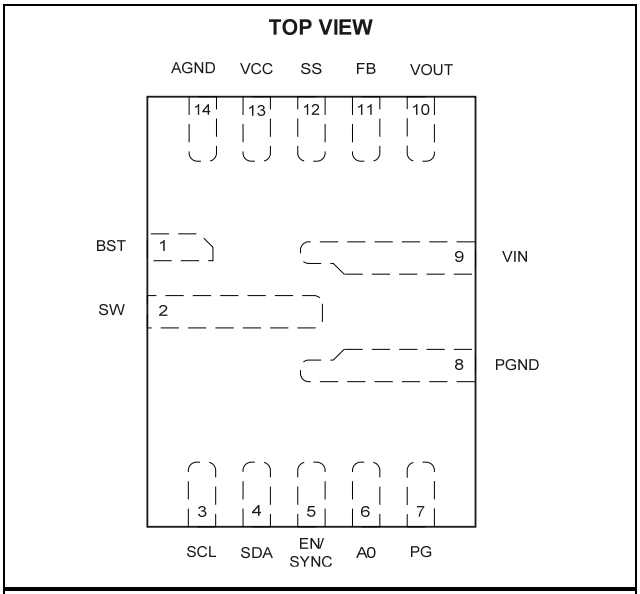
* For Tape & Reel, add suffix –Z (e.g. MP8867GLE–Z)

TOP MARKING

MP YW
8867
LLL

MP: MPS prefix
Y: Year code
W: Week code
8867: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (3mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} …….. .....-0.3V to 19V
V_{SW}.....
-0.3V (-6V for <10ns) to 20V (24V for <10ns)
V_{BST}…… ..... V_{SW}+5.5V
All other pins……..... -0.3V to 5.5V (2)
Continuous power dissipation….(T_A = +25°C) (3)
QFN-14 3x4mm...……..……2.6W
Junction temperature……..….150°C
Lead temperature……..……260°C
Storage temperature……..…-65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN})..……..4.5V to 17V
Output voltage (V_{OUT}) ……0.6V to V_{IN} x D_{MAX} or 5.5V(5)
Operating junction temp. (T_J).. -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-14 (3x4mm) …….. ……..48 ..... 11... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN/SYNC's ABS MAX rating, please refer to the EN/SYNC control section on page 15,.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) The output voltage cannot exceed the 5.5V absolute maximum value at any input condition.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C[7], unless otherwise noted. Typical value is based on the average value when T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		9	13	μA
Supply current (quiescent)	I_q	V_{EN} = 2V, no switching, PFM mode		560	800	μA
HS switch-on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		30		mΩ
LS switch-on resistance	LS_{RDS-ON}	V_{CC} = 5V		15		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V or 0V, T_J = 25°C			1	μA
High-side current limit[8]	I_{LIMIT_H}	Under 40% duty cycle	10			A
Oscillator frequency	f_{SW}	T_J = 25°C	400	500	570	kHz
		T_J = -40°C to 125°C	350		600	
Foldback frequency	f_{VOUT}	V_{FB} = 150mV		0.5		f_{SW}
SYNC frequency range	f_{SYNC}		200		2000	kHz
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV, fs = 500kHz	93	95		%
Minimum on time[8]	t_{ON_MIN}			40		ns
FB voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 85°C [8]	588		612	
V_{OUT}	V_{OUT}=1.2V	T_J = 25°C	1188	1200	1212	mV
	V_{OUT}=1.2V	T_J = -40°C to 85°C [8]	1182		1218	
FB current	I_{FB}	V_{FB} = 620mV		10	50	nA
A0 high level	V_{ADD_H}		2			V
A0 low level	V_{ADD_L}				0.4	V
EN pull-up current	I_{EN_PU}	V_{EN} = 0V, T_J = 25°C	4.3	6.2	7.5	μA
		V_{EN} = 0V, T_J = -40°C to 125°C	3.2		8	
EN rising threshold	V_{EN_Rise}	T_J = 25°C	1.28	1.4	1.5	V
		T_J = -40°C to 125°C	1.26		1.52	
EN hysteresis	V_{EN_HYS}	T_J = 25°C	120	170	220	mV
		T_J = -40°C to 125°C	100		240	
EN turn-off delay	EN_{td-off}			10		μs
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$	T_J = 25°C	4.04	4.2	4.36	V
		T_J = -40°C to 125°C	4.02		4.38	
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$		560	660	740	mV
Power good UV threshold rising	PGVth-Hi	T_J = 25°C	0.85	0.9	0.94	V_{OUT}
		T_J = -40°C to 125°C	0.84		0.95	
Power good UV threshold falling	PGVth-Lo	T_J = 25°C	0.64	0.7	0.73	V_{OUT}
		T_J = -40°C to 125°C	0.63		0.74	

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to 125°C[7], unless otherwise noted. Typical value is based on the average value when T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power good de-glitch time	PGTd			100	160	µs
OVP discharge resistor	R_{OV}	From V_{OUT} to GND		35	70	Ω
OVP rising threshold	V_{EN_Rise}	V_{OUT} and FB, T_J = 25°C	114%	120%	126%	V_{REF}
		V_{OUT} and FB, T_J = -40°C to 125°C	113%		127%	
OVP falling threshold	$V_{EN\ Fall}$	V_{OUT} and FB	101%	105%	108%	V_{REF}
Soft-start current	i_{SS}		7	10	12	µA
VCC voltage	V_{CC}	T_J = -40°C to 125°C	4.75	4.95	5.1	V
VCC load regulation		I_{CC} = 5mA		1	3	%
Thermal shutdown [8]	T_{TSD}			160		°C
Thermal hysteresis [8]	$T_{TSD\ HYS}$			20		°C

NOTES:

7) Not tested in production and guaranteed by over-temperature correlation.

8) Guaranteed by design and characterization test.

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I/O Level Characteristics

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	0.3 V_{Bus}	-0.5	0.3 V_{Bus}	V
High-level input voltage	V_{IH}		0.7 $3V_{Bus}$	V_{Bus}+ 0.5	0.7 V_{Bus}	V_{Bus}+ 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{Bus} > 2V	0.05 V_{Bus}	-	0.05 V_{Bus}	-	V
		V_{Bus} < 2V	0.1 V_{Bus}	-	0.1 V_{Bus}	-	
Low-level output voltage (open-drain) at 3mA sink current	V_{OL}	V_{Bus} > 2V	0	0.4	0	0.4	V
		V_{Bus} < 2V	0	0.2 V_{Bus}	0	0.2 V_{Bus}	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL = 3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at V_{Bus} level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{cs}	SCLH output levels between $0.3V_{Bus}$ and $0.7V_{Bus}$	2	6	2	6	mA
Rise time of the SCLH or SCL signal	t_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	t_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of SDAH signal	t_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Fall time of SDAH signal	t_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O	I_i	Input voltage between $0.1V_{Bus}$ and $0.9V_{Bus}$	-	10	-10	+10	μA
Capacitance for each I/O	C_i		-	10	-	10	pF

NOTE:

V_{Bus} is the I^2C bus voltage, 1.8V to 5.0V range, 3.3V typically.

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I²C Port Signal Characteristics

Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time for a repeated start condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	t_{LOW}		160	-	1300	-	ns
High period of the SCL clock	t_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	t_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated start condition and after an acknowledge bit	t_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	t_{fDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a stop and start condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF
Noise margin at the low level	C_i	For each connected device	-	$0.1V_{Bus}$	$0.1V_{Bus}$	-	V
Noise margin at the high level	V_{nH}	For each connected device	-	$0.2V_{Bus}$	$0.2V_{Bus}$	-	V

NOTE:

V_{Bus} is the I²C bus voltage, 1.8V to 5.0V range, 3.3V typically,

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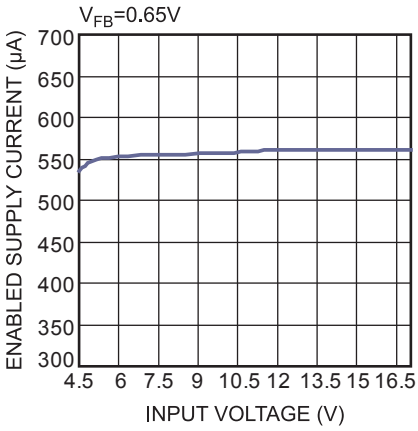
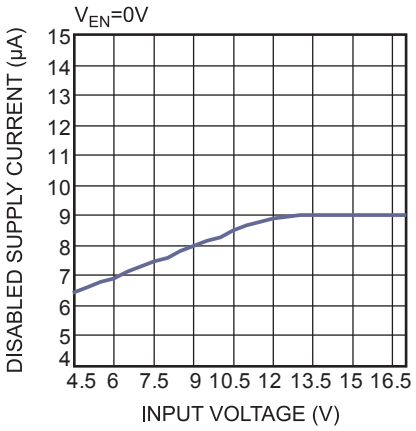
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

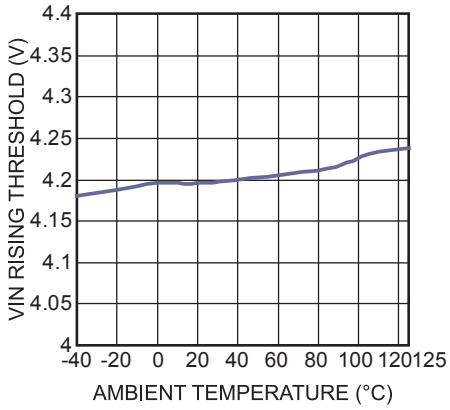
Enabled Supply Current vs. Input Voltage



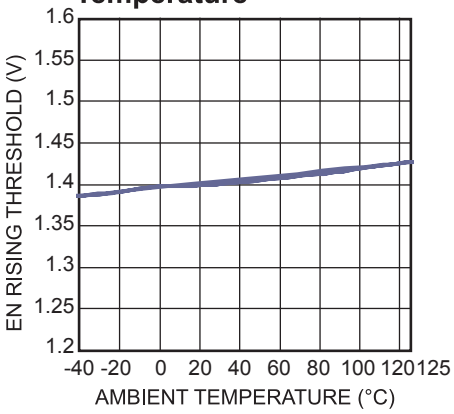
Disabled Supply Current vs. Input Voltage



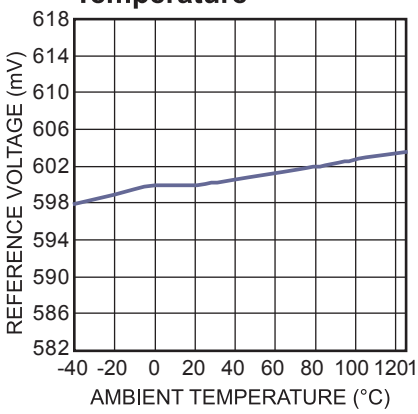
VIN UVLO Rising Threshold vs. Temperature



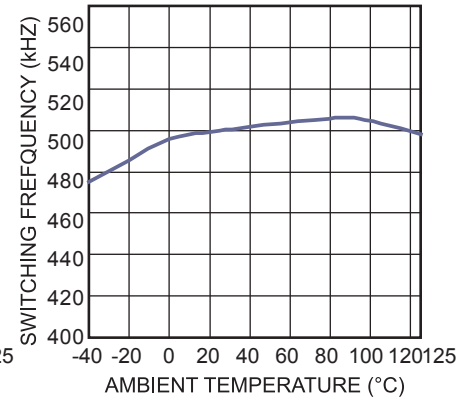
EN Rising Threshold vs. Temperature



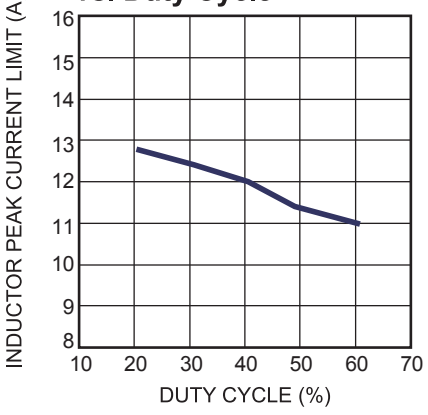
Reference Voltage vs. Temperature



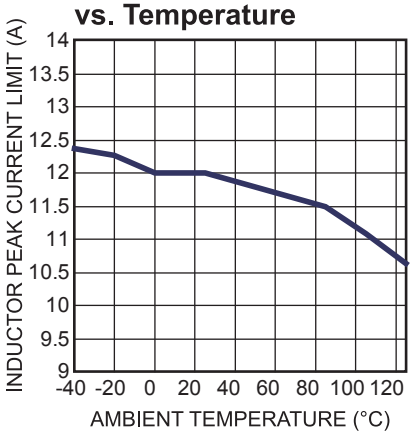
Switching Frequency vs. Ambient Temperature



Inductor Peak Current Limit vs. Duty Cycle



Inductor Peak Current Limit vs. Temperature



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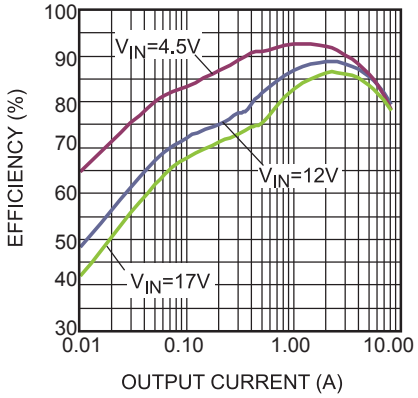
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

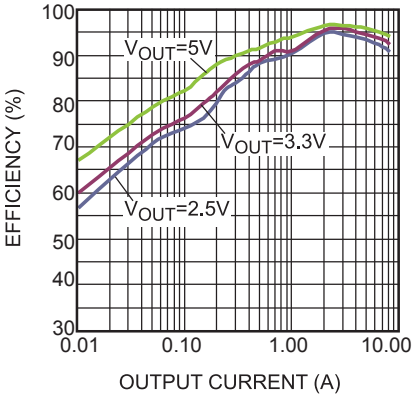
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current

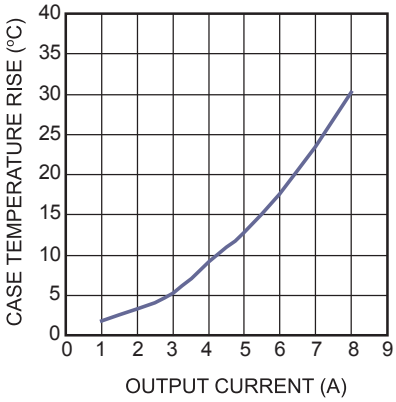


Efficiency vs. Output Current

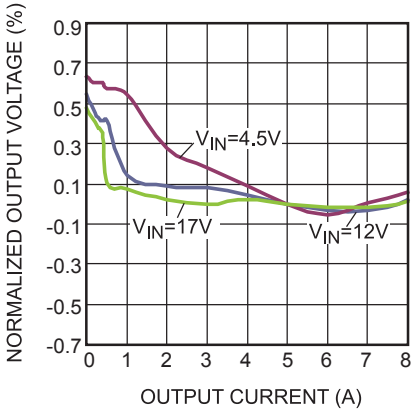
V_{IN}=12V



Case Temperature Rise vs. I_{OUT}

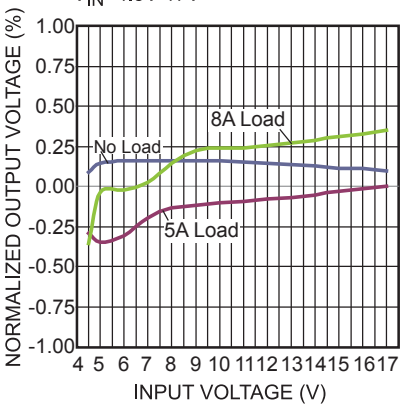


Load Regulation



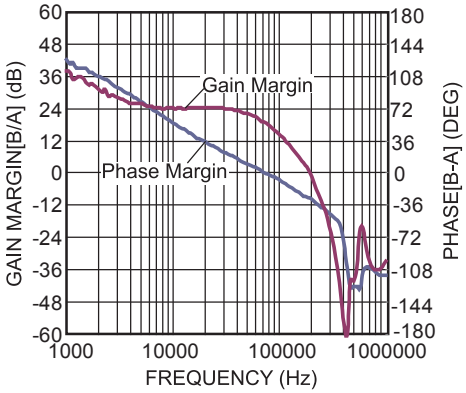
Line Regulation

V_{IN}=4.5V-17V



Bode Plot

I_{OUT}=8A



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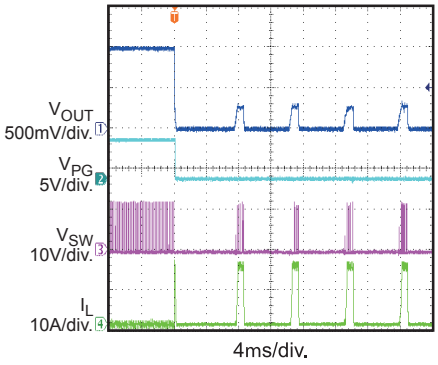
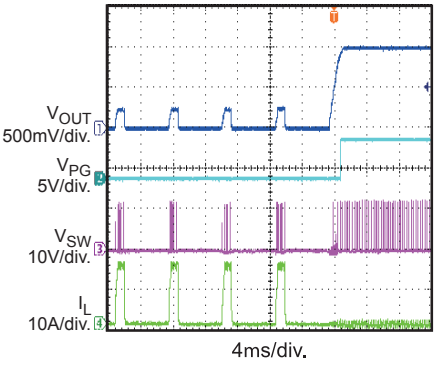
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

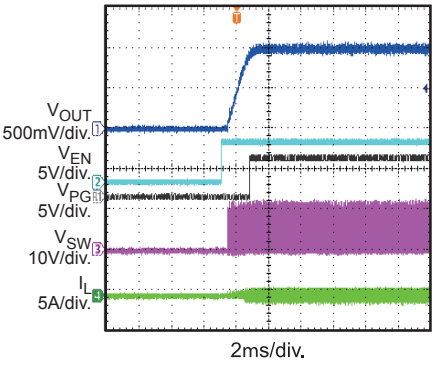
Short Entry
I_{OUT} = 0A



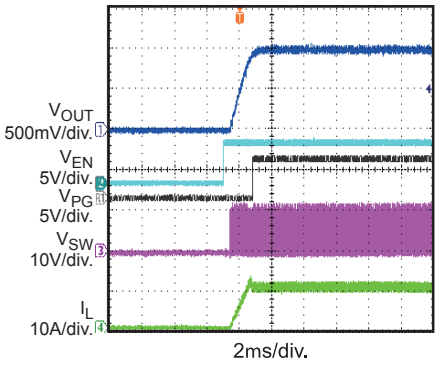
Short Recovery
I_{OUT} = 0A



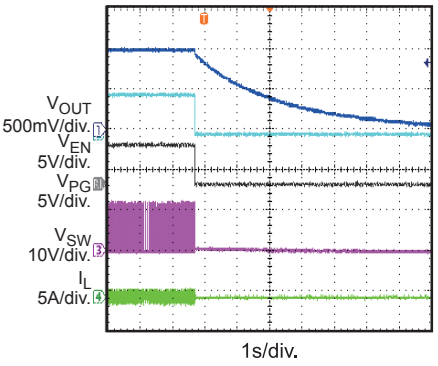
Start-Up through Enable
I_{OUT} = 0A



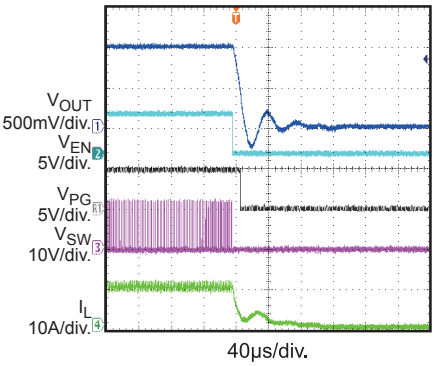
Start-Up through Enable
I_{OUT} = 8A



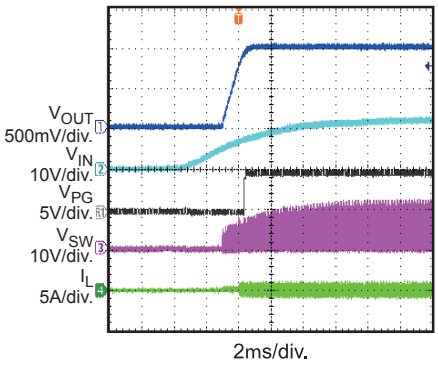
Shutdown through Enable
I_{OUT} = 0A



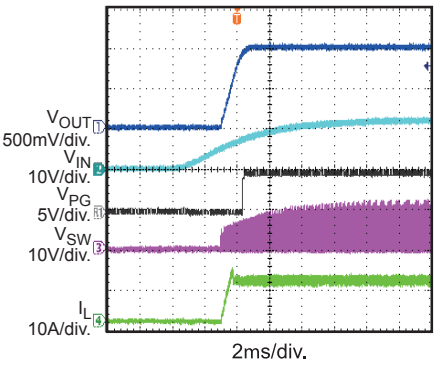
Shutdown through Enable
I_{OUT} = 8A



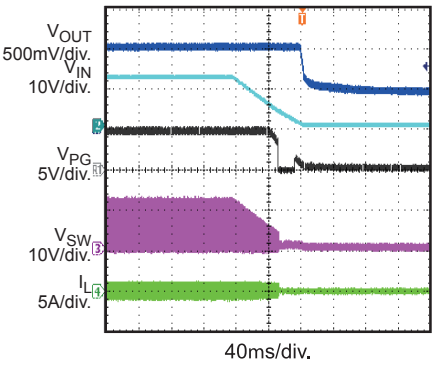
Start-Up through Input Voltage
I_{OUT} = 0A



Start-Up through Input Voltage
I_{OUT} = 8A



Shutdown through Input Voltage
I_{OUT} = 0A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section.

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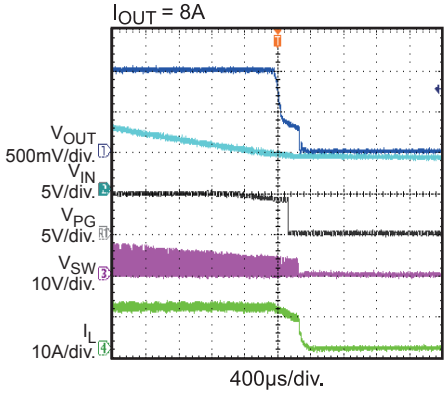
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

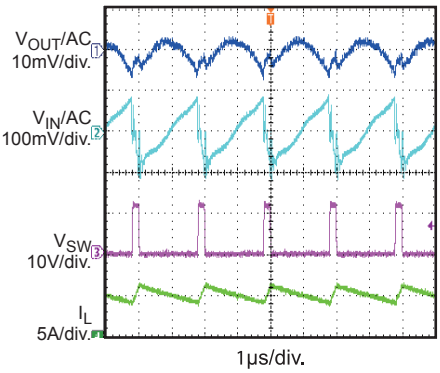
Shutdown through Input Voltage

I_{OUT} = 8A



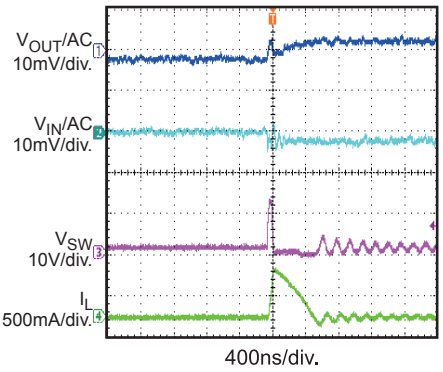
Input/Output Ripple

I_{OUT} = 8A



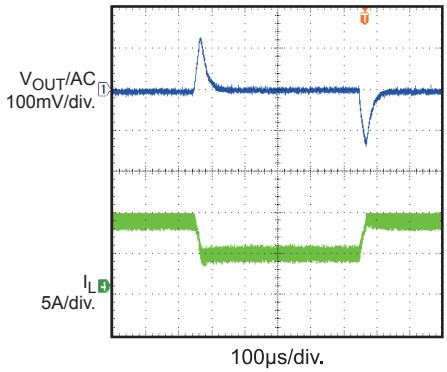
Input/Output Ripple

I_{OUT} = 0A, PFM



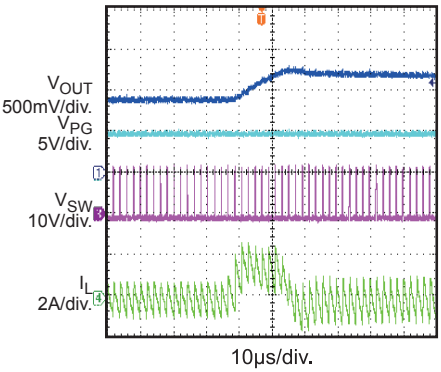
Load Transient Response

I_{OUT} = 4A to 8A



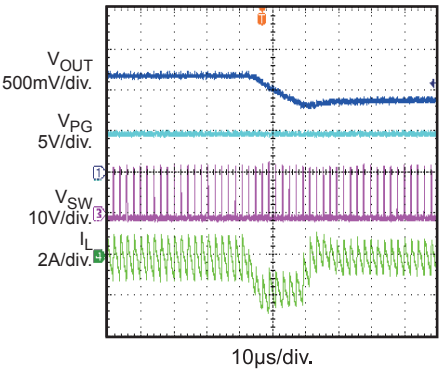
I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 0A, from 0.9V to 1.2V



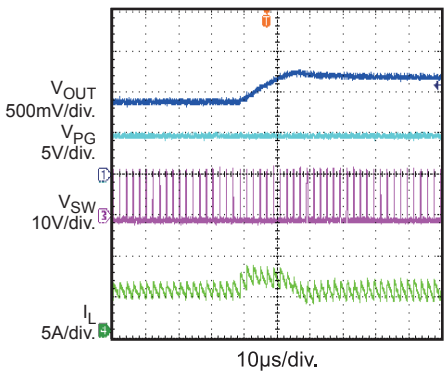
I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 0A, from 1.2V to 0.9V



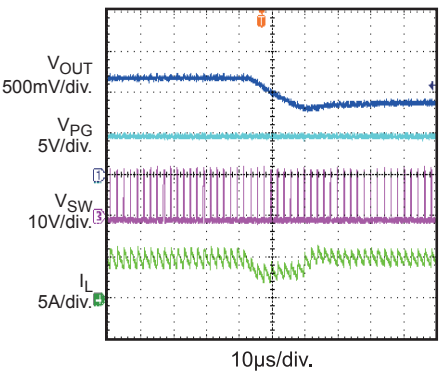
I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 5A, from 0.9V to 1.2V



I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 5A, from 1.2V to 0.9V



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PIN FUNCTIONS

QFN14 PIN#	Name	Description
1	BST	**Bootstrap.** Requires a capacitor between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output.** Connect using a wide PCB trace.
3	SCL	**I^2C serial clock.**
4	SDA	**I^2C serial data.**
5	EN/SYNC	**EN/SYNC high to enable the MP8867.** EN/SYNC has an internal 5.4μA pull-up current of 5V, so the MP8867 can start up automatically when EN/SYNC is floating. Apply an external clock to EN/SYNC to change the switching frequency.
6	A0	**I^2C address set.** Let A0 float or pull it to VCC to set one address. Pull A0 to ground to set a different address.
7	PG	**Power good indication.** PG is an open-drain structure. PG switches low if the output voltage is out of the regulation window. PG indicates UV conditions only.
8	PGND	**System power ground.** PGND is the reference ground of the regulated output voltage. PGND requires special consideration during PCB layout. Connect to ground plane with copper traces and vias.
9	VIN	**Supply voltage.** The MP8867 operates on a 4.5V to 17V input rail. VIN requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
10	VOUT	**Sense input of the output voltage.** Connect VOUT to the positive loading terminal.
11	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage in the FB control loop.
12	SS	**Soft start.** Connect a capacitor from SS to ground to set the soft-start time.
13	VCC	**Internal LDO regulator output.** Decouple with a 0.47μF capacitor.
14	AGND	**Signal ground.** AGND is not connected directly to system ground internally. Make sure AGND connects to system ground in the PCB layout.

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FUNCTIONAL BLOCK DIAGRAM

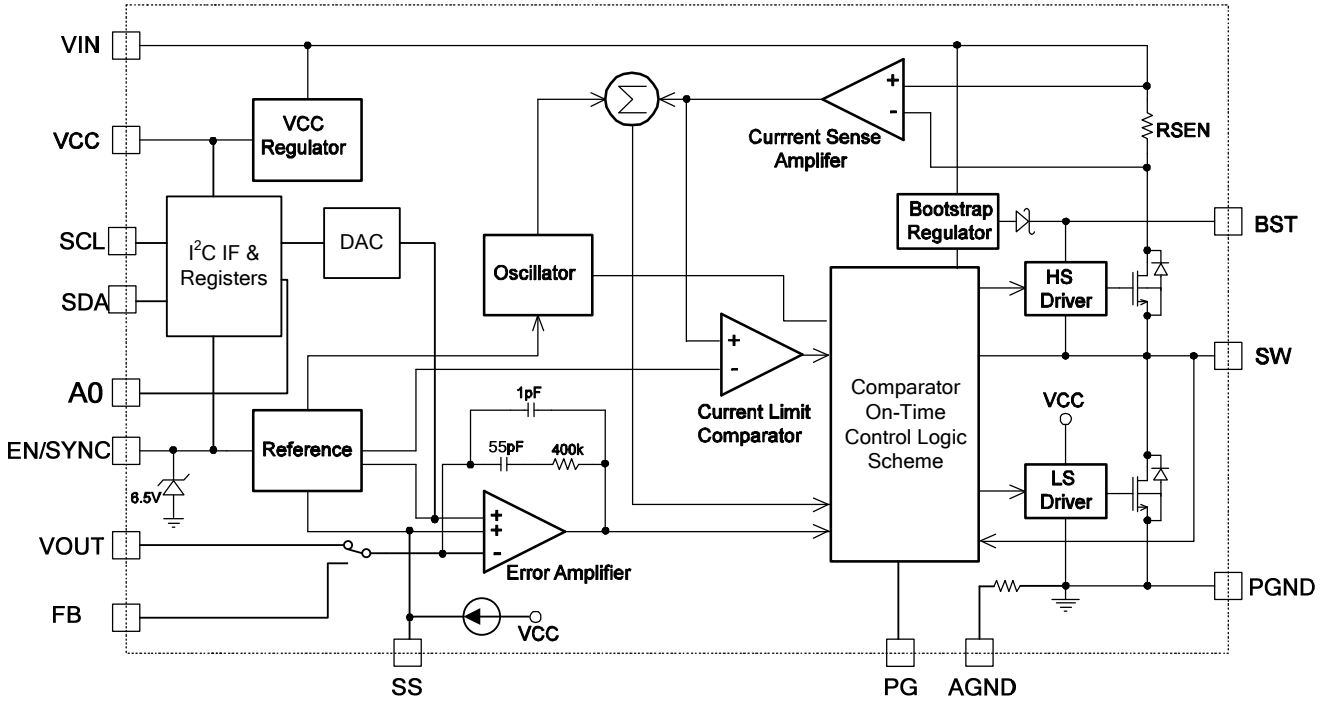

Figure 1: Functional Block Diagram

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OPERATION

The MP8867 is a high-frequency, synchronous rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves an 8A output current with excellent load and line regulation over a wide input supply range.

The MP8867 has three working modes: continuous conduction mode (CCM), advanced asynchronous modulation (AAM) mode, and discontinuous conduction mode (DCM). The MP8867's default operation mode is CCM. The register of the MODE bit (reg01 [0]) in the I^2C can be set to "0."

CCM Control Operation

In CCM, the internal clock initiates the PWM cycle, and the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}. After a period of dead time, the LS-FET turns on and remains on until the next clock cycle begins. The device repeats this operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 95% (500kHz switching frequency) of one PWM period, the HS-FET is forced off.

AAM Control Operation

In a light-load condition, the MP8867 works in AAM mode if the mode bit is set to "0" (see Figure 2). V_{AAM} is fixed internally when the input and output voltages are fixed. V_{COMP} is the error amplifier output, which represents the peak inductor current information. When the V_{COMP} is lower than V_{AAM}, the internal clock is blocked, and the MP8867 skips some pulses, achieving the light-load power save. Refer to AN032 for additional details.

The internal clock resets every time V_{COMP} is higher than V_{AAM}. The HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12V input applications.

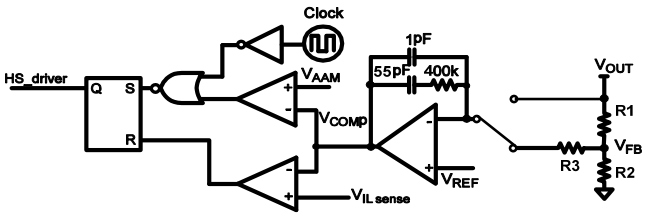

Figure 2: Simplified AAM Control Logic

DCM Control Operation

V_{COMP} ramps up with the increase of the output current. When its minimum value exceeds V_{AAM}, the device enters DCM. In this mode, the internal clock initiates the PWM cycle, and the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (see Figure 3). After a period of dead time, the LS-FET turns on and remains on until the inductor current value decreases to zero. The device will repeat the same operation in every clock cycle to regulate the output voltage.

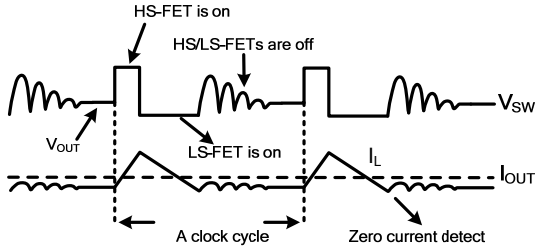

Figure 3: DCM Control Operation

VCC Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. When V_{IN} is lower than 5.0V, the output voltage decreases and follows the input voltage. A 0.47μF ceramic capacitor is required for decoupling purposes.

Error Amplifier (EA)

The error amplifier compares the FB voltage against the internal reference (REF) for the FB control loop and outputs the COMP voltage, which controls the power MOSFET current. In I^2C mode, FB is opened and V_{OUT} is connected to an EA non-inverter input. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

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EN/SYNC Control

EN/SYNC is a digital control pin that turns the regulator block on and off, including I^2C. Drive EN/SYNC high to turn on the regulator; drive EN/SYNC low to turn off the regulator. An internal 5.4μA pull-up current to a 5V power supply allows for automatic start-up when EN/SYNC is floating.

EN/SYNC is clamped internally using a 5.7V series Zener diode (see Figure 4). Connecting the EN/SYNC input through a pull-up resistor to the voltage on V_{IN} limits the EN/SYNC input current to less than 100μA.

For example, with 12V connected to V_{IN}, $R_{PULLUP} \geq (12V - 5.7V) \div 100\mu A = 63k\Omega$.

Connecting EN/SYNC directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to ≤5.5V to prevent damage to the Zener diode.

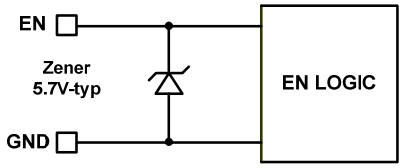

Figure 4: 5.7V Zener Diode Connection

For external clock synchronization, connect a clock with a frequency range between 200kHz and 2MHz to EN/SYNC. The internal clock rising edge will synchronize with the external clock rising edge once the external clock is present. Set the external clock signal with a pulse width of less than 80% of one internal clock cycle time.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8867 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.2V while its falling threshold is 3.54V.

Soft Start (SS)

The MP8867 employs a soft-start (SS) mechanism to ensure a smooth output during power up. When EN/SYNC becomes high, an internal current source (10μA) charges up the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator, and the output voltage ramps up smoothly with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it continues to ramp up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and the MP8867 enters steady-state operation.

The SS capacitor value can be determined with Equation (1):

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

If the output capacitors have large capacitance values, it is not recommended to set a SS time that is too small. Otherwise, the current limit can be hit easily during SS.

Pre-Bias Start-Up

The MP8867 is designed for a monotonic start-up into a pre-biased output voltage. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft-start capacitor is charged. When the soft-start capacitor's voltage exceeds the sensed output voltage at FB[(9)], the part turns on the high-side and low-side power switches sequentially. The output voltage then starts to ramp up with a soft-start slew rate.

NOTE:

9) FB voltage in the FB control loop or V_{OUT} voltage in the I^2C control loop.

Power Good Indicator

The MP8867 uses a power good (PG) output to indicate whether the output voltage of the converter is ready. PG is an open-drain output. Connect PG to VCC or another voltage source through a pull-up resistor (e.g. 100kΩ). When the input voltage is applied, PG is pulled down to GND. When V_{FB}[(9)] is above 90% V_{REF}, PG is pulled high after a 100μs delay. During normal operation, PG is pulled low when V_{FB}[(9)] drops below 70% of the V_{REF} after a 100μs delay.

When UVLO or OTP occurs, PG is pulled low immediately. When OC (over-current) occurs, PG is pulled low when V_{FB}[(9)] drops below 70% of V_{REF} after a 100μs delay.

PG will not respond to an output over-voltage condition.

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The PG bit in the I^2C register has the same indication as the external PG.

Output Over-Voltage Protection (OVP)

The MP8867 monitors both the FB and the V_{OUT} to detect an over-voltage event. When the "V_BOOT" bit = 1, the internal comparator monitors the FB while the "V_BOOT" bit = 0 monitors the V_{OUT}. When the feedback voltage rises above 120% of the internal reference voltage, the controller enters linear discharge mode. During this period, a 35Ω resistor connected between V_{OUT} and ground discharges the output to keep it within the normal range. Once the output voltage drops below 105% of the reference, the controller exits linear discharge mode.

Over-Current Protection and Hiccup Mode

The MP8867 has a cycle-by-cycle, over-current limit. When the inductor current peak value exceeds the set current limit threshold, The HS-FET turns off, and the LS-FET turns on and remains on until the inductor current falls below the internal "valley" current limit threshold. The "valley" current limit circuit is employed to decrease the operation frequency after the "peak" current limit threshold is triggered. Meanwhile, the output voltage drops until V_{FB}(9) is below the under-voltage (UV) threshold, typically 30% below the reference. Once UV is triggered, the MP8867 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. The MP8867 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 160°C, the entire chip shuts down. When the temperature is less than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C5, L1, and C2 (see Figure 5). If V_{IN}-V_{SW} exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C5.

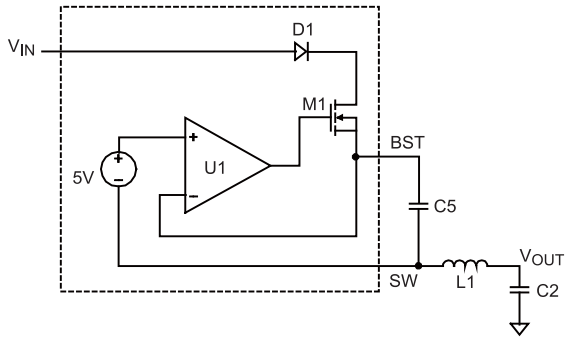

Figure 5: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN/SYNC exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to the shutdown command.

I^2C Control and Default Output Voltage

When the MP8867 is enabled (EN=high and V_{IN}>UVLO), the chip starts up to an output voltage set by the FB resistors with a programmed soft-start time. The I^2C bus can then communicate with the master. If it doesn't receive a constant I^2C communication signal, the chip works through the FB feedback and behaviors similarly to a traditional non-I^2C part.

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Once the I²C receives valid output reference voltage scaling instructions and V_BOOT = "1," the output voltage is determined by the resistor divider R1, R2, and the V_{REF} voltage. The V_{OUT} value is calculated by Equation (2). The V_{REF} default value is 0.6V:

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (2)$$

If V_BOOT = "0", the output voltage is determined by the I²C control, and the FB loop is disabled.

The output reference voltage scaling is realized by adjusting the internal reference voltage (V_REF), which is the non-inverted input of the error amplifier. After the MP8867 receives a valid data byte of the output reference voltage setting, it searches the corresponding reference voltage from the truth table and sends the command to adjust V_{REF} with a controlled slew rate. The slew rate is determined by 3 bits of another register, which can be read and write accordingly.

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I²C INTERFACE

I²C Serial Interface Description

I²C is a 2-wire bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled externally to a bus voltage when they are “idle.” A master device connects to the line, generates the SCL signal and device address, and arranges the communication sequence. The MP8867 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, or other interesting parameters can be controlled instantaneously by the I²C interface. The default I²C address of the MP8867 is “62” (HEX) or “1100010” (BINARY), and “6A” (HEX) or “1101010” (BINARY) if A0 is pulled to ground.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 6).

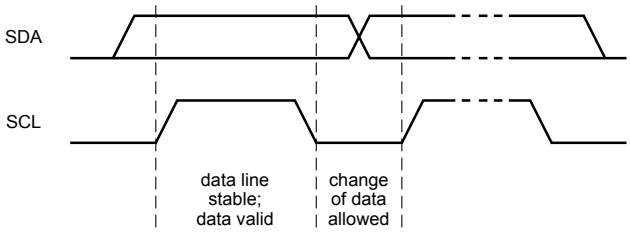

Figure 6: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 7).

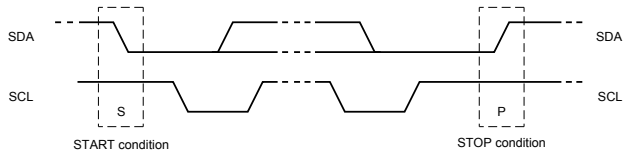

Figure 7: Start and Stop Conditions

Start and stop conditions are always generated by the master. The bus is considered busy after the start condition. The bus is considered free again after a minimum of 4.7μs after the stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains at a stable low during the high period of this clock pulse.

Data transfers follow the format shown in Figure 8. A slave address is sent after the start condition (S). This address is 7 bits long, followed by an eighth bit, which is a data direction bit (R/W). A zero indicates a transmission (write), and a one indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by a master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

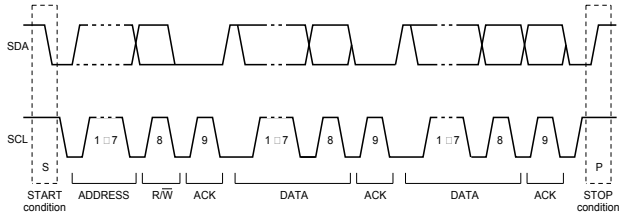

Figure 8: A Complete Data Transfer

The MP8867 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP8867 acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8867, which performs an update on the falling edge of the LSB.

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REGISER DESCRIPTION

Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	V_BOOT	Output Reference						
01	SysCntlreg1	R/W	EN	GO_BIT	Slew Rate			Switching Frequency		Mode
02	ID1	R	Vendor ID				Die ID			
03	Status	R	Reserved			VID_OK	OC	OTEW	OT	PG

Register Description

1. Reg00 VSEL

NAME	BITS	DEFAULT	DESCRIPTION
V_BOOT	D7	1	**FB control loop enable bit.** V_BOOT="1" means the output voltage is determined by the resistor divider connected to FB (FB control loop). V_BOOT="0" means the output voltage is controlled by the I^2C through "V_{OUT}" (I^2C control loop). This bit is helpful for the default output voltage setting before the I^2C signal pulses. If the I^2C is not used, the part works well with FB.
Output Reference	D[6:0]	0000000	**Output setting bit.** Set the output voltage from 0.6V to 1.87V (see Table 1). The default value is 0.6V.

Table 1: Output Voltage Chart

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
000 0000	0.60	010 0000	0.92	100 0000	1.24	110 0000	1.56
000 0001	0.61	010 0001	0.93	100 0001	1.25	110 0001	1.57
000 0010	0.62	010 0010	0.94	100 0010	1.26	110 0010	1.58
000 0011	0.63	010 0011	0.95	100 0011	1.27	110 0011	1.59
000 0100	0.64	010 0100	0.96	100 0100	1.28	110 0100	1.60
000 0101	0.65	010 0101	0.97	100 0101	1.29	110 0101	1.61
000 0110	0.66	010 0110	0.98	100 0110	1.30	110 0110	1.62
000 0111	0.67	010 0111	0.99	100 0111	1.31	110 0111	1.63
000 1000	0.68	010 1000	1.00	100 1000	1.32	110 1000	1.64
000 1001	0.69	010 1001	1.01	100 1001	1.33	110 1001	1.65
000 1010	0.70	010 1010	1.02	100 1010	1.34	110 1010	1.66
000 1011	0.71	010 1011	1.03	100 1011	1.35	110 1011	1.67
000 1100	0.72	010 1100	1.04	100 1100	1.36	110 1100	1.68
000 1101	0.73	010 1101	1.05	100 1101	1.37	110 1101	1.69
000 1110	0.74	010 1110	1.06	100 1110	1.38	110 1110	1.70
000 1111	0.75	010 1111	1.07	100 1111	1.39	110 1111	1.71
001 0000	0.76	011 0000	1.08	101 0000	1.40	111 0000	1.72
001 0001	0.77	011 0001	1.09	101 0001	1.41	111 0001	1.73
001 0010	0.78	011 0010	1.10	101 0010	1.42	111 0010	1.74
001 0011	0.79	011 0011	1.11	101 0011	1.43	111 0011	1.75
001 0100	0.80	011 0100	1.12	101 0100	1.44	111 0100	1.76
001 0101	0.81	011 0101	1.13	101 0101	1.45	111 0101	1.77
001 0110	0.82	011 0110	1.14	101 0110	1.46	111 0110	1.78
001 0111	0.83	011 0111	1.15	101 0111	1.47	111 0111	1.79
001 1000	0.84	011 1000	1.16	101 1000	1.48	111 1000	1.80
001 1001	0.85	011 1001	1.17	101 1001	1.49	111 1001	1.81
001 1010	0.86	011 1010	1.18	101 1010	1.50	111 1010	1.82
001 1011	0.87	011 1011	1.19	101 1011	1.51	111 1011	1.83
001 1100	0.88	011 1100	1.20	101 1100	1.52	111 1100	1.84
001 1101	0.89	011 1101	1.21	101 1101	1.53	111 1101	1.85
001 1110	0.90	011 1110	1.22	101 1110	1.54	111 1110	1.86
001 1111	0.91	011 1111	1.23	101 1111	1.55	111 1111	1.87

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2. Reg01 SysCntlreg1

NAME	BITS	DEFAULT	DESCRIPTION
EN	D[7]	1	**I²C controlled turn on or turn off of the part.** When the external EN is low, the converter is off, and I²C shuts down. When EN is high, the EN bit will take over. The default EN bit is "1."
GO_BIT	D[6]	0	**Switch bit of the I²C writing authority output reference command only.** Set GO_BIT="1" to enable the I²C authority writing output reference. When the command is finished, GO_BIT will auto reset to "0" to prevent false operation of the V_{OUT} scaling. If the reference adjustment is within 50mV, GO_BIT will not reset to "0" automatically. In this case, manually set GO_BIT to "0." It is recommended to write GO_BIT="1" first before writing the output reference voltage.
Slew Rate	D[5:3]	100	D[5:3] Slew Rate D[5:3] Slew Rate 000 64 mV/μs 100 4 mV/μs 001 32 mV/μs 101 2 mV/μs 010 16 mV/μs 110 1 mV/μs 011 8 mV/μs 111 0.5 mV/μs
Switching Frequency	D[2:1]	00	D[2:1] Fs 00 500kHz 01 750KHz 10 1MHz 11 1.5MHz
Mode	D0	1	**PFM enable/disable bit.** A "0" enables PFM mode, and a high disables PFM mode. The default is forced CCM.

3. Reg02 ID1

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000
IC Revision ID	D[3:0]	IC revision

4. Reg03 Status

NAME	BITS	DESCRIPTION
Reserved	D[7:5]	**Reserved for future use.** Always set to 0.
VID_OK	D[4]	**I²C controlled voltage adjustment is done.** The internal circuit compares the DAC output with V_{OUT}. If V_{OUT} is in the 90%-110% range of the DAC output, the VID_OK bit is high, which means the voltage scaling is finished. Otherwise, VID_OK= "0." VID_OK compares DAC with V_{OUT}/FB. UV is 90%+-3%, OV is 110%+-3%.
OC	D[3]	**Output over-current indication.** When the bit is high, the IC is in hiccup mode.
OTEW	D[2]	**Die temperature early warning bit.** When the bit is high, the die temperature is higher than 120˚C.
OT	D[1]	**Over-temperature indication**. When the bit is high, the IC is in thermal shutdown.
PG	D[0]	**Output power good indication.** When the bit is high, V_{OUT} power is good. This means that V_{OUT} is higher than 90% of the designed regulation voltage. See additional details in the Power Good Indicator section.

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APPLICATION INFORMATION

Setting the Output Voltage in a FB Control Loop

The reference voltage and external resistor dividers set the output voltage through FB. The feedback resistors R1 and R3 also set the feedback loop bandwidth with the internal compensation capacitor. Choose the R1 value first and calculate R2 with Equation (3)[10]:

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{REF}} - 1} \quad (3)$$

NOTE:

10) VREF is 0.6V when the power is up or EN is on. After the MP8867 is enabled, V_{REF} can be programmed through the I^2C. Set V_BOOT=1 to enable the FB control loop.

The T-type network (see Figure 9) is highly recommended.

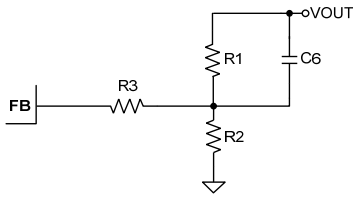

Figure 9: T-Type Network

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages with Default 0.6V V_{REF}[11]

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C6 (pF)	L (μH)
0.9	80.6 (1%)	162 (1%)	51 (1%)	22	1.5
1.0	80.6 (1%)	120 (1%)	51 (1%)	22	1.5
1.2	80.6 (1%)	80.6 (1%)	40.2 (1%)	22	1.5
2.5	60.4 (1%)	19.1 (1%)	30 (1%)	22	2.2
3.3	60.4 (1%)	13.3 (1%)	20 (1%)	33	3.3
5	60.4 (1%)	8.25 (1%)	20 (1%)	33	3.3

NOTE:

11) The recommended parameters are based on a 12V input voltage and a 22μFx4 output capacitor. Different input voltages and output capacitor values may affect the selection of R1, R2, R3, and C6. For additional component parameters, please refer to the Typical Application Circuits section on page 26.

Setting the Output Voltage in an I^2C Control Loop

In addition to setting the output voltage through the FB loop, the I^2C loop also sets the output voltage through V_{OUT} by setting V_BOOT=0. In this case, the output voltage is the set reference voltage. Refer to Table 1 for additional details about the output voltage settings.

Output Voltage Dynamic Scale

To set the output voltage to dynamic scaling during normal operation, refer to Figure 10 and follow the steps below:

1. Write the GO_bit (reg01[6]) to "1."
2. Write reg00 to select the feedback loop by setting V_BOOT (reg00[7]) and set the reference voltage output reference (reg00[0:6]) simultaneously. If the reference adjustment is within 50mV, GO_BIT will not reset to "0" automatically. If this is the case, set GO_BIT to "0" manually.

Repeat these steps if dynamic scaling is needed for other voltages.

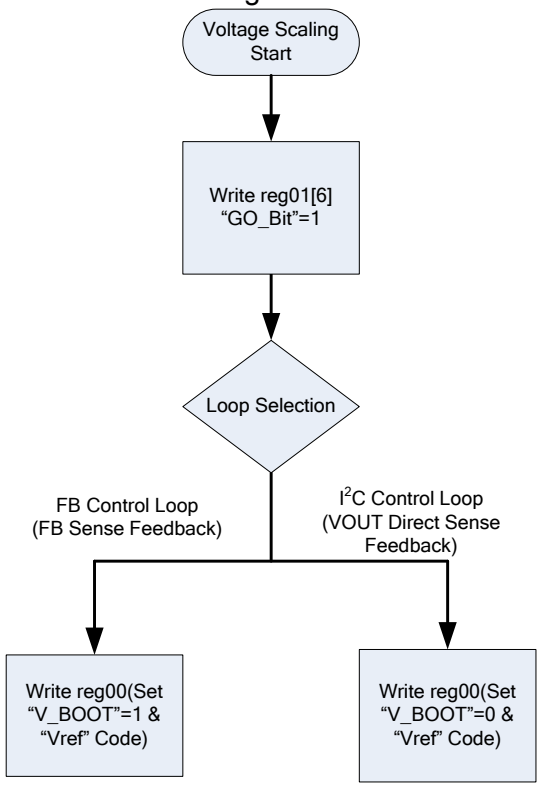

Figure 10: Output Voltage Dynamic Scale Flow Chart

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Selecting the Inductor

Use a 0.47μH to 10μH inductor with a DC current rating at least 25% higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance of less than 15mΩ. For most designs, the inductance value is derived from Equation (4):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (4)$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is calculated with Equation (5):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (5)$$

Use a larger inductor for improved efficiency under light-load conditions below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. For best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, use two-piece 22μF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worse-case condition occurs at $V_{IN}=2V_{OUT}$, shown in Equation (7):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small high-quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

For tantalum or electrolytic capacitors, ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor affect the stability of the regulation system. The MP8867 can be optimized for a wide range of capacitance and ESR values.

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PCB Layout Guidelines [12]

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 11 and follow the guidelines below.

1. Place the high-current paths (PGND, V_{IN}, and SW) as close as possible to the device with short, direct, and wide traces.
2. Keep the IN and GND pads connected with large copper traces and use at least two layers for the IN and GND traces to achieve better thermal performance. To help with thermal dissipation, add several vias close to the IN and GND pads.
3. Place the input capacitors as close to VIN and GND as possible.
4. Place the decoupling capacitor as close to VCC and GND as possible.
5. Place the external feedback resistors next to FB, ensuring that there is no via on the FB trace.
6. Keep the switching node SW short and away from the feedback network.
7. Keep the BST voltage path (BST, C5, and SW) as short as possible. A four-layer layout is strongly recommended to achieve better thermal performance.

NOTE:

12) The recommended layout is based on Figure 13.

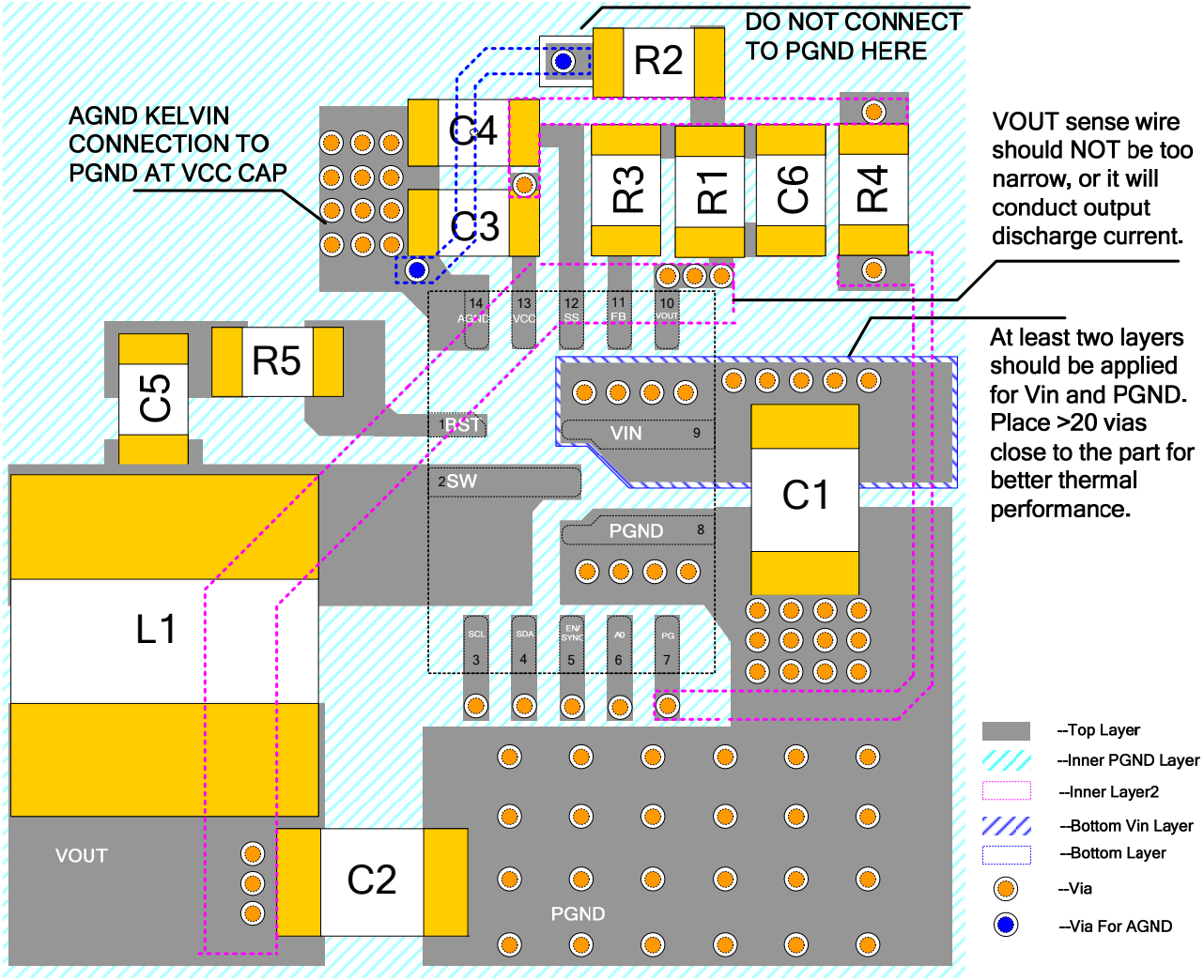

Figure 11: Recommended Layout

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Design Example

Table 2 is a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	1V
I_O	8A

The detailed application schematics are shown in Figure 13. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS (13)

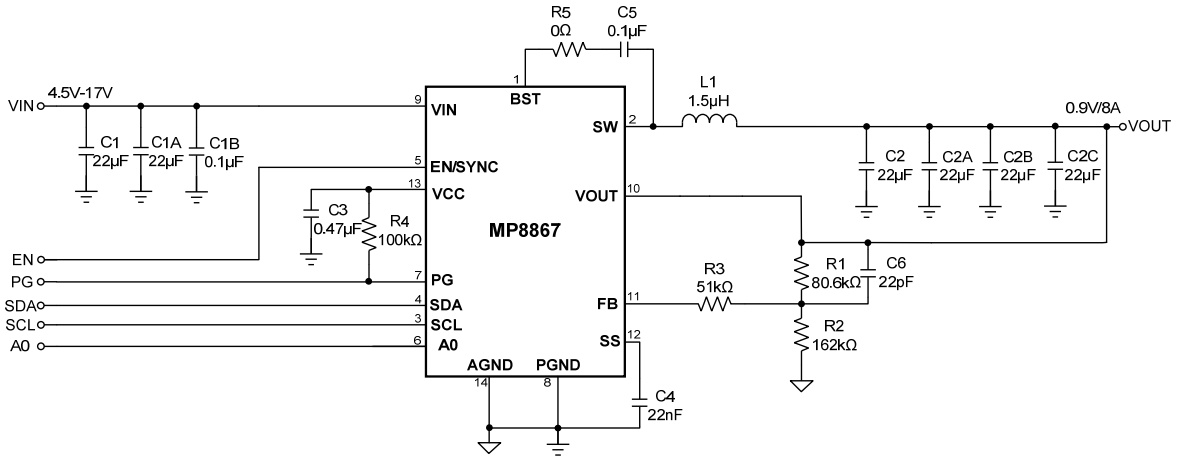

Figure 12: V_{IN} = 4.5-17V, V_{OUT} = 0.9V, I_{OUT} = 8A

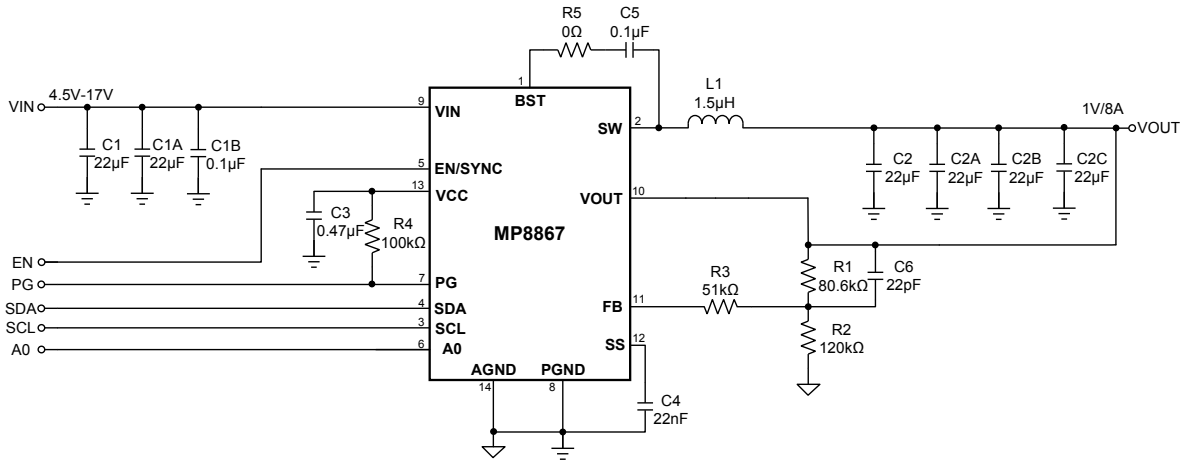

Figure 13: V_{IN} = 4.5-17V, V_{OUT} = 1V, I_{OUT} = 8A

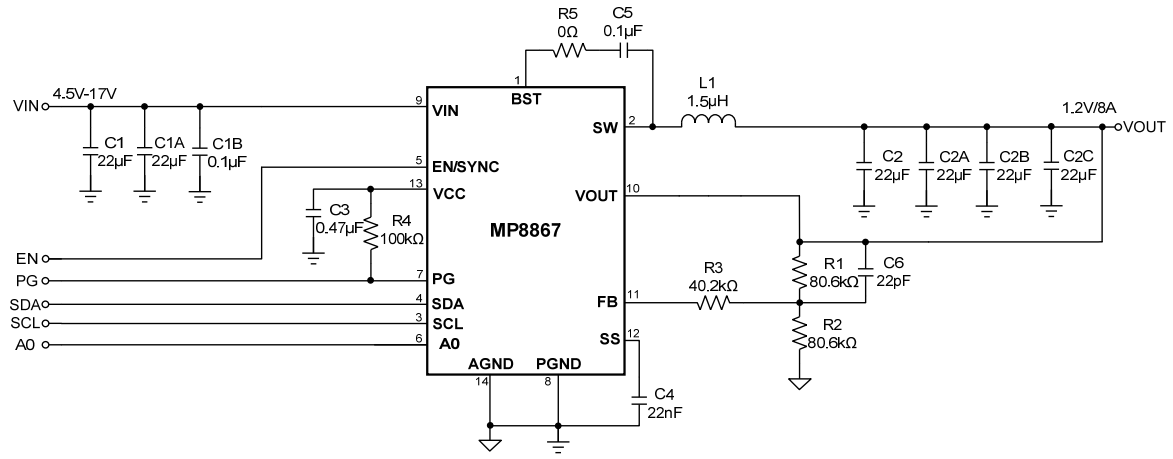

Figure 14: V_{IN} = 4.5-17V, V_{OUT} = 1.2V, I_{OUT} = 8A

NOTE:

13) All circuits are based on a 0.6V default reference voltage.

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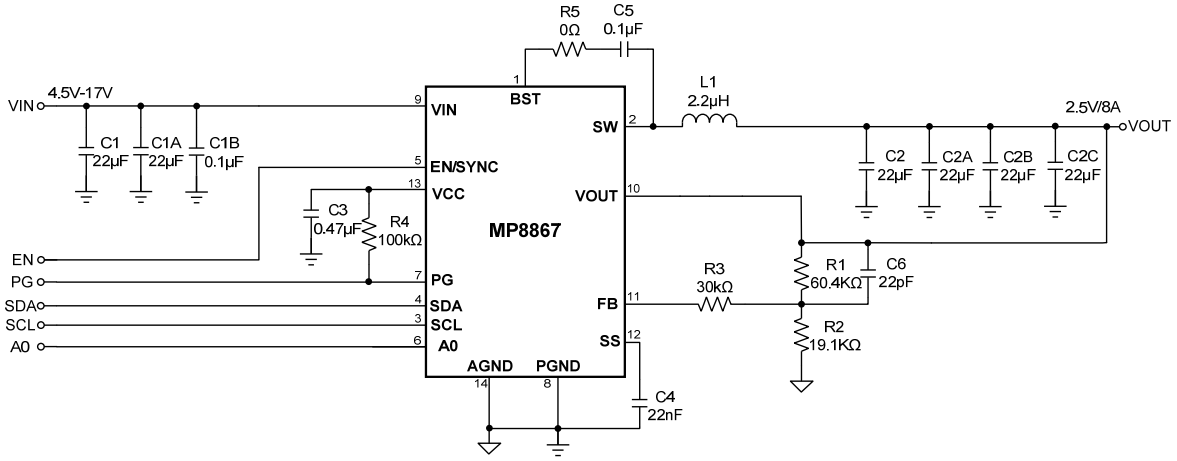

Figure 15: V_{IN} = 4.5-17V, V_{OUT} = 2.5V, I_{OUT} = 8A

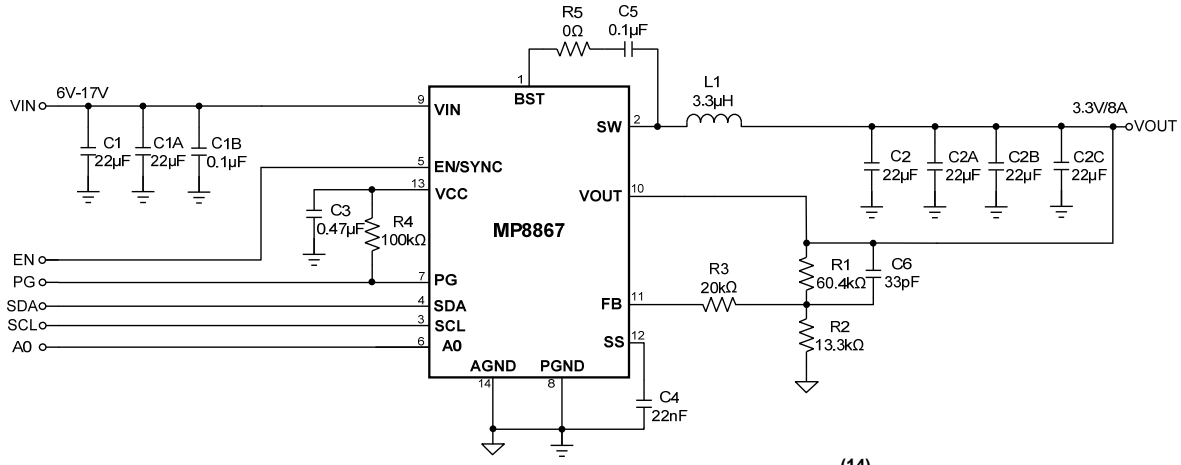

Figure 16: V_{IN} = 6-17V, V_{OUT} = 3.3V, I_{OUT} = 8A(14)

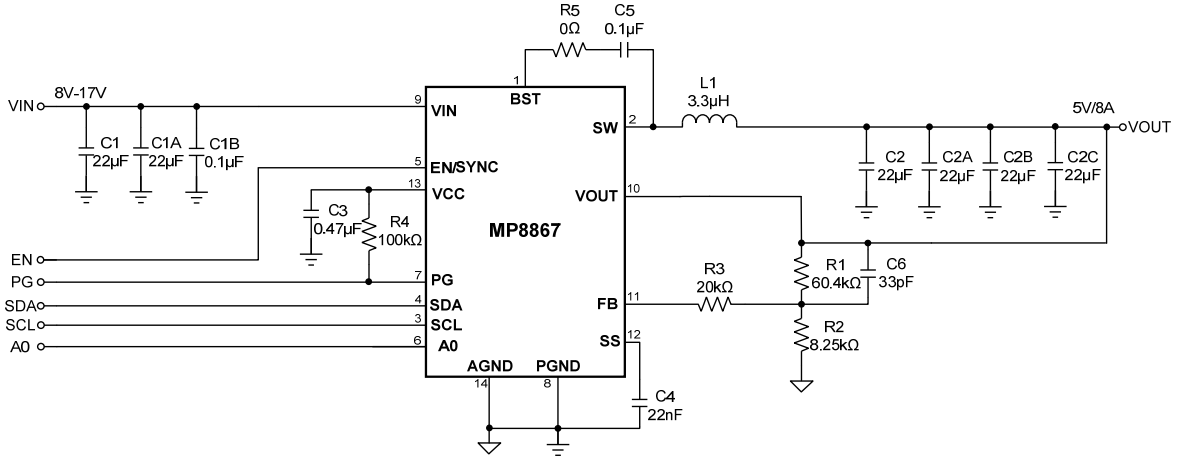

Figure 17: V_{IN} = 8-17V, V_{OUT} = 5V, I_{OUT} = 8A(14)

NOTE:

14) Based on Evaluation Board test results at 25°C ambient temperature. Lower input voltage will trigger over-temperature protection with full load.

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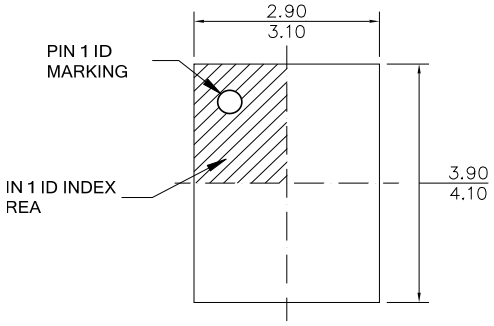
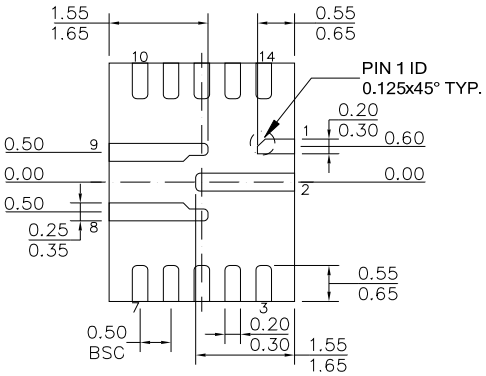
PACKAGE INFORMATION

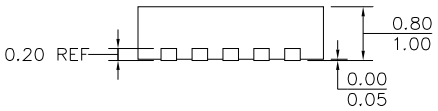
QFN-14 (3x4mm)



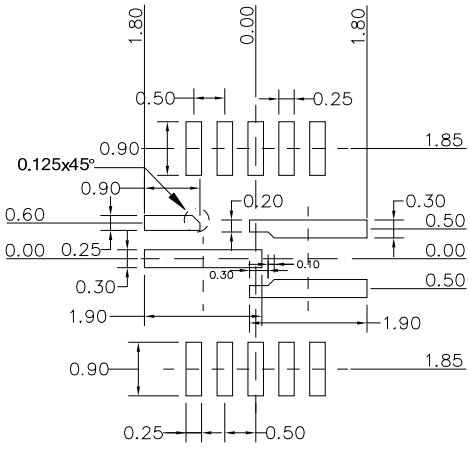
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMET MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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