



The Future of Analog IC Technology®

# MP8847

6A, 2.7V-6V, High-Efficiency, Synchronous, Step-Down Switcher with I<sup>2</sup>C Interface In 2x3mm QFN

## DESCRIPTION

The MP8847 is a highly integrated, high-frequency, synchronous, step-down switcher with an I<sup>2</sup>C control interface. The MP8847 can support up to 6A of load current over an input supply range from 2.7V to 6V with excellent load and line regulation.

Constant-frequency hysteretic mode provides an extremely fast transient response without loop compensation to achieve high efficiency easily under light-load condition.

The output voltage level can be controlled on-the-fly through a 3.4Mbps I<sup>2</sup>C serial interface. The voltage range can be adjusted from 0.6V to 1.235V in 5mV steps. The voltage slew rate, switching frequency, and power-saving mode are also selectable through the I<sup>2</sup>C interface.

Full protection features include internal soft start, over-current protection (OCP), and over-temperature protection (OTP).

The MP8847 requires a minimal number of readily available, standard, external components and is available in a compact QFN-14(2mmx3mm) package.

## FEATURES

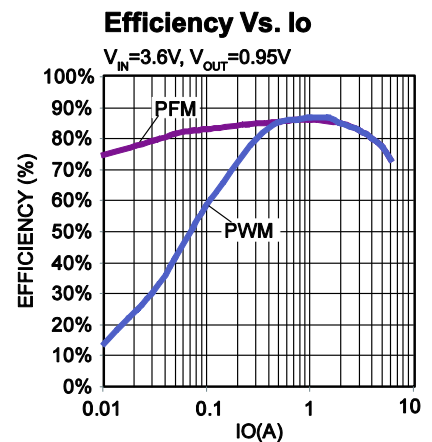
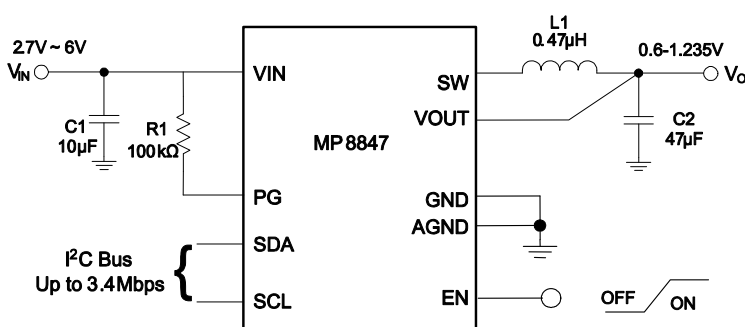
- I<sup>2</sup>C-Programmable Output Range from 0.6V to 1.235V in 5mV Steps
- 2.7V to 6V Input Voltage Range
- Up to 6A Load Current
- Internal 35mΩ High-Side and 15mΩ Low-Side Power MOSFETs
- I<sup>2</sup>C-Compatible Interface up to 3.4Mbps
- Factory Adjustable Switching Frequency from 0.85MHz to 2.2MHz
- Power-Saving Mode Selectable via I<sup>2</sup>C
- Internal 1ms Soft Start
- Power Good Indicator
- Current Overload and Thermal Shutdown Protection
- Available in 2mmx3mm QFN-14 Package

## APPLICATIONS

- Processor Core Supplies
- Micro Converters

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## TYPICAL APPLICATION



### ORDERING INFORMATION

| Part Number | Package             | Top Marking |
|-------------|---------------------|-------------|
| MP8847GD*   | QFN-14 (2mmx3mm)    | See Below   |
| EVKT-8847   | 8847 Evaluation Kit |             |

\* For Tape & Reel, add suffix -Z (e.g. MP8847GD-Z)

### TOP MARKING


  
**AVEY**  
**LLL**

AVE: product code of MP8847GD

Y: year code

LLL: Lot number

### EVALUATION KIT EVKT-8847

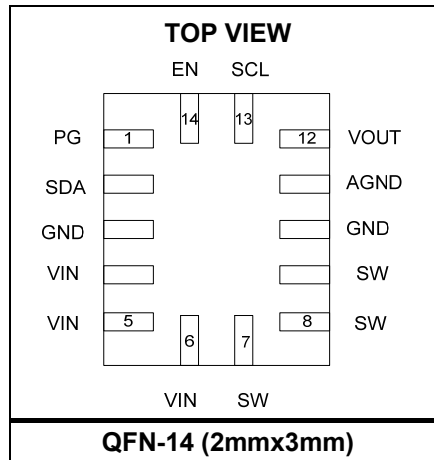
EVKT-8847 Kit contents: (Items below can be ordered separately).

| # | Part Number   | Item   | Quantity |
|---|---------------|--|----------|
| 1 | EV8847-D-00A  | MP8847GD Evaluation Board  | 1        |
| 2 | EVKT-USB2C-02 | Includes one USB to I2C Dongle, one USB Cable, and one Ribbon Cable              | 1        |
| 3 | Tdrive-8847   | USB Flash drive that stores the GUI installation file and supplemental documents | 1        |

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**Figure 1. EVKT-8847 Evaluation Kit Setup**

### PACKAGE REFERENCE



#### **ABSOLUTE MAXIMUM RATINGS (1)**

|  |  |
|--|--|
| Supply voltage (VIN).....  | -0.3V to 7V  |
| V <sub>SW</sub> .....  | -0.3V (-5V for <10ns) to<br>6.5V(8V for <10ns or 10V for <3ns) |
| All other pins .....   | -0.3V to 6.5V  |
| Junction temperature .....   | 150°C  |
| Lead temperature.....  | 260°C  |
| Continuous power dissipation(T <sub>A</sub> = +25°C) (2)(4)<br>QFN ..... | 3.5W   |
| Storage temperature .....  | -65°C to 150°C   |

#### **Recommended Operating Conditions (3)**

|   |                 |
|---|-----------------|
| Supply voltage (VIN).....                     | 2.7V to 6V      |
| Output voltage (VOUT) .....                   | 0.6V to 1.235V  |
| Operating junction Temp (T <sub>J</sub> ) ... | -40°C to +125°C |

#### **Thermal Resistance(4)**

|                       | $\theta_{JA}$ | $\theta_{JC}$ |
|-----------------------|---------------|---------------|
| QFN 2mmx3mm           |               |               |
| EV8847-D-00A(4) ..... | 35            | 8             |
| JESD51-7(5) .....     | 70            | 15            |

#### **NOTES:**

- 1) Exceeding these ratings may damage the device.
  - 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX)-T<sub>A</sub>)/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
  - 3) The device is not guaranteed to function outside of its operating conditions.
  - 4) Measured on EV8847-D-00A, 4-layer PCB, 63mm x 63mm.
  - 5) Measured on JESD51-7, 4-layer PCB.
- note 5) The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values are calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 5V, T<sub>J</sub> = -40°C to +125°C<sup>(6)</sup>, typical value is tested at T<sub>J</sub> = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

| Parameter                       | Symbol              | Condition   | Min   | Typ   | Max   | Units               |
|---------------------------------|---------------------|---|-------|-------|-------|---------------------|
| Input voltage range             | V <sub>IN</sub>     |   | 2.7   |       | 6     | V                   |
| Quiescent current               | I <sub>Q</sub>      | EN=1.8V, no switching,<br>PFM mode  |       | 300   |       | μA                  |
| Shutdown current                | I <sub>S</sub>      | EN=GND, T <sub>J</sub> =25°C  |       |       | 1     | μA                  |
| Internal reference voltage      | V <sub>REF</sub>    | T <sub>J</sub> =25°C  | 0.591 | 0.600 | 0.609 | V                   |
|                                 |                     | -40°C<T <sub>J</sub> <125°C   | 0.585 | 0.600 | 0.615 | V                   |
| Lowest output voltage           | V <sub>LOW</sub>    | Register = 00h, T <sub>J</sub> =25°C  | 0.591 | 0.600 | 0.609 | V                   |
|                                 |                     | -40°C<T <sub>J</sub> <125°C   | 0.585 | 0.600 | 0.615 | V                   |
| Highest output voltage          | V <sub>HIGH</sub>   | Register = 7Fh, T <sub>J</sub> =25°C  | 1.216 | 1.235 | 1.254 | V                   |
|                                 |                     | -40°C<T <sub>J</sub> <125°C   | 1.204 | 1.235 | 1.266 | V                   |
| Output voltage step             | V <sub>STEP</sub>   |   |       | 5     |       | mV                  |
| High-side switch on resistance  | R <sub>HSON</sub>   |   |       | 35    |       | mΩ                  |
| Low-side switch on resistance   | R <sub>LSON</sub>   |   |       | 15    |       | mΩ                  |
| UVLO rising threshold           | V <sub>UVLOR</sub>  |   |       | 2.55  | 2.7   | V                   |
| UVLO hysteretic                 | V <sub>UVLOHY</sub> |   |       | 150   |       | mV                  |
| Switching frequency             | F <sub>SW</sub>     |   | 0.85  |       | 2.2   | MHz                 |
| Frequency variation             | F <sub>SW</sub>     |   |       |       | 25%   |                     |
| Minimum on time <sup>(7)</sup>  | T <sub>MINON</sub>  |   |       | 60    |       | ns                  |
| Switch leakage                  | I <sub>SW</sub>     | V <sub>EN</sub> =0V, V <sub>IN</sub> =5V, V <sub>SW</sub> =0V<br>and 5V, T <sub>J</sub> =25°C |       | 0.1   | 1     | μA                  |
| EN turn on delay <sup>(7)</sup> |                     | EN to SW active   |       | 107   |       | μs                  |
| EN rising threshold             |                     | T <sub>J</sub> =25°C  | 1.38  | 1.55  | 1.72  | V                   |
| EN hysteresis                   |                     | T <sub>J</sub> =25°C  |       | 0.697 |       | V                   |
| Power good UV threshold rising  | PGVth-Hi            | Good  |       | 0.9   |       | V <sub>OUT</sub>    |
| Power good UV threshold falling | PGVth-Lo            | Fault   |       | 0.85  |       | V <sub>OUT</sub>    |
| Power good OV threshold rising  | PGVth-Hi            | Fault   |       | 1.1   |       | V <sub>OUT</sub>    |
| Power good OV threshold falling | PGVth-Lo            | Good  |       | 1.05  |       | V <sub>OUT</sub>    |
| Power good pull-down voltage    | V <sub>PGL</sub>    | I <sub>SINK</sub> =1mA  |       |       | 0.4   | V                   |
| Power good deglitch time        | T <sub>PGd</sub>    |   |       | 50    |       | μs                  |
| Power good leakage              | I <sub>PGd</sub>    |   |       |       | 1     | μA                  |
| V <sub>OUT</sub> OVP threshold  |                     | Rising edge   |       | +10%  |       | V <sub>TARGET</sub> |

### ELECTRICAL CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 5V, T<sub>J</sub> = -40°C to +125°C<sup>(6)</sup>, typical value is tested at T<sub>J</sub> = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

| Parameter  | Symbol              | Condition                              | Min | Typ | Max | Units |
|--|---------------------|--|-----|-----|-----|-------|
| High-side switch peak current limit (source)         | I <sub>peak</sub>   |  | 7   | 9   |     | A     |
| High-side switch valley current limit <sup>(7)</sup> | I <sub>valley</sub> |  |     | 5.8 |     | A     |
| Low-side switch current limit (sink)                 |                     | PFM mode                               |     | 0   |     | A     |
|  |                     | PWM mode <sup>(7)</sup>                |     | -5  |     | A     |
| Soft-start time                                      | T <sub>SS-ON</sub>  | V <sub>OUT</sub> rises from 10% to 90% | 0.4 | 1   | 1.6 | ms    |
| Discharge resistor                                   |                     |  |     | 500 |     | Ω     |
| Thermal warning <sup>(7)</sup>                       |                     |  |     | 130 |     | °C    |
| Thermal shutdown <sup>(7)</sup>                      |                     |  |     | 150 |     | °C    |
| DAC resolution <sup>(7)</sup>                        |                     |  |     | 7   |     | bits  |

**NOTE:**

6) Not tested in production, guaranteed by over-temperature correlation .

7) Data based on sample characterization.

### I/O LEVEL CHARACTERISTICS

| Parameter  | Symbol           | Condition  | HS-Mode             |                      | LS-Mode             |                      | Units |
|--|------------------|--|---------------------|----------------------|---------------------|----------------------|-------|
|  |                  |  | Min                 | Max                  | Min                 | Max                  |       |
| Low-level input voltage  | V <sub>IL</sub>  |  | -0.5                | 0.3V <sub>CC</sub>   | -0.5                | 0.3V <sub>CC</sub>   | V     |
| High-level input voltage   | V <sub>IH</sub>  |  | 0.7V <sub>CC</sub>  | V <sub>CC</sub> +0.5 | 0.7V <sub>CC</sub>  | V <sub>CC</sub> +0.5 | V     |
| Hysteresis of Schmitt trigger inputs   | V <sub>HYS</sub> | V <sub>CC</sub> >2V  | 0.05V <sub>CC</sub> | -                    | 0.05V <sub>CC</sub> | -                    | V     |
|  |                  | V <sub>CC</sub> <2V  | 0.1V <sub>CC</sub>  | -                    | 0.1V <sub>CC</sub>  | -                    |       |
| Low-level output voltage(open drain) at 3mA sink current                       | V <sub>OL</sub>  | V <sub>CC</sub> >2V  | 0                   | 0.4                  | 0                   | 0.4                  | V     |
|  |                  | V <sub>CC</sub> <2V  | 0                   | 0.2V <sub>CC</sub>   | 0                   | 0.2V <sub>CC</sub>   |       |
| Low-level output current   | I <sub>OL</sub>  |  | -                   | 3                    | -                   | 3                    | mA    |
| Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH | R <sub>onL</sub> | VOL level, IOL=3mA   | -                   | 50                   | -                   | 50                   | Ω     |
| Transfer gate on resistance between SDA and SCAH, or SCL and SCLH              | R <sub>onH</sub> | Both signals (SDA and SDAH, or SCL and SCLH) at V <sub>CC</sub> level                    | 50                  | -                    | 50                  | -                    | kΩ    |
| Pull-up current of the SCLH current source                                     | I <sub>cs</sub>  | SCLH output levels between 0.3V <sub>CC</sub> and 0.7V <sub>CC</sub>                     | 2                   | 6                    | 2                   | 6                    | mA    |
| Rise time of the SCLH or SCL signal  | t <sub>rCL</sub> | Output rise time (current source enabled) with an external pull-up current source of 3mA |                     |                      |                     |                      |       |
|  |                  | Capacitive load from 10pF to 100pF   | 10                  | 40                   |                     |                      | ns    |
|  |                  | Capacitive load of 400pF   | 20                  | 80                   |                     |                      | ns    |
| Fall time of the SCLH or SCL signal  | t <sub>rCL</sub> | Output fall time (current source enabled) with an external pull-up current source of 3mA |                     |                      |                     |                      |       |
|  |                  | Capacitive load from 10pF to 100pF   | 10                  | 40                   |                     |                      | ns    |
|  |                  | Capacitive load of 400pF   | 20                  | 80                   | 20                  | 250                  | ns    |
| Rise time of SDAH signal   | t <sub>rDA</sub> | Capacitive load from 10pF to 100pF   | 10                  | 80                   | -                   | -                    | ns    |
|  |                  | Capacitive load of 400pF   | 20                  | 160                  | 20                  | 250                  | ns    |
| Fall time of SDAH signal   | t <sub>rDA</sub> | Capacitive load from 10pF to 100pF   | 10                  | 80                   | -                   | -                    | ns    |
|  |                  | Capacitive load of 400pF   | 20                  | 160                  | 20                  | 250                  | ns    |

**I/O LEVEL CHARACTERISTICS**(continued)

| Parameter   | Symbol          | Condition   | HS-Mode |     | LS-Mode |     | Units |
|---|-----------------|---|---------|-----|---------|-----|-------|
|   |                 |   | Min     | Max | Min     | Max |       |
| Pulse width of spikes that must be suppressed by the input filter | t <sub>SP</sub> |   | 0       | 10  | 0       | 50  | ns    |
| Input current for each I/O pin                                    | I <sub>i</sub>  | Input voltage between 0.1V <sub>CC</sub> and 0.9V <sub>CC</sub> | -       | 10  | -10     | +10 | μA    |
| Capacitance for each I/O pin                                      | C <sub>i</sub>  |   | -       | 10  | -       | 10  | pF    |

## I<sup>2</sup>C PORT SIGNAL CHARACTERISTICS

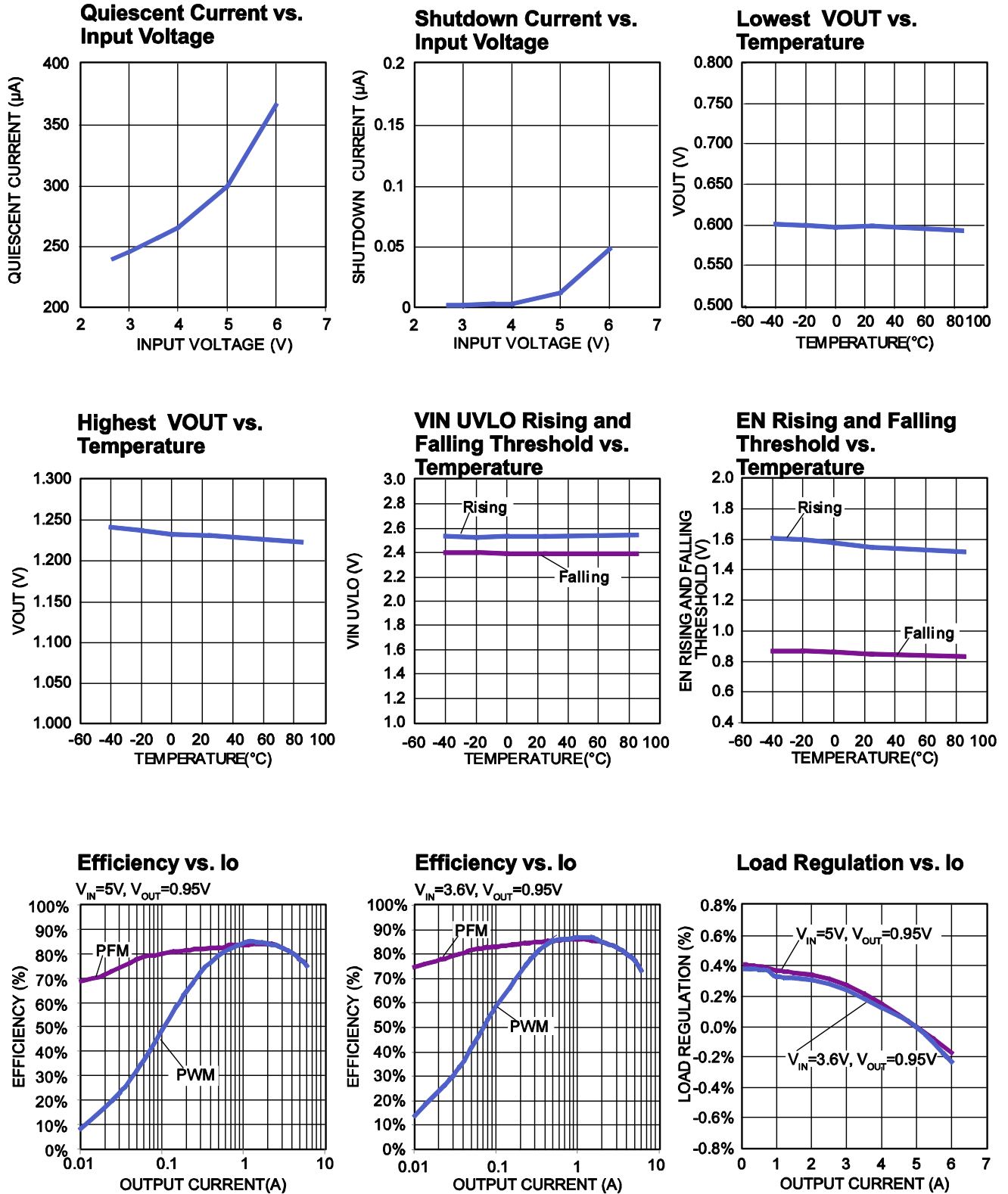
| Parameter  | Symbol              | Condition                       | Cb=100pF |                    | Cb=400pF           |     | Units |
|--|---------------------|---------------------------------|----------|--------------------|--------------------|-----|-------|
|  |                     |                                 | Min      | Max                | Min                | Max |       |
| SCLH and SCL clock frequency   | f <sub>SCHL</sub>   |                                 | 0        | 3.4                | 0                  | 0.4 | MHz   |
| Set-up time for a repeated START condition   | T <sub>SU;STA</sub> |                                 | 160      | -                  | 600                | -   | ns    |
| Hold time (repeated) START condition   | T <sub>HD;STA</sub> |                                 | 160      | -                  | 600                | -   | ns    |
| Low period of the SCL clock  | t <sub>LOW</sub>    |                                 | 160      | -                  | 1300               | -   | ns    |
| High period of the SCL clock   | t <sub>HIGH</sub>   |                                 | 60       | -                  | 600                | -   | ns    |
| Data set-up time   | T <sub>SU;DAT</sub> |                                 | 10       | -                  | 100                | -   | ns    |
| Data hold time   | T <sub>HD;DAT</sub> |                                 | 0        | 70                 | 0                  | -   | ns    |
| Rise time of SCLH signal   | t <sub>rCL</sub>    |                                 | 10       | 40                 | 20*0.1Cb           | 300 | ns    |
| Rise time of SCLH signal after a repeated START condition and after an acknowledge bit | t <sub>rCL1</sub>   |                                 | 10       | 80                 | 20*0.1Cb           | 300 | ns    |
| Fall time of SCLH signal   | T <sub>fCL</sub>    |                                 | 10       | 40                 | 20*0.1Cb           | 300 | ns    |
| Rise time of SDAH signal   | t <sub>rDA</sub>    |                                 | 10       | 80                 | 20*0.1Cb           | 300 | ns    |
| Fall time of SDAH signal   | T <sub>fDA</sub>    |                                 | 10       | 80                 | 20*0.1Cb           | 300 | ns    |
| Set-up time for a stop condition   | T <sub>SU;STO</sub> |                                 | 160      | -                  | 600                | -   | ns    |
| Bus free time between a stop and start condition                                       | T <sub>BUF</sub>    |                                 | 160      | -                  | 1300               | -   | ns    |
| Data valid time  | T <sub>VD;DAT</sub> |                                 | -        | 16                 | -                  | 90  | ns    |
| Data valid acknowledge time  | T <sub>VD;ACK</sub> |                                 | -        | 160                | -                  | 900 | ns    |
| Capacitive load for each bus line  | C <sub>b</sub>      | SDAH and SCLH line              | -        | 100                | -                  | 400 | pF    |
|  |                     | SDAH+SDA line and SCLH+SCL line | -        | 400                | -                  | 400 | pF    |
| Noise margin at the low level  | V <sub>nL</sub>     | For each connected device       | -        | 0.1V <sub>CC</sub> | 0.1V <sub>CC</sub> | -   | V     |
| Noise margin at the high level   | V <sub>nH</sub>     | For each connected device       | -        | 0.2V <sub>CC</sub> | 0.2V <sub>CC</sub> | -   | V     |

**NOTE:** V<sub>CC</sub> is the I<sup>2</sup>C bus voltage, 1.5V to 3.3V range.



### TYPICAL CHARACTERISTICS

V<sub>IN</sub> = 5V, V<sub>OUT</sub> = 0.95V, L = 0.47μH, T<sub>A</sub> = 25°C, PWM, unless otherwise noted.

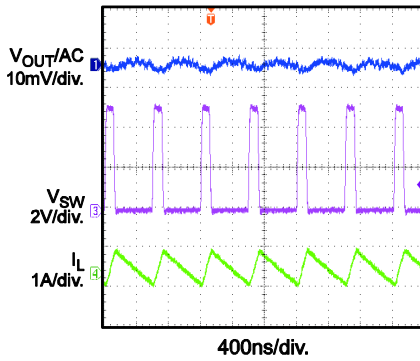


**TYPICAL CHARACTERISTICS** (continued)

V<sub>IN</sub> = 5V, V<sub>OUT</sub> = 0.95V, L = 0.47μH, T<sub>A</sub> = 25°C, PWM, unless otherwise noted.

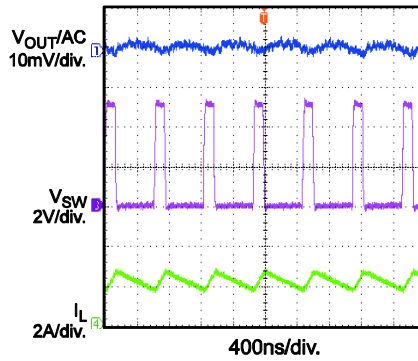
**Output Ripple**

I<sub>OUT</sub> = 0A



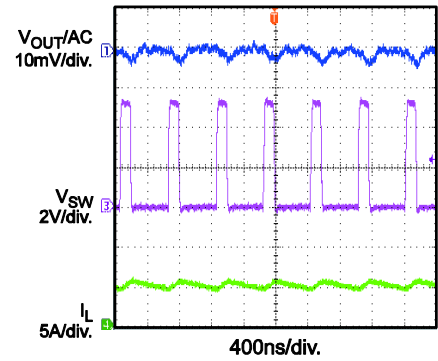
**Output Ripple**

I<sub>OUT</sub> = 2A



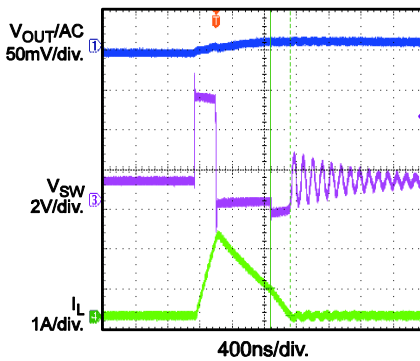
**Output Ripple**

I<sub>OUT</sub> = 5A



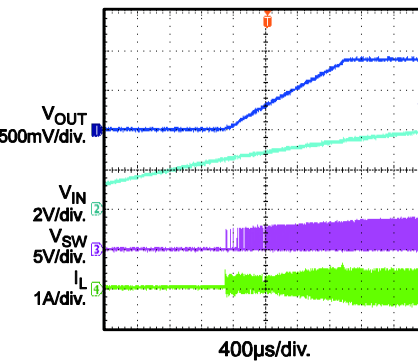
**Output Ripple**

PFM Mode



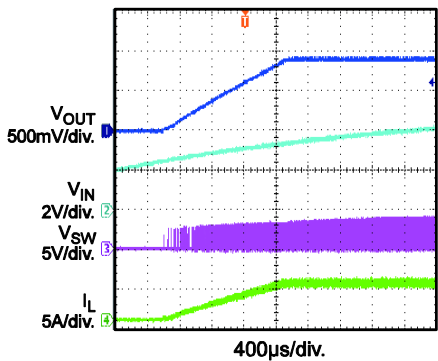
**VIN Power Up**

I<sub>OUT</sub> = 0A



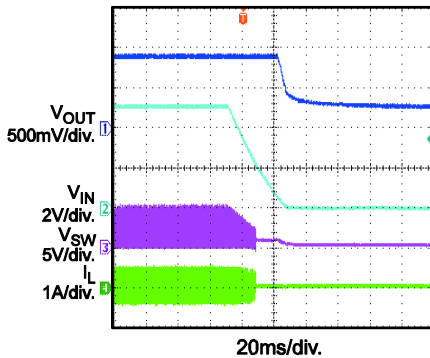
**VIN Power Up**

I<sub>OUT</sub> = 5A



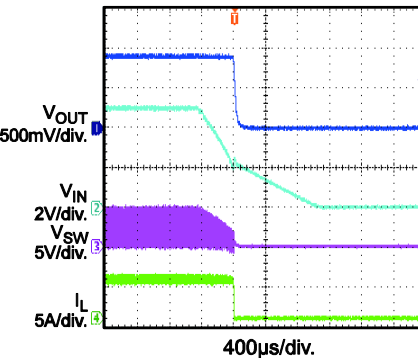
**VIN Power Down**

I<sub>OUT</sub> = 0A



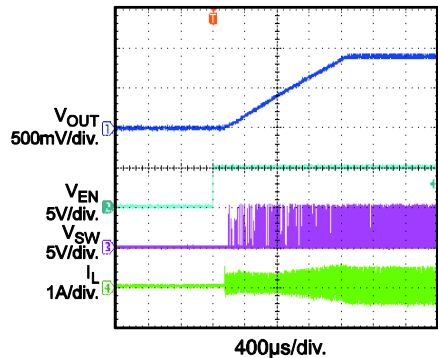
**VIN Power Down**

I<sub>OUT</sub> = 5A



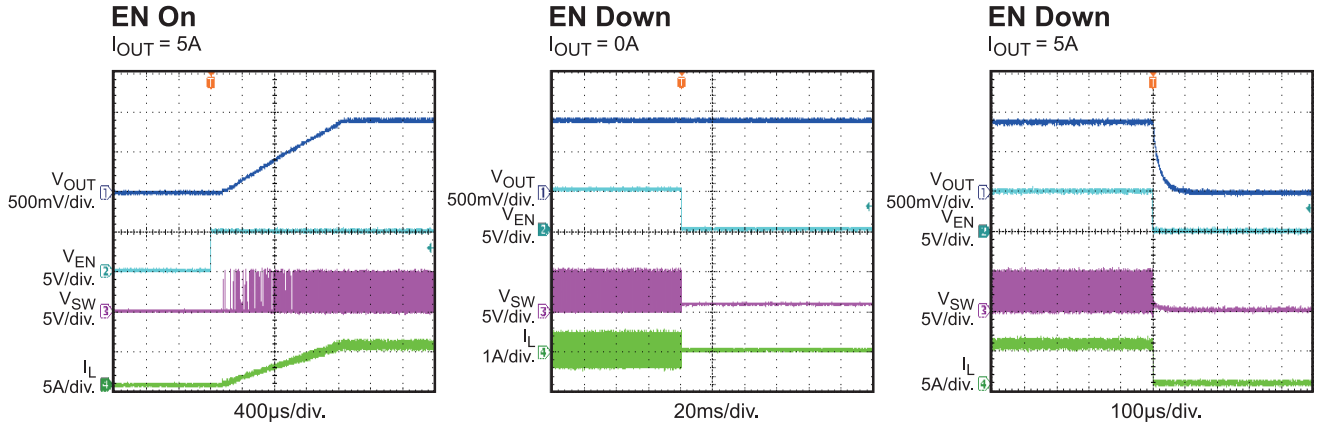
**EN On**

I<sub>OUT</sub> = 0A



**TYPICAL CHARACTERISTICS**(continued)

V<sub>IN</sub> = 5V, V<sub>OUT</sub> = 0.95V, L = 0.47μH, T<sub>A</sub> = 25°C, unless otherwise noted.



## PIN FUNCTIONS

| Package Pin # | Name | Description                    |
|---------------|------|--------------------------------|
| 1             | PG   | Power good output.             |
| 2             | SDA  | I <sup>2</sup> C serial data.  |
| 3, 10         | GND  | Power ground.                  |
| 4, 5, 6       | VIN  | Input supply voltage.          |
| 7, 8, 9       | SW   | Switch node.                   |
| 11            | AGND | Analog ground.                 |
| 12            | VOUT | Output voltage sensing.        |
| 13            | SCL  | I <sup>2</sup> C serial clock. |
| 14            | EN   | On and off control.            |

## REGISTERS AND DESCRIPTION

### Register Map

| ADD | NAME        | R/W | D7                  | D6               | D5  | D4                 | D3      | D2        | D1         | D0      |
|-----|-------------|-----|---------------------|------------------|-----|--------------------|---------|-----------|------------|---------|
| 00  | Status      | R   | ILIM                | UVLO             | OVP | VoOV               | VoUV    | PGOOD     | OTW        | EN stat |
| 01  | VSEL        | R/W | EN                  | Output reference |     |                    |         |           |            |         |
| 02  | SysCntlreg1 | R/W | Switching frequency |                  |     | Transient response |         | Pglohi    | Vinovp     | Mode    |
| 03  | SysCntlreg2 | R/W | Reserved            |                  | Go  | Out-dis            | GI_filt | Slew rate | PG control | PG set  |
| 04  | ID1         | R   | Vendor ID           |                  |     |                    | Die ID  |           |            |         |
| 05  | ID2         | R   | Reserved            |                  |     |                    | Die rev |           |            |         |

**NOTE:** The burst write cannot be on Reg.03.

### Default Value of Registers

| ADD | NAME        | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-------------|-----|----|----|----|----|----|----|----|----|
| 00  | Status      | R   | NA | NA | NA | NA | NA | NA | NA | NA |
| 01  | VSEL        | R/W | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 0  |
| 02  | SysCntlreg1 | R/W | 1  | 0  | 0  | 0  | 1  | 1  | 0  | 0  |
| 03  | SysCntlreg2 | R/W | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  |
| 04  | ID1         | R   | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1  |
| 05  | ID2         | R   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

### Register Description

#### 1. Reg00 Status

| NAME    | BITS | DESCRIPTION  |
|---------|------|--|
| ILIM    | D7   | When the bit is high, IC is in the current limit.  |
| UVLO    | D6   | When the bit is high, VIN is less than the UVLO threshold.   |
| OVP     | D5   | When the bit is high, VIN is greater than the OVP threshold.   |
| VoOV    | D4   | When the bit is high, a voltage higher than 110% of the regulation voltage is presented.                               |
| VoUV    | D3   | When the bit is high, a voltage lower than 90% of the regulation voltage is presented.                                 |
| PGOOD   | D2   | When the bit is high, the output is in regulation; otherwise, the output voltage is out of the ±10% regulation window. |
| OTW     | D1   | When the junction temperature is higher than 130°C, the bit is high; otherwise, the bit is low.                        |
| En stat | D0   | When the bit is high, the SMPS is enabled; when the bit is low, the SMPS is disabled.                                  |

#### 2. Reg01 VSEL

| NAME             | BITS   | DESCRIPTION   |
|------------------|--------|---|
| EN               | D7     | I <sup>2</sup> C controlled enable. When EN is low, the converter is off. When EN is high, the EN bit takes over. |
| Output Reference | D[6:0] | Sets the output voltage from 0.6V to 1.235V (see Table 1).  |



Table 1: Output Voltage Chart

| D[6:0]   | VOUT  | D[6:0]   | VOUT  | D[6:0]   | VOUT  | D[6:0]   | VOUT  |
|----------|-------|----------|-------|----------|-------|----------|-------|
| 000 0000 | 0.600 | 010 0000 | 0.760 | 100 0000 | 0.920 | 110 0000 | 1.080 |
| 000 0001 | 0.605 | 010 0001 | 0.765 | 100 0001 | 0.925 | 110 0001 | 1.085 |
| 000 0010 | 0.610 | 010 0010 | 0.770 | 100 0010 | 0.930 | 110 0010 | 1.090 |
| 000 0011 | 0.615 | 010 0011 | 0.775 | 100 0011 | 0.935 | 110 0011 | 1.095 |
| 000 0100 | 0.620 | 010 0100 | 0.780 | 100 0100 | 0.940 | 110 0100 | 1.100 |
| 000 0101 | 0.625 | 010 0101 | 0.785 | 100 0101 | 0.945 | 110 0101 | 1.105 |
| 000 0110 | 0.630 | 010 0110 | 0.790 | 100 0110 | 0.950 | 110 0110 | 1.110 |
| 000 0111 | 0.635 | 010 0111 | 0.795 | 100 0111 | 0.955 | 110 0111 | 1.115 |
| 000 1000 | 0.640 | 010 1000 | 0.800 | 100 1000 | 0.960 | 110 1000 | 1.120 |
| 000 1001 | 0.645 | 010 1001 | 0.805 | 100 1001 | 0.965 | 110 1001 | 1.125 |
| 000 1010 | 0.650 | 010 1010 | 0.810 | 100 1010 | 0.970 | 110 1010 | 1.130 |
| 000 1011 | 0.655 | 010 1011 | 0.815 | 100 1011 | 0.975 | 110 1011 | 1.135 |
| 000 1100 | 0.660 | 010 1100 | 0.820 | 100 1100 | 0.980 | 110 1100 | 1.140 |
| 000 1101 | 0.665 | 010 1101 | 0.825 | 100 1101 | 0.985 | 110 1101 | 1.145 |
| 000 1110 | 0.670 | 010 1110 | 0.830 | 100 1110 | 0.990 | 110 1110 | 1.150 |
| 000 1111 | 0.675 | 010 1111 | 0.835 | 100 1111 | 0.995 | 110 1111 | 1.155 |
| 001 0000 | 0.680 | 011 0000 | 0.840 | 101 0000 | 1.000 | 111 0000 | 1.160 |
| 001 0001 | 0.685 | 011 0001 | 0.845 | 101 0001 | 1.005 | 111 0001 | 1.165 |
| 001 0010 | 0.690 | 011 0010 | 0.850 | 101 0010 | 1.010 | 111 0010 | 1.170 |
| 001 0011 | 0.695 | 011 0011 | 0.855 | 101 0011 | 1.015 | 111 0011 | 1.175 |
| 001 0100 | 0.700 | 011 0100 | 0.860 | 101 0100 | 1.020 | 111 0100 | 1.180 |
| 001 0101 | 0.705 | 011 0101 | 0.865 | 101 0101 | 1.025 | 111 0101 | 1.185 |
| 001 0110 | 0.710 | 011 0110 | 0.870 | 101 0110 | 1.030 | 111 0110 | 1.190 |
| 001 0111 | 0.715 | 011 0111 | 0.875 | 101 0111 | 1.035 | 111 0111 | 1.195 |
| 001 1000 | 0.720 | 011 1000 | 0.880 | 101 1000 | 1.040 | 111 1000 | 1.200 |
| 001 1001 | 0.725 | 011 1001 | 0.885 | 101 1001 | 1.045 | 111 1001 | 1.205 |
| 001 1010 | 0.730 | 011 1010 | 0.890 | 101 1010 | 1.050 | 111 1010 | 1.210 |
| 001 1011 | 0.735 | 011 1011 | 0.895 | 101 1011 | 1.055 | 111 1011 | 1.215 |
| 001 1100 | 0.740 | 011 1100 | 0.900 | 101 1100 | 1.060 | 111 1100 | 1.220 |
| 001 1101 | 0.745 | 011 1101 | 0.905 | 101 1101 | 1.065 | 111 1101 | 1.225 |
| 001 1110 | 0.750 | 011 1110 | 0.910 | 101 1110 | 1.070 | 111 1110 | 1.230 |
| 001 1111 | 0.755 | 011 1111 | 0.915 | 101 1111 | 1.075 | 111 1111 | 1.235 |

### 3. Reg02 SysCntlreg1

| NAME                | BITS   | DESCRIPTION  |                     |        |                     |
|---------------------|--------|--|---------------------|--------|---------------------|
| Switching Frequency | D[7:5] | D[7:5]   | Switching Frequency | D[7:5] | Switching Frequency |
|                     |        | 000  | 2.2MHz              | 100    | 1.25MHz(default)    |
|                     |        | 001  | 2MHz                | 101    | 1.11MHz             |
|                     |        | 010  | 1.67MHz             | 110    | 0.85MHz             |
|                     |        | 011  | --                  | 111    | --                  |
| Transient Response  | D[4:3] | D[4:3]   | Response Speed      | D[4:3] | Response Speed      |
|                     |        | 00   | Ultra-fast          | 01     | Fast(default)       |
|                     |        | 10   | Normal              | 11     | Slow                |
| PG_LOHI             | D2     | A "0" here sets PGOOD to sense only a negative voltage excursion of VO from the reference. A "1" (default) sets PGOOD to detect both a positive and negative excursion of VO from the reference. |                     |        |                     |
| VIN_OVP             | D1     | A "1" disables the VIN OVP function. The converter continues operating. A "0" (default) turns off the converter when VIN reaches VIN MAX.  |                     |        |                     |
| Mode                | D0     | A "0" enables PFM mode; a high disables PFM mode.  |                     |        |                     |

### 4.Reg03 SysCntlreg2

| NAME             | BITS   | DESCRIPTION  |           |    |           |
|------------------|--------|--|-----------|----|-----------|
| Reserved         | D[7:6] | Reserved.  |           |    |           |
| Go               | D5     | Writing to this bit starts a VOUT transition regardless of its initial value.  |           |    |           |
| Output Discharge | D4     | A "0" disables the output discharge. The output voltage must be discharged by the load. A high enables the internal pull-down. |           |    |           |
| GI_filt          | D3     | A "0" disables PGOOD delay.  |           |    |           |
| Slew Rate        | D2     | D2   | Slew rate | D2 | Slew rate |
|                  |        | 0  | 32mV/μs   | 1  | 8mV/μs    |
| PG Control       | D1     | A "0" enable the PG function. A "1" disables the PG function, and then the PG voltage is set by the PG Set bit.                |           |    |           |
| PG Set           | D0     | When the PG Control bit=1, the PG voltage is pulled high if PG Set=0; otherwise, the PG voltage is pulled low.                 |           |    |           |

### 5. Reg04 ID1

| NAME      | BITS   | DESCRIPTION |
|-----------|--------|-------------|
| Vendor ID | D[7:4] | Vendor ID.  |
| Die ID    | D[3:0] | IC type.    |

### 6.Reg05 ID2

| NAME     | BITS   | DESCRIPTION   |
|----------|--------|---------------|
| Reserved | D[7:4] | Reserved.     |
| Die Rev  | D[3:0] | Die revision. |

### Operation Status

| CONDITION                                    | PG   | REGULATION | LATCH-OFF | STATUS BIT |
|--|------|------------|-----------|------------|
| VIN over-voltage                             | Low  | Off        | No        | OVP        |
| VIN under-voltage                            | Low  | Off        | N/A       | UVLO       |
| Thermal warning                              | Low  | On         | No        | OTW        |
| Thermal shutdown                             | Low  | Off        | Yes       | N/A        |
| Current limit                                | High | On         | No        | ILIM       |
| Output under-voltage                         | Low  | Off        | Yes       | VoUV       |
| Output over-voltage (>110% of target output) | Low  | On         | No        | VoOV       |

## BLOCKDIAGRAM

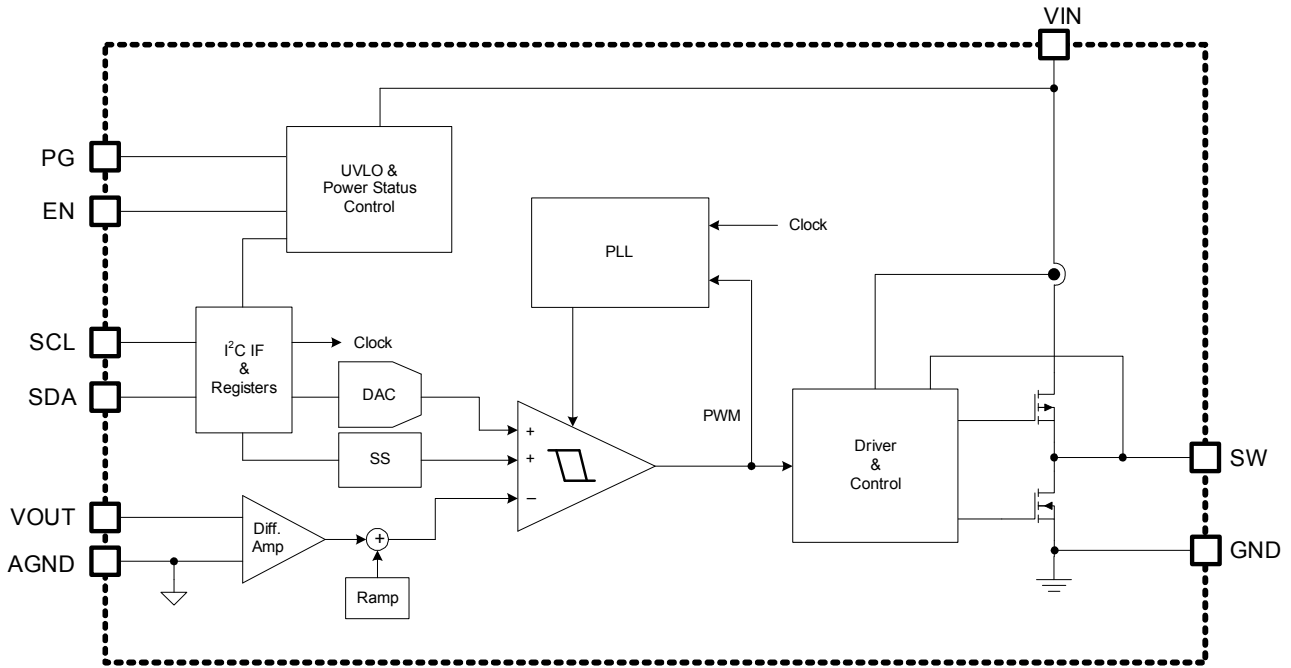


Figure 2: Functional Block Diagram



## OPERATION

The MP8847 is a low-voltage, 6A, synchronous, step-down converter with a controllable I<sup>2</sup>C interface. The MP8847 applies MPS's patented constant-frequency hysteretic control to utilize fast transient response of the hysteretic control and keep the switching frequency constant. No compensation is required, which simplifies the design procedure.

The MP8847 integrates an I<sup>2</sup>C-compatible interface that allows transfers up to 3.4Mbps. This communication interface can be used for dynamic voltage scaling with voltage steps down to 5mV with the output voltage from 0.6V to 1.235V. The voltage transition slew rate can be controlled as well.

### Light-Load Operation

In light-load condition, the MP8847 uses a proprietary control scheme to save power and improve efficiency. The MP8847 turns off the low-side switch when the inductor current begins reversing. The MP8847 then works in discontinuous conduction mode (DCM) operation.

### Enable(EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.55V), the MP8847 can be enabled by pulling EN above 1.55V (typical value). Pull EN down to ground to disable the MP8847. The IC can also be disabled by floating EN. There is an internal 1M $\Omega$  resistor from EN to ground.

### Soft Start (SS)

The MP8847 has a built-in soft start that ramps up the output voltage at a controlled slew rate, preventing inrush current and output voltage overshoot at start-up. The soft-start time is about 1ms.

### Power Good (PG) Indicator

The MP8847 has an open drain output for power good (PG) indication. When the output voltage is within  $\pm 10\%$  of the regulation voltage, PG is pulled up to VIN by the external resistor.

### Current Limit

The MP8847 has a typical 9A current limit for the high-side switch. When the high-side switch reaches the current limit, the MP8847 expands the minimum off time until the current drops to 5.8A before the high-side switch is turned on for the next switching cycle. This prevents the inductor current from continuing to build up and damaging the components.

### Thermal Protection

The MP8847 employs thermal shutdown by monitoring the junction temperature of the IC internally. If the junction temperature exceeds the thermal warning threshold (around 130°C), OTW is set. If there is no action or response from the system, the junction temperature continues rising until it exceeds the thermal shutdown threshold (typically 150°C). After thermal shutdown, a new power start-up cycle is needed to turn on the MP8847 again.

## I<sup>2</sup>C INTERFACE

The MP8847 can communicate with the core and the I<sup>2</sup>C for smart design. MPS has a GUI control interface (see Figure 3). The installation process and usage can be found in the MP884x Family Software Guide.

### I<sup>2</sup>C Address

The I<sup>2</sup>C slave address of the MP8847 is 0xC0H / 0xC1H internally (see Table 2).

**Table 2: I<sup>2</sup>C Slave Address**

| Hex     | A7   | A6 | A5 | A4 | A3 | A2 | A1 | A0  |
|---------|------|----|----|----|----|----|----|-----|
| W 0xC0  | 1    | 1  | 0  | 0  | 0  | 0  | 0  | R/W |
| R 0xC1  |      |    |    |    |    |    |    |     |
| Address | 0x60 |    |    |    |    |    |    |     |

### I<sup>2</sup>C Enable

The MP8847's EN pin can start up and shutdown the converter, and the I<sup>2</sup>C Enable pin can control the converter as well. The Reg01 VSEL D7 bit is I<sup>2</sup>C-controlled enabled. When writing D7=0, the converter is off. When writing D7=1, the converter is on. Both the external EN and I<sup>2</sup>C EN can control the converter. The converter works only when both EN pins are high.

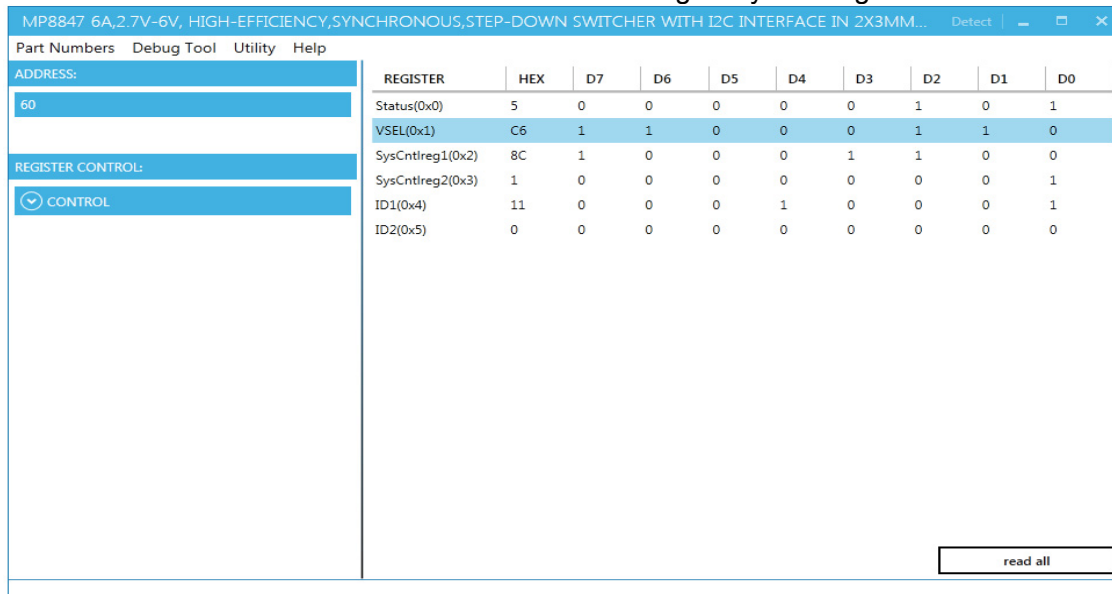
## Output Voltage Selection

The MP8847 output voltage is I<sup>2</sup>C-programmable. There is no need to set feedback resistors to achieve different output voltages. The default output voltage is 0.95V but can be set from 0.6V to 1.235V in 5mV steps via the I<sup>2</sup>C. To change the output voltage, write the Go bit (Reg03 SysCntlreg2 [D5]) to 1. This action means that the output voltage can be set to another value that is not the default Vo voltage. Then write the Output reference bit (Reg01 VSEL [D6:D0]). The output voltage can be changed according to Table 1.

To guarantee a normal output voltage, the input voltage is suggested to be 1.5V higher than the pre-set output voltage.

## Switching Frequency

The default switching frequency of the MP8847 is 1.25MHz. However, the frequency can be changed based on the application. By writing the switching frequency bits (Reg02 SysCntlreg1 [D7:D5]), the switching frequency can be programmed to one of six possible values. Their corresponding data can be found in Reg02 SysCntlreg1.



**Figure 3: MP8847 Control Interface**

### PGOOD Configuration

The MP8847 has an option to use the PG\_LOHI function. This function can be written in the Pgluhi bit (Reg02 Syscntlreg1 [D2]). The default value is 1, where PGOOD senses both a positive and negative excursion of Vo from the reference. If writing this bit to 0, PGOOD only senses a negative voltage excursion of Vo from the reference.

### Input Over-Voltage Protection (OVP)

The MP8847 has an option to use the VIN\_OVP function. This function can be written in the VIN\_OVP bit (Reg02 Syscntlreg1 [D1]). The default value is 0, where the VIN OVP function is enabled. When VIN is higher than 6.3V, the converter is disabled. After VIN recovers to 6.2V, the converter restarts. If the VIN\_OVP bit is set to 1, VIN OVP is disable. The converter will not stop, even if VIN exceeds its safe range.

### Forced Continuous Conduction Mode (CCM)

The MP8847 has auto-pulse-frequency modulation (PFM) mode and forced CCM. This function can be written in the Mode bit (Reg02 Syscntlreg1 [D0]). The default value is 0, where auto-PFM mode is selected. Considering a smaller Vo ripple and regulation for a full load range, forced CCM is recommended. Set this bit to 1 to disable PFM mode.

### Output Discharge

The MP8847 has an output discharge function. Writing the Out-dis bit (Reg03 SysCntlreg2 [D4]) can change the output discharge mode. The default value is 0, and Vo can be discharged by its load when EN is low. Writing D4=1 can enable the function, and then the output voltage

can be discharged by the internal pull-down resistance.

### Output Voltage Transition Slew Rate

When the output voltage switches from low to high or from high to low, the transition slew rate can be different. There are two possible values for selection. Through writing the Slew Rate bits (Reg02 Syscntlreg1[D4: D3]), the transition slew rate can be set at one possible value based on the application. The internal reference follows the set slew rate, but the output voltage slew rate does not always follow the internal reference. Considering the output capacitor and inductor, the actual output voltage slew rate should be a little slower.

### PG Multi-Use

The MP8847 PG pin has multi-usage. When the PG Control bit (Reg03 SysCntlreg2 D1) is 0, PG indicates the Vo status, such as Vo over-voltage or under-voltage. When the PG Control bit (Reg03 sysCntlrg2 D1) is 1, the PG voltage is controlled by the PG Set bit (Reg03 sysCntlrg2 D0).The PG voltage is high if D0=0; otherwise, the PG voltage is low (see Table 3).

**Table 3: PG Multi-Use**

| D1 | D0 | PG             |
|----|----|----------------|
| 0  | 0  | PG indicator   |
| 0  | 1  |                |
| 1  | 0  | PG forced to 1 |
| 1  | 1  | PG forced to 0 |

### I<sup>2</sup>C Register Hold On

The MP8847 has a special function: the I<sup>2</sup>C register can hold on after EN changes low. The updated register can be held for later application conditions, even if the external EN pulls low.

### TYPICAL APPLICATION CIRCUIT

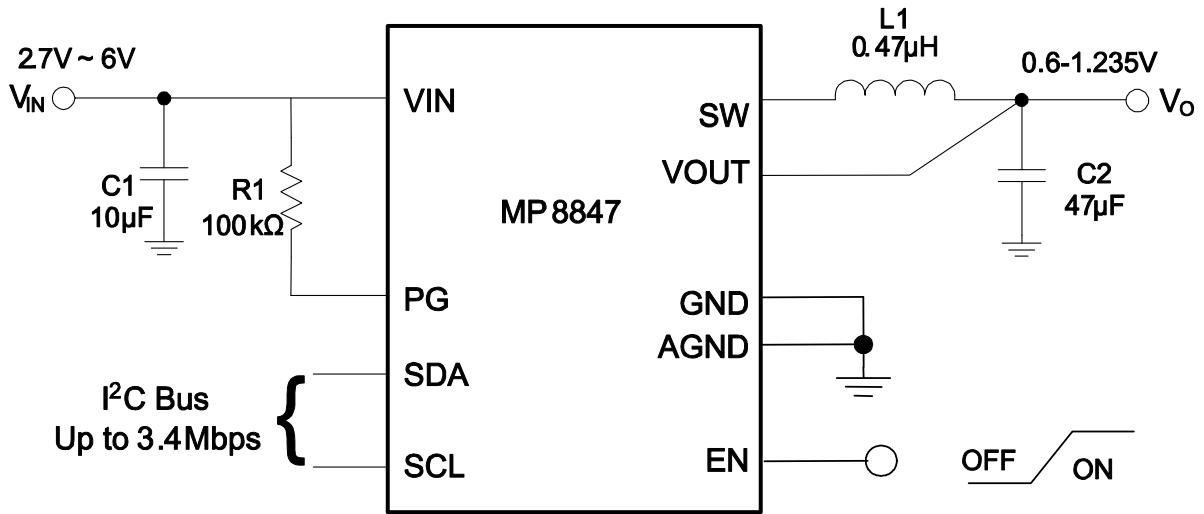
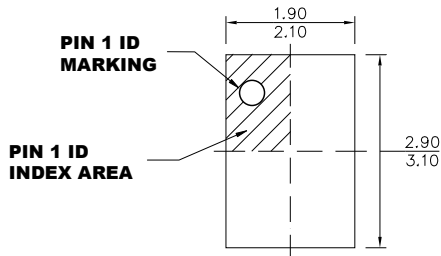


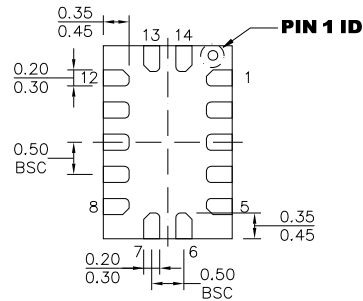
Figure 4: Application Circuit

## PACKAGE INFORMATION

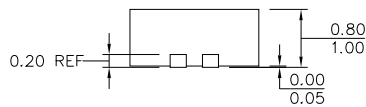
### QFN-14 (2mmx3mm)



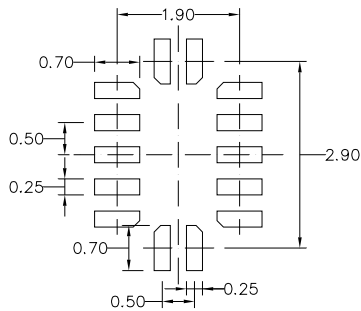
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

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