MP8845

5A, Highly Efficient, Synchronous, Step-Down Switcher with I²C Interface

The Future of Analog IC Technology

DESCRIPTION

The MP8845 is a highly integrated, high-frequency, synchronous, step-down switcher with an I²C control interface. The MP8845 can support up to 5A of load current over a 2.7V to 6V input supply range with excellent load and line regulation.

Fixed-frequency hysteretic control mode provides an extremely fast transient response without loop compensation to achieve high efficiency easily under light-load conditions.

The output voltage level can be controlled on-the-fly through a 3.4Mbps I²C serial interface. The voltage range can be adjusted from 0.6V to 1.1V in 3.9mV steps. The voltage slew rate, switching frequency, and power-saving modes are also selectable through the I²C interface.

Full protection features include internal soft start, over-current protection (OCP), and over-temperature protection (OTP).

The MP8845 requires a minimum number of readily available, standard, external components and is available in a compact WLCSP-20 (1.70mmx2.10mm) package.

FEATURES

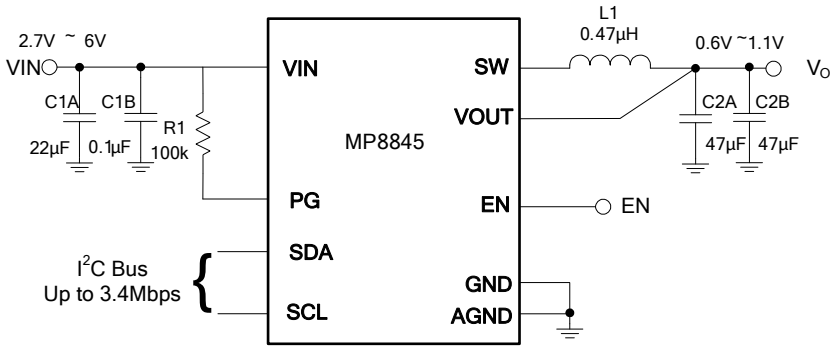
- 2.7V to 6V Input Voltage Range
- Up to 5A Load Current
- Internal 28mΩ High-Side and 17mΩ Low-Side Power MOSFETs
- Fixed-Frequency Hysteretic Mode Control
- I²C-Compatible Interface up to 3.4Mbps
- I²C-Programmable Output Range from 0.6V to 1.1V in 3.9mV Steps
- Factory Adjustable Switching Frequency from 1MHz to 2.2MHz
- I²C-Programmable Voltage Transition Slew Rate
- Power-Saving Mode Selectable via I²C
- Internal Soft Start
- Power Good Indicator
- Current Overload and Thermal Shutdown Protection
- Available in 20-Ball WLCSP-20 (1.70mmx2.10mm) Package

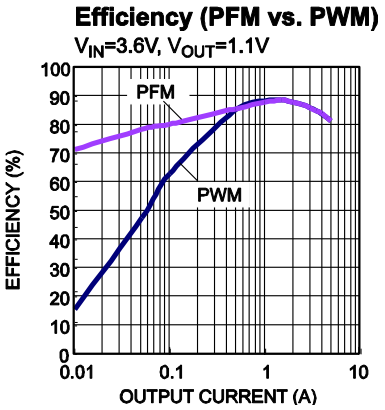
APPLICATIONS

- Processor Core Supply
- Micro Converter

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS” and “The Future of Analog IC Technology” are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8845GC	WLCSP-20 (1.70mmx2.10mm)	*See Below*

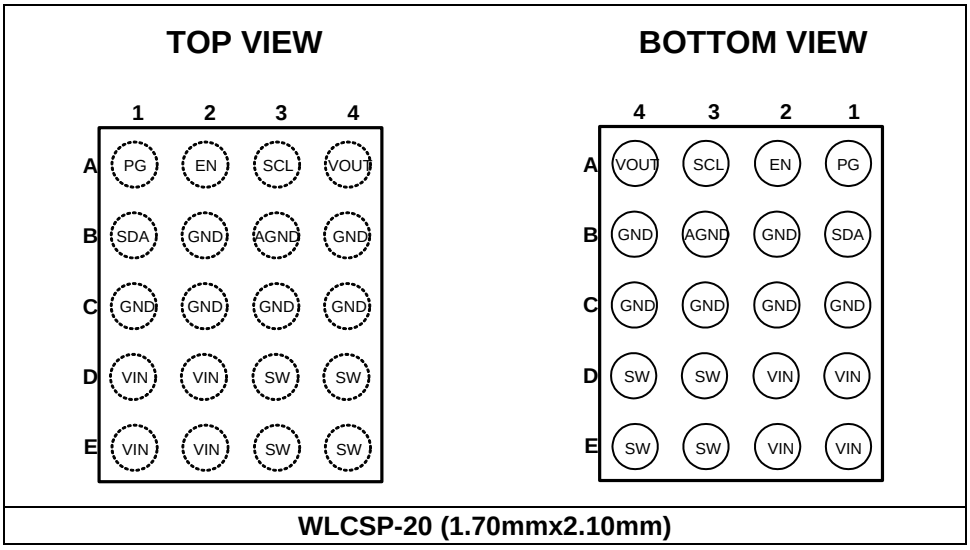
* For Tape & Reel, add suffix –Z (e.g. MP8845GC–Z)

TOP MARKING

ATY
LLL

AT: Product code of MP8845GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



WLCSP-20 (1.70mmx2.10mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to 6.5V
V_{SW} .....-0.3V (-5V for <10ns)
..... to 6.5V (8V for <10ns or 10V for <3ns)
All other pins..... -0.3V to 6.5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
WLCSP-20(1.70mmx2.10mm) 1.32W
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 2.7V to 6V
Output voltage (V_{OUT})..... 0.6V to 1.1V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

WLCSP-20(1.70mmx2.10mm)	95	30	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.7		6	V
Quiescent current(5)	I_Q	EN = 1.8V, no switching, PFM mode		280		µA
		Io = 0A, switching, PWM mode		18		mA
Shutdown current	I_S	EN = GND, T_J = 25°C			1	µA
Internal reference voltage	V_{REF}	T_J = 25°C	0.594	0.6	0.606	V
		T_J = -10°C to 70°C	0.591	0.6	0.609	
		T_J = -40°C to 125°C	0.588	0.6	0.612	
Lowest output voltage	V_{LOW}	Register = 00h, T_J = 25°C	0.594	0.6	0.606	V
		T_J = -10°C to 70°C	0.591	0.6	0.609	
		T_J = -40°C to 125°C	0.588	0.6	0.612	
Highest output voltage	V_{HIGH}	Register = 7Fh, T_J =-10°C to 70°C	1.084	1.1	1.117	V
		T_J = -40°C to 125°C	1.079	1.1	1.122	
Output voltage step	V_{STEP}			3.9		mV
High-side switch on resistance	R_{HSON}			28		mΩ
Low-side switch on resistance	R_{LSON}			17		mΩ
UVLO rising threshold	V_{UVLOR}			2.55	2.7	V
UVLO hysteretic	V_{UVLOHY}			150		mV
Switching frequency	F_{SW}		1		2.2	MHz
Frequency variation					25	%
Minimum on time(5)	T_{MINON}			60		ns
Switch leakage	I_{SW}	V_{EN} = 0V, V_{IN} = 5V, V_{SW} = 0V and 5V, T_J = 25°C			1	µA
EN input current	I_{EN}	V_{EN} = V_{IN} = 5V		5		µA
EN logic low voltage	V_{ENL}				0.4	V
EN logic high voltage	V_{ENH}		1.8			V
Power good upper-trip threshold	V_{PGH}	V_O with respect to the regulation, PG falling		110%		V_{TARGET}
Power good lower-trip threshold	V_{PGL}	V_O with respect to the regulation, PG rising		90%		V_{TARGET}
Power good pull-down voltage	V_{PGL}	I_{SINK} = 1mA			0.4	V
Power good delay	T_{PGd}			50		µs
Power good leakage	I_{PGd}				1	µA
High-side switch peak current limit (source)	I_{peak}		6	7.5	9	A
High-side switch valley current limit (5)	I_{valley}			6.5		A
Low-side switch current limit (sink) (5)		PFM mode		0		A
		PWM mode		-5		A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start time(6)	T_{SS-ON}			1.5		ms
Thermal warning(5)				130		°C
Thermal shutdown(5)				150		°C
DAC resolution				7		bits

NOTES:

5) Guaranteed by design.
6) Guaranteed by characterization.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Rise time of the SCLH or SCL signal	t_{rCL}	Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	t_{fCL}	Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of the SDAH signal	t_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Fall time of the SDAH signal	t_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Capacitance for each I/O pin	C_i		-	10	-	10	pF

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

I²C PORT SIGNAL CHARACTERISTICS

Parameter	Symbol	Condition	Cb = 100pF		Cb = 400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCL}		0	3.4	0	0.4	MHz
Set-up time for a repeated start condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time (repeated) start condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	t_{LOW}		160	-	1300	-	ns
High period of the SCL clock	t_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	t_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated start condition and after an acknowledge bit	t_{rCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	t_{fDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for stop condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a stop and start condition	T_{BUF}		160	-	1300	-	ns
Data valid time	$T_{VD;DAT}$		-	160	-	900	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH + SDA line and SCLH + SCL line	-	400	-	400	pF

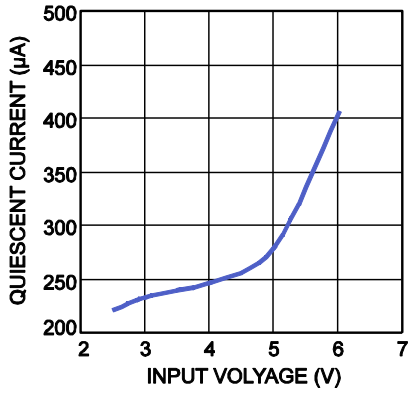
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 0.9V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

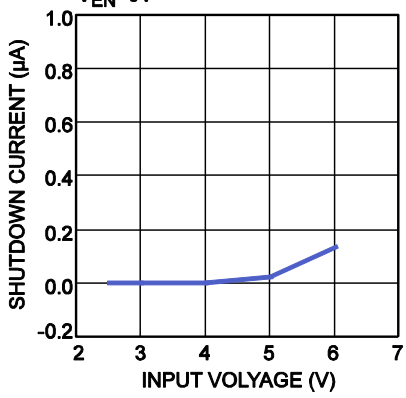
Quiescent Current vs. Input Voltage

PFM

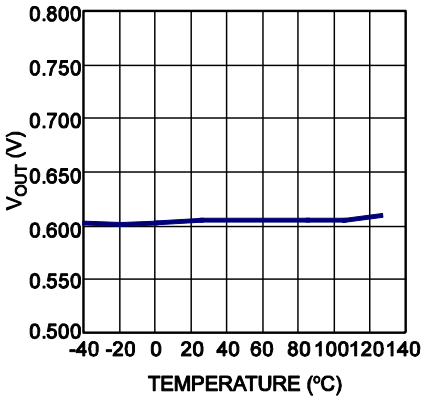


Shutdown Current vs. Input Voltage

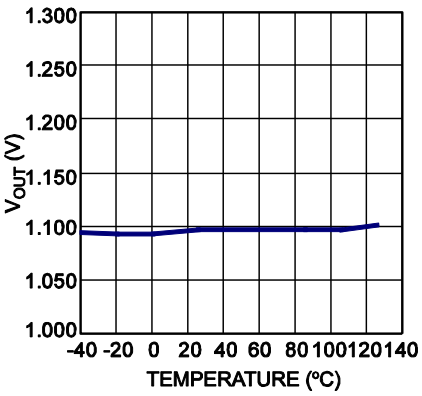
V_{EN}=0V



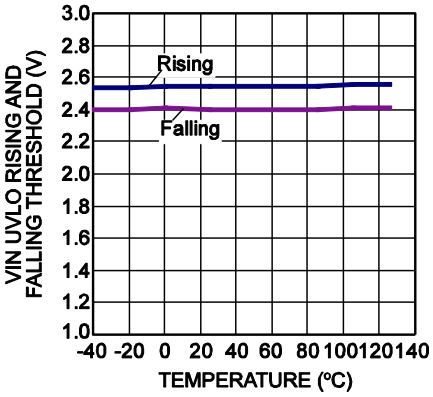
Lowest V_{OUT} vs. Temperature



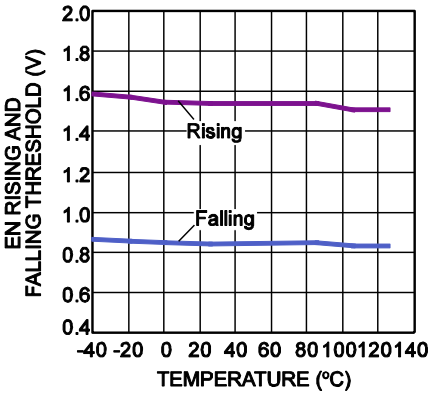
Highest V_{OUT} vs. Temperature



VIN UVLO Rising and Falling Threshold vs. Temperature

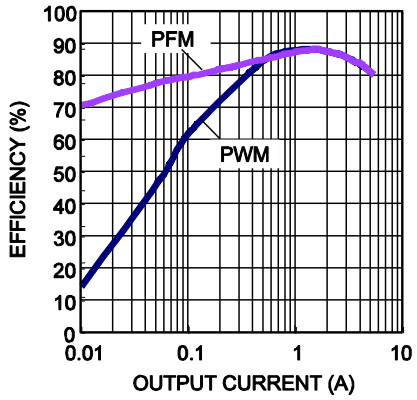


EN Rising and Falling Threshold vs. Temperature



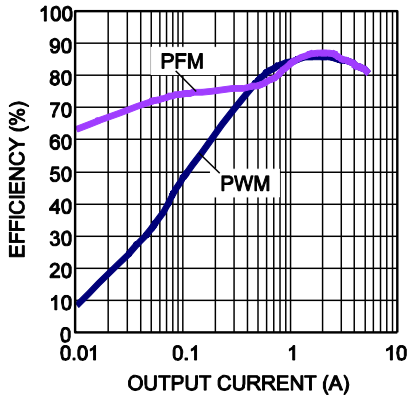
Efficiency (PFM vs. PWM)

V_{IN}=3.6V, V_{OUT}=1.1V

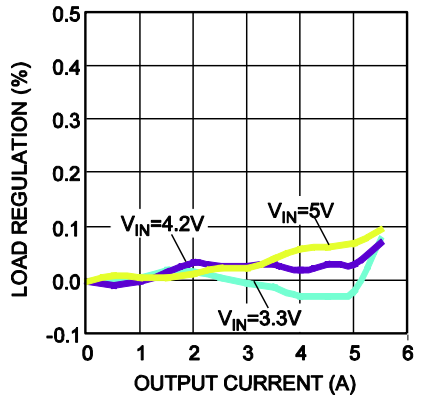


Efficiency (PFM vs. PWM)

V_{IN}=5V, V_{OUT}=1.1V



Load Regulation

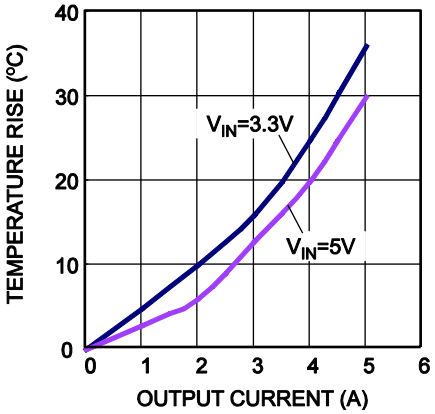


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

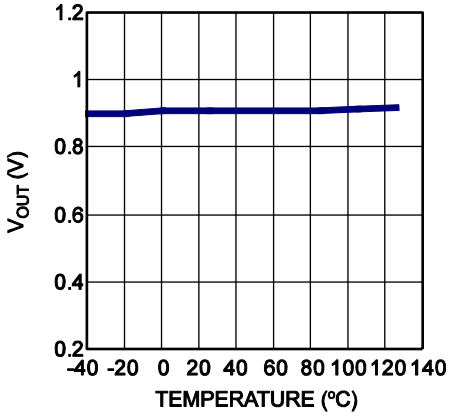
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.9V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

Case Temperature Rise



V_{OUT} vs. Temperature

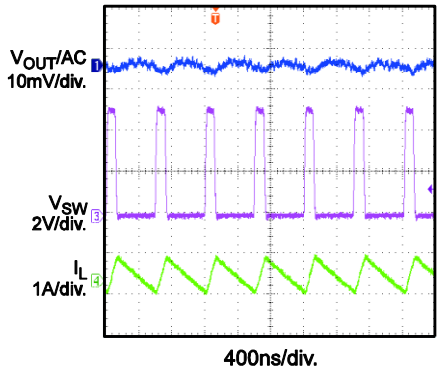


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

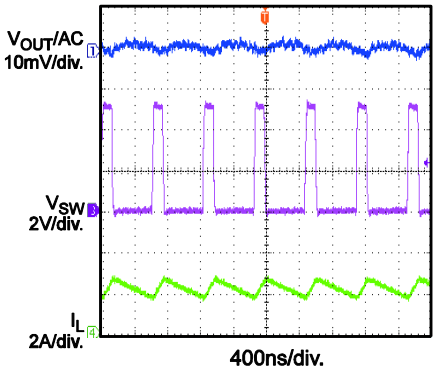
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.9V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

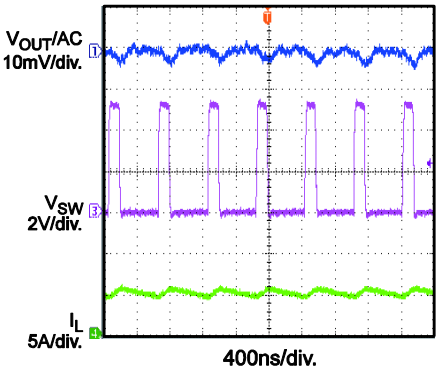
Output Ripple
I_{OUT} = 0A



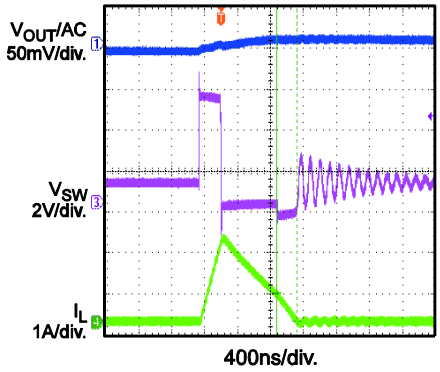
Output Ripple
I_{OUT} = 2A



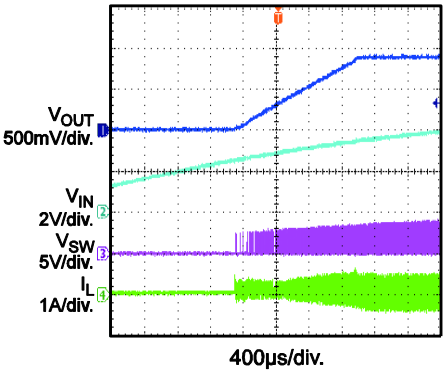
Output Ripple
I_{OUT} = 5A



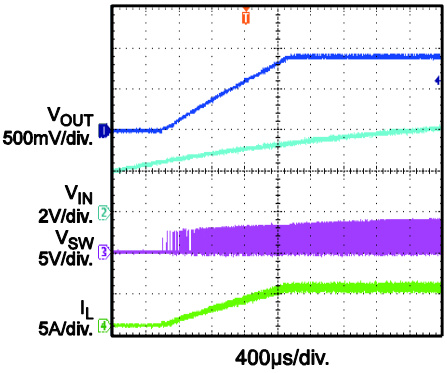
Output Ripple
PFM Mode



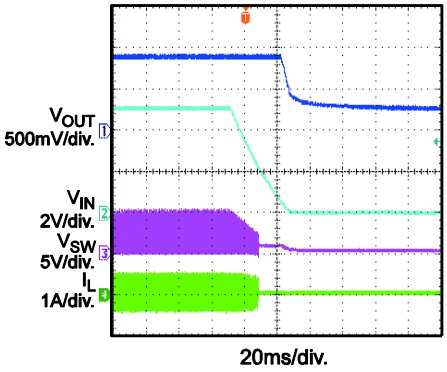
V_{IN} Power Up without Load
I_{OUT} = 0A



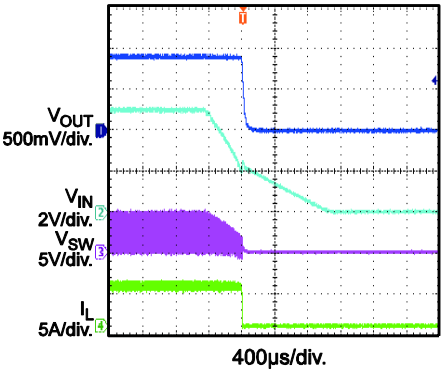
V_{IN} Power Up Full Load
I_{OUT} = 5A



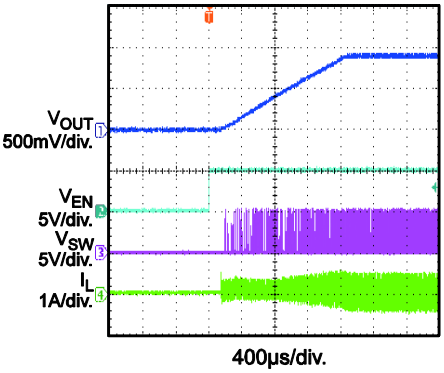
V_{IN} Power Down without Load
I_{OUT} = 0A



V_{IN} Power Down Full Load
I_{OUT} = 5A



EN On without Load
I_{OUT} = 0A



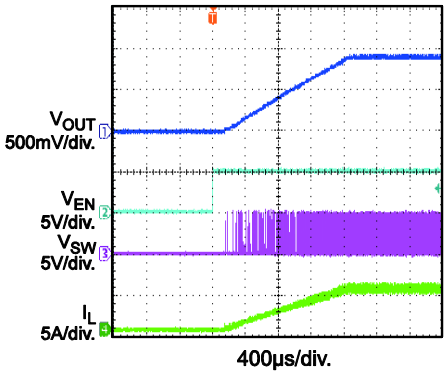
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 0.9V, L = 0.47µH, T_A = 25°C, unless otherwise noted.

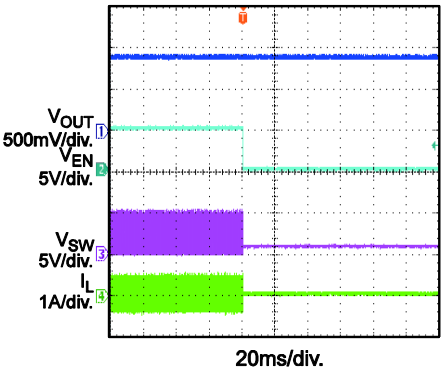
EN On with Full Load

I_{OUT} = 5A



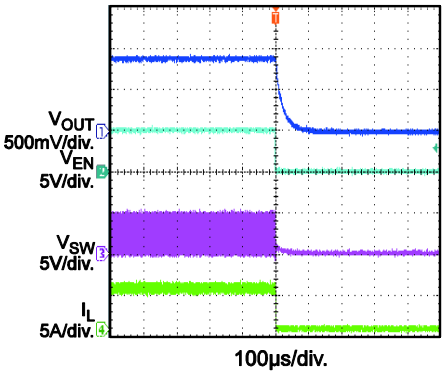
EN Down without Load

I_{OUT} = 0A



EN Down with Full Load

I_{OUT} = 5A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PIN FUNCTIONS

Package Pin #	Name	Description
A1	PG	**Power good output.**
A2	EN	**On and off control.**
A3	SCL	**I²C serial clock.**
A4	VOUT	**Output voltage sensing.**
B1	SDA	**I²C serial data.**
B2, B4, C1-C4	GND	**Power ground.**
B3	AGND	**Analog ground.**
D1, D2, E1, E2	VIN	**Input supply voltage.**
D3, D4, E3, E4	SW	**Switch node.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

REGISTERS AND DESCRIPTIONS

Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	Enable	Output reference						
01	SysCntlreg1	R/W	Switching frequency			GLFILT	Reserved	PG LO HI	VIN OVP	MODE
02	SysCntlreg2	R/W	Reserved		GO	OUT DIS	Reserved	Slew rate		
03	ID1	R	Vendor ID				Die ID			
04	ID2	R	Reserved				Die rev			
05	Status	R	ILIM	UVLO	OVP	V_OOV	V_OUV	PGOOD	OTW	ENSTAT

Default Value of Register

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	1	1	0	0	1	1	0	1
01	SysCntlreg1	R/W	0	1	0	0	1	1	0	1
02	SysCntlreg2	R/W	0	0	0	0	0	0	0	0
03	ID1	R	0	0	0	1	0	0	0	1
04	ID2	R	0	0	0	0	0	0	0	0
05	Status	R	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Register Description

1. Reg00 VSEL

NAME	BITS	DESCRIPTION
Enable	D7	I²C controlled enable bit. When EN is low, the converter is off. When EN is high, the Enable bit takes over.
Output reference	D[6:0]	Set the output voltage from 0.6V to 1.1V (see Table 1).

Table 1: Output Voltage Chart

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
000 0000	0.6000	010 0000	0.7260	100 0000	0.8520	110 0000	0.9780
000 0001	0.6039	010 0001	0.7299	100 0001	0.8559	110 0001	0.9819
000 0010	0.6079	010 0010	0.7339	100 0010	0.8598	110 0010	0.9858
000 0011	0.6118	010 0011	0.7378	100 0011	0.8638	110 0011	0.9898
000 0100	0.6157	010 0100	0.7417	100 0100	0.8677	110 0100	0.9937
000 0101	0.6197	010 0101	0.7457	100 0101	0.8717	110 0101	0.9976
000 0110	0.6236	010 0110	0.7496	100 0110	0.8756	110 0110	1.0016
000 0111	0.6276	010 0111	0.7535	100 0111	0.8795	110 0111	1.0055
000 1000	0.6315	010 1000	0.7575	100 1000	0.8835	110 1000	1.0094
000 1001	0.6354	010 1001	0.7614	100 1001	0.8874	110 1001	1.0134
000 1010	0.6394	010 1010	0.7654	100 1010	0.8913	110 1010	1.0173
000 1011	0.6433	010 1011	0.7693	100 1011	0.8953	110 1011	1.0213
000 1100	0.6472	010 1100	0.7732	100 1100	0.8992	110 1100	1.0252
000 1101	0.6512	010 1101	0.7772	100 1101	0.9031	110 1101	1.0291
000 1110	0.6551	010 1110	0.7811	100 1110	0.9071	110 1110	1.0331
000 1111	0.6591	010 1111	0.7850	100 1111	0.9110	110 1111	1.0370
001 0000	0.6630	011 0000	0.7890	101 0000	0.9150	111 0000	1.0409
001 0001	0.6669	011 0001	0.7929	101 0001	0.9189	111 0001	1.0449
001 0010	0.6709	011 0010	0.7968	101 0010	0.9228	111 0010	1.0488
001 0011	0.6748	011 0011	0.8008	101 0011	0.9268	111 0011	1.0528
001 0100	0.6787	011 0100	0.8047	101 0100	0.9307	111 0100	1.0567
001 0101	0.6827	011 0101	0.8087	101 0101	0.9346	111 0101	1.0606

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Table 1: Output Voltage Chart *(continued)*

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
001 0110	0.6866	011 0110	0.8126	101 0110	0.9386	111 0110	1.0646
001 0111	0.6906	011 0111	0.8165	101 0111	0.9425	111 0111	1.0685
001 1000	0.6945	011 1000	0.8205	101 1000	0.9465	111 1000	1.0724
001 1001	0.6984	011 1001	0.8244	101 1001	0.9504	111 1001	1.0764
001 1010	0.7024	011 1010	0.8283	101 1010	0.9543	111 1010	1.0803
001 1011	0.7063	011 1011	0.8323	101 1011	0.9583	111 1011	1.0843
001 1100	0.7102	011 1100	0.8362	101 1100	0.9622	111 1100	1.0882
001 1101	0.7142	011 1101	0.8402	101 1101	0.9661	111 1101	1.0921
001 1110	0.7181	011 1110	0.8441	101 1110	0.9701	111 1110	1.0961
001 1111	0.7220	011 1111	0.8480	101 1111	0.9740	111 1111	1.1000

2. Reg01 SysCntlreg1

NAME	BITS	DESCRIPTION			
Switching frequency	D[7:5]	D[7:5]	Switching frequency	D[7:5]	Switching frequency
		000	2.2MHz	100	1.25MHz
		001	2MHz	101	1.11MHz
		010	1.67MHz (default)	110	1MHz
		011	--	111	--
GLFILT	D4	A “0” disables the power good delay.			
Reserved	D3	Reserved.			
PG LO HI	D2	A “0” sets PGOOD to sense a negative voltage excursion of VOUT from the reference. A “1” (default) sets PGOOD to detect both a positive and negative excursion of V_O from the reference.			
VIN OVP	D1	A “1” disables the VIN OVP function. The converter continues to operate. A “0” (default) turns off the converter when VIN reaches VIN MAX.			
MODE	D0	A “0” enables PFM mode, a high disables PFM mode.			

3. Reg02 SysCntlreg2

NAME	BITS	DESCRIPTION			
Reserved	D[7:6]	Reserved.			
GO	D5	Writing to this bit starts a VOUT transition regardless of its initial value.			
OUT DIS	D4	A “0” disables the output discharge. The output voltage must be discharged by the load. A high enables the internal pull-down.			
Reserved	D3	Reserved.			
Slew rate	D[2:0]	D[2:0]	Slew Rate	D[2:0]	Slew Rate
		000	64mV/μs	100	4mV/μs
		001	32mV/μs	101	2mV/μs
		010	16mV/μs	110	1mV/μs
		011	8mV/μs	111	0.5mV/μs

4. Reg03 ID1

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	Vendor ID.
Die ID	D[3:0]	IC type.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

5. Reg04 ID2

NAME	BITS	DESCRIPTION
Reserved	D[7:4]	Reserved.
Die rev	D[3:0]	Die revision.

6. Reg05 Status

NAME	BITS	DESCRIPTION
ILIM	D7	When the bit is high, the IC is in the current limit.
UVLO	D6	When the bit is high, VIN is less than the UVLO threshold.
OVP	D5	When the bit is high, VIN is greater than the OVP threshold.
V_OOV	D4	When the bit is high, a voltage higher than 110% of regulation voltage is presented.
V_OUV	D3	When the bit is high, a voltage lower than 90% of regulation voltage is presented.
PGOOD	D2	When the bit is high, the output is in regulation; otherwise, the output voltage is out of the ±10% regulation window.
OTW	D1	When the junction temperature is higher than 130°C, the bit is high; otherwise, it is low.
ENSTAT	D0	When the bit is high, the SMPS is enabled. When the bit is low, the SMPS is disabled.

Operation Status

Condition	PG	Regulation	Latch Off	Status Bit
VIN over-voltage	Low	Off	No	OVP
VIN under-voltage	Low	Off	N/A	UVLO
Thermal warning	Low	On	No	OTW
Thermal shutdown	Low	Off	Yes	N/A
Current limit	High	On	No	ILIM
Output under-voltage (<90% of target output)	Low	Off	Yes	V_OUV
Output over-voltage (>110% of target output)	Low	On	No	V_OOV
Output over-voltage (>1.21V)	Low	Off	Yes	N/A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

BLOCK DIAGRAM

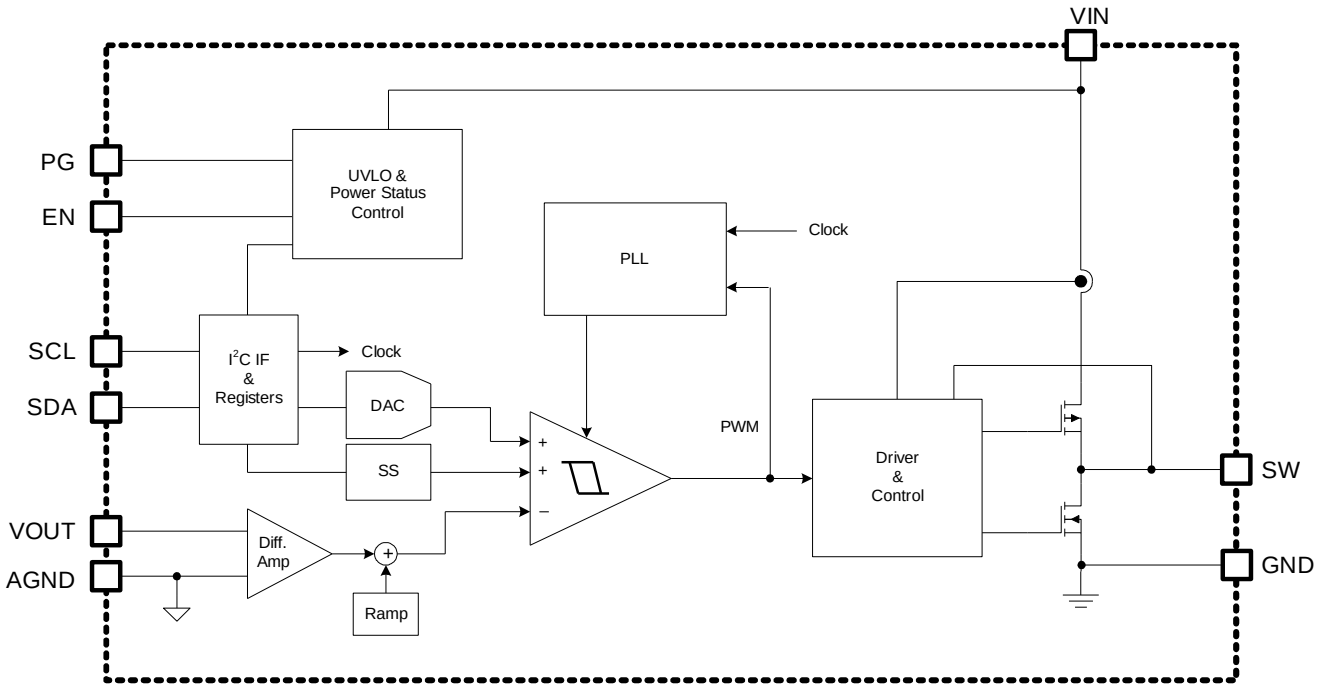


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

OPERATION

The MP8845 is a low-voltage, 5A, synchronous, step-down converter with a controllable I²C interface. The MP8845 applies MPS's patented fixed-frequency hysteretic control to utilize fast transient response of the hysteretic control and keep the switching frequency constant. No compensation is required, which simplifies the design procedure.

The MP8845 integrates an I²C-compatible interface that allows transfers up to 3.4Mbps. This communication interface can be used for dynamic voltage scaling with voltage steps down to 3.9mV with the output voltage from 0.6V to 1.1V. The voltage transition slew rate can be controlled as well.

Fixed-Frequency Hysteretic Control

Compare to fixed-frequency PWM control, hysteretic control offers the advantage of a simpler control loop and faster transient response. By using an internal phase-lock loop, the MP8845 maintains an optimal constant switching frequency across the input and output voltage ranges.

To prevent inductor current runaway during the load transient, the MP8845 fixes the minimum off time at 100ns. This minimum off time limit does not affect operation of the MP8845 in steady state in any way.

Light-Load Operation

In light load condition, the MP8845 uses a proprietary control scheme to save power and improve efficiency. The MP8845 turns off the low-side switch when the inductor current begins reversing. The MP8845 then works in discontinuous conduction mode (DCM) operation.

Enable (EN)

When the input voltage is greater than the under-voltage lockout threshold (UVLO) (typically 2.55V), the MP8845 is enabled automatically. Pull EN down to ground to disable the MP8845. There is an internal 1MΩ resistor from EN to VIN.

Soft Start (SS)

The MP8845 has a built-in soft start (SS) that ramps up the output voltage with a controlled slew rate, avoiding start-up inrush current and output voltage overshoot. The soft-start time is about 1.5ms.

Power Good (PG) Indicator

The MP8845 has an open-drain output for the power good indicator (PG). When the output voltage is within ±10% of the regulation voltage, PG is pulled up to VIN by the external resistor.

Current Limit

The MP8845 has a typical 7.5A current limit for the high-side switch. When the high-side switch reaches the current limit, the MP8845 expands the minimum off time until the current drops to 6.5A. Then the high-side switch is turned on for the next switching cycle. This prevents the inductor current from continuing to build up and damaging the components.

Thermal Protection

The MP8845 employs thermal shutdown by monitoring the junction temperature of the IC internally. If the junction temperature exceeds the thermal warning threshold (around 130°C), OTW is set. If there is no action from the system, the junction temperature continues rising until it exceeds the thermal shutdown threshold (150°C typically). After thermal shutdown, a new power start-up cycle is needed to turn on the MP8845 again.

I²C Interface

The MP8845 can communicate with the core with I²C for smart design. MPS has a GUI control (see Figure 2). The installation process and usage guidelines can be found in the MP8845 Software Guide.

I²C Address

The I²C slave address of the MP8845 is 0xC0H/0xC1H internally (see Table 2). If another slave address is needed, please contact the factory.

Table 2: I²C Slave Address

Hex	A7	A6	A5	A4	A3	A2	A1	A0
W 0xC0	1	1	0	0	0	0	0	R/
R 0XC1	1	1	0	0	0	0	0	W
Address	0x60							

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

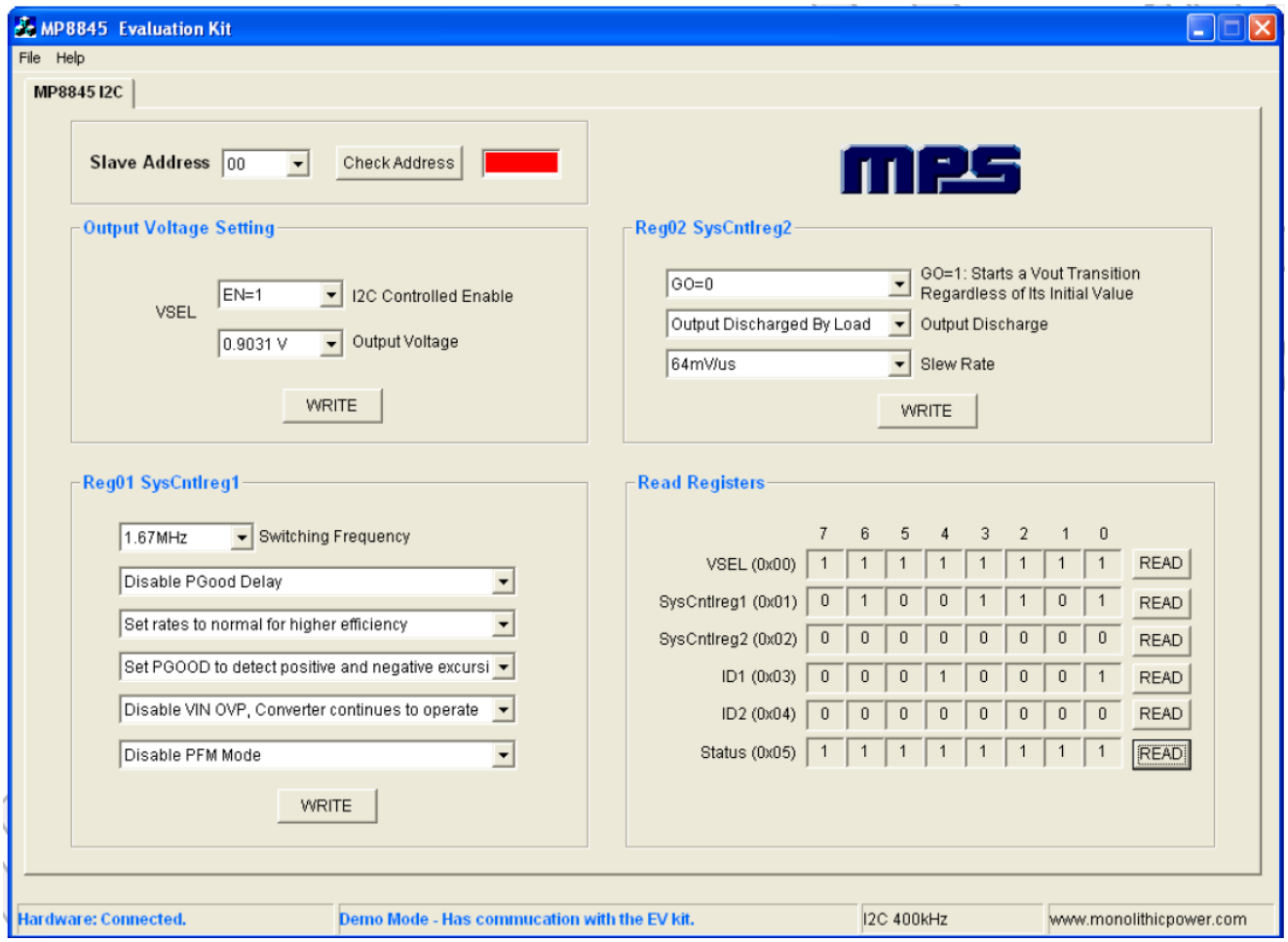


Figure 2: MP8845 Control Interface

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

I²C Enable

Just as EN of the MP8845 can start up and shut down the converter, so can EN of the I²C control the converter. The Reg00 VSEL D7 bit is I²C-controlled enabled. When writing D7 = 0, the converter is off. When writing D7 = 1, the converter is on. Both the external EN and I²C EN can control the converter. The converter works only when both EN pins are high.

Output Voltage Select

The MP8845 output voltage is I²C-programmable. There is no need to set feedback resistors to achieve different output voltages. The default output voltage is 0.9031V but can be set from 0.6V to 1.1V in 3.9mV steps by the I²C.

The process of changing the output voltage is:

1. Write the GO bit (Reg 02 Sycntlreg2 [D5]) to 1. This action means the output voltage can be set to another value that is not the default VOUT voltage.
2. Write the output reference bit (Reg00 VSEL [D6:D0]). The output voltage can be changed according to Table 1.

Switching Frequency

The default switching frequency of the MP8845 is 1.67MHz. However, the frequency can also be changed based on the application. By writing the switching frequency bits (Reg01 SysCntlreg1 [D7:D5], the switching frequency can be programmed as one of six possible values. Their corresponding data can be found in Section 2: Reg01 SysCntlreg1.

PGOOD Configuration

The MP8845 has an option to use the PG LO HI function. This function can be written in the PG LO HI bit (Reg01 Syscntlreg1 [D2]). The default value is 1. PGOOD senses both a positive and negative excursion of VOUT from the reference. If writing this bit to 0, PGOOD only senses a negative voltage excursion of VOUT from the reference.

Input Over-Voltage Protection (OVP)

The MP8845 has an option to use the VIN OVP function. This function can be written through the VIN OVP bit (Reg01 Syscntlreg1 [D1]). The default value is 0, in which the VIN OVP function is enabled. When VIN is higher than 6.1V, the converter is disabled. After VIN recovers to 5.8V, the converter restarts. If the VIN OVP bit is set to 1, VIN OVP is disabled. The converter will not stop, even if VIN exceeds its safe range.

PFM Mode Select

The MP8845 has auto-continuous conduction mode (CCM) and pulse frequency modulation (PFM) mode. Writing the MODE bit (Reg01 Syscntlreg1 [D0]) can change the work mode. The default value of the MODE bit is 1, in which auto-CCM is selected. Considering high efficiency at light load, PFM mode is recommended. Set the MODE bit to 0 to enable PFM mode.

Output Discharge

The MP8845 has an output discharge function. Write the OUT DIS bit (Reg02 SysCntlreg2 [D4]) to change the output discharge mode. The default value is 0 and discharges VOUT by its load when EN is low. Writing D4 = 1 can enable the function, and then the output voltage can be discharged by the internal pull-down resistance.

Output Voltage Transition Slew Rate

When the output voltage transits from low to high or from high to low, the transition slew rate can differ. There are eight possible values for selection. Through writing the Slew Rate bits (Reg02 Syscntlreg2 [D2:D0]), the transition slew rate can be set at one possible value based on the application. The internal reference follows the set slew rate, but the output voltage slew rate does not always follow the internal reference. Considering the output capacitor and inductor, the actual output voltage slew rate should be a little slower.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. For higher output voltages, a 47µF capacitor may be needed for more system stability.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (1):

$$I_C = I_{LOAD}\sqrt{\frac{V_{OUT}}{V_{IN}}(1-\frac{V_{OUT}}{V_{IN}})} \quad (1)$$

The worst-case condition occurs at VIN = 2VOUT, shown in Equation (2):

$$I_C = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e.: 0.1µF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}}(1-\frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Selecting the Output Capacitor

The output capacitor (C2A, C2B) is required to maintain the DC output voltage. Low ESR ceramic capacitors can be used with the MP8845 to keep the output ripple low. Generally, a 47µF output ceramic capacitor is sufficient for most cases. In higher output voltage conditions, more ceramic capacitors may be needed for a more stable system. A larger output capacitor can achieve a smaller output voltage ripple. When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (4):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_g^{\,2} \times L_1 \times C2}(1-\frac{V_{OUT}}{V_{IN}}) \quad (4)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1}(1-\frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (5)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout of the switching power supplies and the high-switching converter especially is critical for stable operation. If the layout is not done carefully, the regulator could show poor line or load regulation and stability issues. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the high-speed, step-down regulator and the input capacitor as close to the IC pins as possible.
   Figure 3 shows a size 0805 ceramic capacitor.
2. Connect the two ends of the ceramic capacitor to VIN and GND directly.
   A 0603 size decoupling ceramic capacitor is strongly recommended.

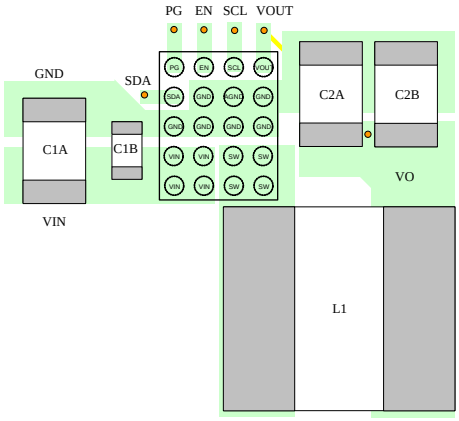


Figure 3: Recommend Layout

Design Example

Table 3 is a design example following the application guidelines for the specifications below.

Table 3: Design Example

V_{IN}	5V
V_{OUT}	0.9V
I_{OUT}	5A

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheet.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

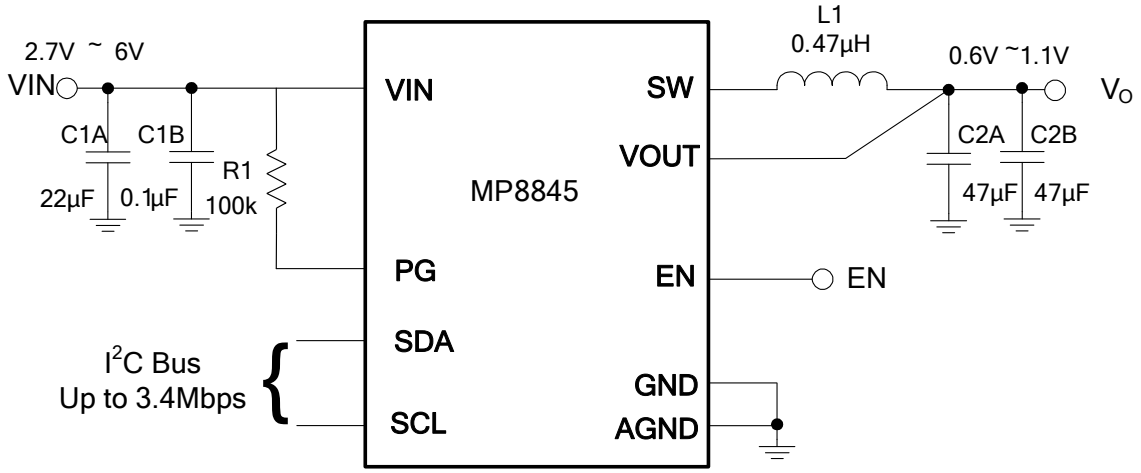
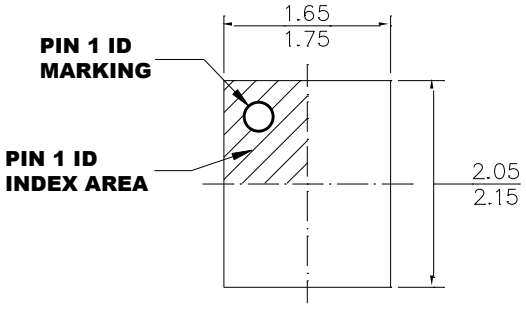


Figure 4: Typical Application Circuit

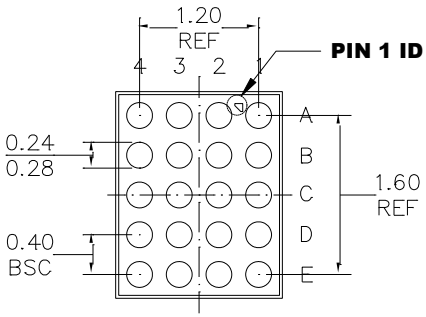
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PACKAGE INFORMATION

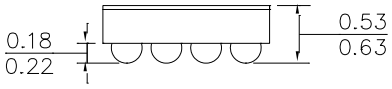
WLCSP-20 (1.70mmx2.10mm)



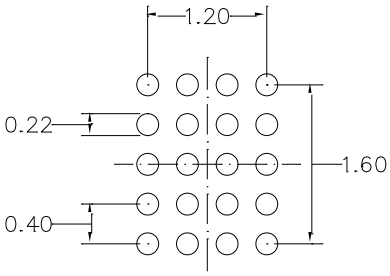
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.