MP8795H

16V, 20A, Synchronous, Step-Down Converter with Adjustable Current Limit, Programmable Frequency, and Voltage Tracking

DESCRIPTION

The MP8795H is a fully integrated, high-frequency, synchronous, buck converter. The MP8795H offers a very compact solution that achieves up to 20A of output current with excellent load and line regulation over a wide input supply range. The MP8795H operates at high efficiency over a wide output current load range.

The MP8795H adopts an internally compensated constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz easily with MODE pin configuration, allowing the MP8795H frequency to remain constant regardless of the input and output voltages.

The output voltage start-up ramp is controlled by an internal 1ms timer and can be increased by adding a capacitor on REF/TRK. An open-drain power good (PGOOD) signal indicates if the output is within its nominal voltage range or not. PGOOD is clamped at around 0.7V with an external pull-up voltage when the input supply fails to power the MP8795H.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP8795H requires a minimal number of readily available, standard, external components and is available in a QFN-21 (3mmx4mm) package.

FEATURES

- Wide Input Voltage Range
  - 2.7V to 16V with External 3.3V VCC Bias
  - 4V to 16V with Internal Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- Programmable Accurate Current Limit Level
- 20A Output Current
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Adaptive COT for Ultrafast Transient Response
- Stable with Zero ESR Output Capacitor
- Forced CCM Operation
- Excellent Load Regulation
- Output Voltage Tracking
- PGOOD Active Clamped at Low Level during Power Failure
- Programmable Soft-Start Time from 1ms
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, OVP, UVP, UVLO, and Thermal Shutdown.
- Output Adjustable from 0.6V to 90% * VIN, up to 5.5V Max
- Available in a QFN-21 (3mmx4mm) Package

APPLICATIONS

- FPGAs
- Flat-Panel televisions and Monitors
- Multi-Functional Printers
- Access Points and Routers
- Optical Modules

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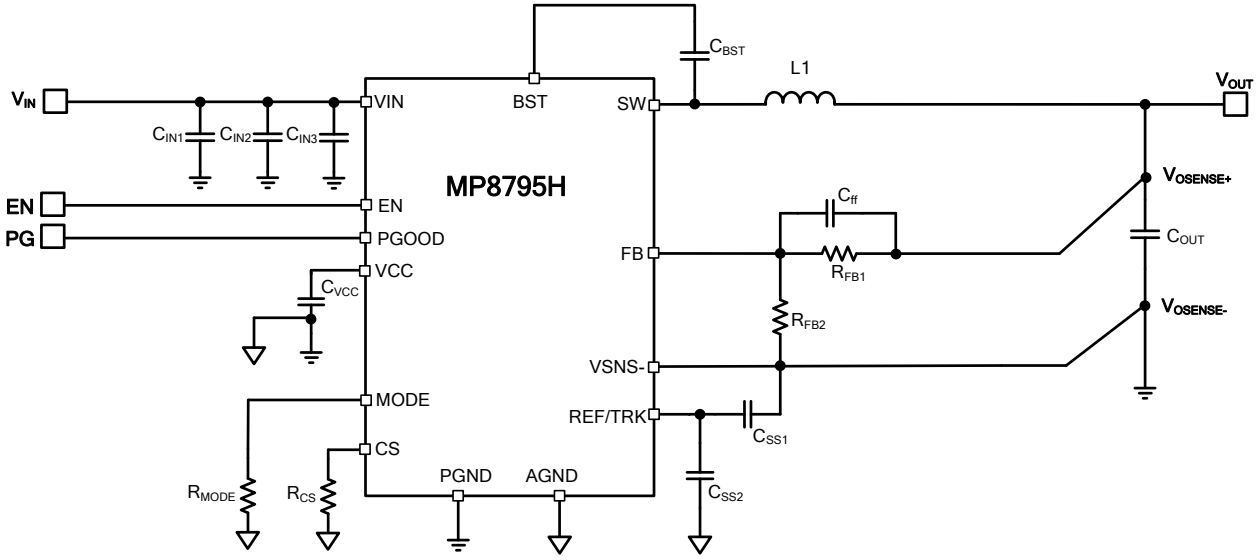
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP8795HGLE*	QFN-21 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MP8795HGLE–Z).

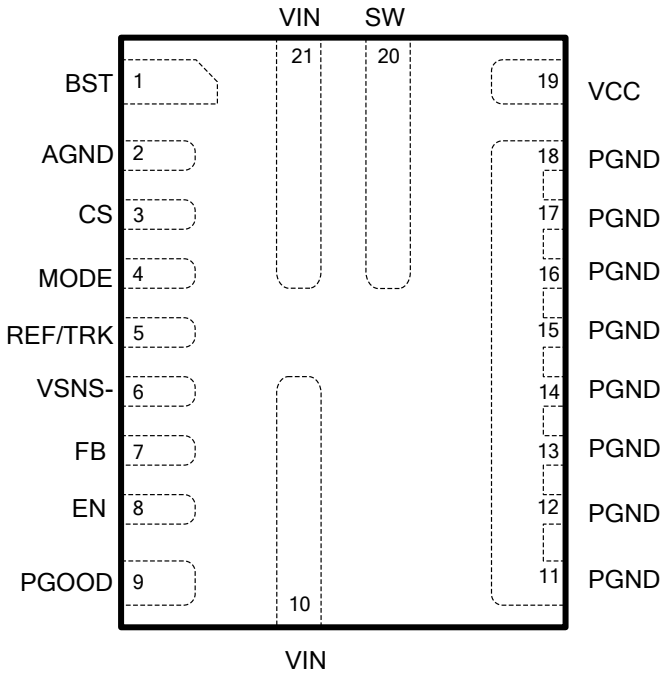
TOP MARKING

MPYW
8795
HLLL
E

MP: MPS prefix
Y: Year code
W: Week code
8795H: Part number
LLL: Lot number
E: Package prefix

PACKAGE REFERENCE

TOP VIEW



QFN-21 (3mmx4mm)

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PIN FUNCTIONS

PIN #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
2	AGND	**Analog ground.** Select AGND as the control circuit reference point.
3	CS	**Current limit.** Connect a resistor to AGND to set the current limit trip point.
4	MODE	**Operation mode selection.** Program MODE to select the operating switching frequency. See Table 1 for additional details.
5	REF/TRK	**External tracking voltage input.** Decouple REF/TRK with a ceramic capacitor placed as close to it as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time. See Equation 2 for additional details.
6	VSNS-	**Differential remote sense negative input.** Connect VSNS- to the negative side of the voltage sense point directly. Short VSNS- to GND if the remote sense is not used.
7	FB	**Feedback (differential remote sense positive input).** An external resistor divider from the output to VSNS- tapped to FB sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	**Enable.** EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
9	PGOOD	**Power good output.** PGOOD is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate a logic high signal if the output voltage is within regulation. There is a delay of about 0.9ms between the time FB becomes greater than or equal to 92.5% and the time PGOOD pulls high.
10, 21	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
11-18	PGND	**System ground.** PGND is the reference ground of the regulated output voltage and requires careful consideration during the PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The driver and control circuits are powered by the VCC voltage. Decouple VCC with a ceramic capacitor at least 1µF placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on time of the PWM duty cycle. The inductor current drives SW low during the off time. Use wide PCB traces to make the connection.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
$V_{SW(DC)}$ ..... -0.3V to V_{IN} + 0.3V
V_{SW} (25ns) (2) ..... -3V to 25V
V_{SW} (25ns) ..... -5V to 25V
V_{BST} ..... -0.3V to 22.3V
V_{CC}, EN 4.5V
All other pins ..... -0.3V to 4.3V
Junction temperature ..... 170°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +170°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
$V_{IN(DC)}$ - $V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
$V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
External VCC bias (V_{CC_EXT}) ..... 3.12V to 3.6V
Maximum output current (I_{OUT_MAX}) 20A
Maximum output current limit (I_{OC_MAX}) 24A
Maximum peak inductor current (I_{L_PEAK}) 28A
EN voltage (V_{EN}) 3.6V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-21 (3mmx4mm)			
EV8795H-LE-00A (5)	29	4	°C/W
JESD51-7 (6)	50	12	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) Measured using a differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) The voltage rating can be in the range of -3V to 23V for a period of 25ns or less with a maximum repetition rate of 1000kHz when the input voltage is 16V.
5) Measured on EV8795H-LE-00A, 4-layer PCB, 78mm x 81mm.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		10	20	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 0.62V		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS}/I_{OUT}	I_{OUT} ≥ 2A	9	10	11	μA/A
Low-side negative current limit	I_{LIM_NEG}			-18		A
Negative current limit time out (7)	t_{NCL_Timer}			200		ns
Switching Frequency						
Switching frequency	f_{SW}	MODE = AGND, I_{OUT} = 0A, V_{OUT} = 1V@25°C	450	600	750	kHz
		MODE = 30.1kΩ to AGND, I_{OUT} = 0A, V_{OUT} = 1V@25°C	650	800	950	kHz
		MODE = 60.4kΩ to AGND, I_{OUT} = 0A, V_{OUT} = 1V@25°C	800	1000	1200	kHz
Minimum on time (7)	T_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time (7)	T_{OFF_MIN}	V_{FB} = 500mV			180	ns
Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft Start						
Feedback voltage	V_{REF}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	mV
REF/TRK sourcing current	I_{TRACK_Source}	$V_{REF/TRK}$ = 0V		42		μA
REF/TRK sinking current	I_{TRACK_Sink}	$V_{REF/TRK}$ = 1V		12		μA
Soft-start time	$t_{REF/TRK}$	C_{TRACK} = 1nF, T_J = +25°C	0.75	1	1.25	ms
Error Amplifier						
Error amplifier offset	V_{OS}		-3	0	3	mV
Feedback current	I_{FB}	V_{FB} = REF		50	100	nA
Enable and UVLO						
Enable input rising threshold	VIH_{EN}		1.17	1.22	1.27	V
Enable hysteresis	$V_{EN\text{-}HYS}$			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VIN UVLO						
VIN under-voltage lockout threshold rising	VIN_{Vth_Rise}	V_{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout threshold falling	VIN_{vth_Fall}		1.55	1.85	2.15	
VCC Regulator						
VCC under-voltage lockout threshold rising	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold falling	VCC_{vth_Fall}		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		Icc = 25mA		0.5		%
Power Good						
Power good high threshold	$PG_{Vth_Hi_Rise}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{Vth_Lo_Rise}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth_Lo_Fall}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low to high delay	PG_{Td}	T_J = 25°C	0.63	0.9	1.17	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.5	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	µA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor@25°C		650	800	mV
	V_{OL_10}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor@25°C		750	900	mV
Thermal Protection						
Thermal shutdown (7)	T_{SD}			160		°C
Thermal shutdown hysteresis (7)				30		°C

NOTE:

7) Guaranteed by design.

8) Guaranteed by design over temperature.

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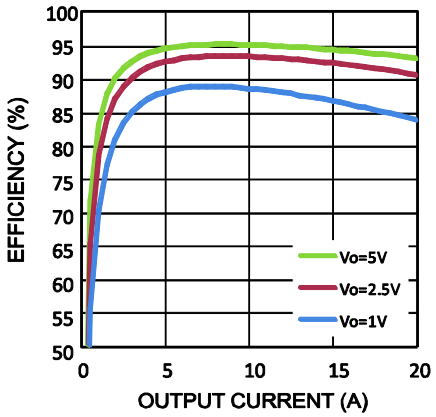
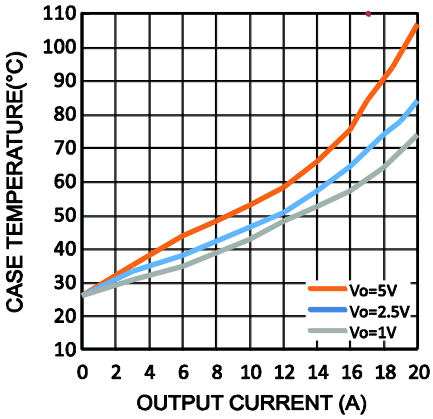
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

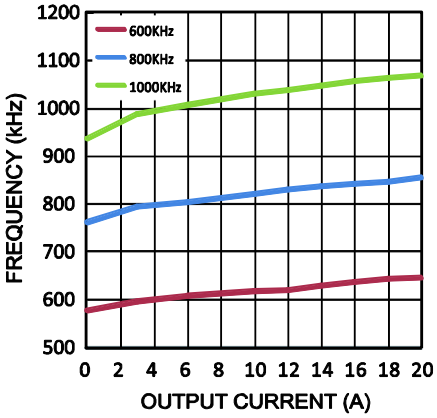
Efficiency
L=0.4µH, 800kHz



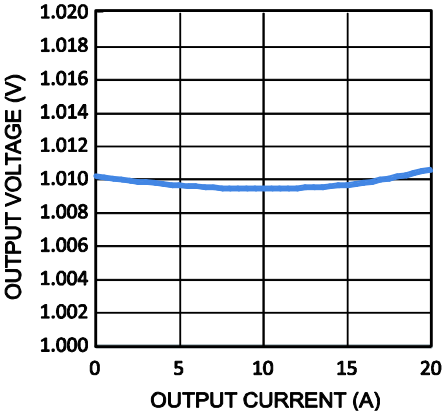
Thermal Results
800kHz, No Air-Flow



Switching Frequency vs. Output Current



Output Voltage Load Regulation



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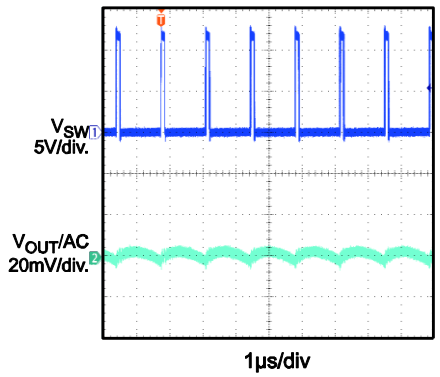
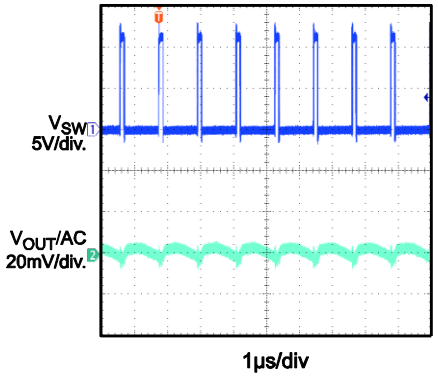
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

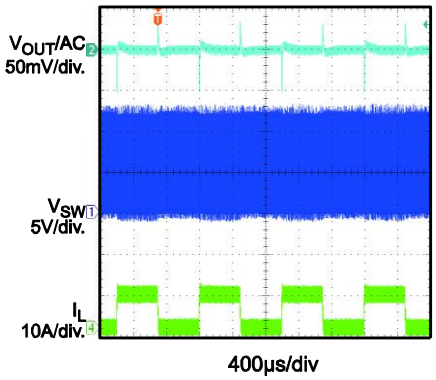
Steady State
I_{OUT} = 0A



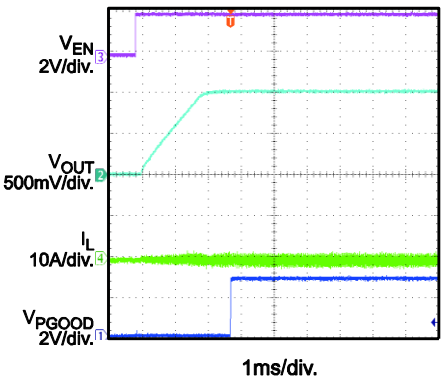
Steady State
I_{OUT} = 20A



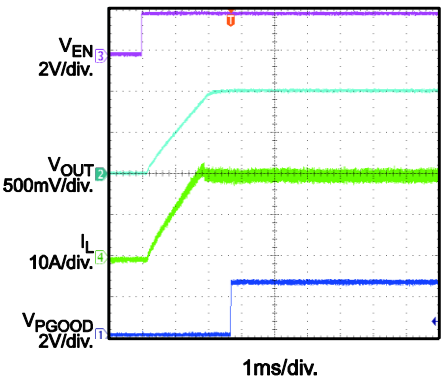
Load Transient
I_{OUT}=0A~8A



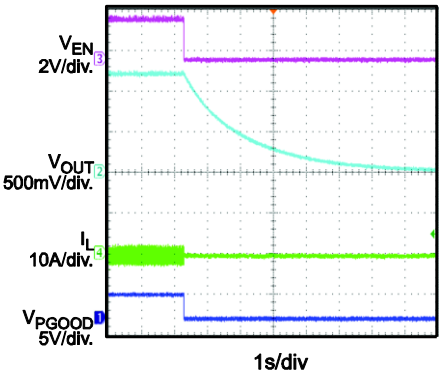
Power Up through EN
I_{OUT} = 0A



Power Up through EN
I_{OUT} = 20A



Power Down through EN
I_{OUT}=0A



Power Down through EN
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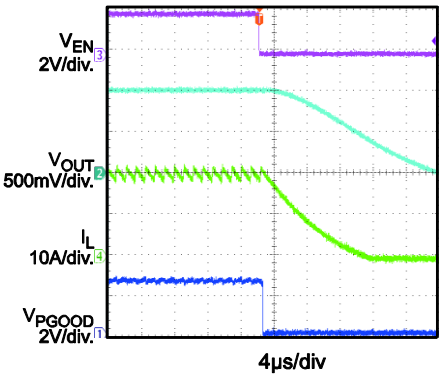
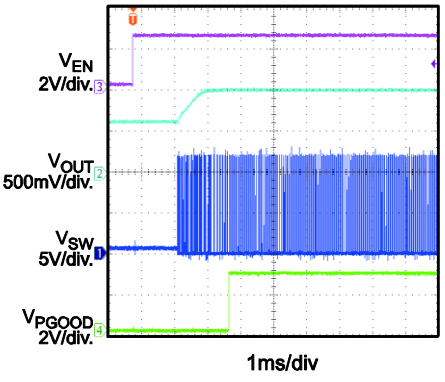
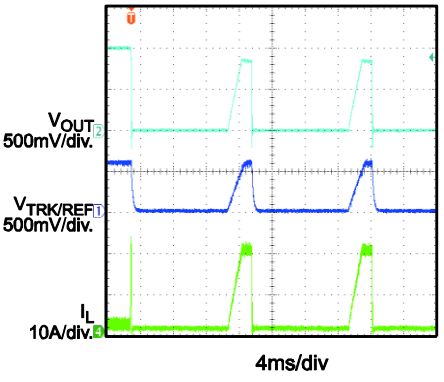


Pre-bias Start-Up



Over-Current
Protection Entry



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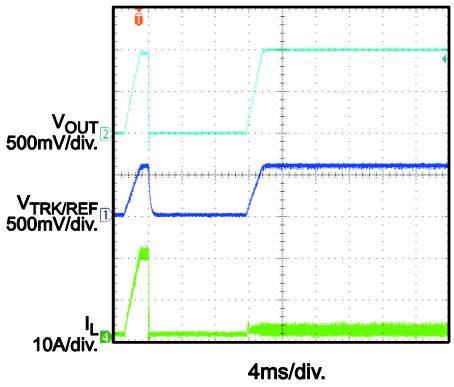
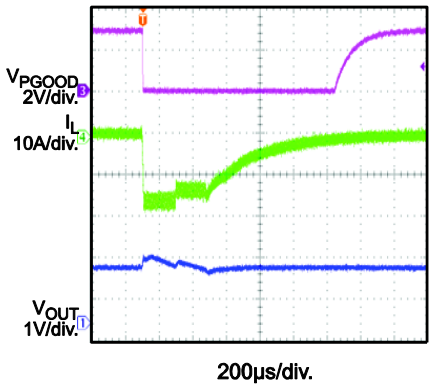
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

Over-Current
Protection Recovery



Over-Voltage Protection



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BLOCK DIAGRAM

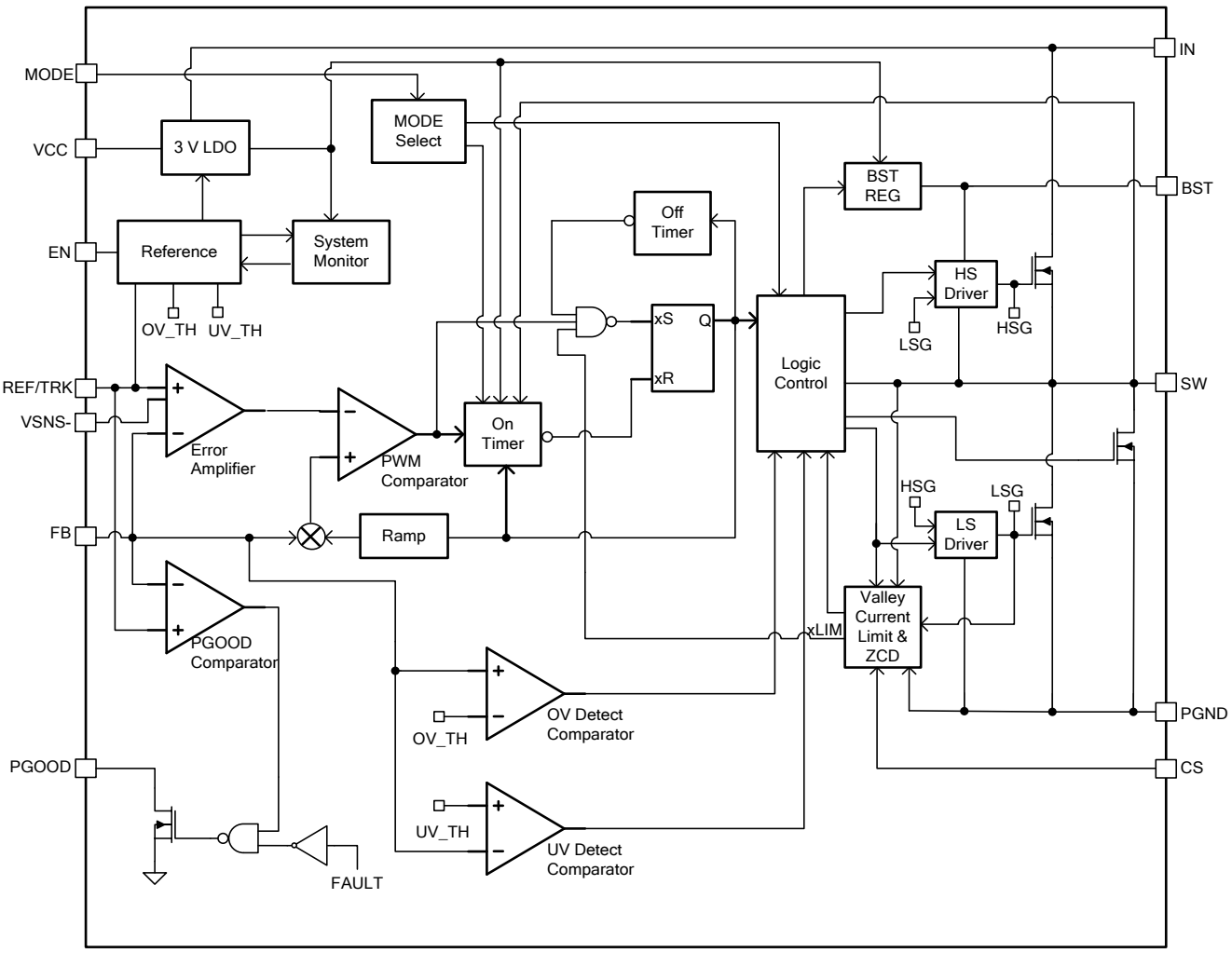

Figure 1: Functional Block Diagram

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OPERATION

Constant-on-Time (COT) Control

The MP8795H employs constant-on-time (COT) control to achieve a fast load transient response. Figure 2 shows the details of the control stage of the MP8795H.

The operational amplifier (AMP) corrects any error voltage between FB and VREF. The MP8795H can use AMP to provide excellent load regulation over the entire load range.

The dedicated VSNS- pin helps provide differential output voltage remote sensing. The remote sense trace pair should be kept at low impedance for the best performance.

The MP8795H uses internal RAMP compensation to support a low ESR MLCC output capacitor solution. The adaptive internal RAMP is optimized so that the MP8795H is stable in the entire operating input and output voltage ranges with a proper design of the output L/C filter.

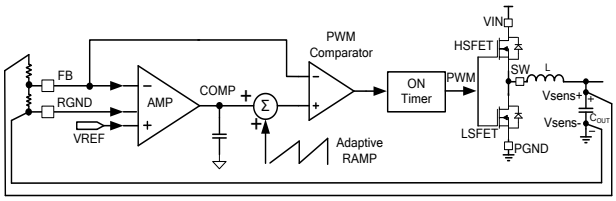

Figure 2: COT Control

Pulse-Width Modulation (PWM) Operation

Figure 3 shows the generation of the pulse-width modulation (PWM) signal. AMP corrects any error between FB and REF and generates a fairly smooth DC voltage (COMP). The internal RAMP is superimposed onto COMP, which is compared with the FB signal. Whenever FB drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) is turned on. The HS-FET remains on for a fixed turn-on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off and turns on again when FB drops below the superimposed COMP. By repeating this operation, the MP8795H regulates the output voltage.

The MP8795H operates in forced continuous conduction mode (CCM). In CCM operation, the switching frequency is fairly constant (PWM mode), and the output ripple remains almost constant throughout the entire load range. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

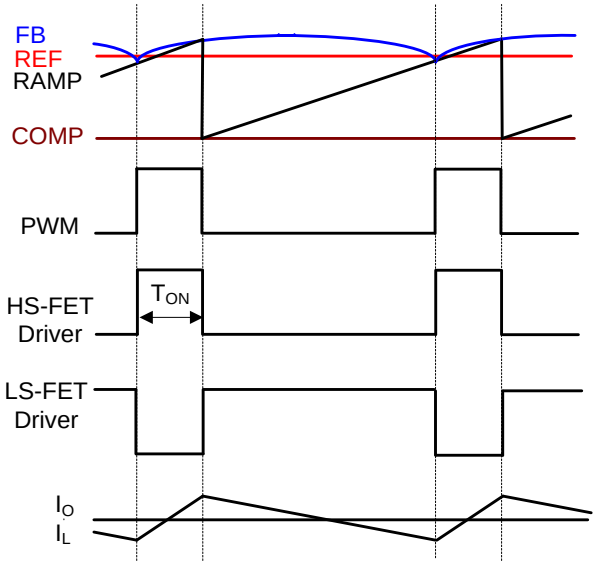

Figure 3: Heavy-Load Operation (PWM)

Mode Selection

The MP8795H provides forced CCM operation over the entire load range. The MP8795H has three selectable switching frequency options: 600kHz, 800kHz, and 1000kHz. Selecting a switching frequency is done by setting the resistance value of the resistor connected between MODE and AGND (see Table 1).

Table 1: MODE Selection

MODE	Switching Frequency
GND	600kHz
30.1kΩ (±20%) to GND	800kHz
60.4kΩ (±20%) to GND	1000kHz

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Soft Start (SS)

The minimum soft-start time is limited at 1ms and can be increased by adding a SS capacitor between REF/TRK and VSNS-.

The total SS capacitor value can be determined with Equation (1):

$$C_{SS}(nF) = \frac{t_{ss}(ms) \times 36\mu A}{0.6(V)} \quad (1)$$

Output Voltage Tracking and Reference

The MP8795H provides an analog input pin (REF/TRK) to track another power supply or accept an external reference. When an external voltage signal is connected to REF/TRK, it acts as a reference for the MP8795H output voltage. The FB voltage follows this external voltage signal exactly, and the soft-start settings are ignored. The REF/TRK input signal can be in the range of 0.3 - 1.4V. During the initial start-up, the REF/TRK must reach at least 600mV first to ensure proper operation. After that, it can be set to any value between 0.3V and 1.4V.

Pre-Bias Start-Up

The MP8795H is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the SS capacitor exceeds the sensed output voltage at FB. Before the REF/TRK voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop in the pre-biased level is negligible.

Current Sense and Over-Current Protection (OCP)

The MP8795H features an on-die current sense and a programmable positive current limit threshold.

The current limit is active when the MP8795H is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, the V_{CS} voltage is proportional to the SW current cycle-by-cycle. The HS-FET is allowed to turn on only when V_{CS} is below the internal over-current protection (OCP) voltage threshold (V_{OCP}) during the LS-FET on state to limit the SW valley current cycle-by-cycle.

Calculate the current limit threshold setting from R_{CS} with Equation (2):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_s})} \quad (2)$$

Where V_{OCP} = 1.2V, G_{CS} = 10μA/A, and I_{LIM} is the desired output current limit (A).

OCP hiccup becomes active 3ms after the MP8795H is enabled. Once the OCP hiccup is active, if the MP8795H detects an over-current condition for 31 consecutive cycles or if FB drops below the under-voltage protection (UVP) threshold, the device enters hiccup mode. In hiccup mode, the MP8795H latches off the HS-FET immediately and latches off the LS-FET after ZCD is detected. Meanwhile, the SS capacitor is also discharged. After about 11ms, the MP8795H attempts to soft start automatically. If the over-current condition still remains after 3ms, the MP8795H repeats this operation cycle until the over-current condition is removed and the output voltage rises back to the regulation level smoothly.

Negative Inductor Current Limit

When the LS-FET detects a -18A current, the MP8795H turns off the LS-FET for 200ns to limit the negative current.

Over-Voltage Protection (OVP)

The MP8795H monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides hiccup over-voltage protection (OVP).

If the FB voltage exceeds 116% of the REF voltage, OVP is triggered. The LS-FET remains on until it triggers the low-side negative current limit (NOCP). Once the LS-FET triggers NOCP, the LS-FET is turned off for 200ns, and the HS-FET is turned on during this period. After 200ns, the LS-FET is turned on again. The MP8795H repeats this operation to discharge any over-voltage on the output. The MP8795H exits this mode when the feedback voltage drops below 105%*REF.

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Over-Temperature Protection (OTP)

The MP8795H has over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the MP8795H latches off the HS-FET immediately and latches off the LS-FET after the ZCD is detected. Meanwhile, the SS capacitor is also discharged. Once the junction temperature drops to about 130°C, a soft start is initiated. The OTP function is effective once the MP8795H is enabled.

Output Voltage Setting and Remote Output Voltage Sensing

First, choose a value for R_{FB1}. Then R_{FB2} can be determined with Equation (3):

$$R_{FB2}(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_{FB1}(k\Omega) \quad (3)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) should be placed in parallel with R_{FB1}. R_{FB1} and C_{FF} add an extra zero to the system, which improves loop response. R_{FB1} and C_{FF} are selected so that the zero formed by R_{FB1} and C_{FF} is located around 20 ~ 60kHz. Calculate this zero with Equation (4):

$$f_Z = \frac{1}{2\pi \times R_{FB1} \times C_{FF}} \quad (4)$$

Power Good (PGOOD)

The MP8795H has a power good output pin (PGOOD). PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source less than 3.6V through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PGOOD is pulled to GND before SS is ready. After the FB voltage reaches 92.5% of the REF voltage, PGOOD is pulled high after a 0.9ms delay.

When the FB voltage drops to 80% of the REF voltage or exceeds 116% of the nominal REF voltage, PGOOD is latched low. PGOOD can only be pulled high again after a new SS.

If the input supply fails to power the MP8795H, PGOOD is clamped low, even though PGOOD is tied to an external DC source through a pull-up resistor. The relationship between the PGOOD voltage and the pull-up current is shown in Figure 4.

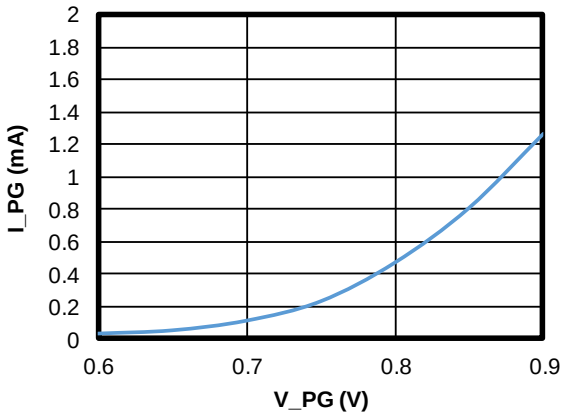

Figure 4: PGOOD Clamped Voltage vs. Pull-Up Current

Enable (EN) Configuration

The MP8795H turns on when EN goes high. The MP8795H turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MP8795H. The MP8795H provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage, at which the MP8795H is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible UVLO bouncing during power-up and power-down. The resistor divider values can be determined with Equation (5):

$$V_{IN_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (5)$$

Where VIH_{EN} is 1.22V, typically.

R_{UP} and R_{DOWN} should be chosen so that V_{EN} does not exceed 3.6V when VIN reaches its maximum value.

EN can also be connected to VIN directly through a pull-up resistor (R_{UP}). R_{UP} should be chosen so that the maximum current going to EN is 50μA. R_{UP} can be calculated with Equation (6):

$$R_{UP}(K\Omega) = \frac{VIN_{MAX}(V)}{0.05(mA)} \quad (6)$$

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APPLICATION INFORMATION

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (7):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (9):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (10):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (10)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors. Estimate the output voltage ripple with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (11)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For simplification, the output ripple can be approximated with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (13)$$

Selecting the Inductor

The inductor supplies a constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical size, a higher series resistance, and a lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current to be 30 - 40% of the maximum switch current limit. Design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (15):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best performance, refer to Figure 5 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP8795H.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Place as many PGND vias as possible as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the BST capacitor as close to BST and SW as possible with traces 20 mil or wider to route the path. It is recommended to use a bootstrap capacitor 0.1 - 1µF.
8. Place the SS capacitor close to REF/TRK to VSNS-.
9. Place vias at least 10mm away from the positive side of the first input decoupling capacitor close to the IC if they must be placed on the PGOOD pad.

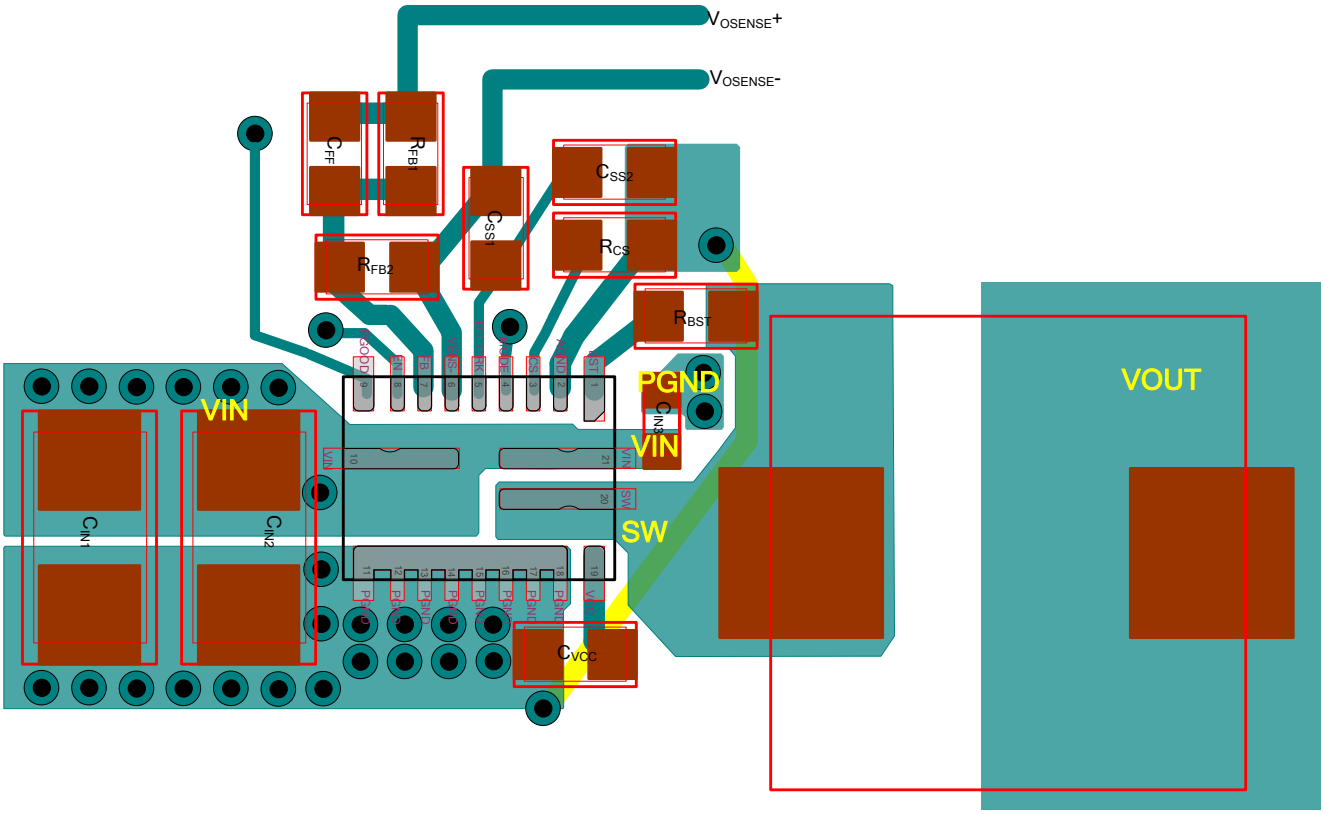

Figure 5: Recommended PCB Layout

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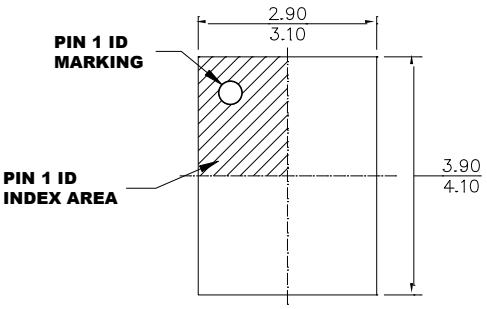
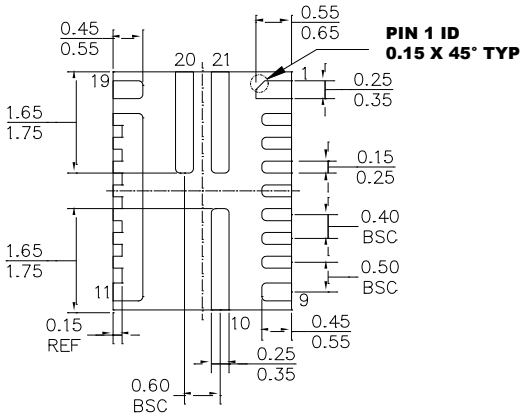
PACKAGE INFORMATION

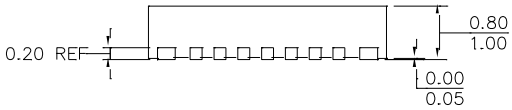
QFN-21 (3mmx4mm)



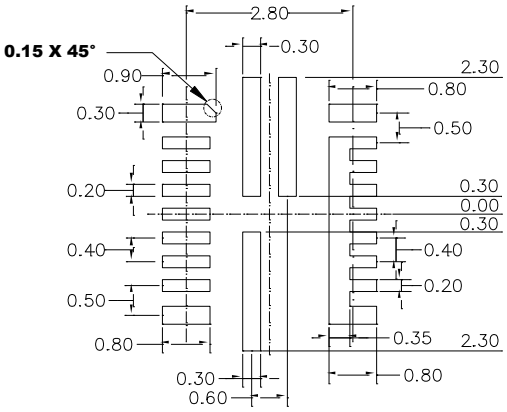
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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