MP8772C

12A, 17V, 700kHz, Synchronous Step-Down Converter with FCCM in QFN-16 Package

DESCRIPTION

The MP8772C is a fully integrated, high-frequency, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs. The device offers a very compact solution that achieves 12A of continuous output current (I_{OUT}), with excellent load and line regulation across a wide input voltage (V_{IN}) range. The MP8772C uses synchronous mode for higher efficiency across the I_{OUT} load range.

Constant-on-time (COT) control operation provides fast transient response, easy loop design, and tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP8772C requires a minimal number of readily available, standard external components, and is available in a space-saving QFN-16 (3mmx3mm) package.

FEATURES

- Forced Continuous Conduction Mode (FCCM)
- Fixed 700kHz Switching Frequency (f_{SW})
- Adjustable Output Voltage (V_{OUT}) from 0.6V
- Wide 3V to 17V Operating Input Voltage (V_{IN}) Range
- 12A Output Current (I_{OUT})
- 16mΩ/5.5mΩ Low On Resistance ($R_{DS(ON)}$) Internal Power MOSFETs
- 100μA Quiescent Current (I_Q)
- High-Efficiency Synchronous Mode
- Pre-Biased Start-Up
- Externally Configurable Soft-Start Time (t_{SS})
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Security Cameras
- Portable Devices and xDSL Devices
- Digital Set-Top Boxes (STBs)
- Flat-Panel Television and Monitors
- General-Purpose Power Supplies

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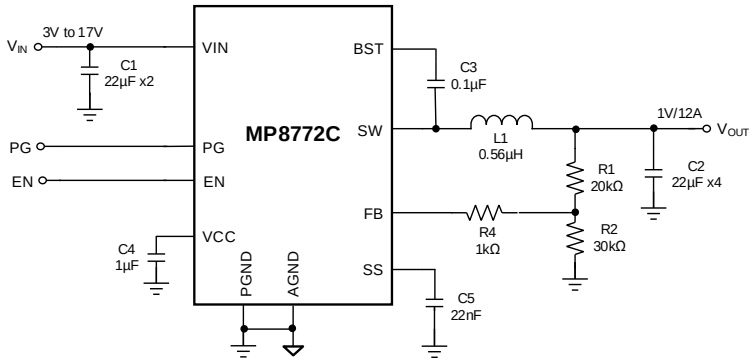
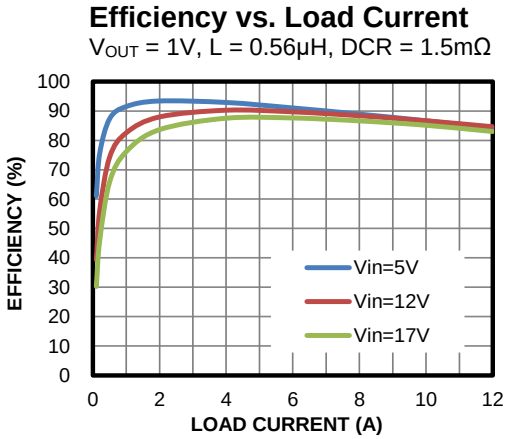
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8772CGQ	QFN-16 (3mmx3mm)	*See Below*	1

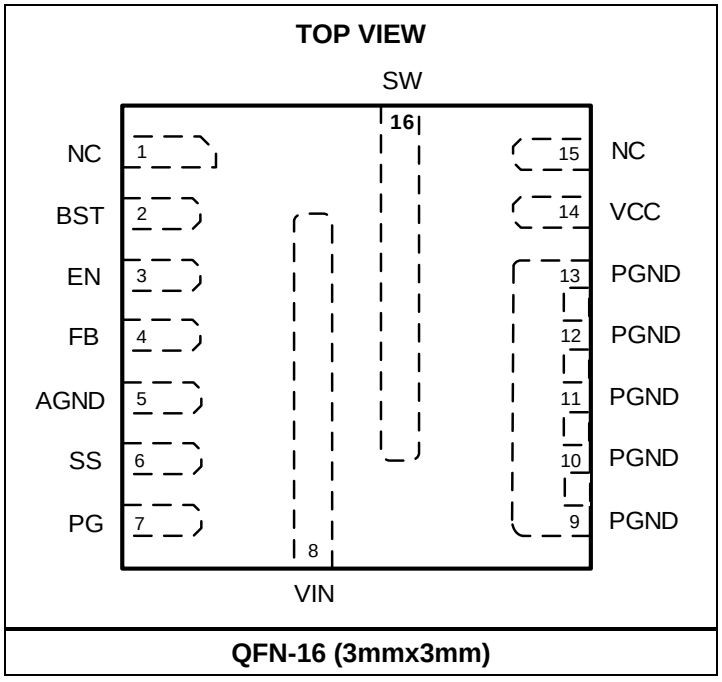
* For Tape & Reel, add suffix -Z (e.g. MP8772CGQ-Z).

TOP MARKING

CEQY
LLLL

CEQ: Product code of MP8772CGQ
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 15	NC	**No connection.** The NC pin must be left floating.
2	BST	**Bootstrap.** Connect a capacitor between the BST and SW pins to form a floating supply across the high-side MOSFET (HS-FET) driver. It is recommended to use a BST resistor (R_{BST}) below 4.7Ω.
3	EN	**Enable.** Pull the EN pin high to enable the MP8772C. When EN is floating, the pin is pulled down to AGND and disabled via an internal 1.2MΩ resistor.
4	FB	**Feedback.** The FB pin sets the output voltage (V_{OUT}) when connected to the tap of an external resistor divider connected between the output and AGND.
5	AGND	**Signal ground.** The AGND pin is not internally connected to the system ground. Ensure that AGND is connected to the system ground in the PCB layout.
6	SS	**Soft start.** Connect a capacitor across the SS pin and AGND to set the soft-start time (t_{SS}), which avoids inrush current at start-up.
7	PG	**Power good output.** The PG pin has an open-drain output. PG goes low if under-voltage protection (UVP), over-current protection (OCP), over-temperature protection (OTP), or over-voltage protection (OVP) occurs.
8	VIN	**Supply voltage.** The MP8772C operates from a 3V to 17V input rail. A capacitor (C1) is required to decouple the input rail. Use a wide PCB trace to make the connection.
9, 10, 11, 12, 13	PGND	**System ground.** The PGND pin is the reference ground of the regulated V_{OUT}. PGND requires careful consideration during the PCB layout. It is recommended to connect PGND to system ground with coppers and vias.
14	VCC	**Internal bias supply output.** Decouple the VCC pin using a 1µF capacitor. Place the VCC capacitor (C_{VCC}) close to VCC and AGND.
16	SW	**Switch output.** Connect the SW pin using a wide PCB trace.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +20V (23V < 10ns)
SW voltage (V_{SW}) ..... -0.3V (-5V < 10ns) ..... to V_{IN} + 0.7V (+23V < 10ns)
BST voltage (V_{BST}) ..... V_{SW} + 4V
EN voltage (V_{EN}) ..... V_{IN}
All other pins ..... -0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (4) 3.2W
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +125°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 17V
Output voltage (V_{OUT}) ..... 0.6V to V_{IN} x D_{MAX} or 12V max
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-16 (3mmx3mm)			
EV8772C-Q-00A (4)	38	10	°C/W
JESD51-7 (5)	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation on EV8772C-Q-00A board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV8772C-Q-00A, a 4-layer PCB (85mmx85mm).
5) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		17	V
Supply Current						
Shutdown supply current	I_{IN}	V_{EN} = 0V			5	µA
Quiescent supply current	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	µA
MOSFET						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST-SW} = 3.3V		16		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 3.3V		5.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 17V, T_J = 25°C			1	µA
Current Limit and Negative Current Limit						
Valley current limit	I_{LIMIT_VY}		12	14		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
Negative current limit	I_{NCL}			-3.5		A
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}		600	700	800	kHz
Minimum on time (7)	t_{ON_MIN}			50		ns
Minimum off time (7)	t_{OFF_MIN}			100		ns
Reference and Soft Start (SS)						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C (6)	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start (SS) current	I_{SS_START}		4	6	8	µA
Enable and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.1	1.25	1.4	V
EN falling threshold	$V_{EN_FALLING}$		0.9	1	1.1	V
EN pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
V_{CC} under-voltage lockout (UVLO) rising threshold	V_{CC_VTH}		2.6	2.8	3	V
V_{CC} UVLO threshold hysteresis	V_{CC_HYS}			350		mV
VCC regulator	V_{CC}			3.4		V
VCC load regulation	V_{REG_VCC}	I_{CC} = 5mA		3		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (6), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Good (PG)						
PG under-voltage (UV) rising threshold	$V_{PG_UV_VTH_HI}$		0.85	0.9	0.95	V_{FB}
PG UV falling threshold	$V_{PG_UV_VTH_LO}$		0.75	0.80	0.85	V_{FB}
PG over-voltage (OV) rising threshold	$V_{PG_OV_VTH_HI}$		1.15	1.2	1.25	V_{FB}
PG OV falling threshold	$V_{PG_OV_VTH_LO}$		1.05	1.1	1.15	V_{FB}
PG delay	t_{PG_D}	Both edges		50		µs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 4V			10	µA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD_HYS}			20		°C

Notes:

6) Derived by over-temperature correlation. Not tested in production.
7) Derived by sample characterization. Not tested in production.

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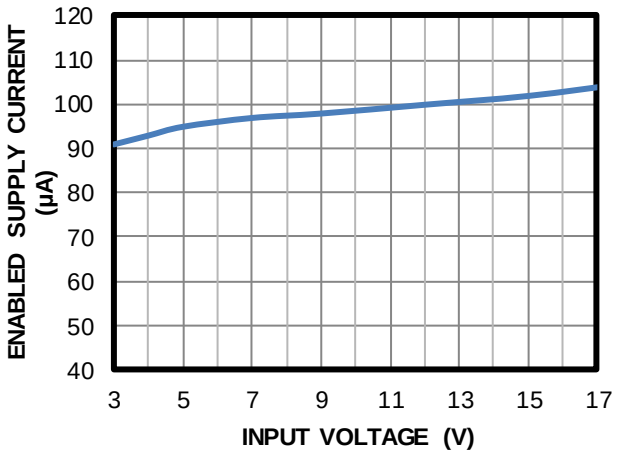
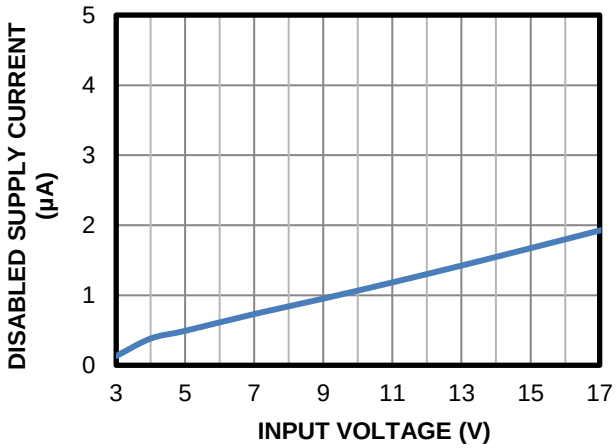
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

Enabled Supply Current vs. Input Voltage



Disabled Supply Current vs. Input Voltage



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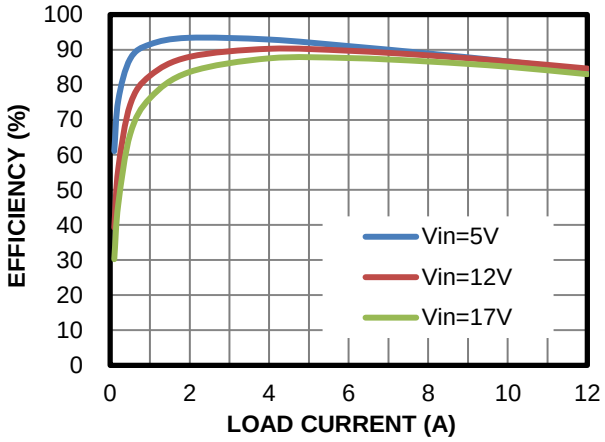
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

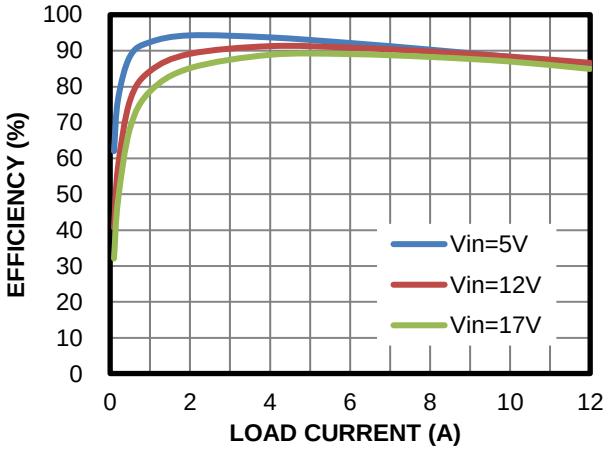
Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.56µH, DCR = 1.5mΩ



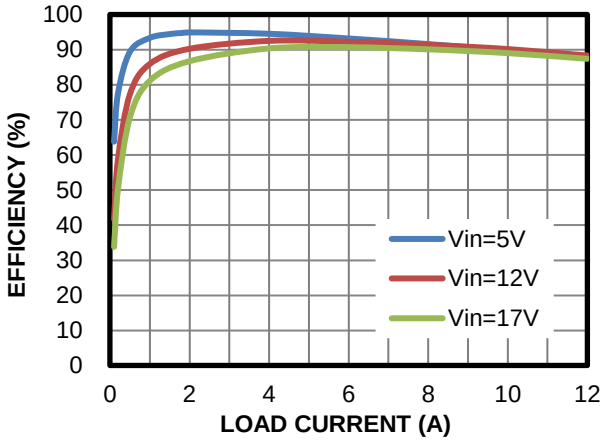
Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 0.56µH, DCR = 1.5mΩ



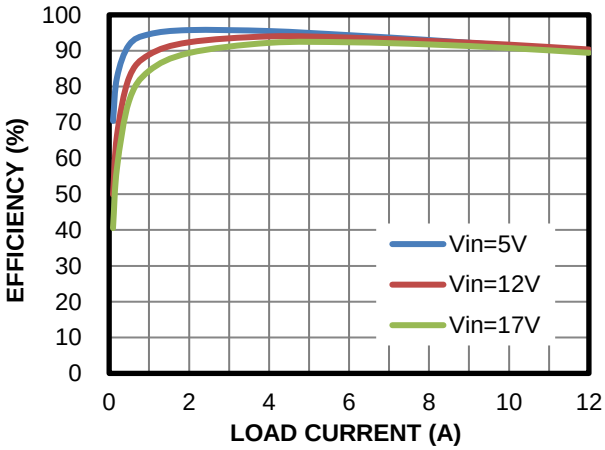
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 0.56µH, DCR = 1.5mΩ



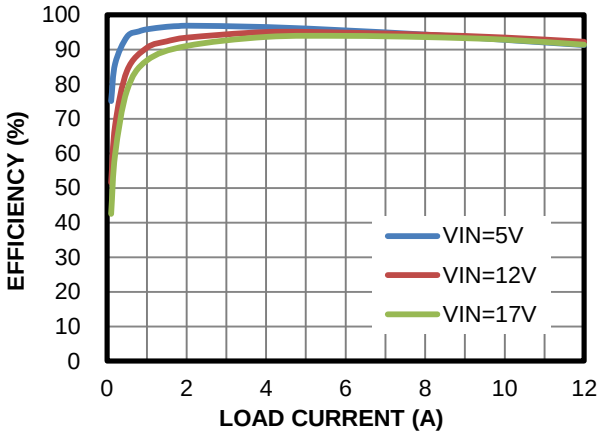
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 0.82µH, DCR = 0.9mΩ



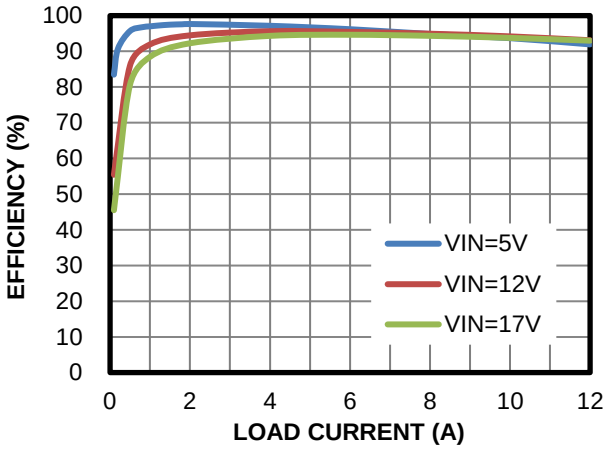
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 0.82µH, DCR = 0.9mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 1µH, DCR = 1.35mΩ



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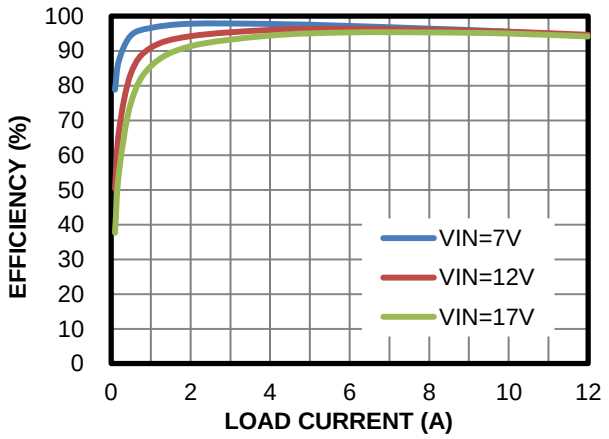
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

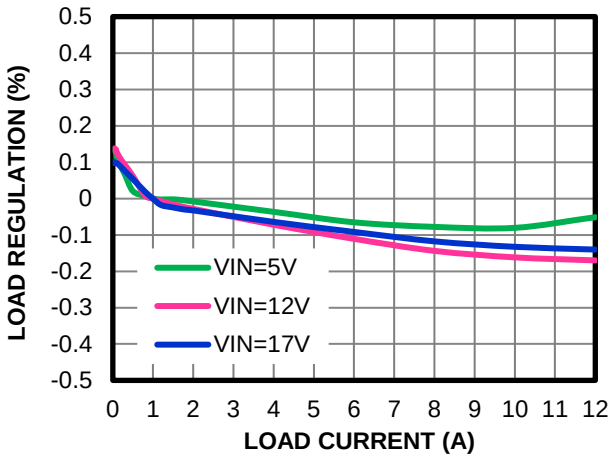
Efficiency vs. Load Current

V_{OUT} = 5V, L = 1.2µH, DCR = 1.8mΩ

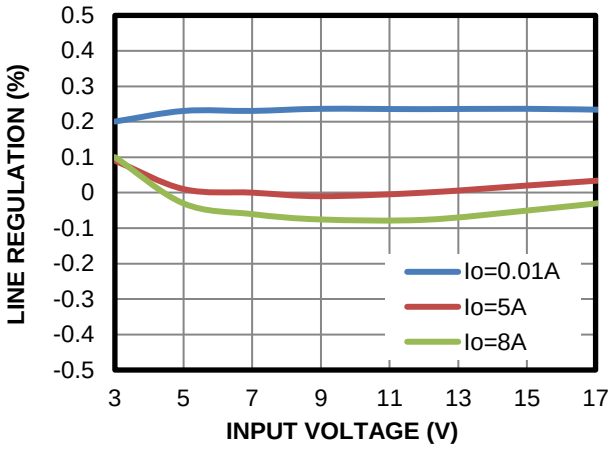


Load Regulation vs. Load Current

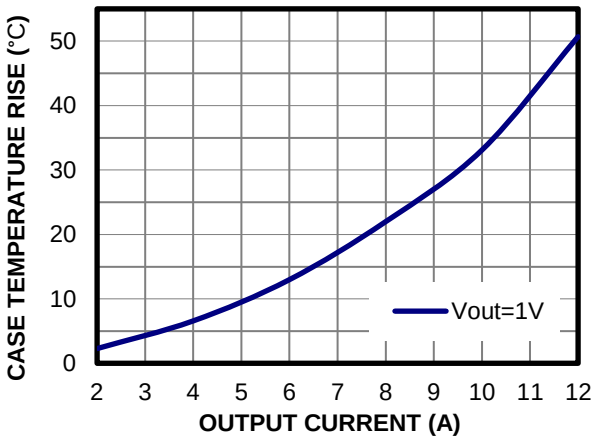
V_{OUT} = 1V



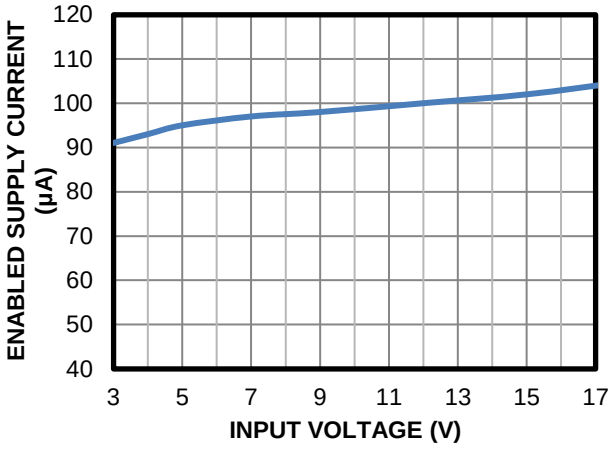
Line Regulation vs. Input Voltage



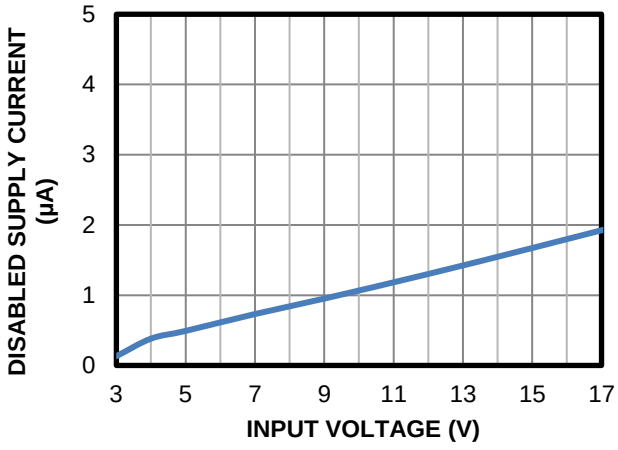
Case Temperature Rise vs. Output Current



Enabled Supply Current vs. Input Voltage



Disabled Supply Current vs. Input Voltage



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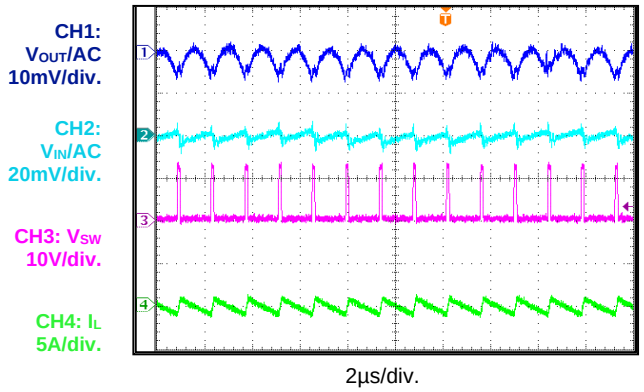
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

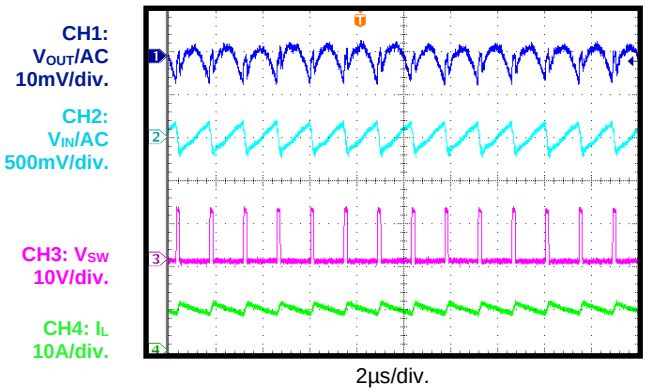
Input/Output Ripple

I_{OUT} = 0A



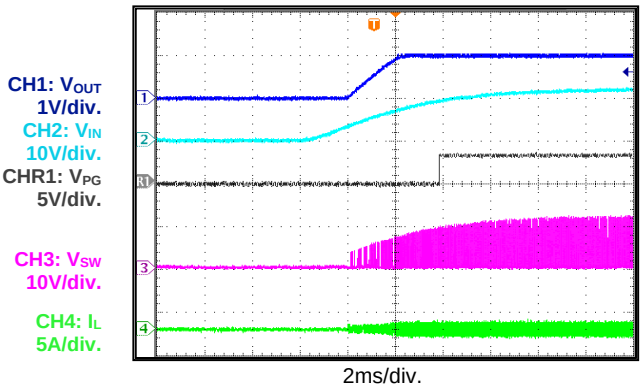
Input/Output Ripple

I_{OUT} = 12A



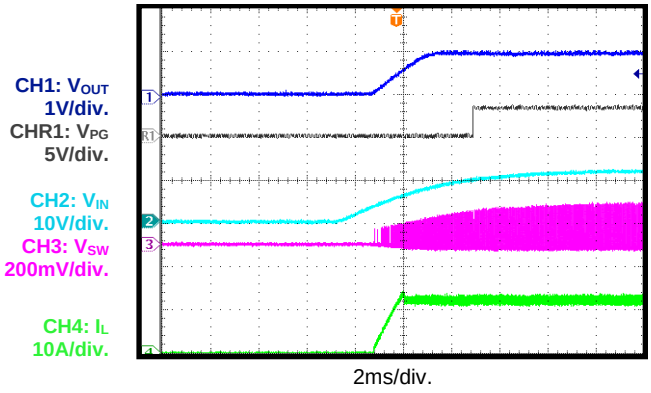
Start-Up through VIN

I_{OUT} = 0A



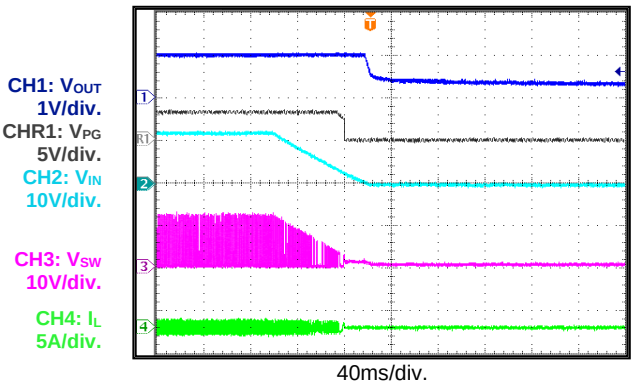
Start-Up through VIN

I_{OUT} = 12A



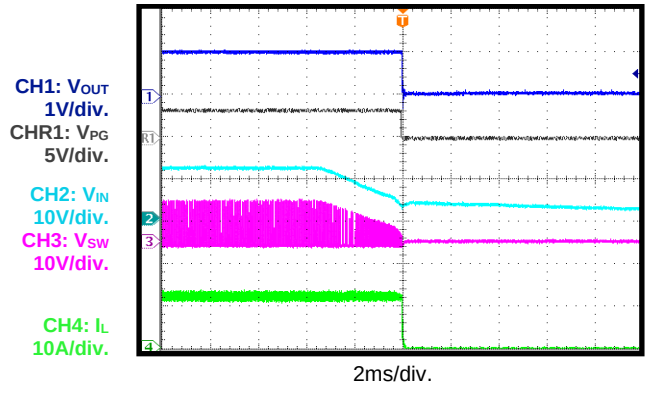
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 12A



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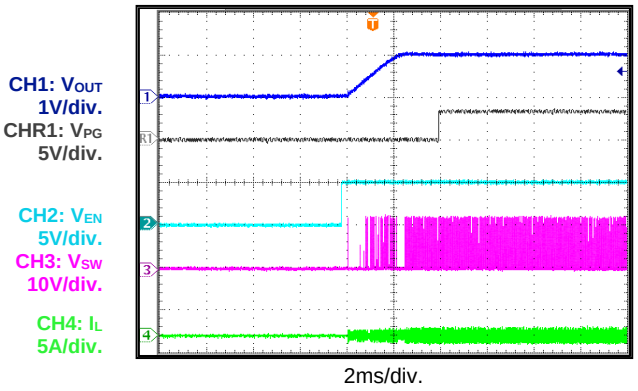
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

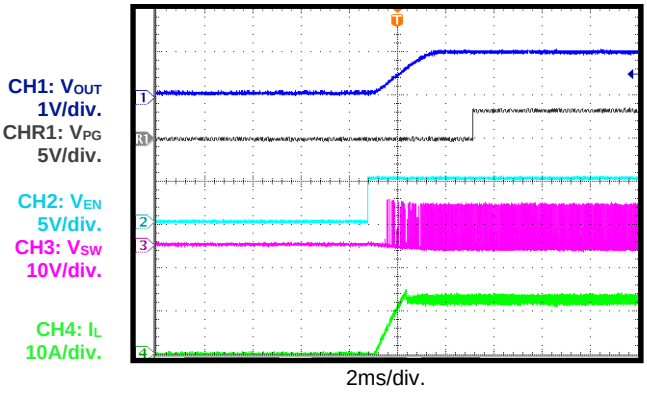
Start-Up through EN

I_{OUT} = 0A



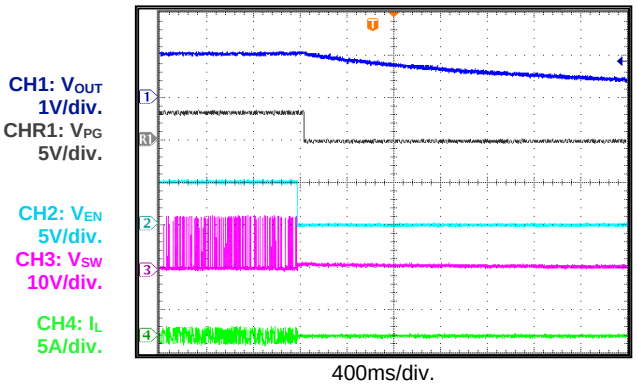
Start-Up through EN

I_{OUT} = 12A



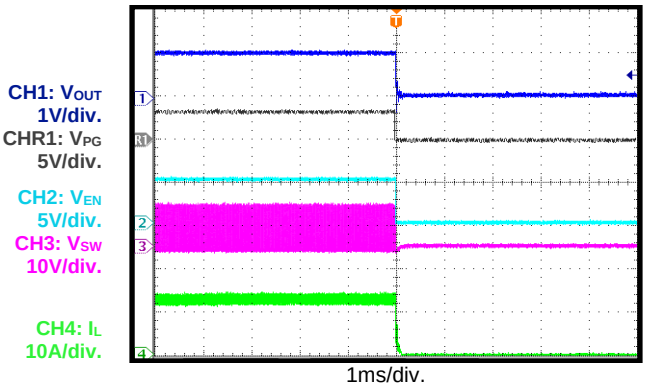
Shutdown through EN

I_{OUT} = 0A



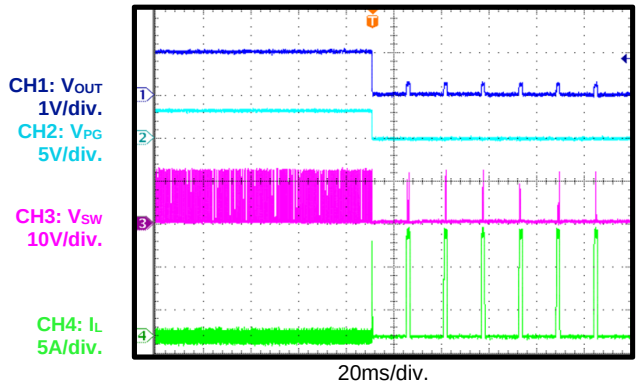
Shutdown through EN

I_{OUT} = 12A



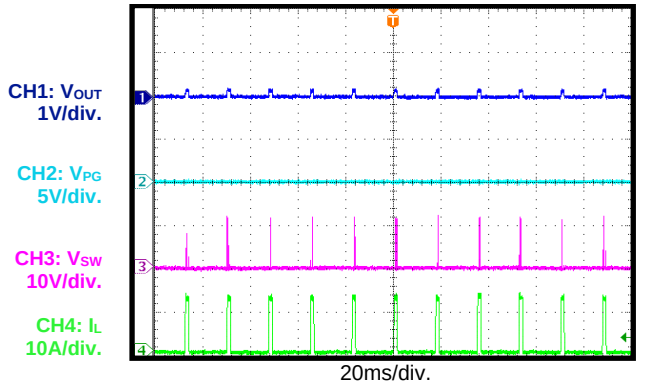
Short-Circuit Protection Entry

I_{OUT} = 0A



Short-Circuit Protection Steady State

Short output to GND



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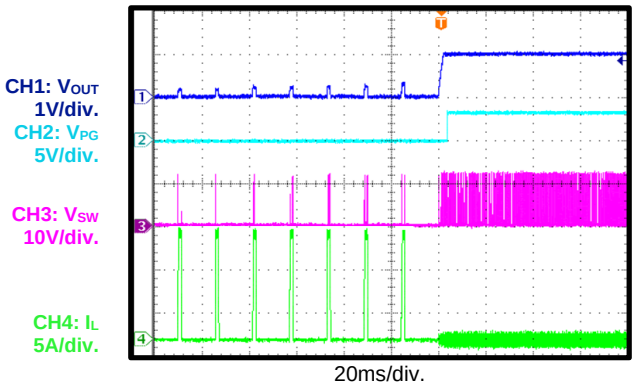
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

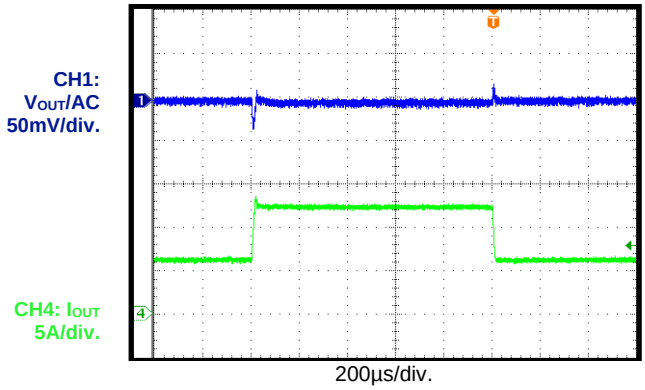
Short-Circuit Protection Recovery

I_{OUT} = 0A



Load Transient

I_{OUT} = 6A to 12A



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FUNCTIONAL BLOCK DIAGRAM

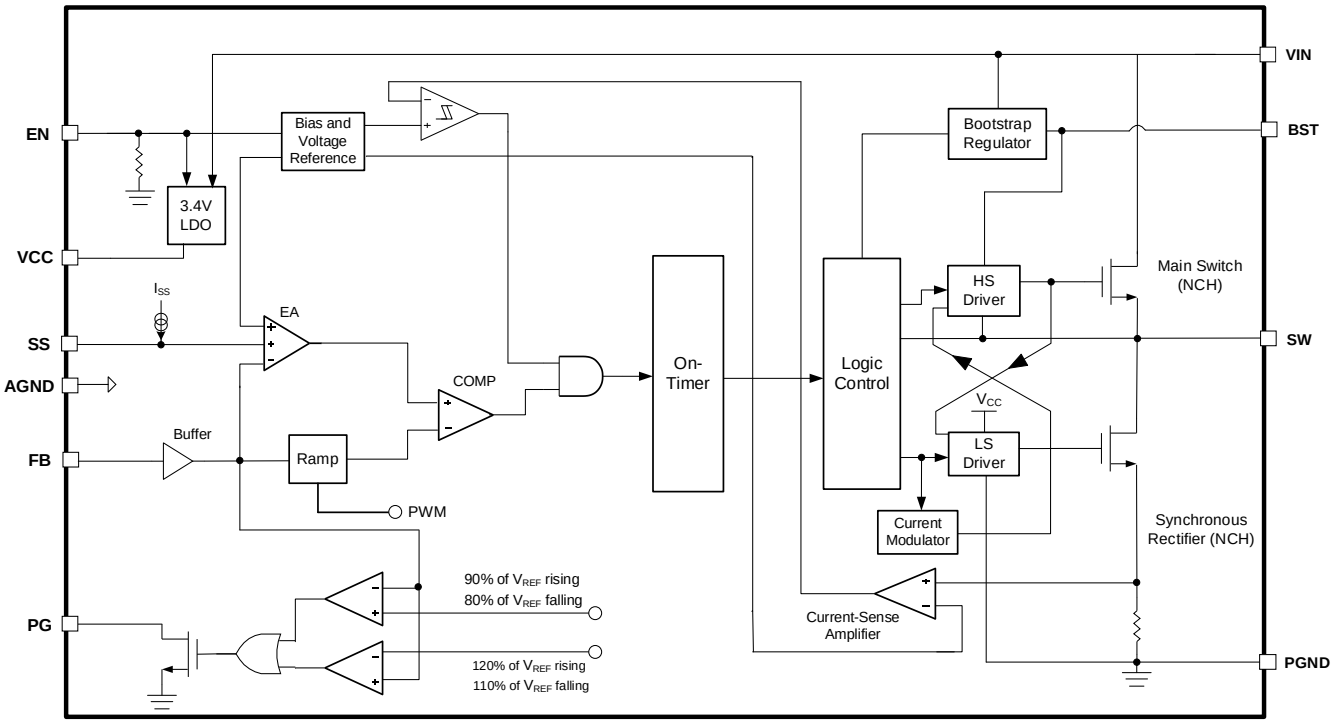

Figure 1: Functional Block Diagram

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OPERATION

The MP8772C is a fully integrated, synchronous, rectified, step-down switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. Figure 2 shows the MP8772C's simplified ramp compensation block.

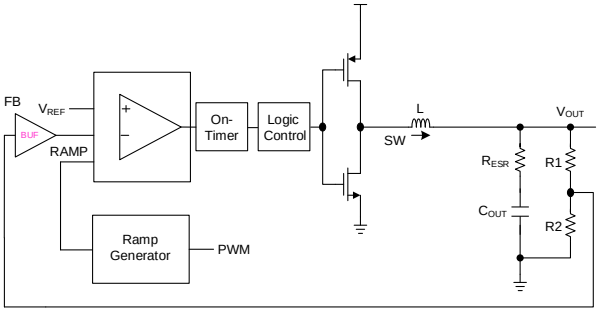

Figure 2: Simplified Ramp Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage (V_{OUT}). The on period is determined by V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the V_{IN} range.

After the on period elapses, the HS-FET turns off. The HS-FET turns on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates V_{OUT}.

The MP8772C operates in forced continuous conduction mode (FCCM). The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. There is a dead short between the input and ground if both the HS-FET and LS-FET turn on at the same time; this is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period, or vice versa.

Internal compensation is applied for COT control to provide more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting line or load regulation.

VCC Regulator

The 3.4V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates across the full V_{IN} range. If V_{IN} exceeds 3.4V, then the regulator's output is in full regulation. If V_{IN} drops below 3.4V, then the regulator's output (V_{CC}) also decreases. A 1µF decoupling ceramic capacitor is required at the VCC pin.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Pull EN above 1.25V to turn the regulator on; pull EN below 1V to turn the regulator off. When EN is floating, the pin is pulled down to AGND via an internal 1.2MΩ resistor. EN can be connected to V_{IN} directly and supports a 17V input range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8772C's UVLO comparator monitors the internal regulator's output voltage (V_{CC}). The V_{CC} UVLO rising threshold is about 2.8V, while the V_{CC} UVLO falling threshold is 2.45V.

If V_{IN} exceeds its UVLO rising threshold, then the MP8772C starts up. If V_{IN} is below its UVLO falling threshold, then the MP8772C shuts down. This is a non-latch protection.

Soft Start (SS)

The MP8772C employs a soft start (SS) mechanism to ensure smooth output ramping during start-up. When EN goes high, an internal current source (6µA) charges up the SS capacitor (C_{SS}). V_{OUT} ramps up smoothly with the SS voltage (V_{SS}). If V_{SS} exceeds V_{REF}, then it continues to ramp up until V_{REF} takes over. At this point, SS finishes, and the device enters steady-state operation.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = 0.83 \times \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

If the output capacitance (C_{OUT}) is large, then it is not recommended to set the SS time (t_{SS}) too short; otherwise, the current limit can be reached easily during SS. It is recommended to select a C_{SS} above 4.7nF.

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Power Good (PG) Indicator

The PG pin is the open drain of a MOSFET connected to VCC or another voltage source via a resistor (e.g. 100kΩ). If V_{IN} is applied, then the MOSFET turns on, meaning PG is pulled to ground before SS is ready. After V_{FB} reaches 90% of V_{REF}, PG is pulled high after a 50μs delay. If V_{FB} drops to 80% of V_{REF}, then PG is pulled low.

If UVLO or over-temperature protection (OTP) is triggered, then PG is pulled low immediately. If an over-current (OC) condition occurs, then PG is pulled low once V_{FB} drops below 80% of V_{REF} after a 0.05ms delay. If an over-voltage (OV) condition occurs, then PG is pulled low when V_{FB} exceeds 120% of V_{REF} after a 0.05ms delay. If V_{FB} falls below 110% of V_{REF}, then PG is pulled high after a 0.05ms delay.

If the input supply fails to power the MP8772C, then PG is clamped low, even though PG is connected to an external DC source via a pull-up resistor. Figure 3 shows the relationship between the PG clamped voltage and the pull-up current.

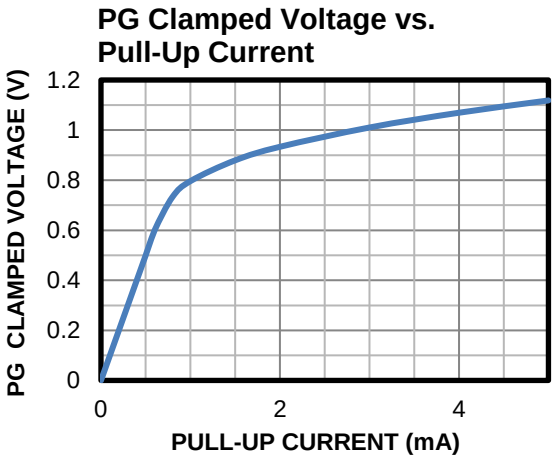

Figure 3: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP8772C provides valley limit control. The LS-FET monitors the current flowing through the LS-FET. The HS-FET waits until the valley current limit is removed before turning on again. Meanwhile, V_{OUT} drops until V_{FB} is below the under-voltage (UV) threshold (typically 50% below V_{REF}). Once a UV condition is triggered, the MP8772C enters hiccup mode to restart the part periodically.

During over-current protection (OCP), the device attempts to recover from the OC fault with hiccup mode. This means that the chip disables the output power stage, discharges C_{SS}, and attempts to soft start again automatically. If the OC condition remains after SS ends, then the device repeats this operation cycle until the OC condition is removed, and then V_{OUT} rises back to the regulation level. OCP is a non-latch protection.

Pre-Biased Start-Up

The MP8772C is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, then the BST voltage (V_{BST}) is refreshed and charged, and the C_{SS} voltage is charged as well. If V_{BST} exceeds its rising threshold and the C_{SS} voltage exceeds the sensed output voltage at FB, then the part begins normal operation.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 150°C, then the entire chip shuts down. If the temperature drops below its lower threshold (typically 130°C), then the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor (C_{BST}) powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a 1.7V rising threshold and a 150mV hysteresis. V_{IN} regulates the C_{BST} voltage internally through D1, M1, R4, C4, the output inductor (L_{OUT}), and C_{OUT} (see Figure 4). If the difference between V_{IN} and V_{SW} exceeds 5V, then U2 regulates M1 to maintain a 3.3V V_{BST} across C4. The BST resistor (R4, also called R_{BST}) is recommended to be below 4.7Ω.

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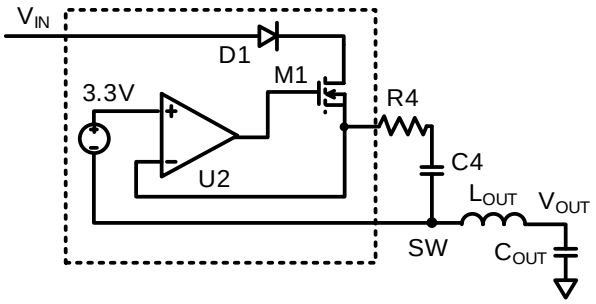

Figure 4: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If V_{IN} and the EN voltage (V_{EN}) exceed the V_{IN} UVLO rising threshold and EN rising threshold, respectively, then the chip starts up. The reference block starts first, generating a stable V_{REF} and reference current, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: low V_{EN}, low V_{IN}, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

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APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider sets the output voltage (V_{OUT}). First, select a proper value for R2. A small R2 leads to considerable quiescent current (I_Q) loss, while a large R2 makes FB noise-sensitive. R2 is recommended to be between 2kΩ and 100kΩ. Typically, set the current flowing through R2 to be below 250μA to achieve a good balance between system stability and no-load loss. Then R1 can be calculated with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 5 shows the feedback circuit.

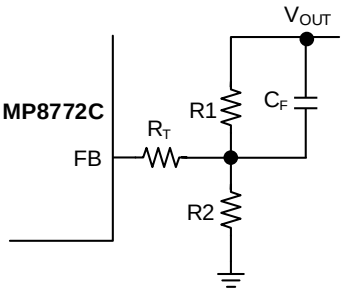

Figure 5: Feedback Network

Table 1 shows the recommended resistances for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_F (pF)	R_T (kΩ)
1	20	30	0.56	56	1
1.2	20	20	0.56	56	1
1.5	20	13	0.56	56	1
1.8	20	10	0.82	56	1
2.5	20	6.34	0.82	56	1
3.3	20	4.42	1	56	1
5	20	2.7	1.2	56	1

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance is to design the peak-to-peak ripple current in the inductor to be between 30% and 40% of the maximum output current, and ensure that the peak inductor current is below the maximum switching current limit. The inductance (L) can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the peak inductor current (I_{LP}), where I_{LP} can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The input current (I_{IN}) to the step-down converter is discontinuous, and requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they remain fairly stable under temperature fluctuations.

The capacitors must also have a ripple current rating greater than the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor (C_{IN}) with an RMS current rating greater than half of the maximum load current.

C_{IN} determines the converter's input voltage ripple (ΔV_{IN}). If there is a ΔV_{IN} requirement in the system, then choose C_{IN} to meet the specification.

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ΔV_{IN} can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple (ΔV_{OUT}) can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

If using ceramic capacitors, the impedance at the switching frequency (f_{SW}) is dominated by the capacitance. ΔV_{OUT} is mainly caused by the capacitance. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

ΔV_{OUT} caused by the ESR is very small. Therefore, an external ramp is required to stabilize the system. The external ramp can be generated via a resistor (R_{RAMP}) and a capacitor (C_R).

If using POSCAP capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

In addition to considering ΔV_{OUT}, choosing a larger C_{OUT} can achieve better load transient response. It is important to consider the maximum C_{OUT} limit in the design application. If C_{OUT} is too high, then V_{OUT} cannot reach the design value during the soft-start time (t_{SS}) and fails to regulate.

The maximum output capacitance (C_{OUT_MAX}) can be estimated with Equation (12):

$$C_{OUT_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period.

Design Example

Table 2 shows a design example where ceramic capacitors are applied.

Table 2: Design Example

V_{IN}	V_{OUT}	I_{OUT}
12V	1V	12A

For the detailed application schematics, see Figure 7 on page 20 to Figure 13 on page 22. For the typical performance and waveforms, see the Typical Characteristics section on page 7. For more device applications, refer to the related evaluation board datasheet.

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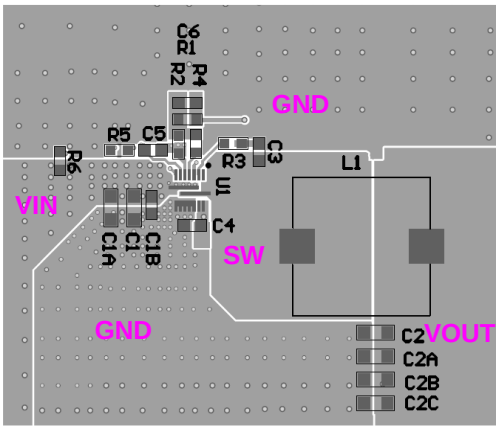
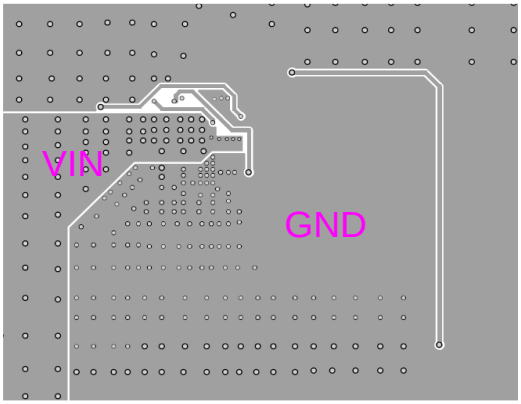
PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For better performance, it is recommended to use a 4-layer layout, where the two middle layers are PGND. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, and SW) very close to the device using short, direct, and wide traces.
2. Place C_{IN} as close to VIN and PGND as possible.
3. Place a VCC decoupling capacitor close to the device.
4. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
5. Place the external feedback resistors next to FB.
6. Keep the switching node (SW) short and away from the feedback network.



Top Layer



Bottom Layer

Figure 6: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

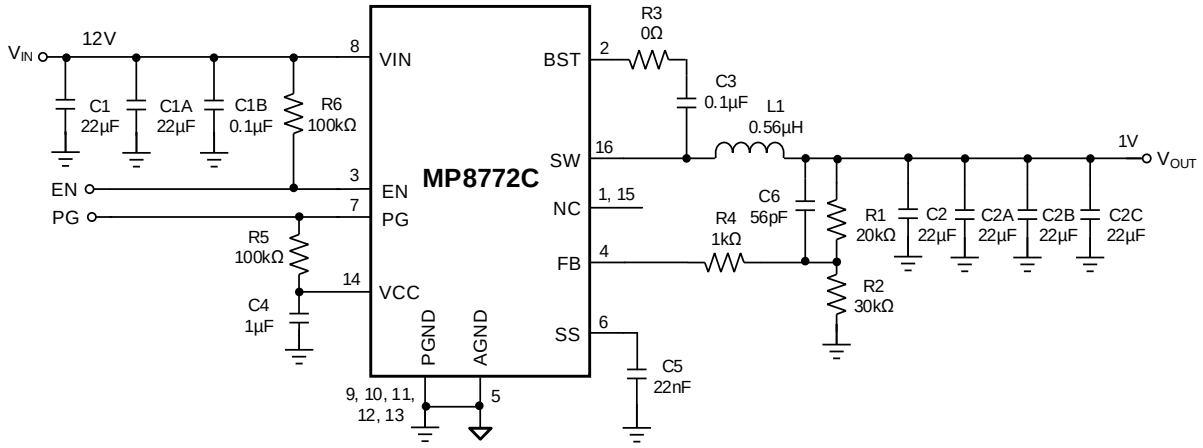

Figure 7: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A) (8)

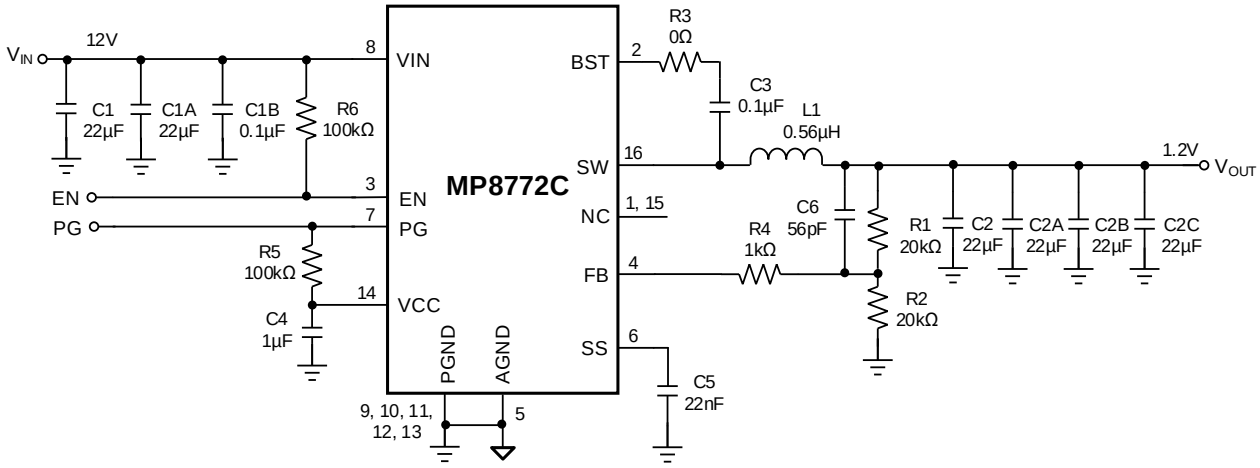

Figure 8: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 12A) (8)

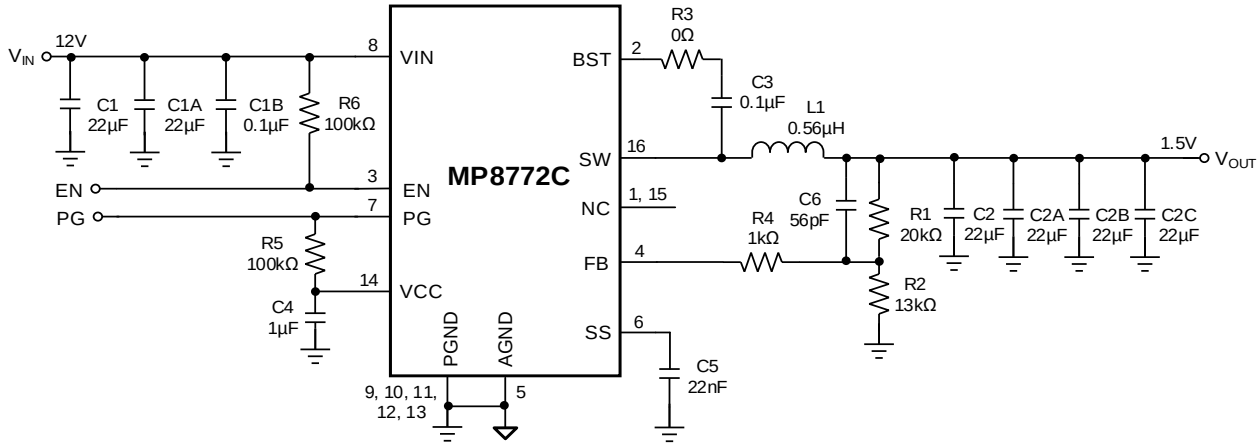

Figure 9: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A) (8)

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TYPICAL APPLICATION CIRCUITS *(continued)*

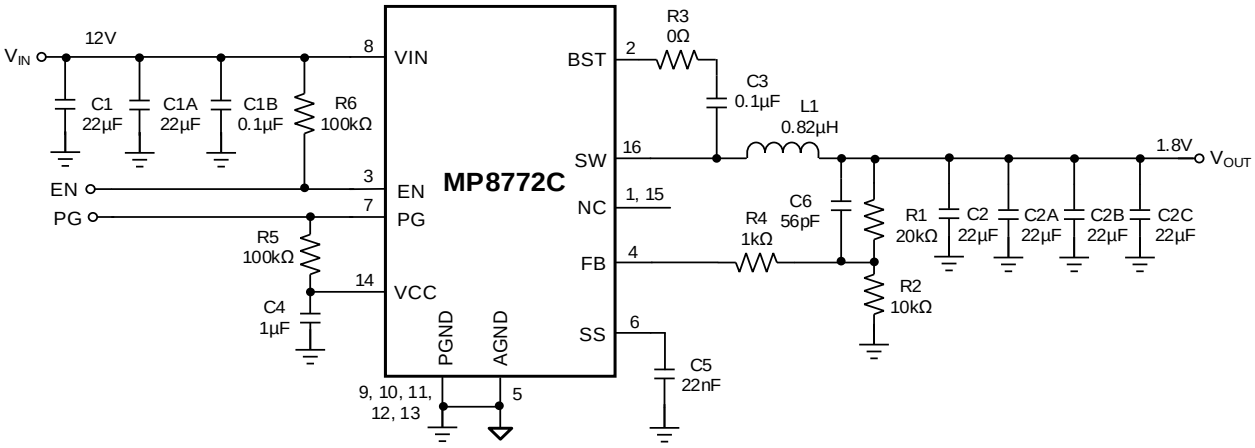

Figure 10: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 12A) (8)

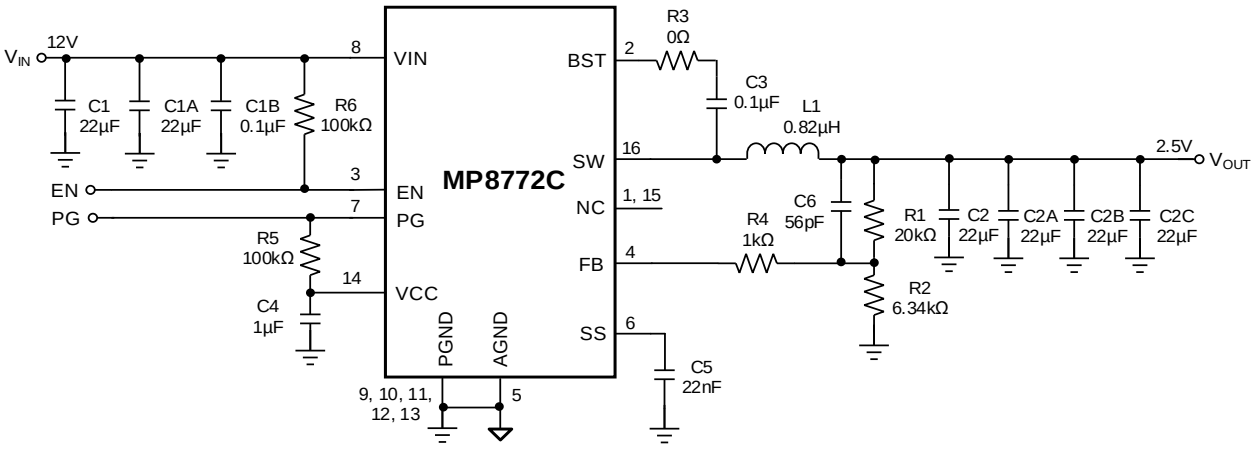

Figure 11: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 12A) (8)

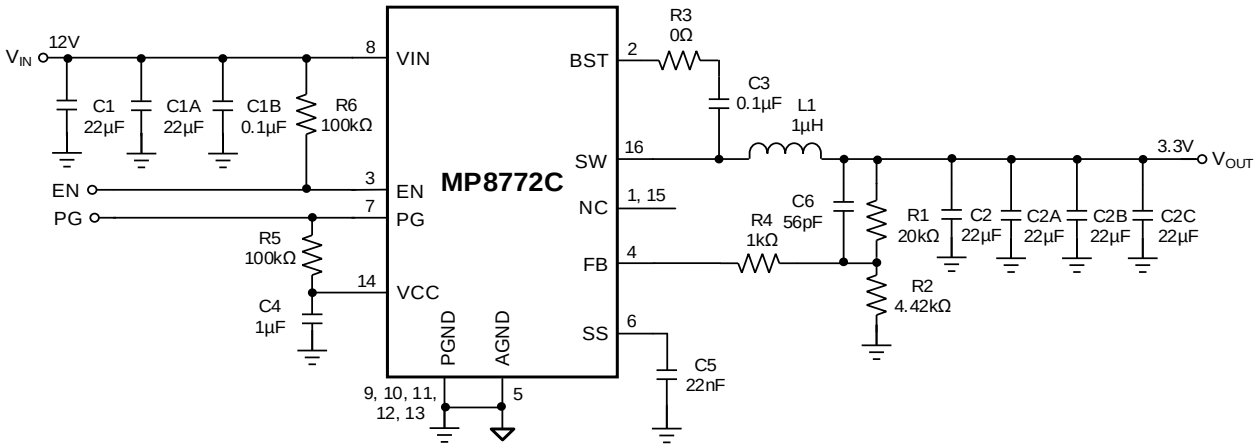

Figure 12: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 12A) (8)

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TYPICAL APPLICATION CIRCUITS *(continued)*

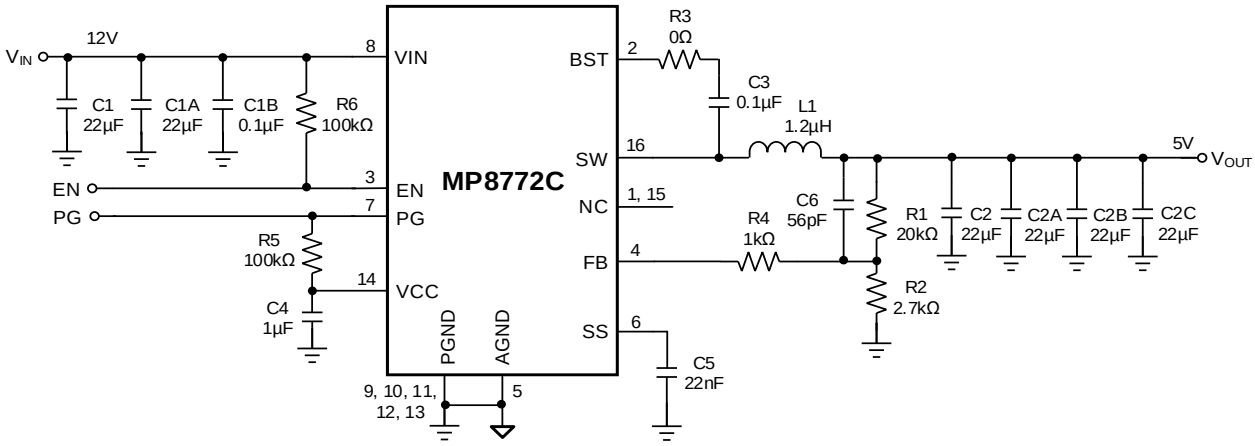

Figure 13: Typical Application Circuit (V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 12A) (8)

Note:

8) If V_{IN} is low, see the Selecting the Input Capacitor section on page 17.

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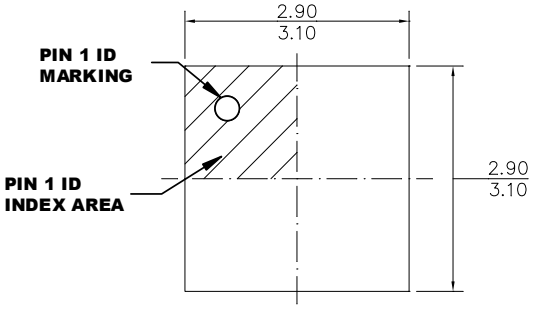
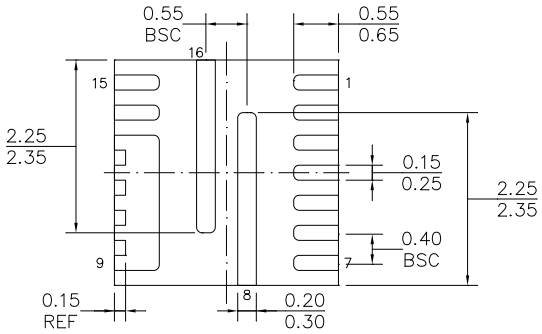
PACKAGE INFORMATION

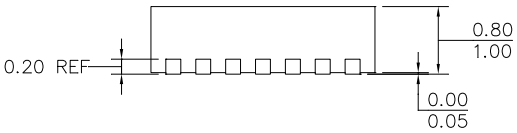
QFN-16 (3mmx3mm)



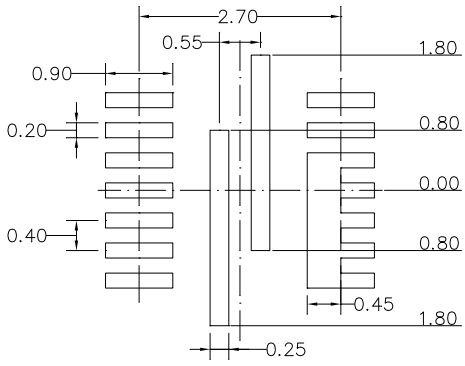
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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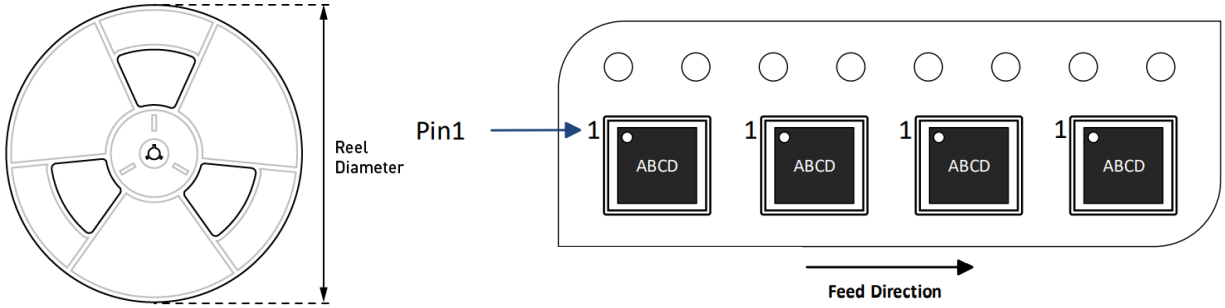
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8772CGQ-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/19/2025	Initial Release	-

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