MP8764

High Efficiency, 12A, 18V Synchronous Step-Down Converter with Latch-off OCP

The Future of Analog IC Technology

DESCRIPTION

The MP8764 is a fully integrated high frequency synchronous rectified step-down switch mode converter. It offers a very compact solution to achieve 12A output current over a wide input supply range with excellent load and line regulation. The MP8764 operates at high efficiency over a wide output current load range.

The MP8764 adopts Constant-On-Time (COT) control mode that provides fast transient response and eases loop stabilization.

Operation frequency can be programmed easily from 200kHz to 1MHz by an external resistor and keeps nearly constant as input supply varies by the feedforward compensation.

VCC under voltage lockout is internally set at 3.9V, but can be increased by programming the threshold with a resistor network on the enable pin. The output voltage startup ramp is controlled by the soft start pin. An open drain power good signal indicates the output is within its nominal voltage range.

Full integrated protection features include OCP, OVP and thermal shutdown.

The MP8764 requires a minimum number of readily available standard external components and are available in QFN 3X4 package.

FEATURES

- 2.5V to 18V Operating Input Range with External 5V Bias
- 4.5V to 18V Operating Input Range with Internal Bias
- 12A Output Current
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultrafast Transient Response
- 1.5% Reference Voltage Over -40°C to +125°C Junction Temperature Range
- Programmable Soft Start Time
- Pre-Bias Start up
- Programmable Switching Frequency from 200kHz to 1MHz
- OVP, latch-off SCP, Protection and Thermal Shutdown
- Output Adjustable from 0.611V to 13V

APPLICATIONS

- Set-top Boxes
- XDSL Modem/DSLAM
- Small-cell Base Stations
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

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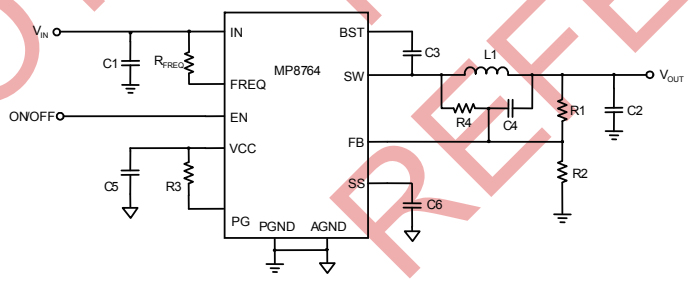
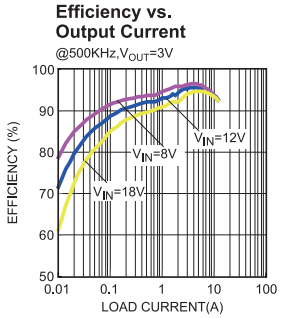
TYPICAL APPLICATION





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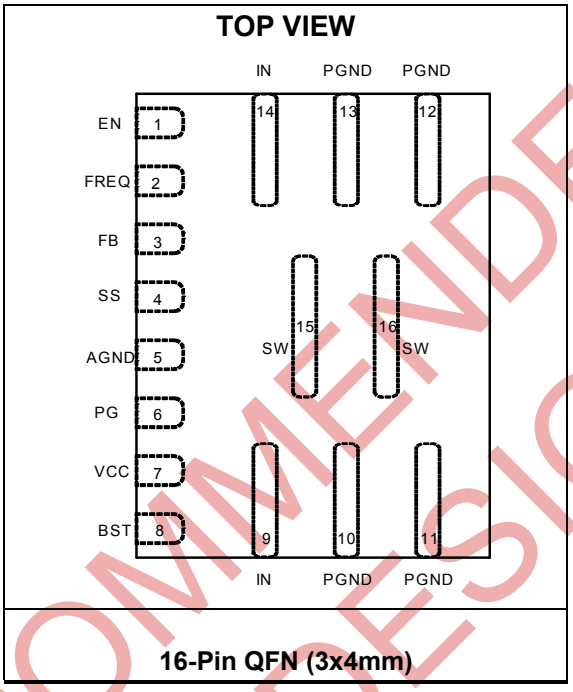
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8764GLE	16-Pin QFN（3X4mm）	MP8764 E

* For Tape & Reel, add suffix –Z (e.g. MP8764GLE–Z);

PACKAGE REFERENCE



16-Pin QFN (3x4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 21V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{SW} (30ns) ..... -3V to V_{IN} + 3V
V_{BST} ..... V_{SW} + 6V
Enable Current I_{EN} (2) 2.5mA
All Other Pins ..... –0.3V to +6V
Continuous Power Dissipation (T_A=+25°) (3)
QFN3X4 ..... 2.7W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 4.5V to 18V
Output Voltage V_{OUT} ..... 0.611V to 13V
I_{EN} ..... 0mA to 1mA
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN (3x4mm)	46	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to the section “Configuring the EN Control”.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0	1	μA
Supply Current (Quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V	760	860	960	μA
MOSFET						
High-side Switch On Resistance	HS_{RDS-ON}	T_J =25°C		21		mΩ
Low-side Switch On Resistance	LS_{RDS-ON}	T_J =25°C		7		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V		0	1	μA
Current Limit						
Low-side Valley Current Limit (6)	I_{LIMIT_VALLEY}		12			A
Low-side Negative Current Limit (6)	$I_{LIMIT_NEGATIVE}$		-4	-2.5	-1	A
Timer						
Minimum On Time (6)	T_{ON_MIN}			30		ns
One-Shot On Time	T_{ON}	R_{FREQ}=453kΩ, V_{OUT}=1.2V		250		ns
Minimum Off Time(6)	T_{OFF_MIN}			180		ns
Over-voltage and Under-voltage Protection						
OVP Latch Threshold (6)	V_{OVP_LATCH}			130%		V_{FB}
OVP Non-latch Threshold	$V_{OVP_NON-LATCH}$		117%	120%	123%	V_{FB}
OVP Delay	T_{OVP}			2		μs
UVP Threshold (6)	V_{UVP}			50%		V_{FB}
Reference And Soft Start						
Reference Voltage	V_{REF}	T_J = -40°C to +125°C (7)	602	611	620	mV
		T_J = +25°C	605	611	617	
Feedback Current	I_{FB}	V_{FB} = 650mV		50	100	nA
Soft Start Charging Current	I_{SS}	V_{SS}=0V	16	20	25	μA
Enable And UVLO						
Enable Input Low Voltage	VIL_{EN}		1.1	1.3	1.5	V
Enable Hysteresis	V_{EN-HYS}			250		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0		μA
		V_{EN} = 0V		0		

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}		3.75	3.9	4.05	V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			600		mV
VCC Regulator	V_{CC}		4.65	4.8	4.95	V
VCC Load Regulation		Icc=5mA		0.5		%
Power Good						
Power Good Rising Threshold	PG_{Vth-Hi}			97%		V_{FB}
Power Good Falling Threshold	PG_{Vth-Lo}			90%		V_{FB}
Power Good Lower to High Delay	PG_{Td}			2.5		ms
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	I_{PG_LEAK}	V_{PG} = 3.3V		10	100	nA
Thermal Protection						
Thermal Shutdown (6)	T_{SD}		150			°C
Thermal Shutdown Hysteresis (6)				25		°C

Note:

6) Guaranteed by design

7) Not production test, guaranteed by characterization..

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PIN FUNCTIONS

PIN# 16-Pin QFN	Name	Description
1	EN	Enable pin. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Connect EN to IN through a pull-up resistor or a resistive voltage divider for automatic startup. Do not float this pin. See Enable Control section for more details.
2	FREQ	Frequency set during CCM operation. A resistor connected between FREQ and IN is required to set the switching frequency. The ON time is determined by the input voltage and the resistor connected to the FREQ pin. IN connect through a resistor is used for line feed-forward and makes the frequency basically constant during input voltage's variation.
3	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. It is recommended to place the resistor divider as close to FB pin as possible. Vias should be avoided on the FB traces.
4	SS	Soft Start. Connect an external capacitor to program the soft start time for the switch mode regulator.
5	AGND	Analog ground. Select this pin as the control circuit reference point.
6	PG	Power good output, the output of this pin is an open drain signal and a pull-up resistor connected to a DC voltage is required to indicate high if the output voltage is higher than 97% of the nominal voltage. There is a delay from FB ≥ 97% to PG goes high.
7	VCC	Internal 4.8V LDO output. The driver and control circuits are powered from this voltage. Decouple with a minimum 1μF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
8	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
9, 14	IN	Supply Voltage. The IN pin supplies power for internal MOSFET and regulator. The MP8764 operates from a +2.5V to +18V input rail with 5V external bias and a +4.5V to +18V input rail with internal bias. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
10,11,12,13	PGND	System Ground. This pin is the reference ground of the regulated output voltage. For this reason care must be taken in PCB layout. Use wide PCB traces to make the connection.
15, 16	SW	Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to the V_{IN} voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives the SW pin negative during the off-time. The on-resistance of the low-side switch and the internal Schottky diode fixes the negative voltage. Use wide PCB traces to make the connection.

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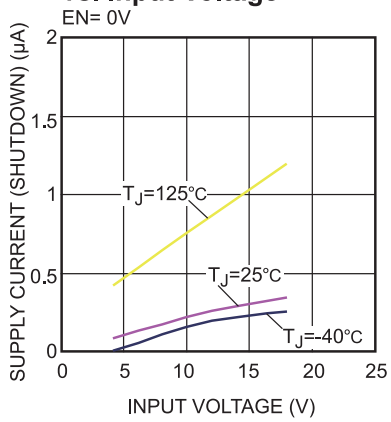
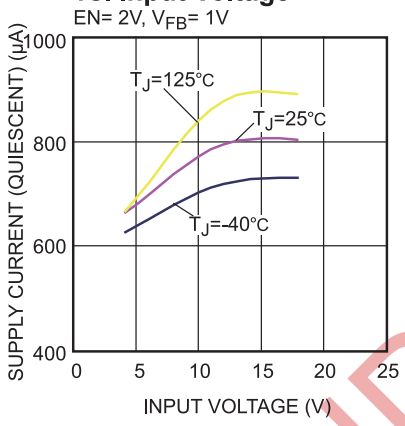
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3V, L = 1µH, T_A = 25ºC, unless otherwise noted.

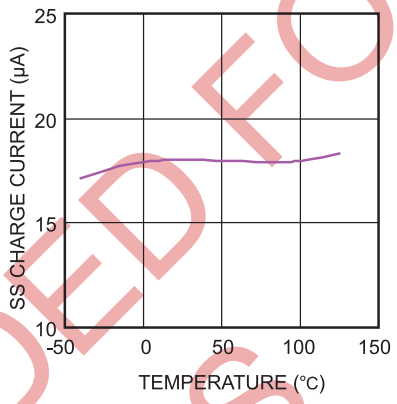
Supply Current (Shutdown) vs. Input Voltage



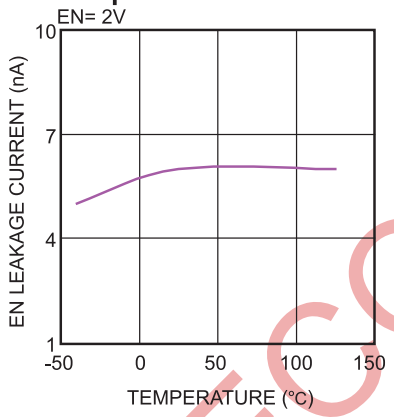
Supply Current (Quiescent) vs. Input Voltage



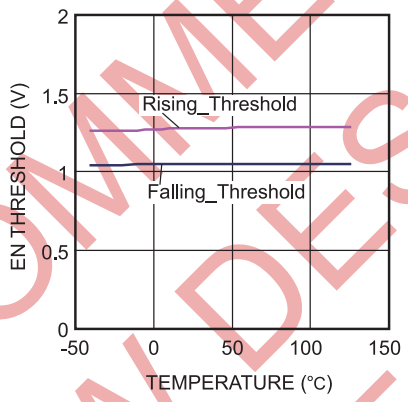
SS Charge Current vs. Temperature



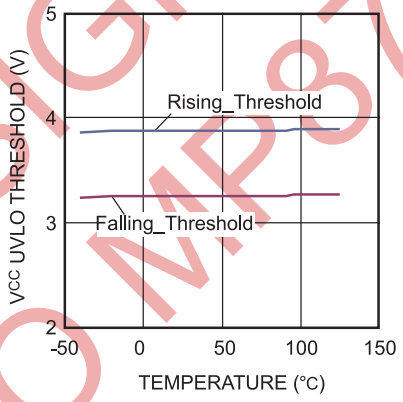
EN Leakage Current vs. Temperature



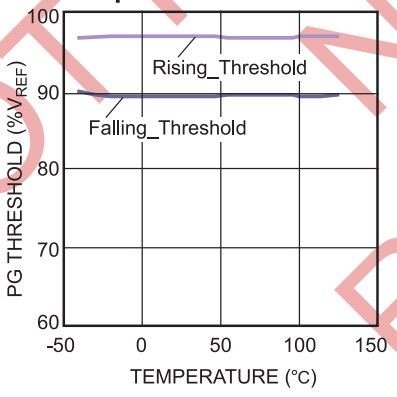
EN Threshold vs. Temperature



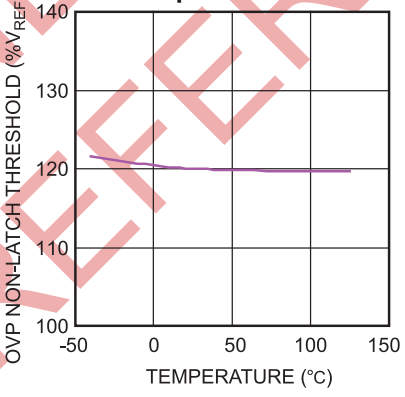
VCC UVLO Threshold vs. Temperature



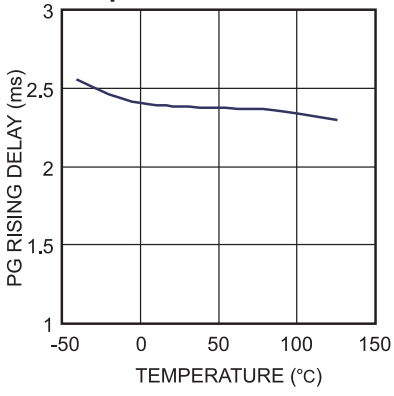
PG Threshold vs. Temperature



OVP Non-Latch Threshold vs. Temperature



PG Rising Delay vs. Temperature



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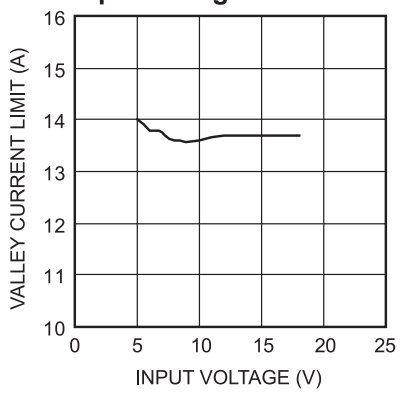
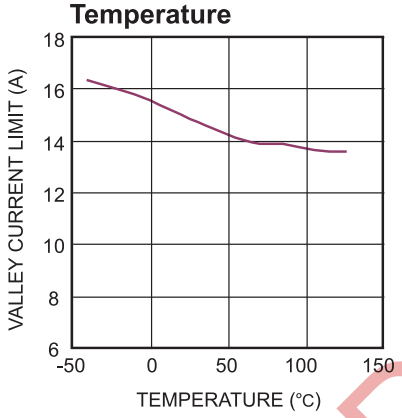
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3V, L = 1µH, T_A = 25ºC, unless otherwise noted.

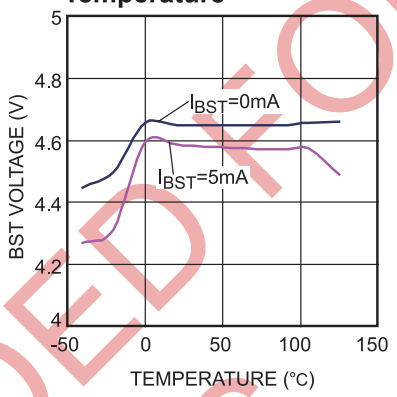
Valley Current Limit vs. Input Voltage



Vally Current Limit vs. Temperature

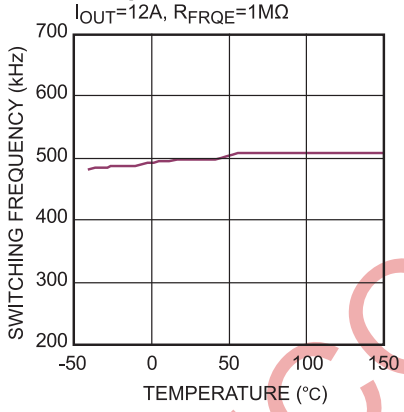


BST Voltage vs. Temperature



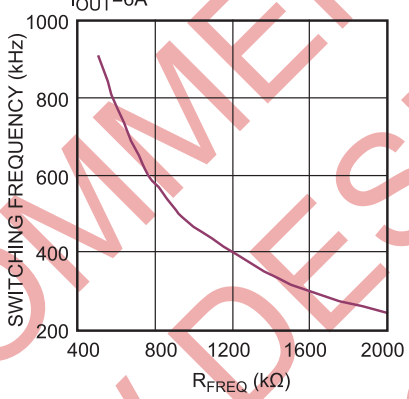
Switching Frequency vs. Temperature

I_{OUT}=12A, R_{FRQE}=1MΩ



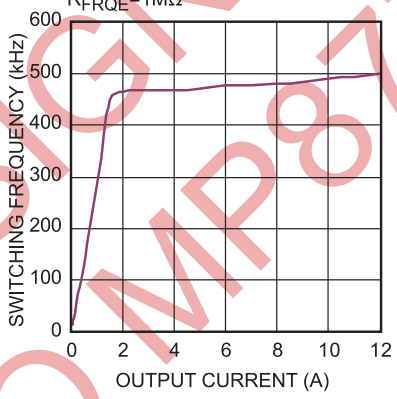
Switching Frequency vs. R_{FREQ}

I_{OUT}=6A



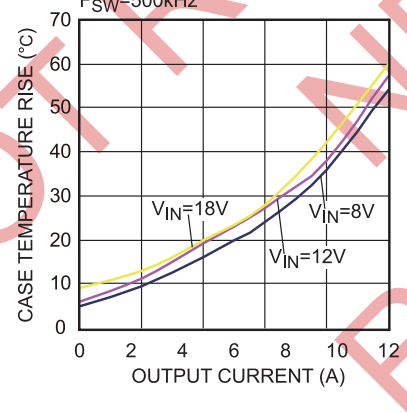
Switching Frequency vs. Output Current

R_{FRQE}=1MΩ

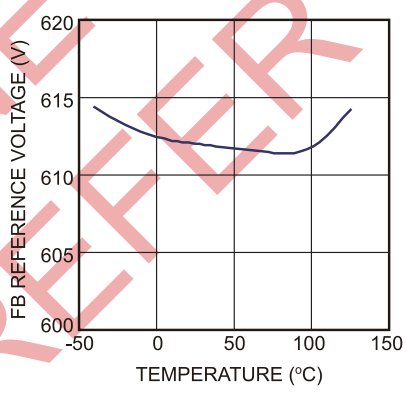


Case Temperature Rise vs. Output Current

F_{SW}=500kHz



FB Reference Voltage vs. Temperature



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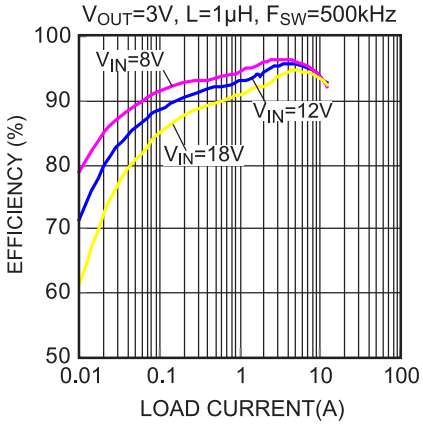
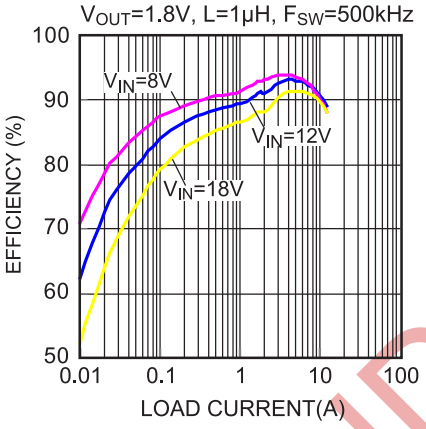
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3V, L = 1µH, T_A = 25ºC, unless otherwise noted.

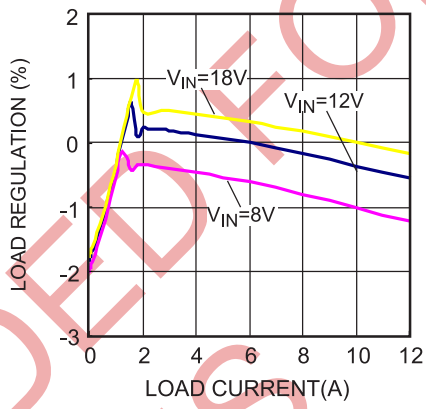
Efficiency vs. Output Current



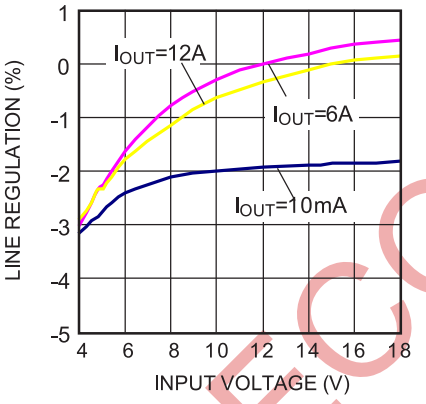
Efficiency vs. Output Current



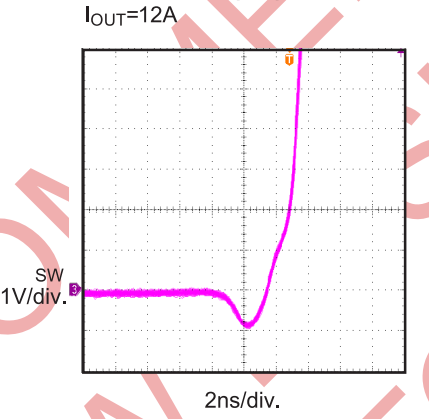
Load Regulation vs. Output Current



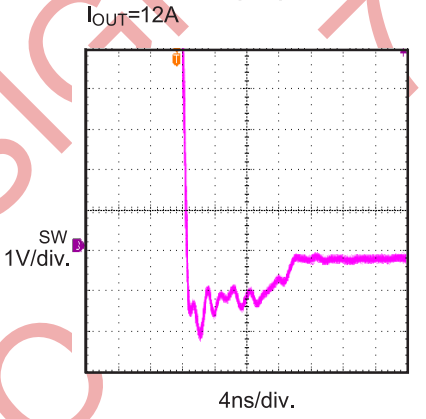
Line Regulation vs. Input Voltage



Dead Time (on)



Dead Time (off)



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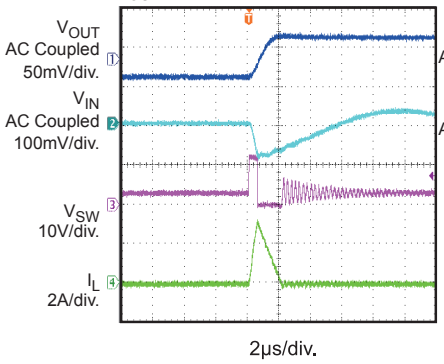
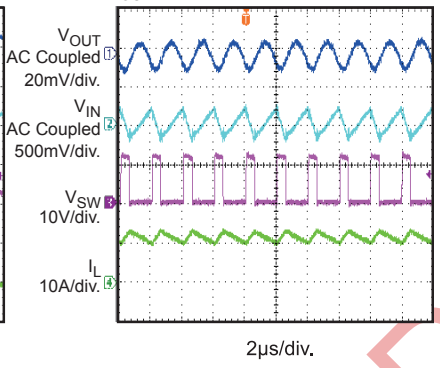
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3V, L = 1µH, T_A = 25ºC, unless otherwise noted.

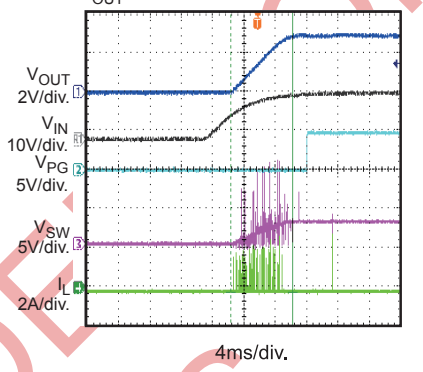
Input/Output Voltage Ripple
I_{OUT}=0A



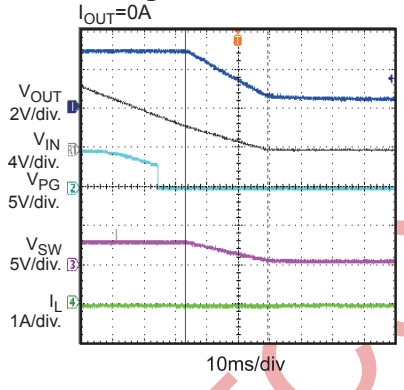
Input/Output Voltage Ripple
I_{OUT}=12A



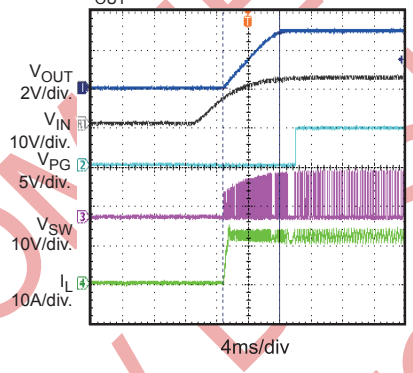
Start Up through Input Voltage
I_{OUT}=0A



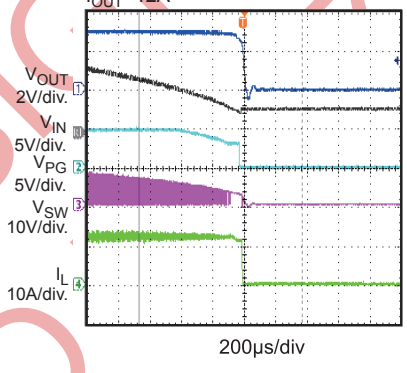
Shutdown through Input Voltage
I_{OUT}=0A



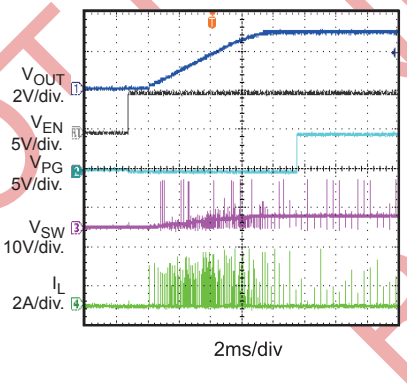
Start Up through Input Voltage
I_{OUT}=12A



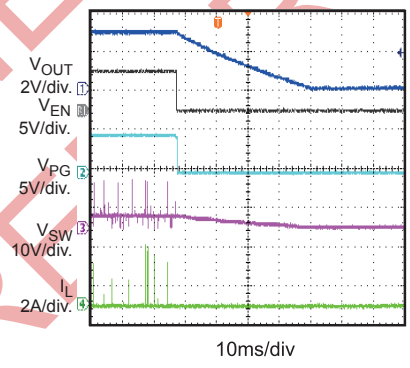
Shutdown through Input Voltage
I_{OUT}=12A



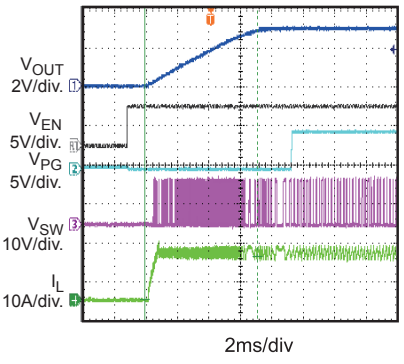
Start Up through EN
I_{OUT}=10mA



Shutdown through EN
I_{OUT}=10mA



Start Up through Enable
I_{OUT}=12A



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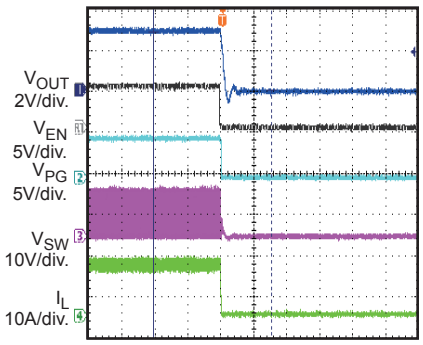
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3V, L = 1µH, T_A = 25ºC, unless otherwise noted.

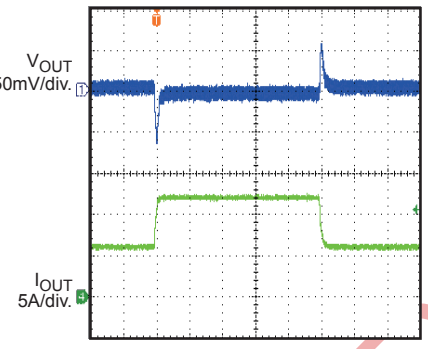
Shutdown through Enable

I_{OUT}=12A

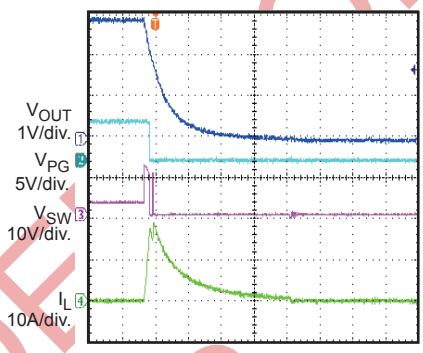


Transient Response

I_{OUT}=6A-12A, 2.5A/µs

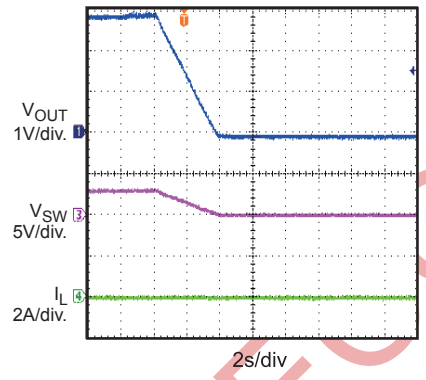


Short Circuit Protection



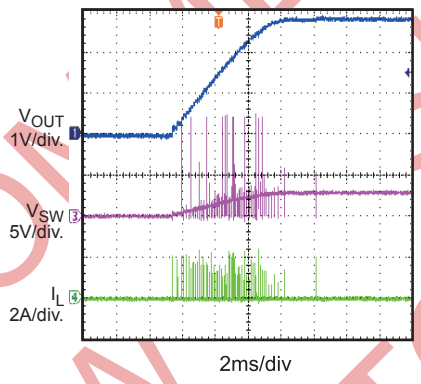
Thermal Shutdown

I_{OUT}=0A, V_{OUT}=3V



Thermal Recovery

I_{OUT}=0A, V_{OUT}=3V



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BLOCK DIAGRAM

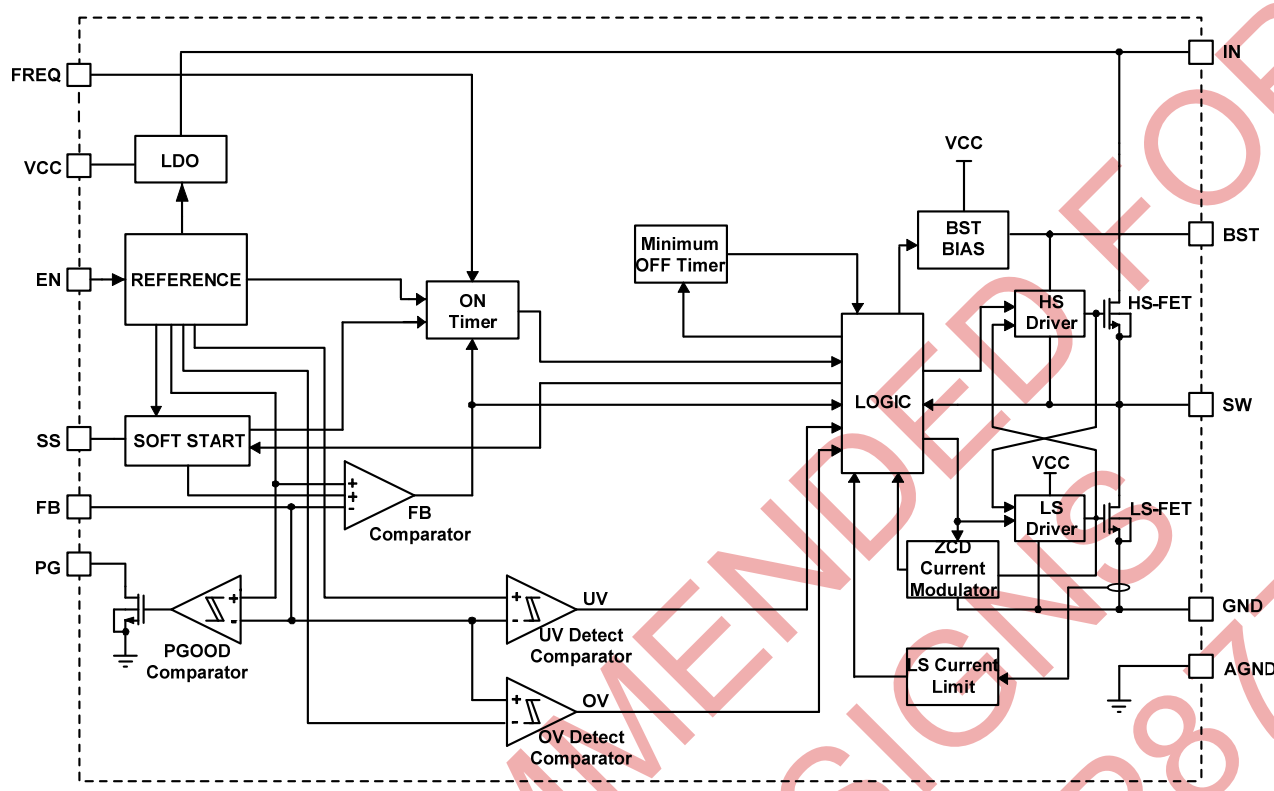

Figure 1—Functional Block Diagram

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OPERATION

PWM Operation

The MP8764 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by the input voltage and the frequency-set resistor as follows:

$$T_{ON}(ns) = \frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \quad (1)$$

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

Heavy-Load Operation

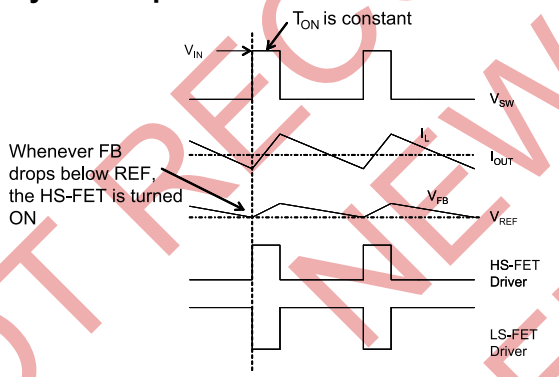

Figure 2—Heavy Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). The CCM mode operation is shown in Figure 2. When V_{FB} is below V_{REF}, HS-FET is turned on for a fixed interval which is determined by one-shot on-timer as equation 1 shown. When the HS-FET is turned off, the LS-FET is turned on until next period.

In CCM mode operation, the switching frequency is fairly constant and it is called PWM mode.

Light-Load Operation

As the load decreases, the inductor current decreases too. When the inductor current touches zero, the operation is transited from continuous-conduction-mode (CCM) to discontinuous-conduction-mode (DCM).

The light load operation is shown in Figure 3. When V_{FB} is below V_{REF}, HS-FET is turned on for a fixed interval which is determined by one- shot on-timer as equation 1 shown. When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes over the control of LS-FET and limits the inductor current to less than -1mA. Hence, the output capacitors discharge slowly to GND through LS-FET. As a result, the efficiency at light load condition is greatly improved. At light load condition, the HS-FET is not turned ON as frequently as at heavy load condition. This is called skip mode.

At light load or no load condition, the output drops very slowly and the MP8764 reduces the switching frequency naturally and then high efficiency is achieved at light load.

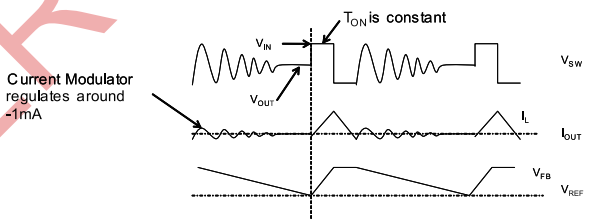

Figure 3—Light Load Operation

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As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

Where F_{SW} is the switching frequency.

It turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Switching Frequency

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and capacitance to maintain low output voltage ripple.

For MP8764，the on time can be set using FREQ pin, then the frequency is set in steady state operation at CCM mode.

Adaptive constant-on-time (COT) control is used in MP8764 and there is no dedicated oscillator in the IC. Connect FREQ pin to IN pin through resistor R_{FREQ} and the input voltage is feed-forwarded to the one-shot on-time timer through the resistor R_{FREQ}. When in steady state operation at CCM, the duty ratio is kept as V_{OUT}/V_{IN}. Hence the switching frequency is fairly constant over the input voltage range. The switching frequency can be set as follows:

$$F_{SW}(kHz) = \frac{10^6}{\frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay. It's about 5ns. After adding load, the frequency may be affected a little because power MOSFET voltage drop will affect the duty cycle.

Generally, the MP8764 is set for 200kHz to 1MHz application. It is optimized to operate at high switching frequency with high efficiency.

High switching frequency makes it possible to utilize small sized LC filter components to save system PCB space.

Jitter and FB Ramp Slope

Figure 4 and Figure 5 show jitter occurring in both PWM mode and skip mode. When there is noise in the V_{FB} downward slope, the ON time of HS-FET deviates from its intended location and produces jitter. It is necessary to understand that there is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope. The slope steepness of the V_{FB} ripple dominates in noise immunity. The magnitude of the V_{FB} ripple doesn't affect the noise immunity directly.

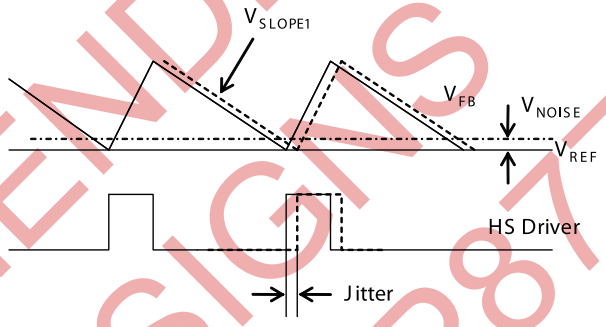

Figure 4—Jitter in PWM Mode

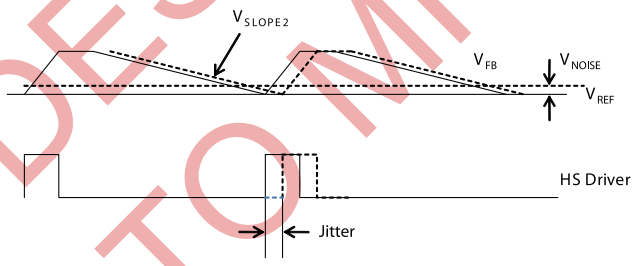

Figure 5—Jitter in Skip Mode

Ramp with Large ESR Capacitor

In the case of POSCAP or other types of capacitor with lager ESR is applied as output capacitor, the ESR ripple dominates the output ripple, and the slope on the FB is quite ESR related. Figure 6 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Turn to application

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information section for design steps with large ESR capacitors.

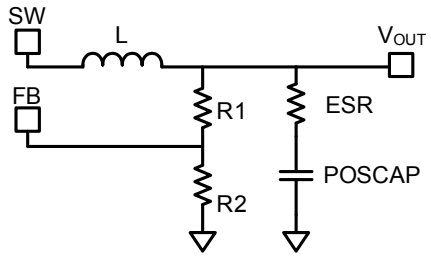

Figure 6—Simplified Circuit in PWM Mode without External Ramp Compensation

To realize the stability when no external ramp is applied, usually the ESR value should be chosen as follow:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}}{C_{OUT}} \quad (4)$$

Where T_{SW} is the switching period.

Ramp with Small ESR Capacitor

When the output capacitors are ceramic ones, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with small ESR caps.

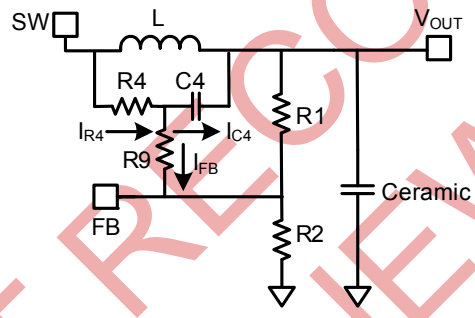

Figure 7—Simplified Circuit in PWM Mode with External Ramp Compensation

In PWM mode, an equivalent circuit with HS-FET off and the use of an external ramp compensation circuit (R4, C4) is simplified in Figure 7. The external ramp is derived from the inductor ripple current. If one chooses C4, R9, R1 and R2 to meet the following condition:

$$\frac{1}{2\pi\times F_{SW}\times C4} < \frac{1}{5}\times\left(\frac{R1\times R2}{R1+R2}+R9\right) \quad (5)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (6)$$

And the ramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN}-V_{OUT}}{R4\times C4}\times T_{ON}\times\left(\frac{R1//R2}{R1//R2+R9}\right) \quad (7)$$

The downward slope of the V_{FB} ripple then follows:

$$V_{SLOPE1} = \frac{V_{RAMP}}{T_{OFF}} = \frac{-V_{OUT}}{R4\times C4} \quad (8)$$

As can be seen from equation 8, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to limitation from equation 5, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be design follow equation 9.

$$-V_{SLOPE1} \geq \frac{\frac{T_{SW}}{0.7\times\pi}+\frac{T_{ON}}{2}-R_{ESR}\times C_{OUT}}{2\times L\times C_{OUT}}\times V_{OUT}+\frac{I_{OUT}\times 10^{-3}}{T_{SW}-T_{ON}} \quad (9)$$

Where I_{OUT} is the load current.

In skip mode, the downward slope of the V_{FB} ripple is almost same whether the external ramp is used or not. Fig.8 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.

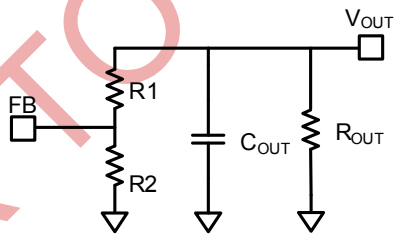

Figure 8—Simplified Circuit in skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as follows:

$$V_{SLOPE2} = \frac{-V_{REF}}{[(R1+R2)//R_{OUT}]\times C_{OUT}} \quad (10)$$

Where R_{OUT} is the equivalent load resistor.

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As described in Fig.5, V_{SLOPE2} in the skip mode is lower than that is in the PWM mode, so it is reasonable that the jitter in the skip mode is larger. If one wants a system with less jitter during ultra light load condition, the values of the V_{FB} resistors should not be too big, however, that will decrease the light load efficiency.

Configuring the EN Control

En high to turn on the regulator and EN low to turn it off. Do not float the pin.

For automatic start-up the EN pin can be pulled up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from **V_{IN}** pin to EN pin) and the pull-down resistor(R_{DOWN} from EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.5 \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} (V) \quad (11)$$

For example, for R_{UP}=100kΩ and R_{DOWN}=51kΩ, the $V_{IN-START}$ is set at 4.44V.

To avoid noise, a 10nF ceramic capacitor from EN to GND is recommended.

There is an internal zener diode on the EN pin, which clamps the EN pin voltage to prevent it from running away. The maximum pull up current assuming a worst case 6V internal zener clamp should be less than 1mA.

Therefore, when EN is driven by an external logic signal, the EN voltage should be lower than 6V; when EN is connected with **V_{IN}** through a pull-up resistor or a resistive voltage divider, the resistance selection should ensure the maximum pull up current less than 1mA.

If using a resistive voltage divider and V_{IN} higher than 6V, the allowed minimum pull-up resistor R_{UP} should meet the following equation:

$$\frac{V_{IN} - 6V}{R_{UP}} - \frac{6V}{R_{DOWN}} \le 1mA \quad (12)$$

Especially, just using the pull-up resistor R_{UP} (the pull-down resistor is not connected), the $V_{IN-START}$ is determined by VCC UVLO, and the minimum resistor value is:

$$R_{UP} \ge \frac{V_{IN} - 6V}{1mA} (\Omega) \quad (13)$$

A typical pull-up resistor is 100kΩ.

External VCC bias

An external 5V VCC bias can disable the internal LDO, in this case, Vin can be as low as 2.5V.

Soft Start

The MP8764 employs soft start (SS) mechanism to ensure smooth output during power-up. When the EN pin becomes high, an internal current source (20μA) charges up the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and it enters into steady state operation.

The SS capacitor value can be determined as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (14)$$

If the output capacitors have large capacitance value, it's not recommended to set the SS time too small. Otherwise, it's easy to hit the current limit during SS.

Pre-Bias Startup

The MP8764 has been designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the soft-start capacitor exceeds the sensed output voltage at the FB pin.

Power Good (PG)

The MP8764 have power-good (PG) output. The PG pin is the open drain of a MOSFET. It should be connected to VCC or other voltage source that is less 5.5V through a pull-up resistor (e.g. 100k). After VCC is ready, the MOSFET is turned on so that the PG pin is pulled to GND before SS is ready. After FB voltage reaches 97% of REF voltage, the PG pin is pulled high after a 2.5ms delay.

When the FB voltage drops to 90% of REF voltage or exceeds 120% of the nominal REF voltage, the PG pin will be pulled low.

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If the MP8764 doesn't work, the PG pin is also pulled low even though this pin is tied to an external DC source through a pull-up resistor(e.g. 100k).

Over-Current Protection (OCP)

The MP8764 features three current limit levels for over-current conditions: high-side peak current limit, low-side valley current limit and low-side negative current limit.

High-side peak current limit: MP8764 has cycle-by-cycle over-current limiting function. During HS-FET ON state, the inductor current is monitored. When the sensed inductor current hits the peak current limit, the HS limit comparator (shown in Figure 1) turns over, the device enters over-current protection mode immediately, turns off HS-FET and turns on LS-FET.

Low-side valley current limit: During LS-FET ON state, the inductor current is also monitored. At the end of OFF time, the LS-FET sourcing current is compared to the internal positive valley current limit. If the LS-FET sourcing current is exceeded the valley current limit, the HS-FET is not turned on and the LS-FET keeps on for the next ON time. Until the LS-FET sourcing current is below the valley current limit the HS-FET is turned on again.

After soft-start ends, if the over-current condition holds 180us, or VFB<300mV and current limit is triggered, MP8764 will trigger latch off protection.

Low-side negative current limit: If the LS-FET sensed negative current exceeds the negative current limit, e.g. over-voltage protection (OVP) the LS-FET is turned off immediately for the the rest of OFF time. In this situation, both MOSFETs are off until the end of a fixed interval. The body diode of HS-FET conducts the inductor current for the fixed time.

Over -voltage Protection (OVP)

The MP8764 monitors the output voltage through a resistor divider feedback (FB) voltage to detect over-voltage on the output.

If the FB voltage is higher than nominal REF voltage but lower than 120% of the REF voltage (0.611V), both MOSFETs are off,

When the FB voltage is higher than 120% but lower than 130% of the REF voltage, the LS-FET will be turned on while the HS-FET keeps off. The LS-FET keeps on until the FB voltage drops below 110% of the REF voltage or the low-side negative current limit is trigged.

If the FB voltage is higher than 130% of the REF voltage, then the device is latched off. Cycling the input power supply or EN is needed to restart.

UVLO protection

The MP8764 has under-voltage lock-out protection (UVLO). When the VCC voltage is higher than the UVLO rising threshold voltage, the MP8764 will be powered up. It shuts off when the VCC voltage is lower than the UVLO falling threshold voltage. This is non-latch protection.

The MP8764 is disabled when the VCC voltage falls below 3.3 V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 9 to adjust the startup input voltage by using two external resistors. It is recommended to use the enable resistors to set the input voltage falling threshold (V_{STOP}) above 3.6 V. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations.

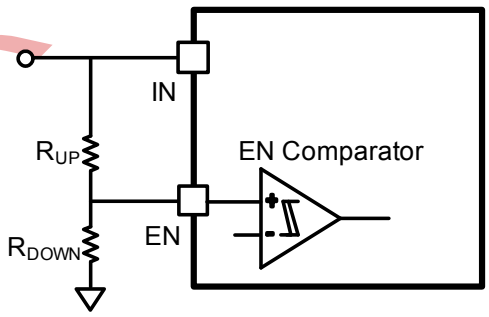

Figure 9—Adjustable UVLO

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Thermal Shutdown

Thermal shutdown is employed in the MP8764. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (minimum 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a soft startup.

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APPLICATION INFORMATION

Setting the Output Voltage-Large ESR Caps

For applications that electrolytic capacitor or POS capacitor with a controlled output of ESR is set as output capacitors. The output voltage is set by feedback resistors R1 and R2. As figure 10 shows.

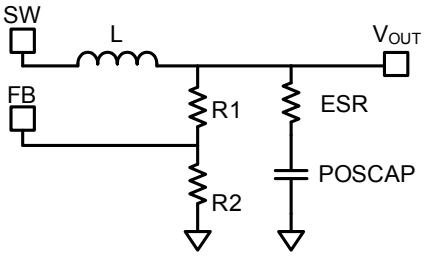

Figure 10—Simplified Circuit of POS Capacitor

First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. Then R1 is determined as follow with the output ripple considered:

$$R1 = \frac{V_{OUT} - \frac{1}{2} \times \Delta V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (15)$$

ΔV_{OUT} is the output ripple determined by equation 24.

Setting the Output Voltage-Small ESR Caps

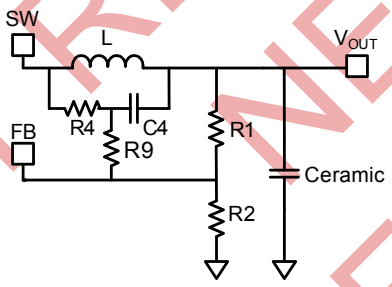

Figure 11—Simplified Circuit of Ceramic Capacitor

When low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4.The output voltage is influenced by ramp voltage V_{RAMP} besides resistor divider as shown in figure 11. The V_{RAMP} can be calculated as shown in equation 7. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when V_{OUT} is low, and a smaller R2 when V_{OUT} is high. And the value of R1 then is determined as follow:

$$R1 = \frac{R2}{\frac{V_{FB(AVG)}}{V_{OUT} - V_{FB(AVG)}} - \frac{R2}{R4 + R9}} \quad (16)$$

The $V_{FB(AVG)}$ is the average value on the FB. $V_{FB(AVG)}$ varies with the V_{IN}, V_{OUT}, and load condition, etc.. Its value on the skip mode would be lower than that of the PWM mode, which means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$,if one wants to gets a better load or line regulation, a lower V_{RAMP} is suggested once it meets equation 9.

For PWM operation, $V_{FB(AVG)}$ value can be deduced from equation 17.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} \times V_{RAMP} \quad (17)$$

Usually, R9 is set to 0Ω, and it can also be set following equation 18 for a better noise immunity. It also should be set to be 5 timers smaller than R1//R2 to minimize its influence on V_{RAMP}.

$$R9 < \frac{1}{5} \times \frac{R1 \times R2}{R1 + R2} \quad (18)$$

Using equation 16 and 17 to calculate the output voltage can be complicated. To simplify the calculation of R1 in equation 11, a DC-blocking capacitor C_{DC} can be added to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using equation 19 for PWM mode operation.

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$$R1 = \frac{V_{OUT} - V_{REF} - \frac{1}{2} \times V_{RAMP}}{V_{REF} + \frac{1}{2} \times V_{RAMP}} \times R2 \quad (19)$$

C_{DC} is suggested to be at least 10 times larger than C4 for better DC blocking performance, and should be not larger than 0.47uF considering start up performance. In case one wants to use larger C_{DC} for a better FB noise immunity, combined with reduced R1 and R2 to limit the C_{DC} in a reasonable value without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still V_{RAMP} related.

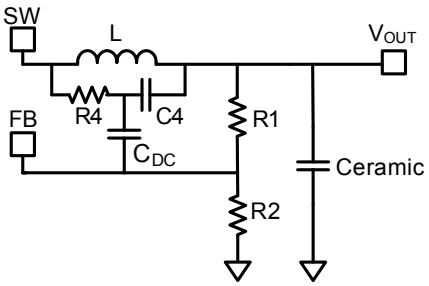

Figure 12—Simplified Circuit of Ceramic Capacitor with DC blocking capacitor

Input Capacitor

The input current to the step-down converter is discontinuous. Therefore, a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance. In the layout, it's recommended to put the input capacitors as close to the IN pin as possible.

The capacitance varies significantly over temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (20)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (21)$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is input voltage ripple requirement in the system design, choose the input capacitor that meets the specification

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (22)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (23)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (24)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4 following equation 5, 8 and 9.

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In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value around 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (26)$$

Inductor

The inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger value inductor will result in less ripple current and lower output ripple voltage. However, a larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 30~40% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (27)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (28)$$

The inductors listed in Table 1 are highly recommended for the high efficiency they can provide.

Table 1—Inductor Selection Guide

Part Number	Manufacturer	Inductance (μH)	DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm³)	Switching Frequency (kHz)
PCMC-135T-R68MF	Cyntec	0.68	1.7	34	13.5 x 12.6 x 4.8	600
FDA1254-1R0M	TOKO	1	2	25.2	13.5 x 12.6 x 5.4	300~600
FDA1254-1R2M	TOKO	1.2	2.05	20.2	13.5 x 12.6 x 5.4	300~600

Typical Design Parameter Tables

The following tables include recommended component values for typical output voltages (1V, 2.5V, 3.3V) and switching frequencies (500kHz). Refer to Tables 2 for design cases without external ramp compensation and Tables 3 for design cases with external ramp compensation. External ramp is not needed when high-ESR capacitors, such as electrolytic or POSCAPs are used. External ramp is needed when low-ESR capacitors, such as ceramic capacitors are used. For cases not listed in this datasheet, a calculator in excel spreadsheet can also be requested through a local sales representative to assist with the calculation.

Table 2—F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R7[8] (kΩ)
1	1	12.7	20	340
2.5	1.5	61.9	20	825
3.3	2.2	88.7	20	1083

Table 3—F_{SW}=500kHz, V_{IN}=12V

V_{OUT} (V)	L (μH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7[8] (kΩ)
1	1	12.7	20	750	220	340
2.5	1.5	64.9	20	1000	220	825
3.3	2.2	93.1	20	1200	220	1083

Notes:

8) Frequency is about 500kHz at full load condition.

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LAYOUT RECOMMENDATION

1. Place high current paths (GND, IN, and SW) very close to the device with short, direct and wide traces.
2. Put a decoupling capacitor as close to the VCC and AGND pins as possible.
3. Keep the switching node (SW) plane as small as possible and far away from the feedback network.
4. Place the external feedback resistors next to the FB pin. Make sure that there are no vias on the FB trace. The feedback resistors should refer to AGND instead of PGND.
5. Keep the BST voltage path (BST, C3, and SW) as short as possible.
6. Recommend strongly a four-layer layout to improve thermal performance.

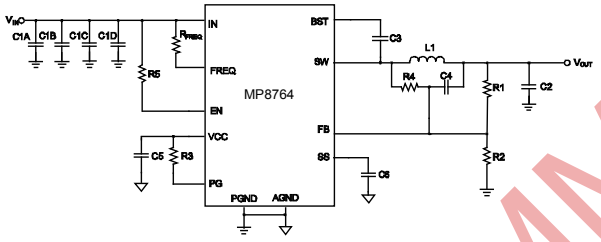
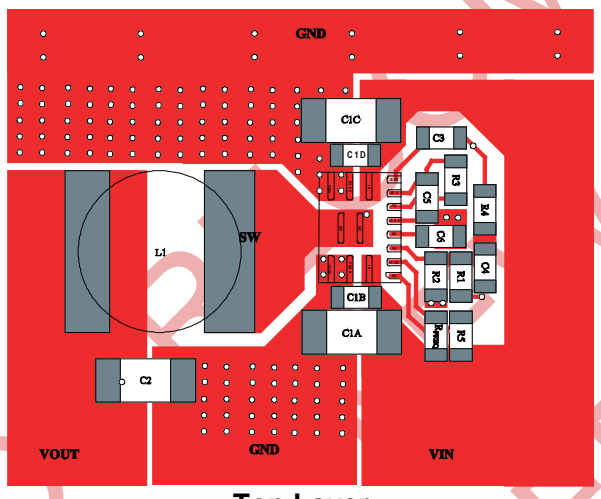
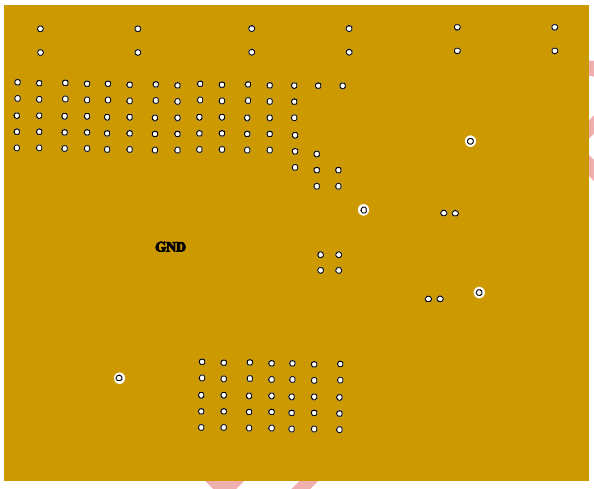


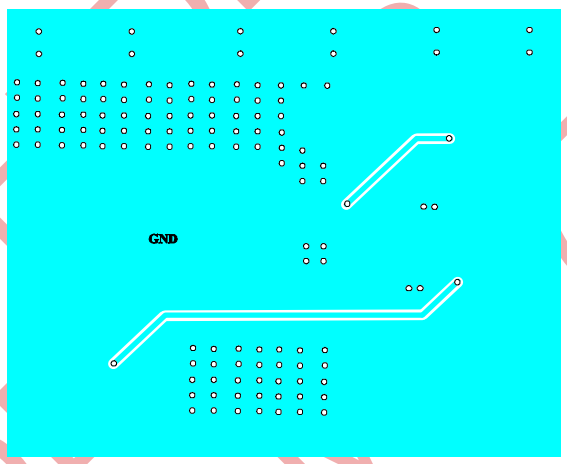
Figure 13—Schematic For PCB Layout Guide



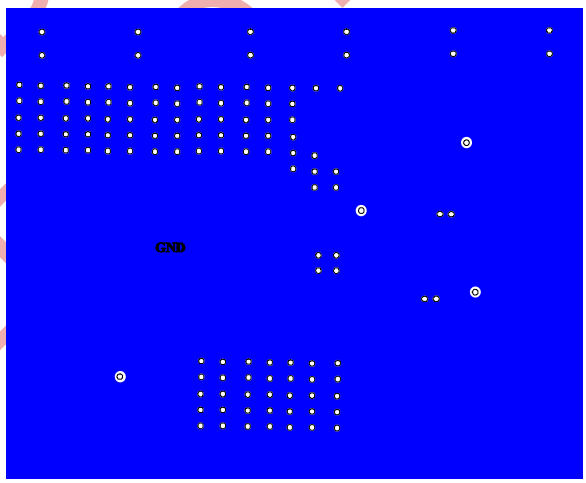
Top Layer



Inner1 Layer



Inner2 Layer



Bottom Layer

Figure 14—PCB Layout Guide for MP8764GLE

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DESIGN EXAMPLE

Table 4 lists the specifications for a design example that follows the application guidelines:

Table 4—Design Example

V_{IN}	12V
V_{OUT}	3V
F_{SW}	500kHz

The detailed application schematic is shown in Figure 15. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheet.

TYPICAL APPLICATION

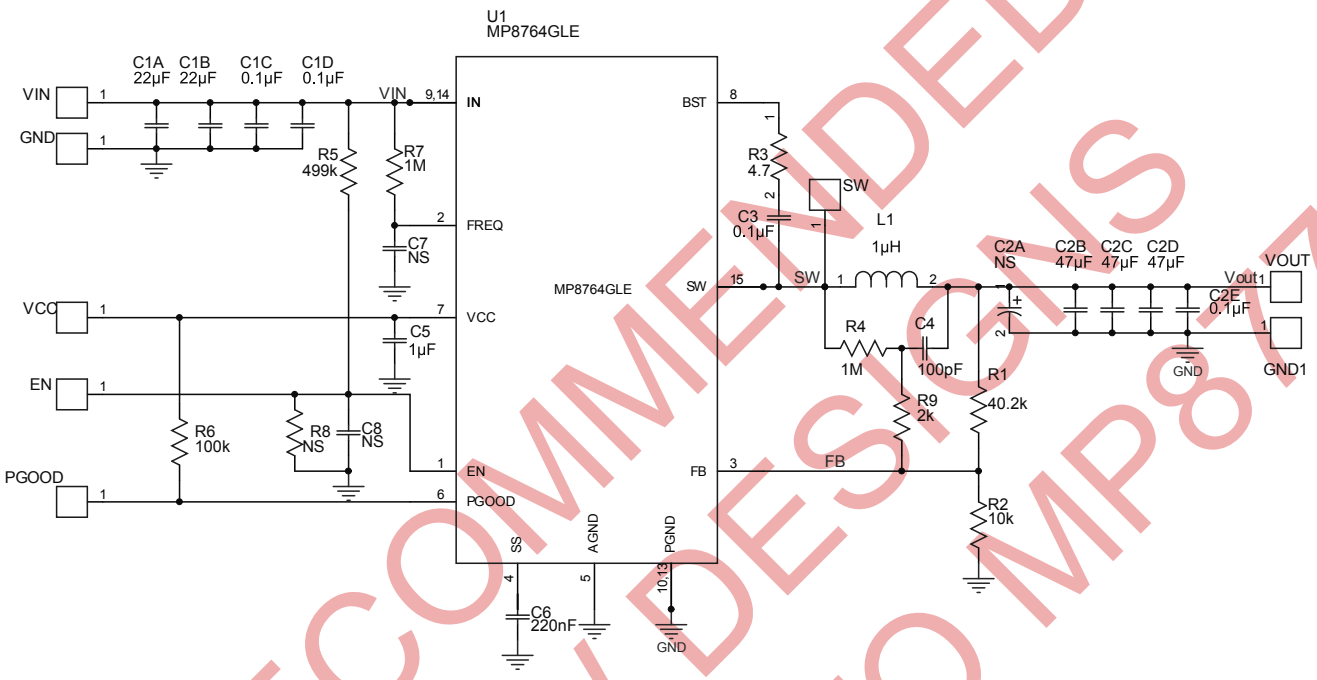

Figure 15—Typical Application Circuit with Low ESR Ceramic Capacitor

V_{IN}=12V, V_{OUT}=3V, I_{OUT}=12A, F_{SW}=500kHz

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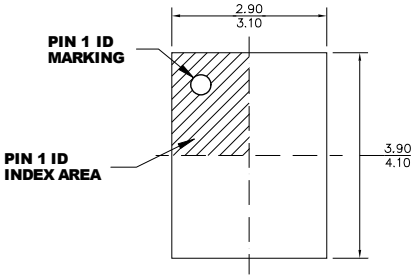
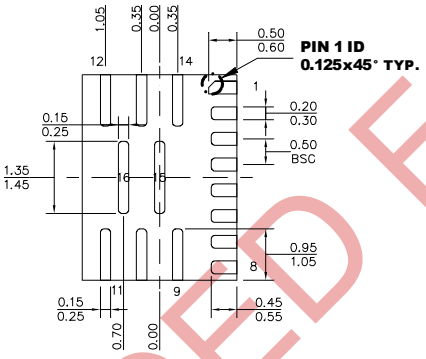
PACKAGE INFORMATION

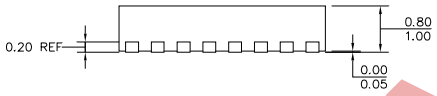
16-Pin QFN (3×4mm)



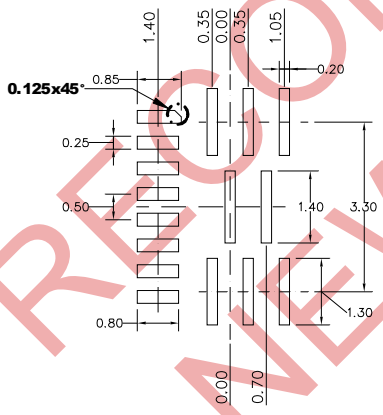
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE

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