# MP87180

## 80A Intelli-Phase™ DrMOS Solution with Quiet Switcher™ Technology and 5V PVCC in a TLGA-41 (5mmx6mm) Package

## DESCRIPTION

The MP87180 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. It can achieve up to 80A of continuous output current across a wide input voltage ($V_{IN}$) range.

The Quiet Switcher™ technology (QST) utilizes a proprietary circuit design that can only be achieved in a monolithic architecture to suppress voltage ringing. This technology limits the peak switching voltage to <2V above $V_{IN}$, improving device reliability, lowering EMI, and reducing sensitivity to PCB layout.

The MP87180 offers many features to simplify system design. The device is compatible with tri-state pulse-width modulation (PWM) signal controllers, has Accu-Sense™ current sensing to monitor the inductor current ($I_L$), and has temperature sensing to report the junction temperature ($T_J$).

The MP87180 is ideal for server and telecommunication applications where efficiency and small size are critical, and is available in a TLGA-41 (5mmx6mm) package.

## FEATURES

- Quiet Switcher™ Technology (QST) Limits Peak Switching Voltages to <2V above the Input Voltage ($V_{IN}$) with Minimal Reliance on PCB Layout
- Wide 3V to 16V Operating $V_{IN}$ Range
- Up to 80A Output Current ($I_{OUT}$)
- 5V PVCC Operation
- Accu-Sense™ Current Sense (CS)
- Temperature Sense
- Tri-State Pulse-Width Modulation (PWM) Signal Compatible
- Over-Current Protection (OCP)
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in a TLGA-41 (5mmx6mm) Package

## APPLICATIONS

- Server Core Voltages
- Telecom and Networking Systems
- Power Modules

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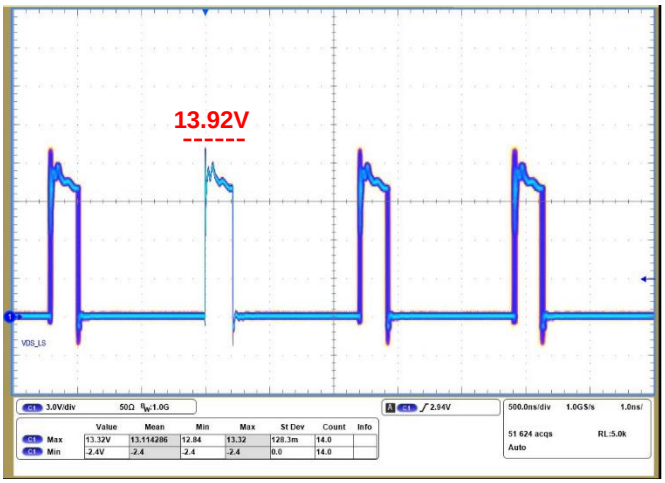
## QUIET SWITCHER WAVEFORM

$V_{IN}$ = 12V, $I_{OUT}$ = 80A, products without QST reach 26.5V





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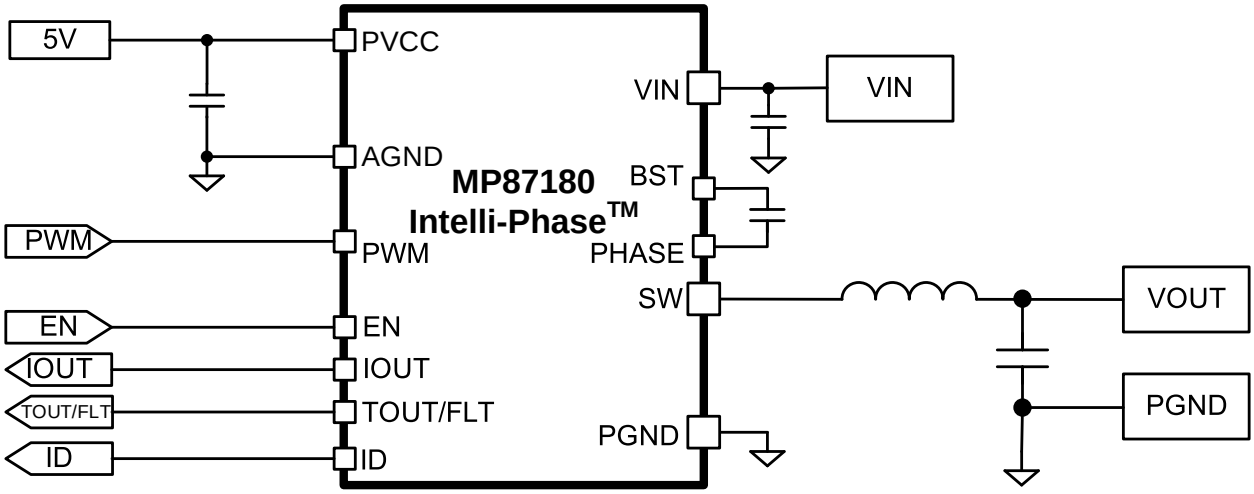
## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP87180GMJTH | TLGA-41 (5mmx6mm) | *See Below* | 3 |

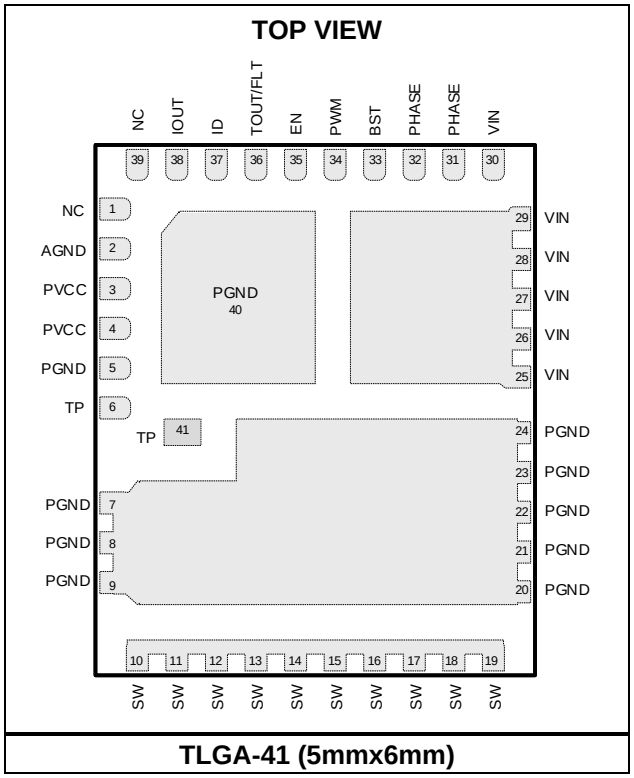
* For Tape & Reel, add suffix -Z (e.g. MP87180GMJTH-Z).

## TOP MARKING
## (MP87180GMJTH)

**MPSYYWW**
**MP87180**
**LLLLLLL**
**TH**

MPS: MPS prefix
YY: Year code
WW: Week code
MP87180: Part number
LLLLLLL: Lot number
TH: Thin package

## PACKAGE REFERENCE




TLGA-41 (5mmx6mm)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## PIN FUNCTIONS

| Pin # | Name | Descriptions |
|---|---|---|
| 1, 39 | NC | **Not connected**. |
| 2 | AGND | **Analog ground**. |
| 3,4 | PVCC | **Supply voltage for the 5V input**. Decouple the PVCC pin using a 1µF to 10µF decoupling capacitor connected to AGND. Connect the AGND and PGND pins at the PVCC capacitor ($C_{PVCC}$). |
| 5, 7, 8, 9, 20, 21, 22, 23, 24, 40 | PGND | **Power ground.** |
| 6, 41 | TP | **Test pin.** Float the TP pin. |
| 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 | SW | **Phase node.** |
| 25, 26, 27, 28, 29, 30 | VIN | **Input voltage.** Place the ceramic input capacitors close to the device to support the switching current with reduced parasitic inductance. |
| 31, 32 | PHASE | **Switching node for the bootstrap capacitor connection.** The PHASE pin is connected to the SW pin internally. |
| 33 | BST | **Bootstrap.** The BST pin requires a 0.1µF to 0.22µF capacitor to drive the power MOSFET's gate above the input voltage ($V_{IN}$). Connect the bootstrap (BST) capacitor ($C_{BST}$) between the BST and PHASE pins to form a floating supply across the power MOSFET driver. |
| 34 | PWM | **Pulse-width modulation input.** Float the PWM pin or pull PWM to a middle-state to force SW into a high impedance (Hi-Z) state. |
| 35 | EN | **Enable.** Pull the EN pin low to disable the device and place SW in a Hi-Z state. |
| 36 | TOUT/FLT | **Single pin temperature sense and fault reporting.** If a fault occurs, the TOUT/FLT pin is pulled up to 3.3V. |
| 37 | ID | **Vender ID voltage output.** Connect the ID pin to the controller that supports the ID function. Float ID if not used. |
| 38 | IOUT | **Current-sense output.** The IOUT pin is a bidirectional current output that is proportional to the inductor current ($I_L$). Connect IOUT to the PWM controller's current-sense input. Connect a resistor to a common-mode voltage to form the differential voltage, which is proportional to $I_L$. |


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## ABSOLUTE MAXIMUM RATINGS (1)

$V_{IN}$ to $V_{PGND}$ .....-0.3V to +20V
$V_{IN}$ to $V_{PHASE}$ (DC) .....-0.3V to +24V
$V_{IN}$ to $V_{PHASE}$ (10ns).....-5V to +32V
$V_{SW}$ to $V_{PGND}$ (DC) .....-0.3V to +20V
$V_{SW}$ to $V_{PGND}$ (10ns) .....-5V to +28V
$V_{BST}$ to $V_{PHASE}$ (DC) .....-0.3V to +4V
$V_{BST}$ to $V_{PHASE}$ (10ns).....-3V to +5V
$V_{PVCC}$, $V_{EN}$ .....-0.3V to +6V
All other pins .....-0.3V to +3.6V
Instantaneous current ..... 130A
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

### *ESD Ratings*

Human body model (HBM).....Class 1C
Charged device model (CDM).....Class C2B

### *Recommended Operating Conditions* (2)

Input voltage ($V_{IN}$) .....3V to 16V
Driver voltage ($V_{PVCC}$).....4.5V to 5.5V
Operating junction temp ($T_J$).... -40°C to +125°C

### *Thermal Resistance* (3) (4) $\theta_{JB}$ $\theta_{JC_TOP}$

TLGA-41 (5mmx6mm)…….....2.5.....2.5....°C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) $\theta_{JB}$ is the thermal resistance from the junction to the board around the PGND soldering point.
4) $\theta_{JC_TOP}$ is the thermal resistance from the junction to the top of the package.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, PVCC = 5V, EN = 3.3V, $T_A$ = 25°C for typical value and $T_J$ = -40°C to 125°C for max and min values, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Shutdown current | $I_{SD}$ | $V_{EN}$ is low | | 5 | | µA |
| $I_{PVCC}$ shutdown | | $V_{EN}$ is low | | 430 | | µA |
| $V_{IN}$ under-voltage lockout (UVLO) rising threshold | | | | 2.5 | 3 | V |
| $V_{IN}$ UVLO hysteresis | | | | 200 | | mV |
| PVCC current | $I_{PVCC}$ | PWM is in a Hi-Z state | | 1.5 | | mA |
| High-side MOSFET (HS-FET) current limit (5) | $I_{LIMIT_TOUT/FLT}$ | Cycle by cycle, up to 10 cycles | | 120 | | A |
| Low-side MOSFET (LS-FET) current limit (5) | | $I_{LIMIT_NEG}$, cycle by cycle, no fault report | | -50 | | A |
| Negative current limit LS-FET off time (5) | | | | 200 | | ns |
| HS-FET current limit shutdown counter (5) | | | | 10 | | times |
| SW rising dead time (DT) (5) | | | | 2 | | ns |
| SW falling DT (5) | | Positive inductor current | | 6 | | ns |
| | | Negative inductor current | | 15 | | ns |
| EN input high voltage | | | 1.4 | | | V |
| EN input low voltage | | | | | 0.9 | V |
| PWM high to SW rising delay (5) | | $V_{EN}$ = 5V | | 260 | | µA |
| PWM low to SW falling delay (5) | $t_{RISING}$ | | | 15 | | ns |
| Negative current limit LS-FET off time (5) | $t_{FALLING}$ | | | 15 | | ns |
| PWM tri-state to SW Hi-Z delay (5) | $t_{LT}$ | | | 40 | | ns |
| | $t_{TL}$ | | | 20 | | ns |
| | $t_{HT}$ | | | 40 | | ns |
| | $t_{TH}$ | | | 20 | | ns |
| Minimum PWM pulse width (5) | | | | 15 | | ns |
| IOUT sense gain accuracy | | $T_J$ = 25°C | -2 | 0 | +2 | % |
| IOUT sense gain | $G_{IOUT}$ | | | 5 | | µA/A |
| IOUT voltage range (5) | $V_{IOUT}$ | | 0.7 | | 2.1 | V |
| TOUT/FLT sense gain (5) | | | | 8 | | mV/°C |
| TOUT/FLT sense offset | | $T_J$ = 25°C | | 800 | | mV |
| Over-temperature protection (OTP) threshold and fault flag (5) | | | | 160 | | °C |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, PVCC = 5V, EN = 3.3V, $T_A$ = 25°C for typical value and $T_J$ = -40°C to 125°C for max and min values, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| PWM source current | | $V_{PWM}$ = 0V | | 500 | | μA |
| PWM sink current | | $V_{PWM}$ = 3.3V | | -500 | | μA |
| ID source current | | $V_{ID}$ = 1.1V | | 720 | | μA |
| ID sink current | | $V_{ID}$ = 1.3V | | -200 | | μA |
| PWM Hi-Z voltage | | PWM is in a Hi-Z state | | 1.6 | | V |
| PWM logic high voltage | | | 2.6 | | | V |
| PWM tri-state range | | | 1.1 | | 2.1 | V |
| PWM logic low voltage | | | | | 0.6 | V |
| ID voltage | | | 1.1 | 1.2 | 1.3 | V |
| ID voltage delay | | | | 100 | | μs |

**Note:**

5) Guaranteed by design or characterization data. Not tested in production.

## PWM TIMING DIAGRAM

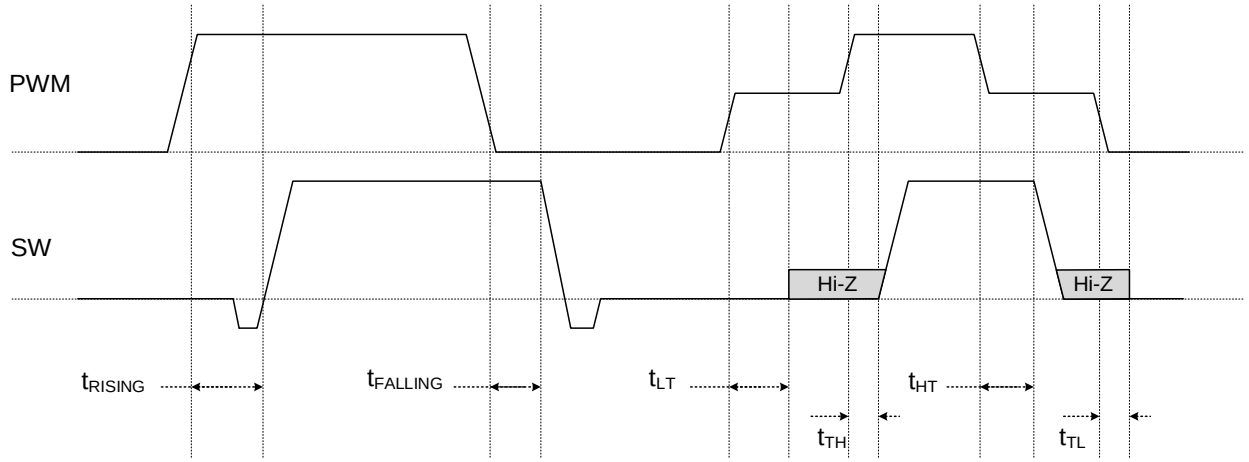


**Figure 1: PWM Timing Diagram**


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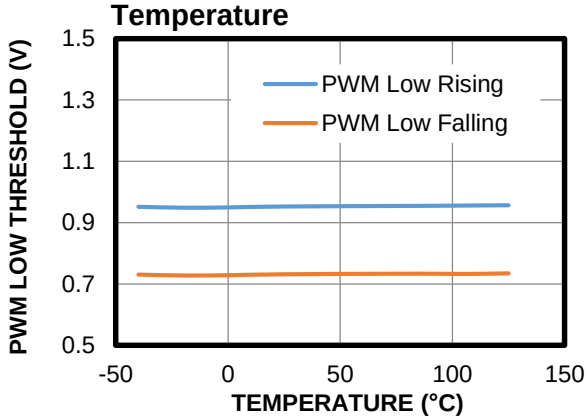
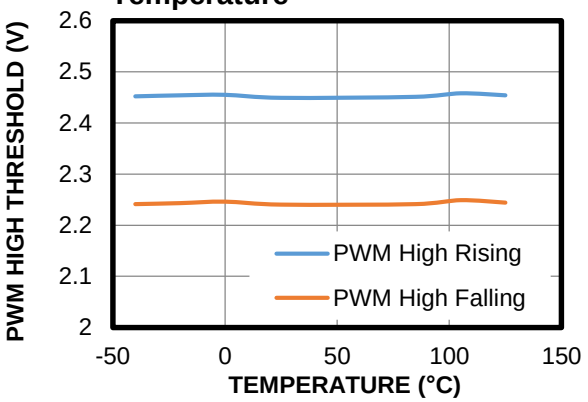
## TYPICAL CHARACTERISTICS

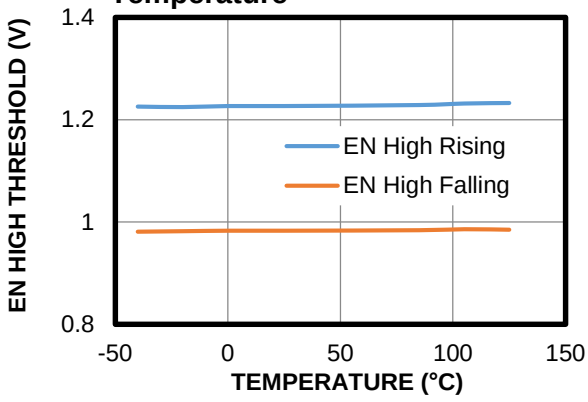
**PWM Low Threshold vs. Temperature**




**PWM High Threshold vs. Temperature**

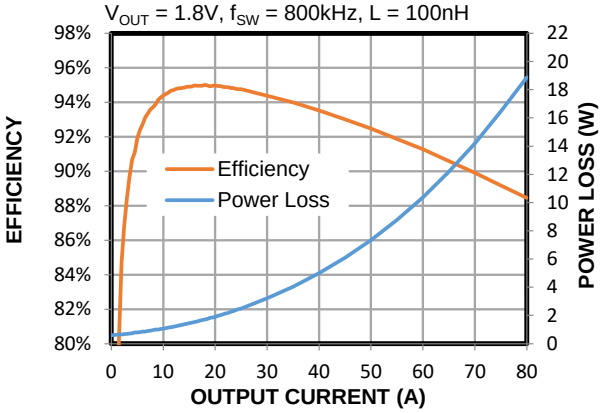



**EN High Threshold vs. Temperature**




**Efficiency vs. Output Current vs. Power Loss**

$V_{OUT}$ = 1.8V, $f_{SW}$ = 800kHz, L = 100nH





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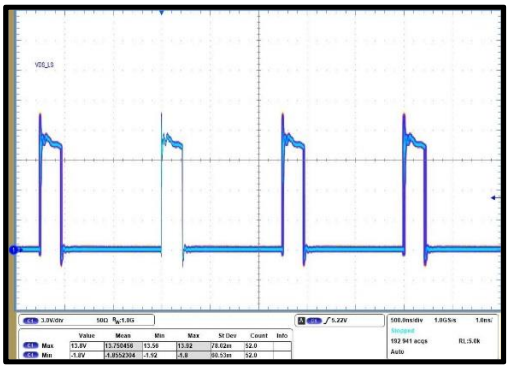
# TYPICAL PERFORMANCE CHARACTERISTICS

### Switching

$V_{IN}$ = 12V, L = 100nH, load = 70A

CH1: $V_{SW}$ 3V/div.

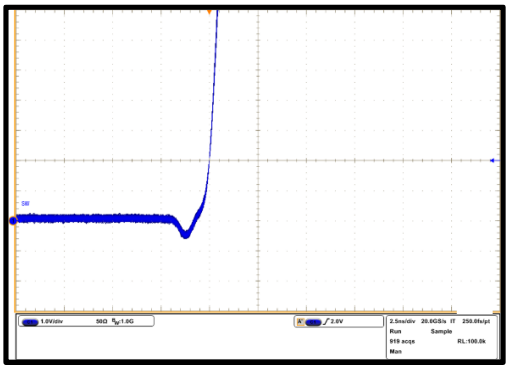


500ns/div.

### SW Rising Dead Time

Load = 30A

CH1: $V_{SW}$ 1V/div.



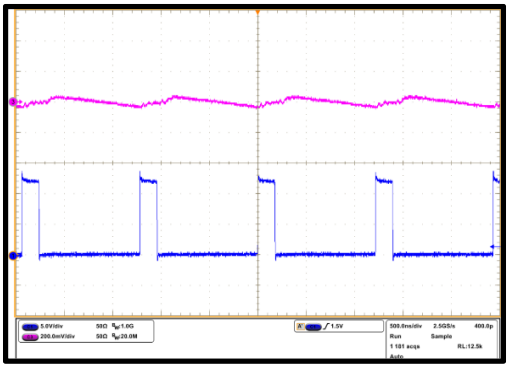
2.5ns/div.

### Current-Sense Output

Load = 0A

CH3: $V_{IOUT}$ 200mV/div.

CH1: $V_{SW}$ 5V/div.



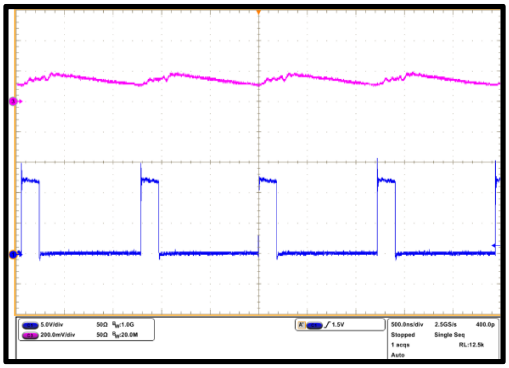
500ns/div.

### Current-Sense Output

Load = 30A

CH3: $V_{IOUT}$ 200mV/div.

CH1: $V_{SW}$ 5V/div.



500ns/div.

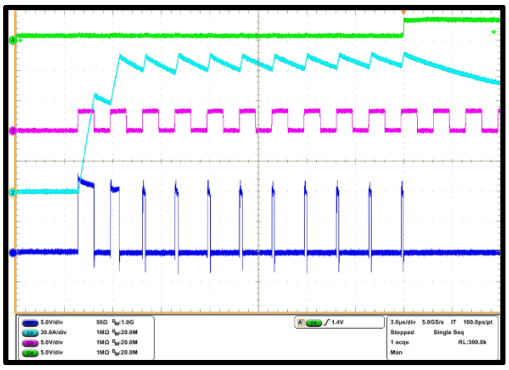
### HS-FET Current Limit

CH4: $V_{FAULT}$ 5V/div.

CH3: $V_{PWM}$ 5V/div.

CH2: $I_L$ 30A/div.

CH1: $V_{SW}$ 5V/div.



3µs/div.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# FUNCTIONAL BLOCK DIAGRAM

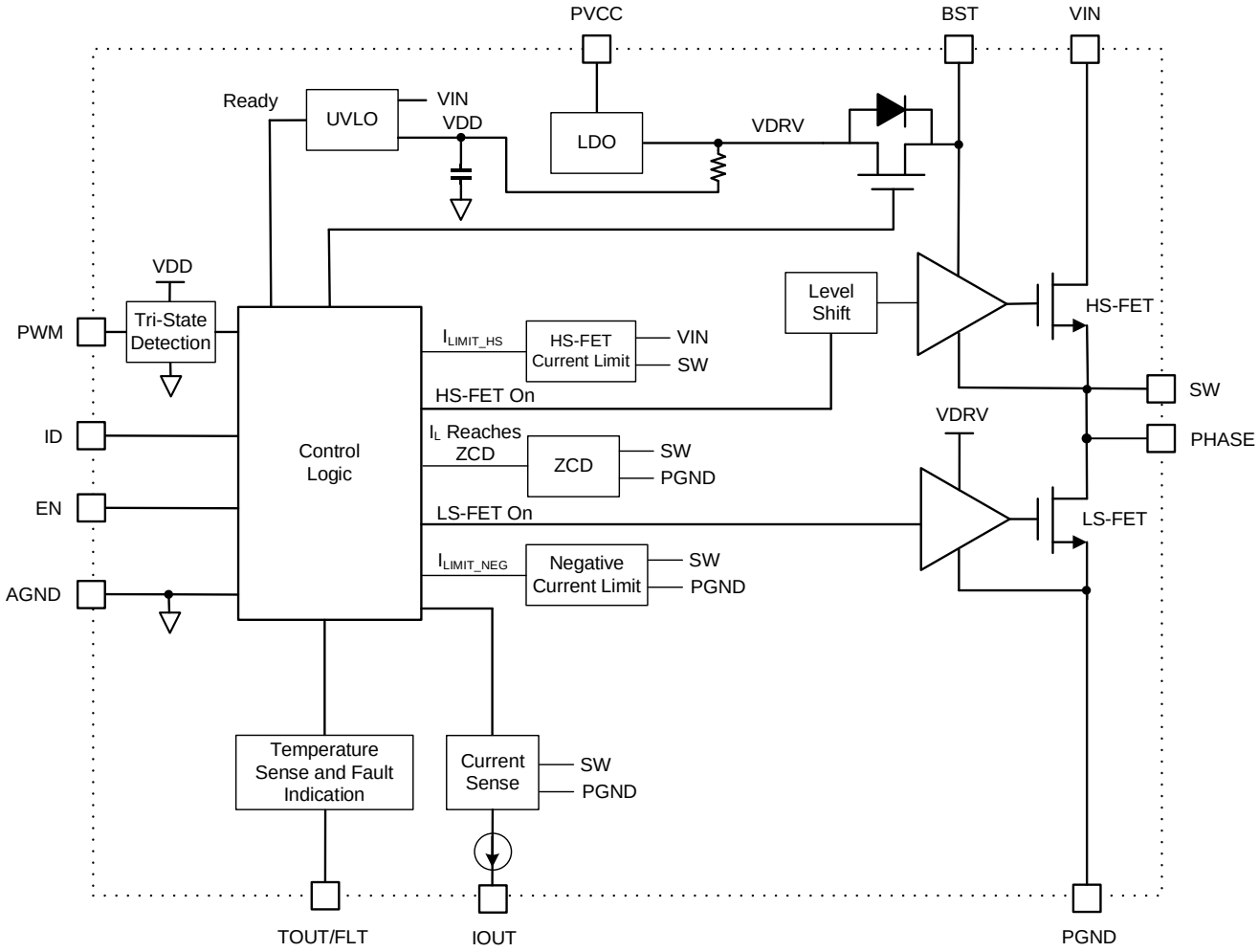


**Figure 2: Functional Block Diagram**


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# OPERATION

The MP87180 is an 80A, monolithic half-bridge driver with integrated that is ideally suited for multi-phase buck regulator applications. An external 5V power supply is required to supply the PVCC pin. Once the VIN, PVCC, and EN signals are sufficiently high, the device begins operating.

### Quiet Switcher™ Technology (QST)

Quiet Switcher™ technology (QST) is a proprietary feedback control architecture that controls the effect of parasitic kickback in the circuit. This suppresses the level of voltage overshoot during fast switching at frequencies up to 1.5MHz.

### Pulse-Width Modulation (PWM)

The pulse-width modulation (PWM) pin can operate as a tri-state input. If the PWM input signal is within the tri-state threshold window ($t_{HT}$ or $t_{LT}$) for a set time (typically 40ns), the high-side MOSFET (HS-FET) turns off and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET operates in diode emulation mode until zero-current detection (ZCD). The tri-state PWM input can come from a forced middle-voltage PWM signal or can be made by floating the PWM pin. The internal current source charges the signal to a middle voltage. See the PWM timing diagram in Figure 1 on page 7 for the propagation delay definition between the PWM and SW pins.

### Diode Emulation Mode

In diode emulation mode, PWM is in a tri-state input. If the inductor current ($I_L$) is positive, then the LS-FET turns on. If $I_L$ is negative or if $I_L$ crosses the ZCD threshold, the LS-FET turns off. Pull PWM to a middle voltage or float PWM to enable diode emulation mode.

### Current Sense (CS)

IOUT is a bidirectional current-source pin that is proportional to $I_L$. The current-sense gain ($G_{IOUT}$) is 5μA/A. If necessary, use a resistor to configure the voltage gain so that it is proportional to $I_L$.

The IOUT pin's output has two states (see Table 1). If the output is disabled (EN is low), then the current-sense circuit is disabled, and IOUT is in a high impedance (Hi-Z) state.

**Table 1: IOUT Output States**

| PWM | EN | IOUT |
|---|---|---|
| PWM | High | Active |
| x | Low | Hi-Z |

An IOUT voltage ($V_{IOUT}$) between 0.7V and 2.1V is required to achieve accurate output current ($I_{OUT}$) reporting. A resistor ($R_{IOUT}$) is typically connected between the IOUT pin and a reference voltage ($V_{CM}$) that is capable of sinking small currents, which provide a sufficient voltage to meet the required operating voltage range.

$V_{CM}$ can be calculated with Equation (1):

$$0.7V < I_{IOUT} \times R_{IOUT} + V_{CM} < 2.1V \quad (1)$$

The IOUT pin's current ($I_{IOUT}$) can be calculated with Equation (2):

$$I_{IOUT} = I_{SW} \times G_{IOUT} \quad (2)$$

The Intelli-Phase™ CS output is used by the controller to accurately monitor $I_{OUT}$. The cycle-by-cycle current information from IOUT can be used for phase-current balancing, over-current protection (OCP), and active voltage positioning (output voltage droop).

### Positive and Negative Inductor Current limit

If an HS-FET over-current (OC) fault is detected, then the HS-FET turns off for one PWM cycle. If an HS-FET OC fault is detected for ten consecutive cycles, then the HS-FET latches off, the TOUT/FLT pin is pulled to 3.3V, and the LS-FET turns on until ZCD. Release the fault latch by toggling EN, or cycling the power on VIN or PVCC.

If the LS-FET detects a -50A valley current, then the LS-FET turns off and the HS-FET turns on for 200ns to limit the negative current cycle by cycle. The LS-FET negative current limit does not trigger a fault report.

### Temperature-Sense Output with Fault Indication (TOUT/FLT)

The TMON/FLT pin has dual functions. It acts as the device's junction temperature sense and fault detection. These functions are described on page 12.


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### *Junction Temperature Sense*

If the part is active, then the TOUT/FLT pin voltage output is proportional to the junction temperature ($T_J$). The gain is 8mV/°C with an 800mV offset at 25°C. For example, $V_{TOUT/FLT}$ is 0.8V at $T_J$ = 25°C, and is 1.6V at $T_J$ = 125°C.

### *Fault Function*

If a fault occurs, TOUT/FLT is pulled to 3.3V to report the fault, regardless of $T_J$. After a 200ns delay, PWM's resistance changes accordingly to indicate the fault event.

Table 2 shows the PWM resistance for each fault event.

**Table 2: PWM Resistance for Each Fault Event**

| Fault Type | PWM |
|---|---|
| Over-current (OC) fault | 10kΩ to AGND |
| Over-temperature (OT) fault | 20kΩ to AGND |
| SW to PGND short | 1kΩ to 3.3V |

TMON/FLT monitors three different fault events: OC, over-temperature (OT), and SW to PGND short.

1. OC fault: Ten consecutive current-limit faults trigger an OC fault. Once a fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns on, then turns off once $I_L$ reaches 0A. The PWM pin uses a 10kΩ resistor connected to AGND to indicate this fault event.
2. OT fault: At $T_J$ > 160°C, the part latches off to turn off the HS-FET. The LS-FET turns on, then turns off once $I_L$ reaches 0A. PWM uses a 20kΩ resistor connected to AGND to indicate this fault event.
3. SW to PGND short: If this fault occurs, the part latches off to turn off the HS-FET. PWM is pulled to 3.3V via a 1kΩ to indicate this fault event.

Release a fault latch by toggling EN, or cycling the power on VIN or PVCC.

For multi-phase operation, connect the TOUT/FLT pin of each Intelli-Phase™ together (see Figure 3).

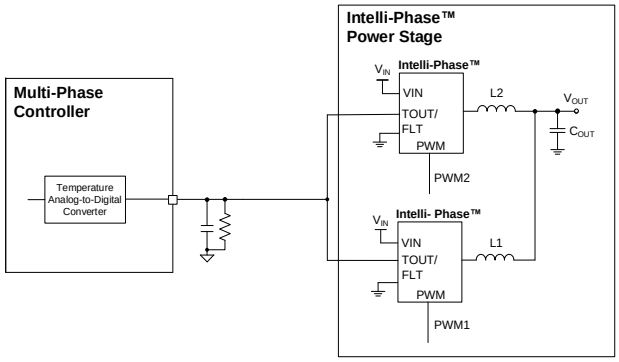


**Figure 3: Multi-Phase Temperature Sense**


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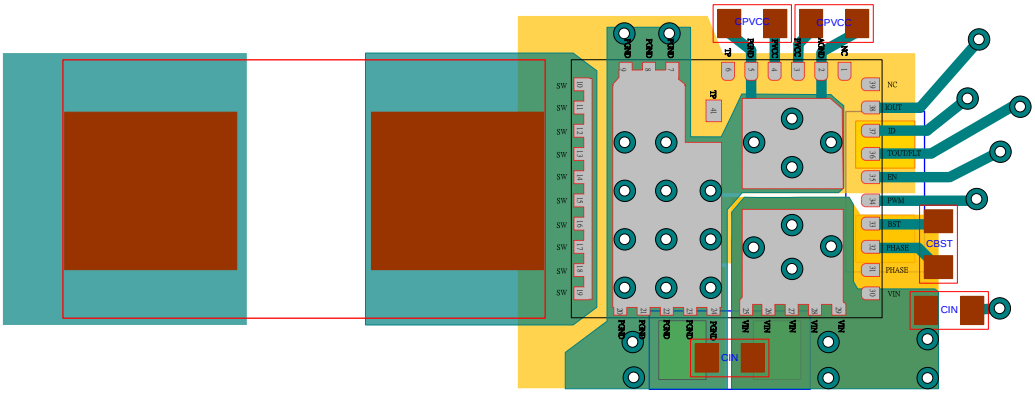
# APPLICATION INFORMATION

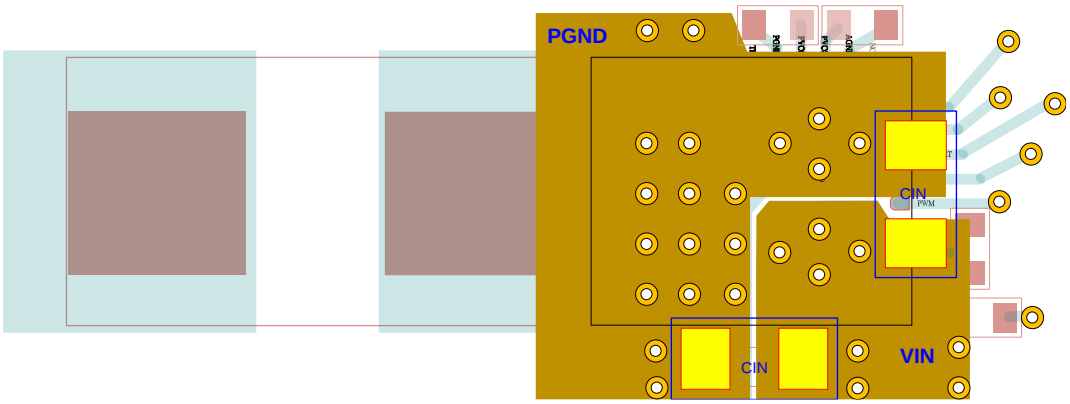
## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the MLCC input capacitors as close to VIN and PGND as possible.
2. Place as many VIN and PGND vias underneath the package as possible. Place these vias between the VIN or PGND long pads.
3. Place a VIN copper plane on mid-layer 2 to form the PCB stack (positive/negative/positive) to reduce parasitic impedance from the MLCC input capacitor to the IC.
4. Ensure that the copper plane on mid-layer 2 at least covers the VIN vias underneath the package and the MLCC input capacitors.
5. Place multiple PGND vias as close to the PGND pin and pad as possible to minimize parasitic resistance, parasitic impedance, and thermal resistance.
6. Place the BST and PVCC capacitor as close to the IC's pins as possible.
7. Route the BST path using a >20mils trace width. Avoid placing vias on the BST driving path.
8. Keep the IOUT signal trace away from high-voltage and high-current slew-rate nodes, such as SW, PWM, the VIN vias, and the PGND vias.




**Placement and Top Layer**




**Placement and Bottom Layer**

**Figure 4: Recommended PCB Layout**

Input Capacitor: 0402 Package (Top Side) and 0805 Package (Bottom Side)

Inductor: 10mmx6mm Package

PVCC and BST Capacitors: 0402 Package

Via Size: 20/10mils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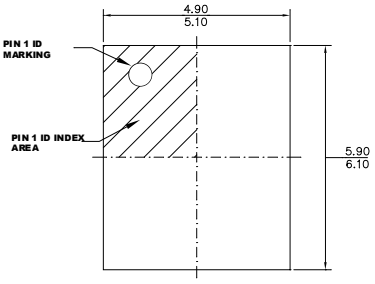
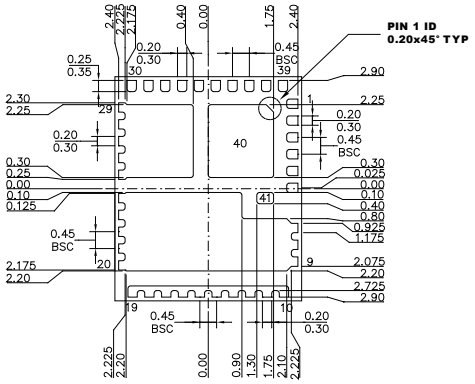
# PACKAGE INFORMATION

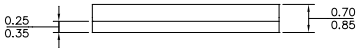
## TLGA-41 (5mmx6mm)



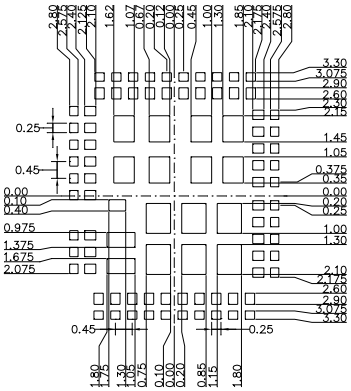

TOP VIEW



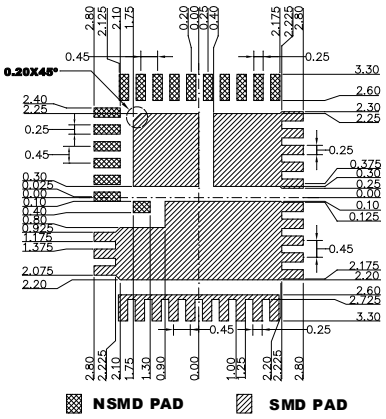

BOTTOM VIEW




SIDE VIEW



RECOMMENDED STENCIL OPENING




RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.
5) THE ACCURACY FOE COMPONENT PLACEMENT SHOULD BE ADJUSTED TO ±30 MICROMETRES.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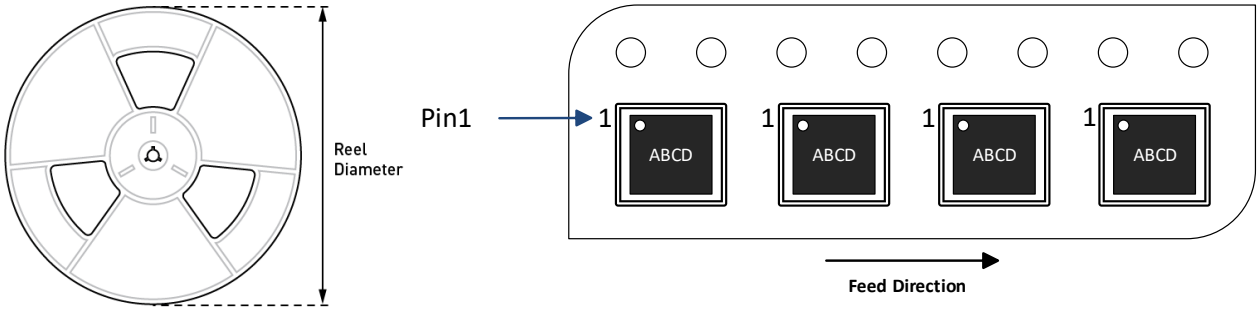
## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP87180GMJTH-Z | TLGA-41 (5mmx6mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |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## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 6/16/2022 | Initial Release | - |
| 1.1 | 7/10/2023 | Updated Figure 4 | 13 |
| | | Updated the Recommended Land Pattern and Recommended Stencil Opening in the Package Information section | 14 |

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