MP86936

Intelli-Phase™ Solution with Integrated Driver and HS-FETs/LS-FETs

DESCRIPTION

The MP86936 is a monolithic half-bridge Intelli-Phase™ solution with built-in internal power MOSFETs and gate drivers. It achieves 60A of continuous output current across a wide input supply range.

The MP86936 utilizes a monolithic IC approach to drive up to 60A per phase. Integrated drivers and MOSFETs provide high efficiency by optimizing dead time and reducing parasitic inductance. This device works with controllers with a tri-state PWM signal, and can operate at frequencies from 100kHz to 3MHz.

Features to simplify system design include an accurate current sense (Accu-Sense™) to monitor the inductor current, and temperature sense to report the junction temperature.

The MP86936 is ideal for server applications where efficiency and small size are at a premium. It is available in a very small TQFN-23 (3mmx6mm) package.

FEATURES

- Wide 3V to 16V Operating Input Range
- 60A Output Current
- Accu-Sense™ Current Sense
- Temperature Sense
- Accepts Tri-State PWM Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in a 3mmx6mm TQFN-23 Package

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Power Modules

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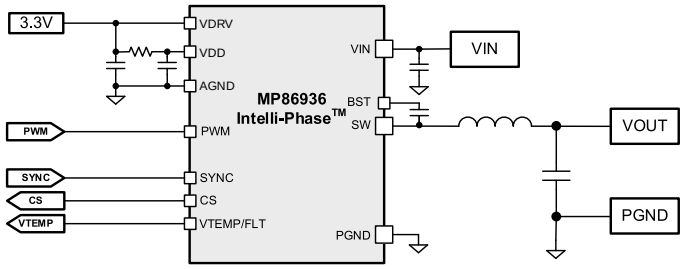
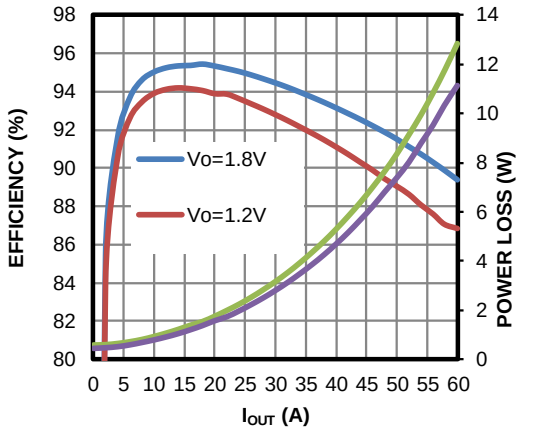
TYPICAL APPLICATION



Efficiency vs. Output Current vs. Power Loss

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 500kHz, L = 150nH



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP86936GRJT*	TQFN-23 (3mmx6mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP86936GRJT-Z).

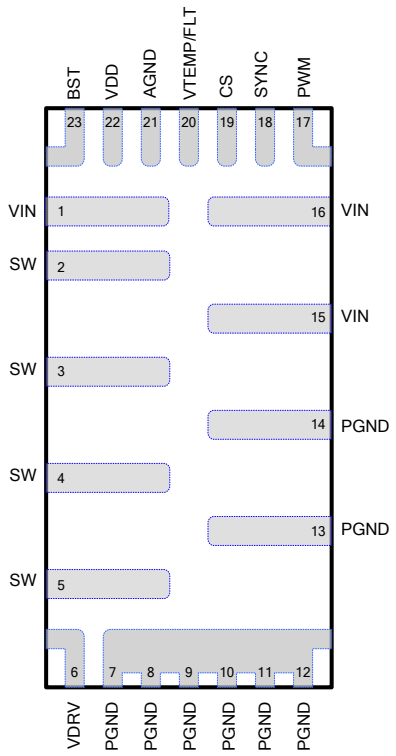
TOP MARKING

MPYW
8693
6LLL

MP: MPS prefix
Y: Year code
W: Week code
86936: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



TQFN-23 (3mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 15, 16	VIN	**Supply voltage.** Place the input capacitor (C_{IN}) close to the device to support the switching current and reduce voltage spikes at the input.
2, 3, 4, 5	SW	**Phase node.**
6	VDRV	**Driver voltage.** Connect this pin to a 3.3V supply and decouple with a 1µF to 4.7µF ceramic capacitor.
7, 8, 9, 10, 11, 12, 13, 14	PGND	**Power ground.**
17	PWM	**Pulse width modulation (PWM) input.** Leave PWM floating or drive it to a mid-state to put SW in a high-impedance state.
18	SYNC	**Diode emulation mode and standby mode selection.** Leave SYNC floating or drive it to a mid-state to enter standby mode. Pull this pin high for continuous conduction mode (CCM). Pull this pin low to enable diode emulation mode.
19	CS	**Current-sense output.** Use an external resistor to adjust the voltage to be proportional to the inductor current.
20	VTEMP/FLT	**Single-pin temperature sense and fault reporting.** If a fault occurs, this pin is pulled up to 3.3V.
21	AGND	**Analog ground.**
22	VDD	**Internal circuitry voltage.** Connect this pin to VDRV through a 2.2Ω resistor and decouple with a 1µF capacitor to AGND. Connect AGND and PGND at the VDD capacitor.
23	BST	**Bootstrap.** BST requires a 0.1µF to 0.22µF capacitor to drive the power switch gate above the supply voltage. Connect the capacitor between SW and BST pins to form a floating supply across the power switch driver.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{IN} to V_{SW} (DC) ..... -0.3V to +25V
V_{IN} to V_{SW} (10ns) ..... -5V to +32V
V_{SW} to PGND (DC) ..... -0.3V to V_{IN} + 0.3V
V_{SW} to PGND (25ns) ..... -5V to +25V
V_{BST} ..... V_{SW} + 4V
V_{DD}, V_{DRV} ..... -0.3V to +4V
All other pins ..... -0.3V to V_{DD} + 0.3V
Instantaneous current 95A
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... Class 1C
Charged device model (CDM) ..... Class C2B

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) ..... 3.0V to 16V
Driver voltage (V_{DRV}) ..... 3.0V to 3.6V
Logic voltage (V_{DD}) ..... 3.0V to 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

TQFN-23 (3mmx6mm) ..... 1.8 ..... 15… °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB}: Thermal resistance from the junction to board around the PGND soldering point.
   θ_{JC_TOP}: Thermal resistance from the junction to the top of the package.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DRV} = V_{DD} = SYNC = 3.3V, typical values at T_A = 25°C and max and min values at T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown	I_{IN_OFF}	SYNC = Hi-Z		90	180	µA
V_{IN} under-voltage lockout (UVLO) rising threshold				2.5	3.0	V
V_{IN} UVLO hysteresis				450		mV
I_{VDRV} quiescent current		PWM = low		250	350	µA
I_{VDD} quiescent current		PWM = low		4		mA
V_{DD} UVLO rising threshold				2.65	2.9	V
V_{DD} UVLO hysteresis				300		mV
High-side current limit (4)	I_{LIM_FLT}	Cycle by cycle up to four cycles		90		A
Low-side current limit (4)		Negative current limit, cycle by cycle, no fault report		-30		A
Negative current limit low-side off time (4)				200		ns
High-side current limit shutdown counter (4)				4		times
Dead time rising (4)				2		ns
Dead time falling (4)		Positive inductor current		6		ns
		Negative inductor current		25		ns
SYNC logic high voltage		V_{DD} = 3V	2.4			V
		V_{DD} = 3.6V	2.6			V
SYNC tri-state region		V_{DD} = 3V	1.10		1.65	V
		V_{DD} = 3.6V	1.3		1.95	V
SYNC logic low voltage		V_{DD} = 3V			0.6	V
		V_{DD} = 3.6V			0.7	V
PWM high to SW rising delay (4)	t_{RISING}			15		ns
PWM low to SW falling delay (4)	$t_{FALLING}$			15		ns
PWM tri-state to SW Hi-Z delay(4)	t_{LT}			40		ns
	t_{TL}			50		ns
	t_{HT}			40		ns
	t_{TH}			50		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

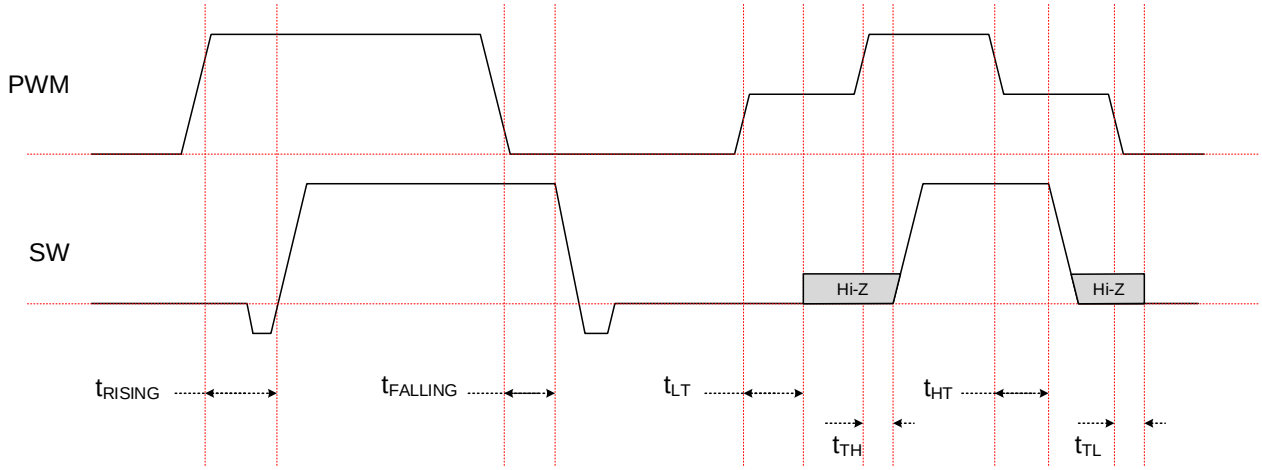
V_{IN} = 12V, V_{DRV} = V_{DD} = SYNC = 3.3V, typical values at T_A = 25°C and max and min values at T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum PWM pulse width (4)				30		ns
Current-sense (CS) gain accuracy (4)		20A ⩽ I_{SW} ⩽ 60A	-2		+2	%
CS gain				8.5		µA/A
CS offset		I_{SW} = 0A, V_{CS} = 1.2V, T_J = 25°C	-2		+2	µA
		SW = Hi-Z, V_{CS} = 1.2V	-1		+1	µA
CS voltage range (4)	V_{CS}		0.7		2.1	V
VTEMP/FLT sense gain (4)				10		mV/°C
VTEMP/FLT sense offset (4)		T_J = 25°C		150		mV
Over-temperature (OT) shutdown and fault flag (4)				160		°C
VTEMP/FLT when a fault occurs			3.0	3.3		V
PWM resistor		Pull up, SYNC = low or high		6		kΩ
		Pull down		5		kΩ
PWM logic high voltage		V_{DD} = 3V	2.40			V
		V_{DD} = 3.6V	2.40			V
PWM tri-state region		V_{DD} = 3V	1.10		1.80	V
		V_{DD} = 3.6V	1.10		1.80	V
PWM logic low voltage		V_{DD} = 3V			0.80	V
		V_{DD} = 3.6V			0.80	V

Notes:

4) Guaranteed by design or characterization data. Not tested in production.

PWM TIMING DIAGRAM



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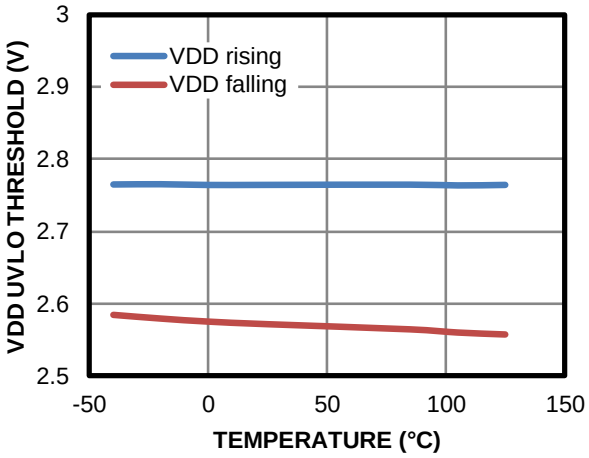
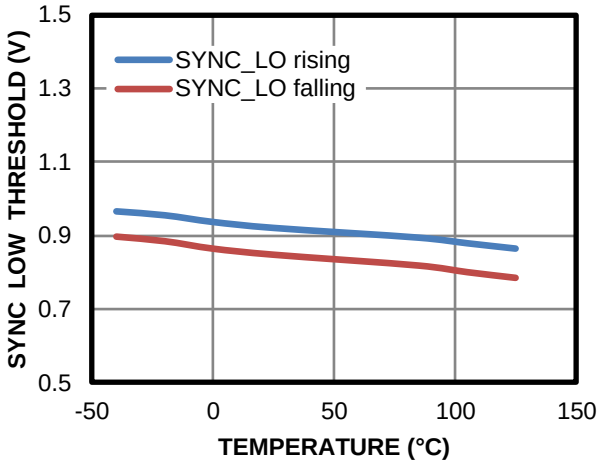
TYPICAL CHARACTERISTICS

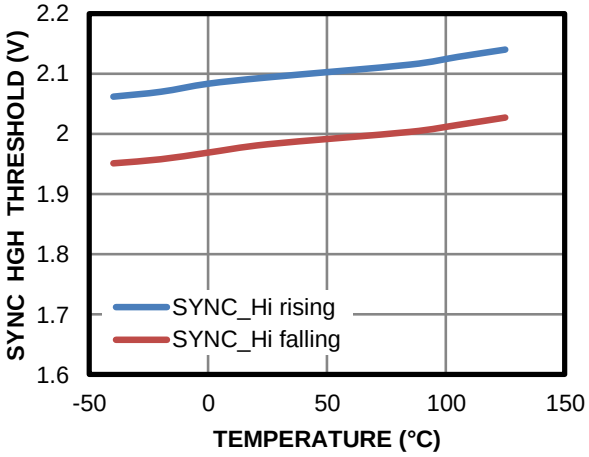
VDD UVLO Threshold vs. Temperature



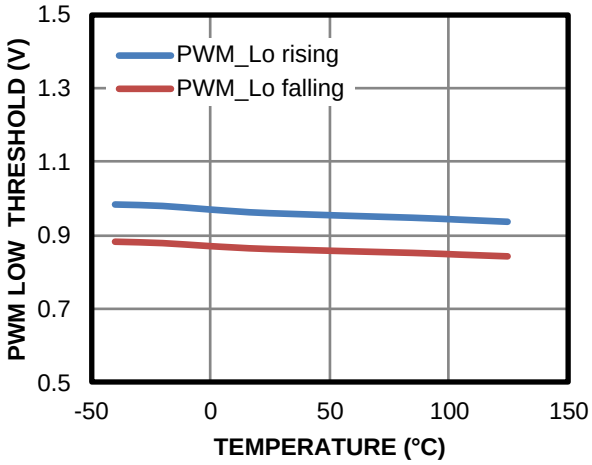
SYNC Low Threshold vs. Temperature



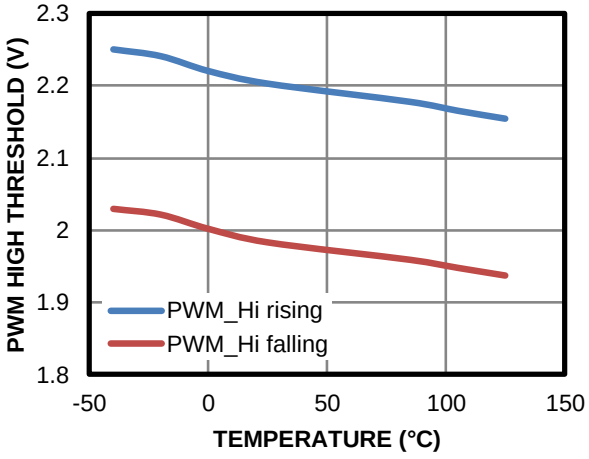
SYNC High Threshold vs. Temperature



PWM Low Threshold vs. Temperature

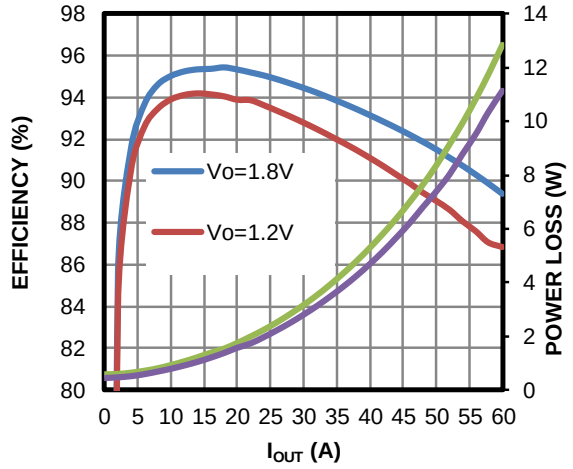


PWM High Threshold vs. Temperature



Efficiency vs. Output Current vs. Power Loss

V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 500kHz, L = 150nH



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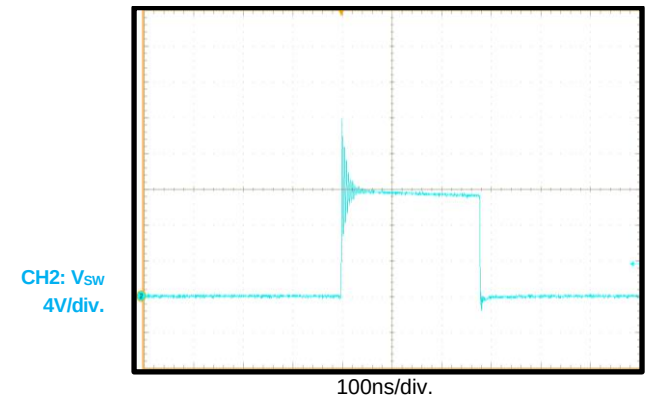
TYPICAL PERFORMANCE CHARACTERISTICS

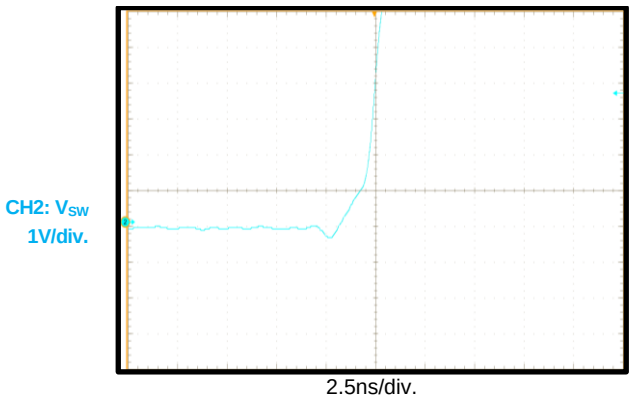
Switching Waveform

V_{IN} = 12V, L = 150nH, I_{OUT} = 30A



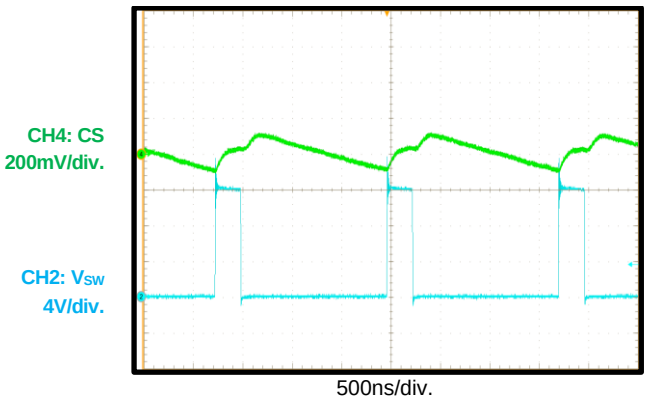
Dead Time at SW Rising

I_{OUT} = 30A



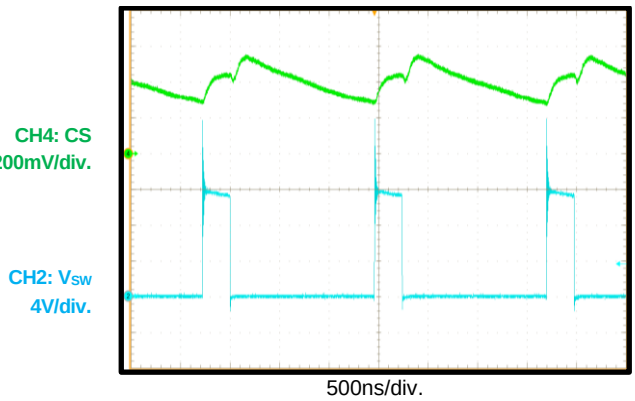
Current-Sense Output Waveform

I_{OUT} = 0A

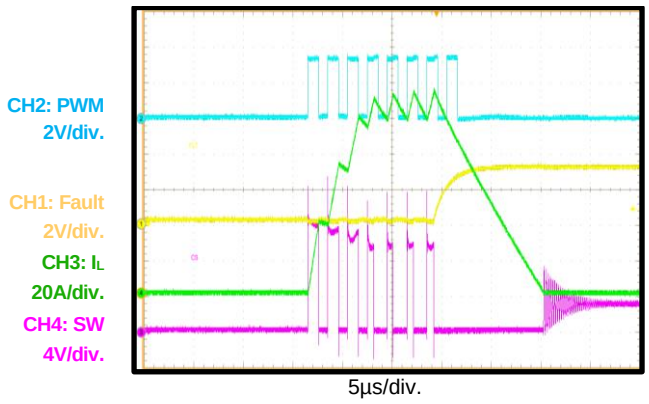


Current-Sense Output Waveform

I_{OUT} = 30A



High-Side Current Limit



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FUNCTIONAL BLOCK DIAGRAM

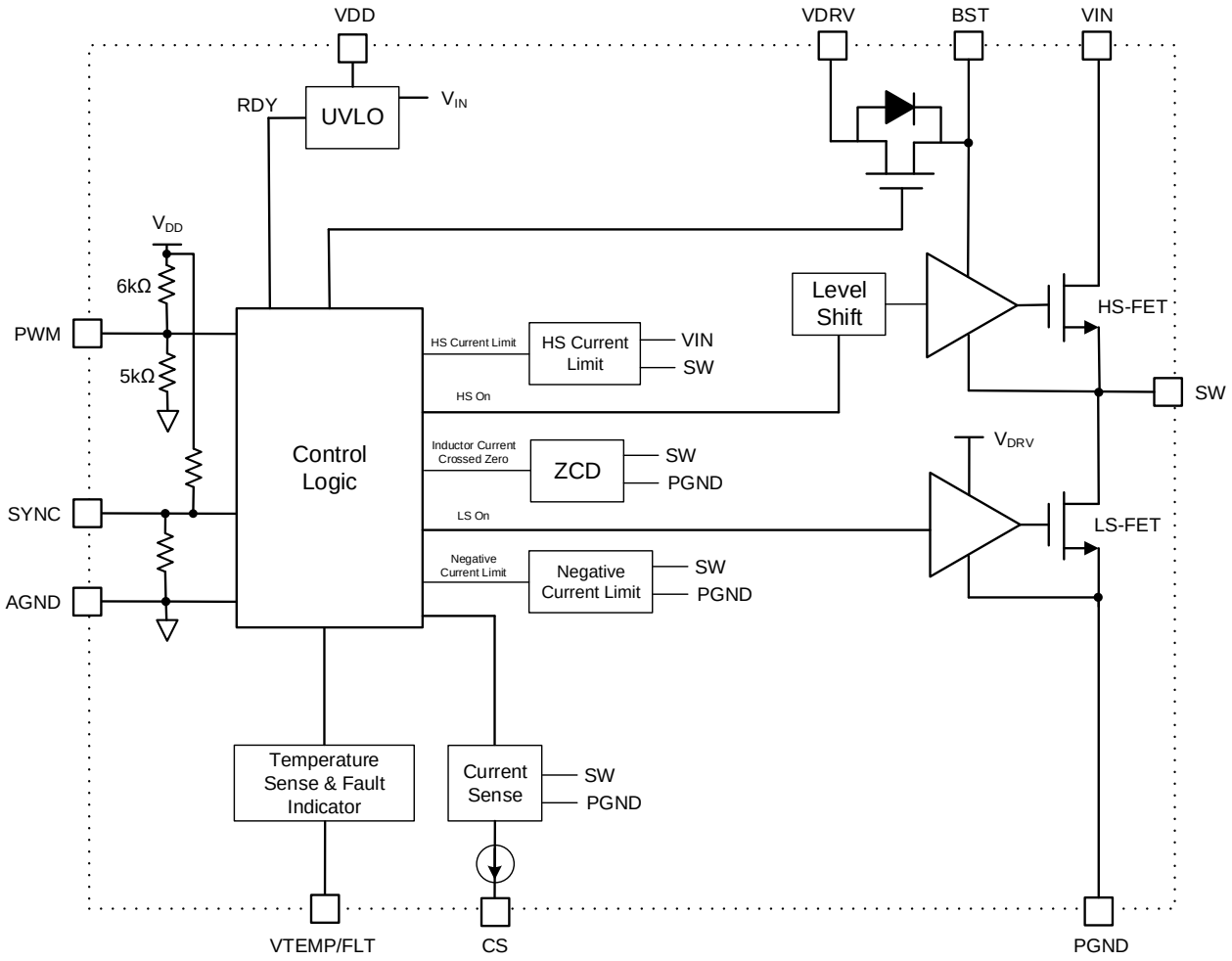

Figure 1: Functional Block Diagram

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OPERATION

The MP86936 is a 60A, monolithic half-bridge driver with integrated MOSFETs. This Intelli-Phase™ solution is ideal for multi-phase buck regulators. An external 3.3V is required to supply both VDD and VDRV. When the VIN and VDD signals are sufficiently high, operation begins.

APPLICATION INFORMATION

Pulse-Width Modulation (PWM)

The PWM pin is capable of handling tri-state input. When the PWM input signal is within the tri-state threshold window for 50ns, the high-side MOSFET (HS-FET) turns off and the low-side MOSFET (LS-FET) turns on and remains in diode emulation mode until zero-current detection (ZCD) is reached. The tri-state PWM input can be from a forced mid-voltage PWM signal or made by floating the PWM input, in which case the internal current source charges the signal to a middle voltage. See the PWM Timing Diagram on page 5 for the propagation delay definition from PWM to the SW node.

Standby Mode

When the SYNC pin is floating or forced to a mid-state voltage for 2μs, the MP86936 enters standby mode. In standby mode, the part shuts down and both the CS and VTEMP/FLT outputs are disabled. The fault latch (VTEMP/FLT) is not be reset by entering standby mode.

Diode Emulation Mode

In diode emulation mode, if PWM is either low or in tri-state input and the inductor current (I_L) is positive, the LS-FET turns. The LS-FET turns off if I_L goes negative or crosses the ZCD threshold. Diode emulation mode can be enabled by any of the following conditions:

- Pulling the SYNC pin low
- Drive PWM to a middle state
- Floating the PWM pin

Current Sense (CS)

CS is a bidirectional current source proportional to I_L. The current-sense gain (G_{CS}) is 8.5μA/A, and a resistor is used to program the voltage gain proportional to I_L if needed.

The CS output has two states: active and standby (see Table 1). In standby mode, the CS circuit is disabled, and requires 40μs to wake up from standby mode to active mode.

Table 1: CS Output States

PWM	SYNC	CS
PWM	Hi	Active
PWM	Low	Active
x	Hi-Z (or middle)	Standby

The CS voltage (V_{CS}) range (0.7V to 2.1V) is required to achieve an accurate CS current output report. Connect a resistor (R_{CS}) from the CS pin to an external voltage that is capable of sinking a small current to provide enough voltage to meet the required operating voltage range. A proper reference voltage (V_{CM}) and R_{CS} value can be calculated with Equation (1):

$$0.7V < I_{CS} \times R_{CS} + V_{CM} < 2.1V \quad (1)$$

Where V_{CM} is a reference voltage connected to R_{CS}.

I_{CS} can be calculated with Equation (2):

$$I_{CS} = I_L \times G_{CS} \quad (2)$$

The Intelli-Phase™'s current-sense output can be used by the controller to accurately monitor the output current (I_{OUT}). The cycle-by-cycle current information from the CS pin can be used for phase current balancing, over-current protection (OCP), and active voltage positioning (output voltage droop).

Positive and Negative Inductor Current limit

If an over-current (OC) condition is detected on the HS-FET, the HS-FET turns off for that PWM cycle. If the HS current limit is exceeded for four consecutive cycles, then the HS-FET latches off, VTEMP/FLT is pulled high to VDD, the LS-FET turns on until ZCD is reached, and then the LS-FET turns off. Recycle the power on VIN and VDD to release the latch and restart the device. Once the latch is released and the MP86936 restarts, it resumes normal operation.

If the LS-FET detects a -30A current, the LS-FET turns off for 200ns to limit the negative current. The LS-FET's negative current limit does not trigger a fault report.

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Temperature-Sense Output with Fault Indicator (VTEMP/FLT)

VTEMP/FLT is a pin with dual functions:

1. Junction temperature sense: VTEMP/FLT is a voltage output proportional to the junction temperature (T_J) whenever V_{DD} is above its under-voltage lockout (UVLO) threshold and the part is in active mode. The gain is 10mV/°C, with a 150mV offset at 25°C. For example, the gain is 0V at T_J < 10°C, 0.15V at T_J = 25°C, and 0.9V at T_J = 100°C.
2. Fault indication: If any fault occurs, the VTEMP/FLT pin is pulled to V_{DD} (regardless of the temperature) to report the fault event. If the fault lasts for longer than 200ns, the PWM impedance changes accordingly to represent the fault type. Table 2 shows the PWM status regarding each fault event.

Table 2: PWM Resistance when a Fault Occurs

Fault Type	PWM
Current-limit protection	10kΩ to AGND
Over-temperature protection (OTP)	20kΩ to AGND
SW-PGND short protection	1kΩ to VDD

The VTEMP/FLT pin monitors for three different fault events:

1. Over-current (OC) limit: If the current limit is exceeded for four consecutive PWM cycles, this fault is triggered. Once the fault is triggered, the MP86936 latches off to turn off the HS-FET. The LS-FET turns off once I_L reaches zero. When this fault occurs, PWM changes to a 10kΩ to AGND register configuration to indicate the fault type.
2. Over-temperature protection (OTP): If T_J exceeds 160°C, this fault is triggered. Once the fault is triggered, the MP86936 latches off to turn off the HS-FET. The LS-FET turns off once I_L reaches zero. When this fault occurs, PWM changes to a 20kΩ to AGND register configuration to indicate the fault type.
3. SW to PGND short: Once the fault is triggered, the MP86936 latches off to turn off the HS-FET. When this fault occurs, PWM is pulled high (1kΩ to VDD) to indicate the fault type.

The fault latch cannot be reset by entering standby mode. Recycle the power on VIN or VDD to release of fault latch.

For multi-phase operation, connect the VTEMP/FLT pins of each Intelli-Phase™ together (see Figure 2).

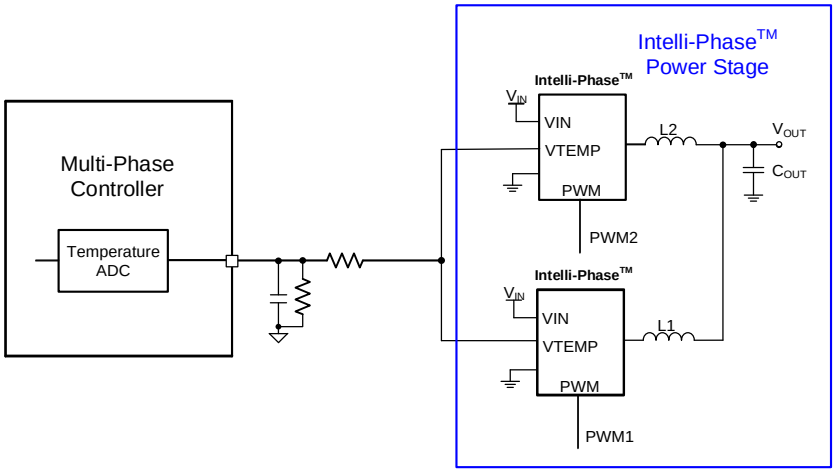

Figure 2: Multi-Phase Temperature-Sense Utilization

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For optimal performance, refer to Figure 3 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible. Place the major MLCC capacitors on the same layer as the MP86936.
2. Place as many VIN and PGND vias underneath the package as possible, in between VIN or PGND long pads.
3. Place a VIN copper plane on the second inner layer to form the PCB stacking (+/-/+) to reduce parasitic impedance from the input MLCC capacitor to the MP86936. The copper plane on the inner layer must cover the VIN vias underneath the package and the input MLCC capacitors.
4. Place more PGND vias close to PGND pin and pad to minimize parasitic resistance and thermal resistance.
5. Place the BST capacitor and VDRV capacitor as close to the device's pins as possible. Use a ⩾20mils trace width to route the path. Avoid the via for the BST driving path. The bootstrap capacitor is recommended to be 0.1μF to 0.22μF.
6. Place the VDD decoupling capacitor close to the MP86936. Connect AGND and PGND at the point of the VDD capacitor's ground connection.
7. Keep the CS signal trace away from high current paths, such as SW and PWM.

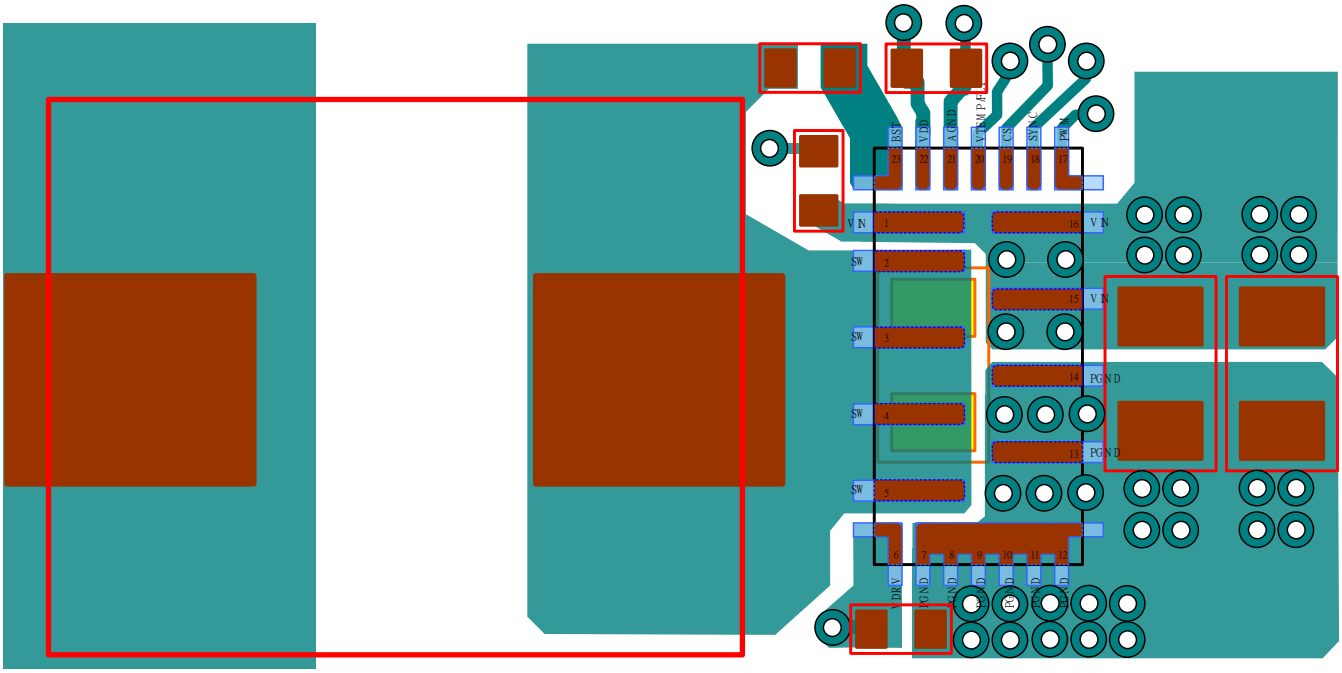

Figure 3: Recommended PCB Layout (Placement and Top Layer PCB)

Input capacitor: 0805 package (top side and bottom side), 0402 package (top side)

Inductor: 11nnx8nn package

VDD/BST/VDRV capacitor: 0402 package

Via size: 20/10 ils

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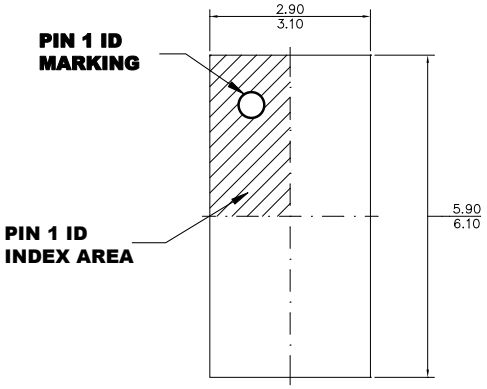
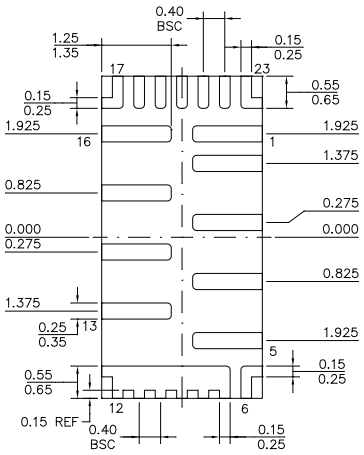
PACKAGE INFORMATION

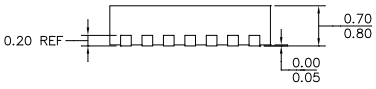
TQFN-23 (3mmx6mm)



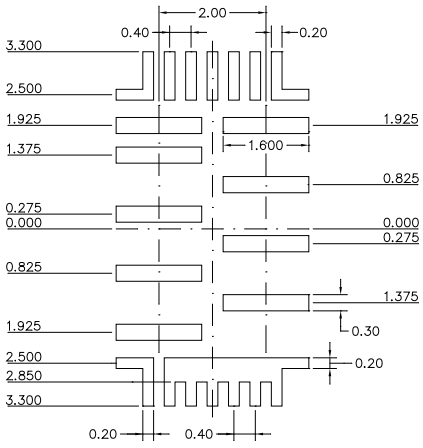
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PINS 1–5 AND PINS 13–16 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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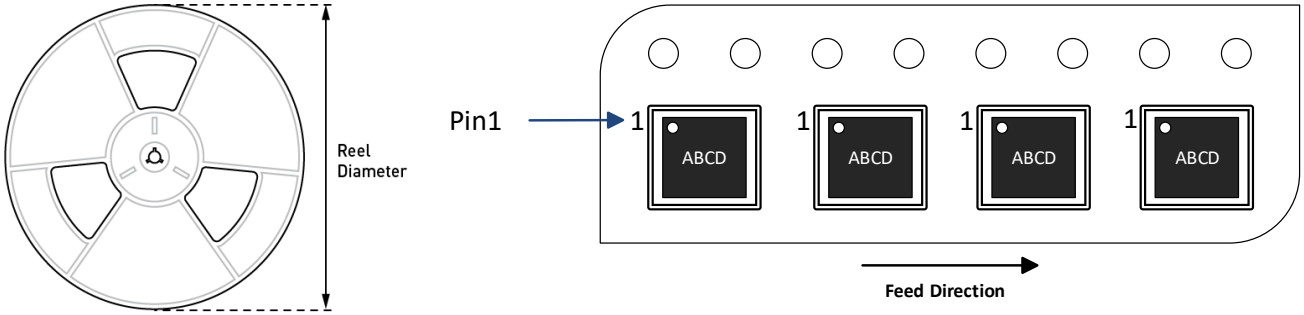
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP86936GRJT-Z	TQFN-23 (3mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/8/2021	Initial Release	-
1.1	8/4/2023	Updated MSL Rating from “3” to “1” in the Ordering Information section	2
		Updated “–Z” to “-Z” in the Ordering Information and Carrier Information sections	2, 13

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