MP86933

16V, Intelli-Phase Solution in a TQFN 3x3 Package

DESCRIPTION

The MP86933 is a monolithic, half-bridge driver with built-in, internal power MOSFETs and gate drivers. The MP86933 achieves 12A of continuous output current over a wide input supply range and can operate from 100kHz to 2MHz.

The integration of a driver and MOSFETs results in high efficiency due to an optimal dead time and parasitic inductance reduction.

The MP86933 works with tri-state output controllers and comes with a general-purpose current sense and temperature sense.

The MP86933 is ideal for server and telecom applications where efficiency and small size are a premium. The MP86933 is available in a small FC-TQFN-13 (3mmx3mm) package.

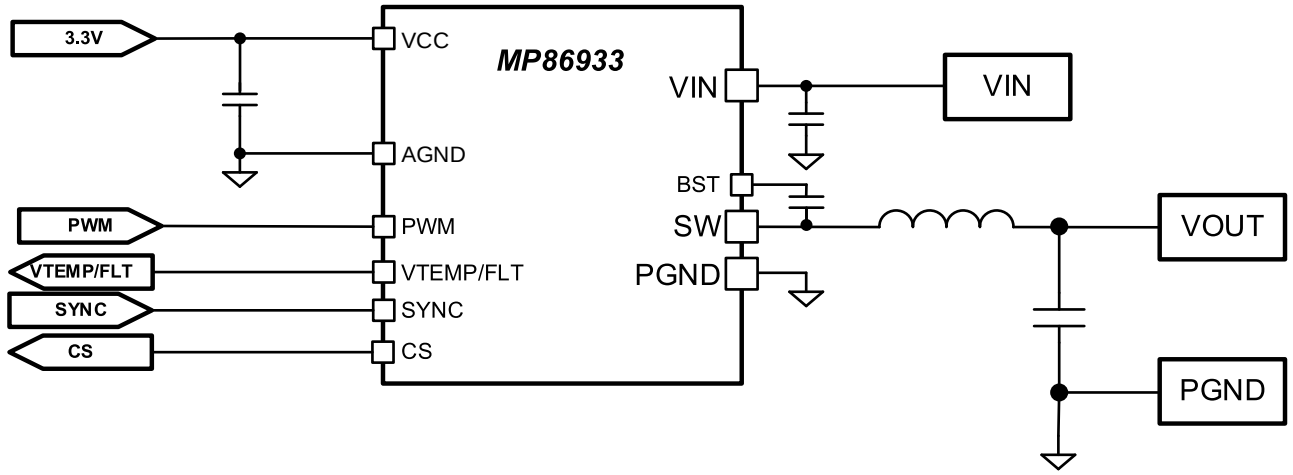
FEATURES

- Wide 4.5V to 16V Operating Input Range
- Compliant with Intel DrMOS V4.0 Spec
- 12A Output Current
- Accepts Tri-State PWM Signal
- Built-In Switch for Bootstrap
- Current Sense
- Temperature Sense
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting: Over-Current and Over-Temperature
- Used for Multi-Phase Operation
- Available in a TQFN-13 (3mmx3mm) Package

APPLICATIONS

- Server and Telecom Voltage Regulators
- Graphic Card Core Regulators
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP86933GQT	TQFN-13 (3mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP86933GQT–Z)

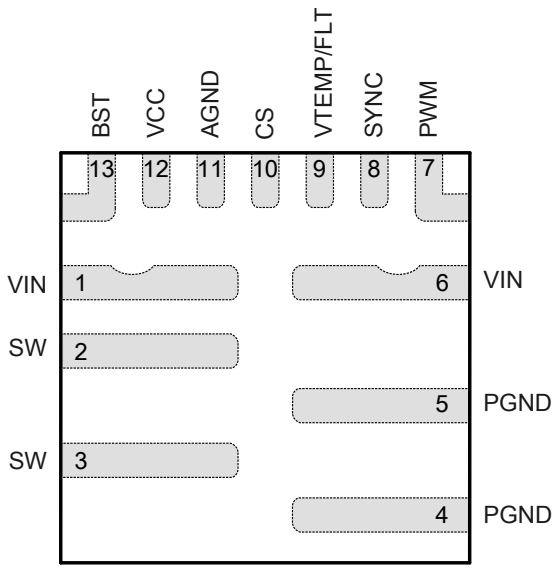
TOP MARKING

AQLY
LLL

AQL: Product code of MP86933GQT
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



TQFN-13 (3mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 18V
V_{SW} (DC) .....-0.3V to VIN + 0.3V
V_{SW} (25ns).....-3V to 25V
VIN - V_{SW} (10ns) .....-5V to 32V
V_{BST} - V_{SW} (25ns)..... 5V
V_{BST} ..... V_{SW} + 4V
All other pins .....-0.3V to +4V
Instantaneous current 25A
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (2)

Supply voltage (VIN) .....4.5V to 16V
Driver voltage (VCC).....3.0V to 3.6V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

TQFN-13 (3mmx3mm)	5.2	42.9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point.
   θ_{JC_TOP} is the thermal resistance from junction to the top of the package.

ELECTRICAL CHARACTERISTICS

VIN = 12V, VCC = 3.3V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN under voltage lockout threshold rising				4.1	4.5	V
VIN under voltage lockout threshold hysteresis				380		mV
VIN quiescent current in standby mode	$I_{IN\ Stby}$	PWM = Hi-Z, SYNC = Hi-Z, VIN = 4.5V to 22V			1	µA
VCC quiescent current in active mode	$I_{CC\ Quiescent}$	PWM = low, no switching, SYNC = high or low			3	mA
VCC quiescent current in standby mode	$I_{CC\ Stby}$	SYNC = Hi-Z			30	µA
VCC voltage UVLO rising			2.5	2.7	2.9	V
VCC voltage UVLO hysteresis				200		mV
High-side current limit	I_{LIM_FLT}			25		A
High-side current limit shutdown counter (4)				4		Times
Low-side current limit (4)				-5		A
Low-side off time in negative current limit (4)				40		ns
Dead-time rising (4)				3		ns
Dead-time falling(4)		Positive inductor current		8		ns
		Negative inductor current		40		ns
SYNC logic high voltage			2.40			V
SYNC tri-state region			1.3		1.7	V
SYNC logic low voltage					0.70	V
PWM high to SW rising delay (4)	t_{Rising}			20		ns
PWM low to SW falling delay (4)	$t_{Falling}$			20		ns
PWM tri-state to SW Hi-Z delay (54)	t_{Lo-HiZ}			50		ns
	t_{HiZ-Lo}			50		ns
	t_{HiZ-Hi}			50		ns
Minimum SW pulse width (4)				30		ns
Current sense gain accuracy		5A ≤ I_{SW} ≤ 15A	-3	0	3	%
Current sense gain				10		µA/A
Current sense offset		I_{OUT} = 0A	-5	0	5	µA
		SW Hi-Z	-2	0	2	µA
Current sense common mode voltage range	V_{CS_COM}		0.8		2.0	V
Temperature sense gain (4)				10		mV/°C
Temperature sense offset (4)				-100		mV
Temperature sense voltage range (4)		T = 150°C		1.4		V
		T = 100°C		0.90		V
		T = 25°C		0.15		V

ELECTRICAL CHARACTERISTICS *(continued)*

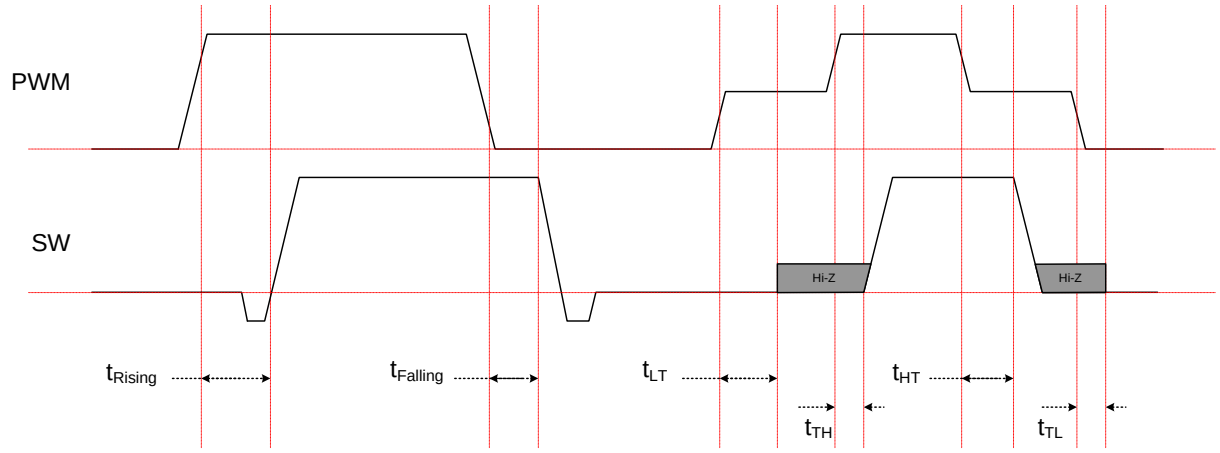
VIN = 12V, VCC = 3.3V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over-temperature shutdown (4)				160		°C
OTP threshold hysteresis (4)				20		C
VTEMP during fault (4)			3.0	3.3		V
PWM resistor		Pull up, SYNC = low or high		6		kΩ
		Pull down		5		kΩ
PWM logic high voltage			2.30			V
PWM tri-state region			1.1		1.9	V
PWM logic low voltage					0.7	V

NOTE:

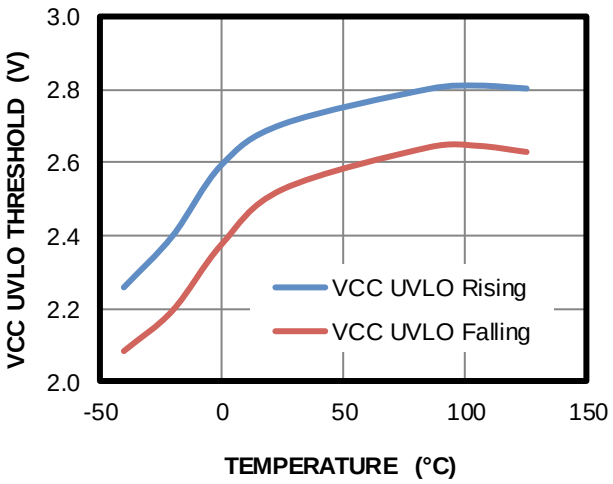
4) Guaranteed by design, not tested in production. The parameter is tested during parameters characterization.

PWM TIMING CHART

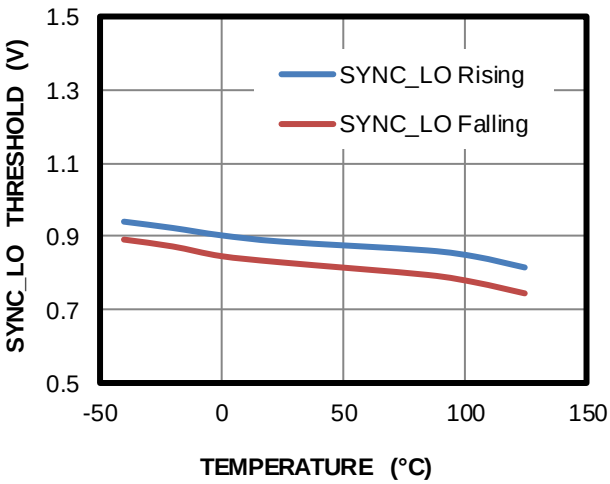


TYPICAL PERFORMANCE CHARACTERISTICS

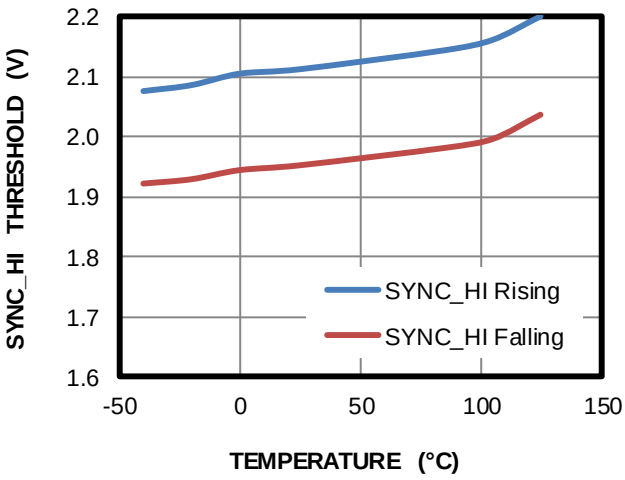
VCC UVLO



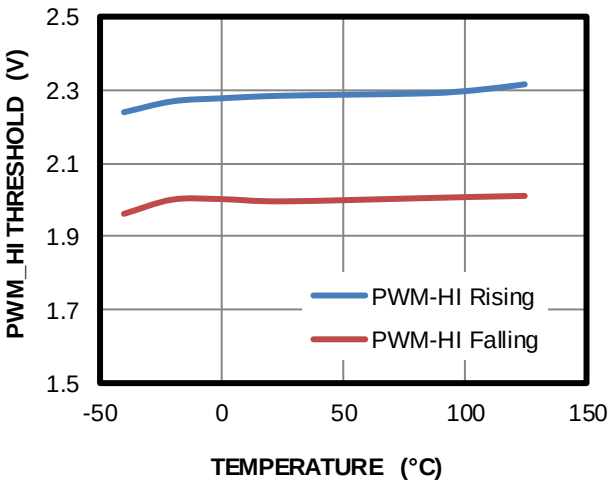
SYNC Low



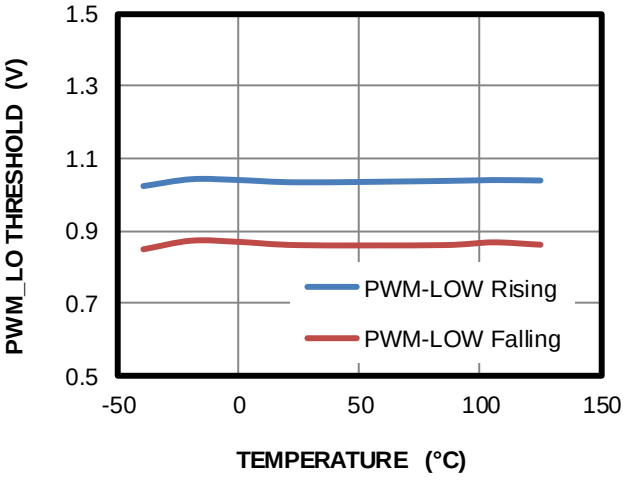
SYNC High



PWM High

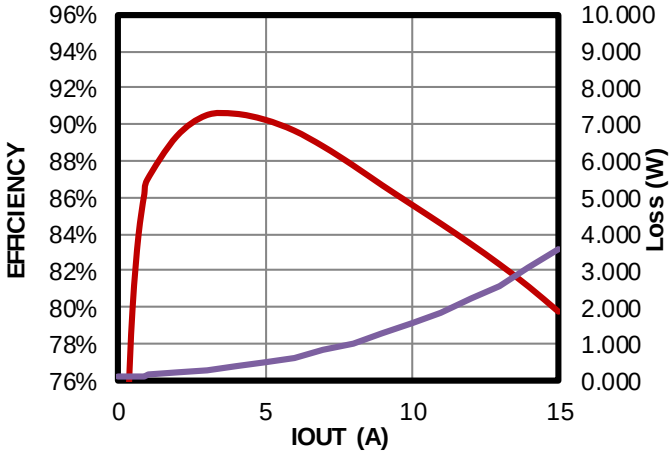


PWM Low



MP86933 Device Efficiency/Loss

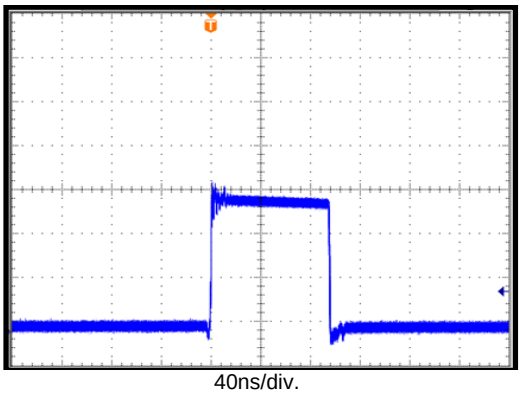
V_{IN} = 12V, V_{OUT} = 0.9V, F_{SW} = 800kHz, L = 360nH



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

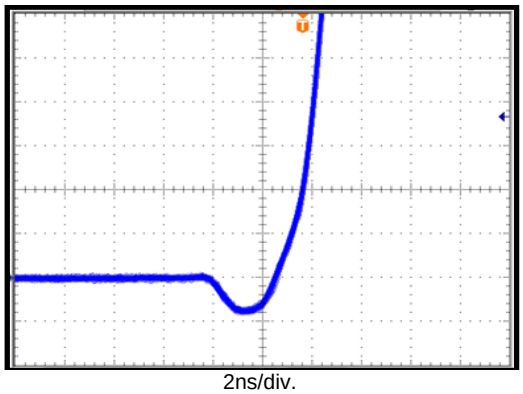
Switching Waveform

V_{IN} = 12A, L = 150nH, I_{OUT} = 6A



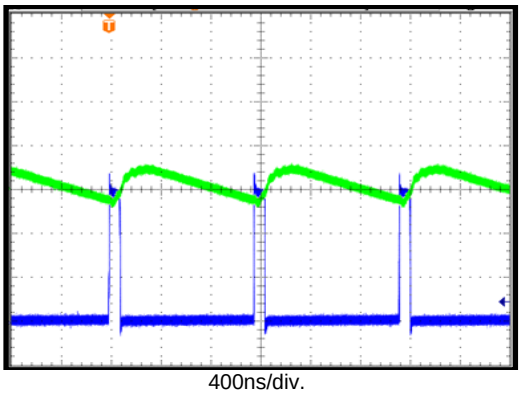
Dead Time @ SW Rising

I_{OUT} = 10A



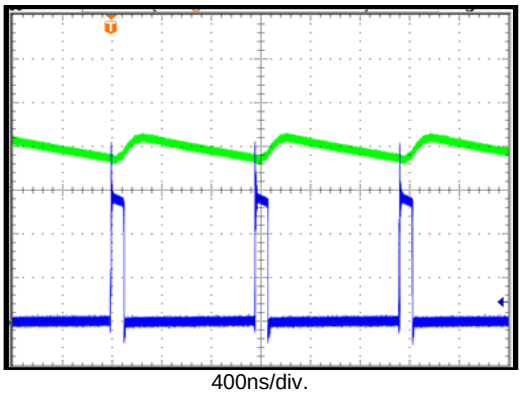
CS Output Waveform

I_{OUT} = 0A

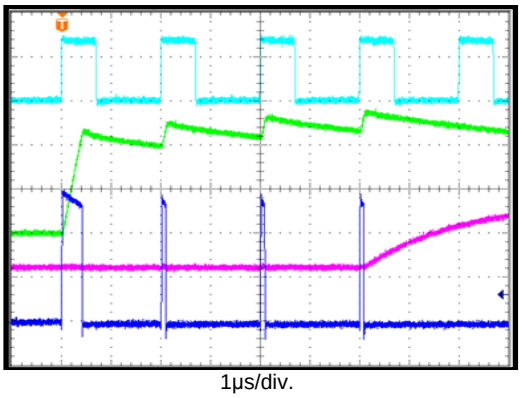


CS Output Waveform

I_{OUT} = 12A



HS Current Limit



PIN FUNCTIONS

Pin #	Name	Description
1, 6	VIN	**Supply voltage.** Place a capacitor (C_{IN}) close to the device to support the switching current reducing voltage spikes at the input.
2, 3	SW	**Switch output.**
4, 5	PGND	**Power ground.** Place multiple vias on the inner solid ground layers to minimize parasitic impedance and thermal resistance.
7	PWM	**Pulse-width modulation input.** Leave PWM floating or drive PWM to middle-state to enable diode emulation mode.
8	SYNC	**Diode emulation mode and standby mode selection.** Leave SYNC floating or drive SYNC to middle-state to enter standby mode. Pull SYNC high for normal operation. Pull SYNC low to enable diode emulation mode.
9	VTEMP/FLT	**Single pin temperature sense and fault reporting.**
10	CS	**Current sense output.**
11	AGND	**Analog ground.** Connect AGND to the PGND plane at the VCC decoupling capacitor.
12	VCC	**3.3V supply input for internal circuitry and gate driver.** Decouple VCC with a ceramic capacitor (1μF or higher) to AGND.
13	BST	**Bootstrap.** BST requires a 0.1μF to 1μF capacitor to drive the power switch's gate above the supply voltage. Connect the capacitor between SW and BST to form a floating supply across the power switch driver.

BLOCK DIAGRAM

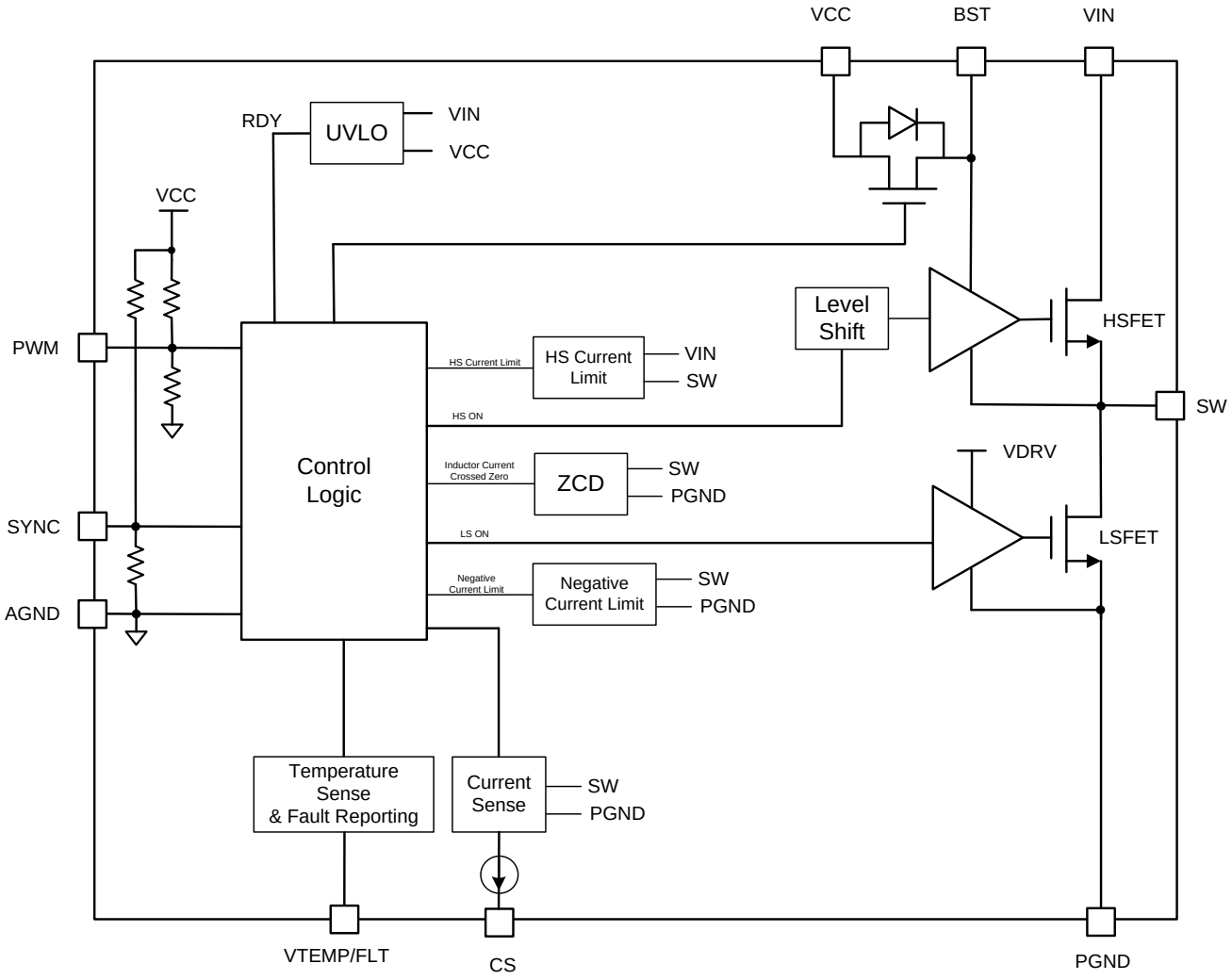


Figure 1: Functional Block Diagram

OPERATION

The MP86933 is a 12A, monolithic, half-bridge driver with MOSFETs ideally suited for multi-phase buck regulators.

Operation begins when VIN, VCC, and V_{BST} signals are sufficiently high.

Pulse-Width Modulation (PWM)

The PWM input pin is capable of tri-state input. When the PWM input signal is within the tri-state threshold window for 50ns, typically (T_{HT} or T_{LT}), the high-side MOSFET (HS-FET) is turned off immediately, and the low-side MOSFET (LS-FET) is in diode emulation mode, which is on until zero-current detection. The tri-state PWM input can be from a forced middle voltage PWM signal or made by floating the PWM input, and the internal current source charges the signal to a middle voltage. Please refer to the PWM timing diagram for the propagation delay definition from PWM to the SW node.

Standby Mode

When SYNC is floating or forced to a middle-state voltage for 2μs, the MP86933 enters standby mode. In standby mode, the part shuts down, and both the CS and VTEMP/FLT outputs are disabled. The fault latch cannot be reset by entering standby mode.

Diode Emulation Mode

In diode emulation mode, when PWM is either low or in a tri-state input, the LS-FET is turned on whenever the inductor current is positive. The LS-FET is off if the inductor current crosses the zero current. Diode emulation mode can be enabled by pulling SYNC low, driving PWM to middle state, or floating PWM.

Positive and Negative Inductor Current Limit

When HS-FET over-current is detected for four consecutive cycles, the HS-FET latches off, VTEMP/FLT is pulled to 3.3V, and the LS-FET turns on until zero-current detection. Recycle VIN/VCC or toggle EN to release the latch and restart the device.

When the LS-FET detects a -5A current, the MP86933 turns off the LS-FET for 40ns to limit the negative current. The LS-FET's negative current limit will not trigger a fault report.

Over-Temperature Protection (OTP)

When the junction temperature reaches the over-temperature threshold, the HS-FET latches off, VTEMP/FLT is pulled to 3.3V, and the LS-FET turns on until zero-current detection.

Temperature Sense Output with Fault Indicator (VTEMP/FLT)

VTEMP/FLT is a pin with dual functions.

1) Junction Temperature Sense: VTEMP/FLT is a voltage output proportional to the junction temperature whenever VCC is higher than its UVLO and is in active mode. The gain is 10mV/°C with a -100mV offset at 25°C (i.e.: 0V @ T_J < 10°C, 0.15V @ T_J = 25°C and 0.9V @ T_J = 100°C).

2) Fault Function: When any fault occurs, VTEMP/FLT is pulled to 3.3V, typically (3.0V minimum) regardless of the temperature to report the fault event. VTEMP/FLT monitors three fault events.

   i. Over-Current Limit: To trip the over-current fault, the current limit must be exceeded four consecutive times. Once the fault occurs, the MP86933 latches off to turn the HS-FET off. The LS-FET is turned off when the inductor current reaches zero.

   ii. Over-Temperature Fault at T_J > 160°C: Once the fault occurs, the MP86933 latches off to turn the HS-FET off. The LS-FET is turned off when the inductor current reaches zero.

   iii. SW to PGND Short: Once the fault occurs, the MP86933 latches off to turn the HS-FET off.

   The fault latch cannot be reset by entering standby mode. The fault latch can be released by recycling either VIN or VCC.

Current Sense Output (CS)

CS is a bidirectional current source proportional to the inductor current. The current sensing gain is 10μA/A. A resistor is used to program the voltage gain proportional to the inductor current if needed.

The CS output has two states (see Table 1). In standby mode, the CS circuit is disabled and needs 20μs to wake up and enter active mode if needed.

Table 1: CS Output States

PWM	SYNC	CS
PWM	High	Active
PWM	High	Active
PWM	Low	Active
x	Hi-Z (or middle)	Standby

The CS voltage range of 0.7V to 2.1V is required to obtain an accurate CS current output up to +500μA/-200μA (i.e.: +50A/-12A). Generally, there is a resistor (R_{CS}) connected from CS to an external voltage which is capable of sinking small currents to provide enough of a voltage level to meet the required operating voltage range.

Figure 2 shows the typical circuit diagram of the CS connection to achieve a differential voltage source reflected in the inductor current.

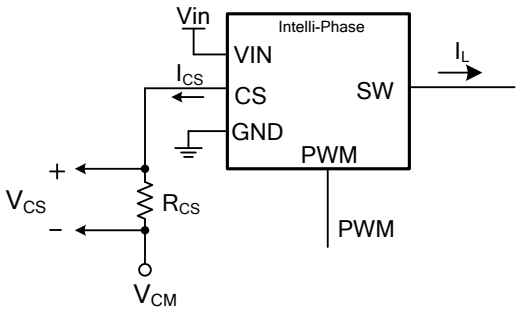


Figure 2: Typical Circuit Diagram for CS Connection

To keep V_{CS} within the operating range, design R_{CS} with Equation (1) and Equation (2):

$$0.7V < I_{CS} \times R_{CS} + V_{CM} < 2.1V \quad (1)$$

$$I_{CS} = I_L \times G_{CS} \quad (2)$$

Where V_{CM} is the reference voltage connected to R_{CS}.

V_{CM} can be from a voltage divider from 3.3V (i.e.: VCC) (see Figure 3).

Make R_{CS} much larger than R_1 parallel to R_2 to minimize V_{CM} variation over I_{CS}.

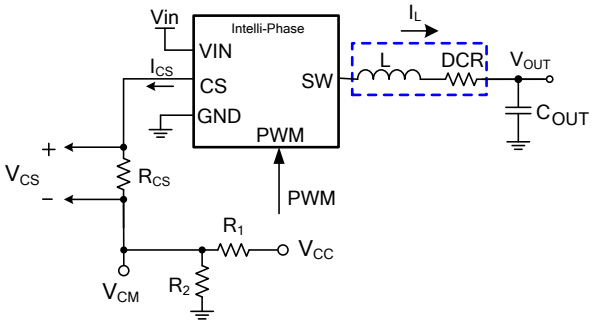


Figure 3: Use VCC to Generate V_{CM} for CS Signal

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best performance, refer to Figure 4 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP86933.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Place as many PGND vias as possible close to PGND to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the BST capacitor as close to BST and SW as possible.
8. Route the path with trace widths 20 mils or higher.
9. Use 0.1µF to 1µF bootstrap capacitors.
10. Keep the CS signal trace away from high-current paths like SW and PWM.

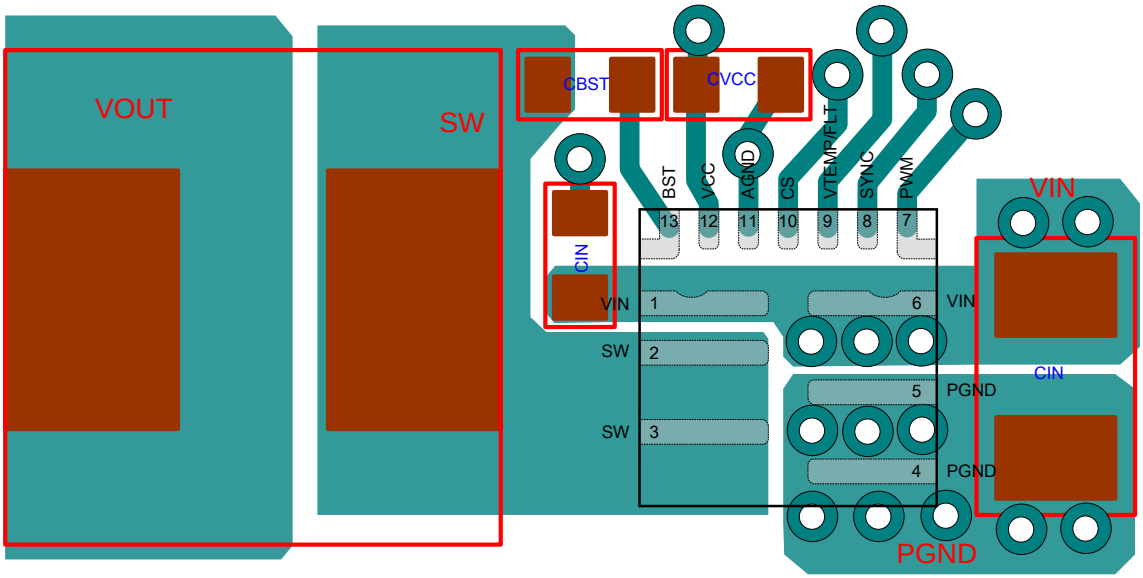


Figure 4: Example of PCB Layout (Placement & Top Layer PCB)

Input Capacitor: 0805 & 0402 package

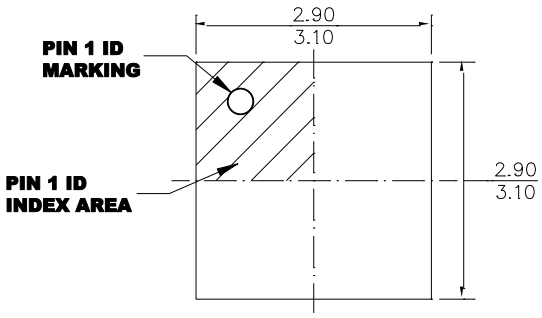
Inductor: 6.5 x 6.5 (mm)

VCC/BST capacitor: 0402 package

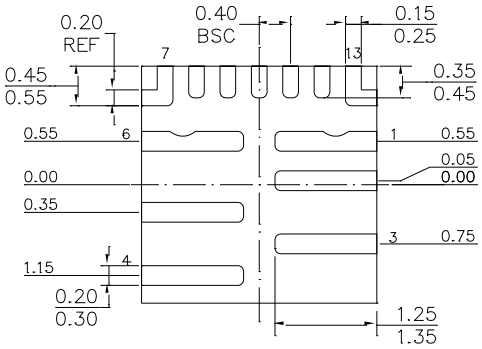
Via size: 20/10 mils

PACKAGE INFORMATION

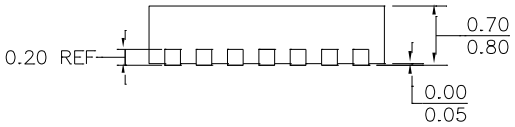
TQFN-13 (3mmx3mm)



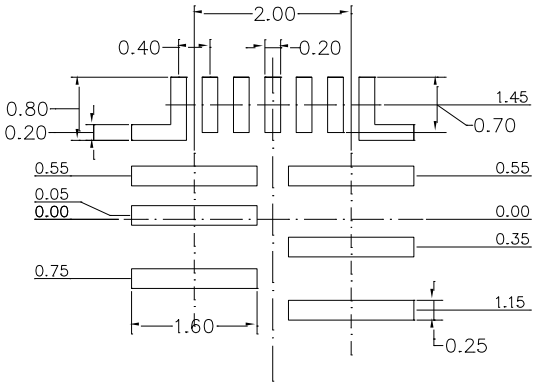
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
r1.1	5/19/2020	Correct/add the “Vin-Vsw (10ns) ……. -5V to 32V” on absMax rating.	Page 3
r1.2	5/26/2021	Update the thermal impedance.	Page 3