MP8642

Dual 3A, 23V, 600kHz Step-Down Converter with Frequency Synchronization

END OF LIFE, REFER TO MP2393

DESCRIPTION

The MP8642 is a dual monolithic step-down switch mode converter with built-in internal power MOSFETs. It achieves 3A continuous output current for each output over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP8642 requires a minimum number of readily available standard external components.

FEATURES

- 3A Current for Each Output
- 80mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- Power Good Indicator
- Fixed 600kHz Frequency
- Synchronizable to >1MHz External Clock
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.5V to 23V Operating Input Range
- Each Output Adjustable from 0.8V to 20V
- Available in a 5mm x 5mm 32-Pin QFN Package

APPLICATIONS

- Point of Load Regulator in Distributed Power Systems
- Digital Set Top Boxes
- Personal Video Recorders
- Broadband Communications
- Flat Panel Television and Monitors

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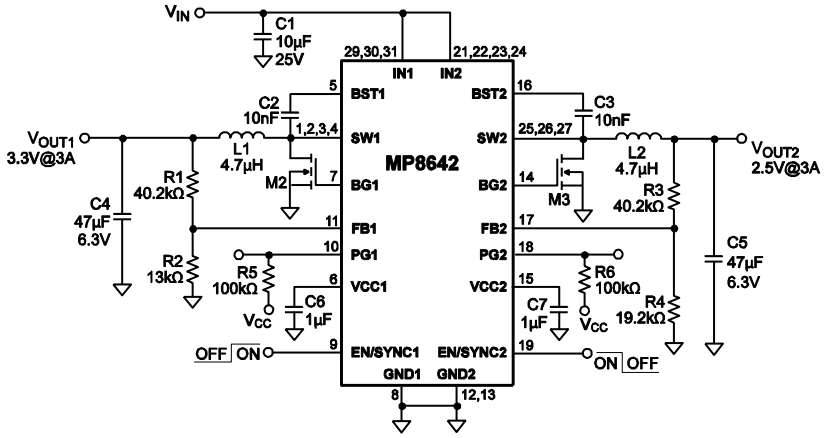
TYPICAL APPLICATION



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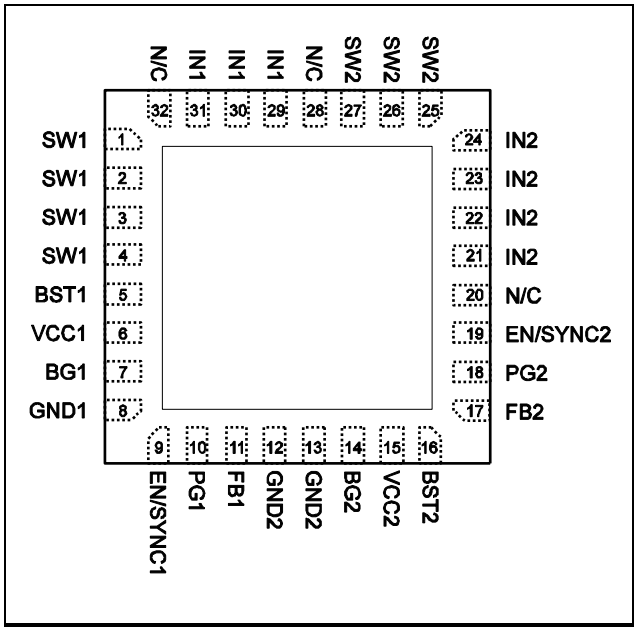
END OF LIFE, REFER TO MP2393

ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP8642DU	QFN32 (5mm x5mm)	M8642DU	–40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP MP8642DU–Z);
For RoHS compliant packaging, add suffix –LF; (e.g. MP8642DU–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 25V
V_{SW} ..... -0.3V(-5V for < 10ns) to 26V
V_{BS} ..... V_{SW} + 6V
All Other Pins..... –0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
..... 3.47W
Junction Temperature..... 150°C
Lead Temperature ..... 260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 4.5V to 23V
Output Voltage V_{OUT}..... 0.8V to 20V
Operating Junct. Temp (T_J)..... –40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

5x5 QFN32	36	8 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 23V	0.788	0.808	0.828	V
Feedback Current	I_{FB}	V_{FB} = 0.8V		10		nA
Switch On Resistance (5)	$R_{DS(ON)}$			80		mΩ
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0.1	10	μA
Current Limit (5)			4			A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	400	600	800	kHz
Fold-back Frequency		V_{FB} = 0V	60	150	240	kHz
Maximum Duty Cycle		V_{FB} = 0.6V	85	90		%
Minimum On Time (4)	t_{ON}			100		ns
Under Voltage Lockout Threshold Rising			3.9	4.1	4.3	V
Under Voltage Lockout Threshold Hysteresis				880		mV
EN Input Low Voltage					0.4	V
En Input High Voltage			1.5			V
EN Input Current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0.1		
Supply Current (Shutdown)		V_{EN} = 0V		0.1	10	μA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V		0.9	1.1	mA
Thermal Shutdown				150		°C
BG Driver Bias Supply Voltage	V_{CC}		4.5	5		V
Gate Driver Sink Impedance (5)	R_{SINK}			1	2	Ω
Gate Driver Source Impedance (5)	R_{SOURCE}			4	5.5	Ω
Gate Drive Current Sense Trip Threshold				20		mV
Power Good Threshold			0.69	0.74	0.79	V
Power Good Threshold Hysteresis				40		mV
PG Pin Level	V_{PG}	PG Sink 4mA			0.4	V

Note:

5) Guaranteed by design.

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PIN FUNCTIONS

Pin #	Name	Description
1, 2, 3, 4	SW1	Switch Output Channel 1
5	BST1	Bootstrap Channel 1. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW1 and BST1pins to form a floating supply across the power switch driver.
6	VCC1	BG Driver Bias Supply Channel 1. Decouple with a 1µF ceramic capacitor.
7	BG1	Gate Driver Output Channel 1. Connect this pin to the synchronous MOSFET Gate
8	GND1	Ground Channel 1.
9	EN/SYNC1	On/Off Control and External Frequency Synchronization Input Channel 1.
10	PG1	Power Good Indicator Channel 1. Connect this pin to VCC or VOUT by a 100kΩ pull-up resistor. The output of this pin is low if the output voltage is 10% less than the nominal voltage, otherwise it is an open drain.
11	FB1	Feedback Channel 1. An external resistor divider from the output1 to GND1, tapped to the FB1 pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV.
12, 13	GND2	Ground Channel 2.
14	BG2	Gate Driver Output Channel 2. Connect this pin to the synchronous MOSFET Gate
15	VCC2	G Driver Bias Supply Channel 2. Decouple with a 1µF ceramic capacitor.
16	BST2	Bootstrap channel 2. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW2 and BST2 pins to form a floating supply across the power switch driver.
17	FB2	Feedback Channel 2. An external resistor divider from the output2 to GND2, tapped to the FB2 pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV.
18	PG2	Power Good Indicator Channel 2. Connect this pin to V_{CC} or V_{OUT} by a 100kΩ pull-up resistor. The output of this pin is low if the output voltage is 10% less than the nominal voltage, otherwise it is an open drain.
19	EN/SYNC2	On/Off Control and External Frequency Synchronization Input Channel 2.
20, 28, 32	N/C	No Connect
21, 22, 23, 24	IN2	Supply Voltage Channel 2. The MP8642 operates from a +4.5V to +23V unregulated input.
25, 26, 27	SW2	Switch Output Channel 2
29, 30, 31	IN1	Supply Voltage Channel 1. The MP8642 operates from a +4.5V to +23V unregulated input.

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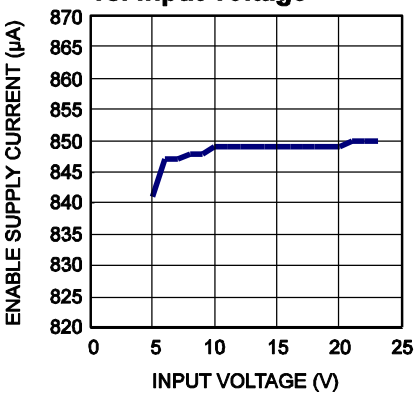
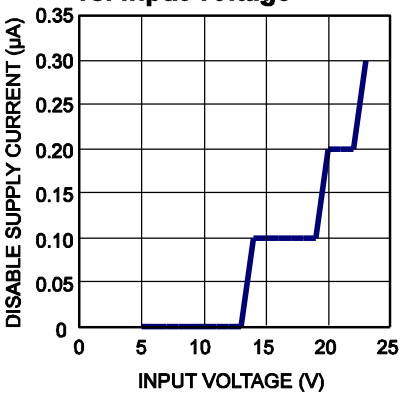
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L =3.9µH, T_A = +25ºC, unless otherwise noted.

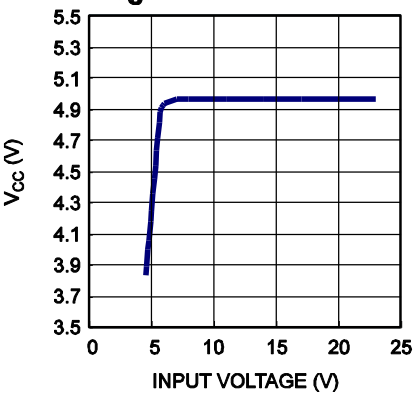
Enable Supply Current vs. Input Voltage



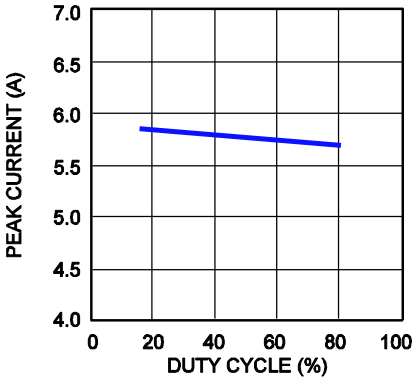
Disable Supply Current vs. Input Voltage



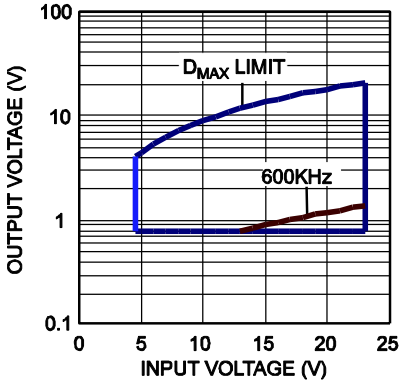
V_{CC} Regulator Line Regulation



Peak Current vs. Duty Cycle

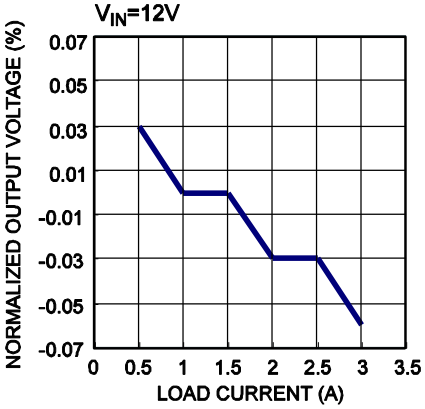


Operating Range



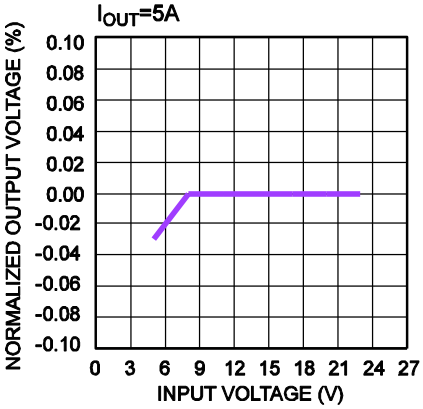
Load Regulation

V_{IN}=12V

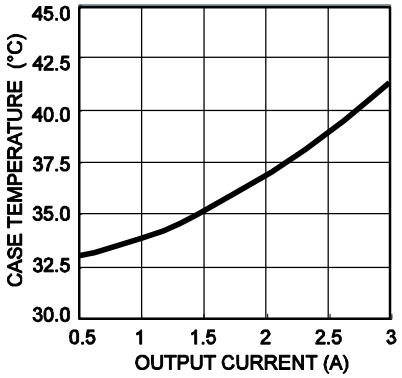


Line Regulation

I_{OUT}=5A



Case Temperature vs. Output Current



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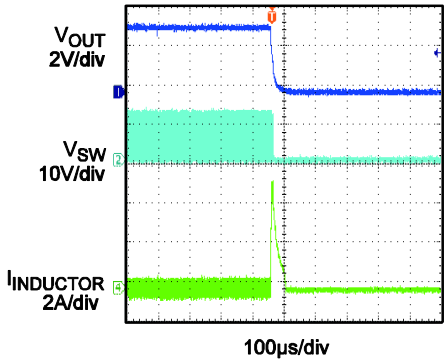
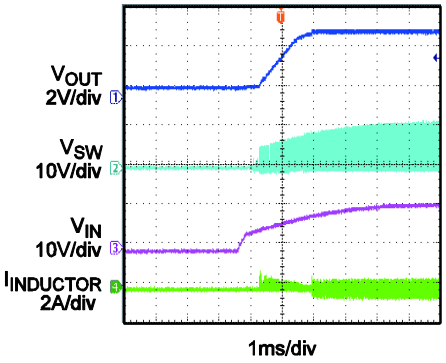
TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

V_{IN} = 12V, V_{OUT} = 3.3V, L =3.9µH, T_A = +25°C, unless otherwise noted.

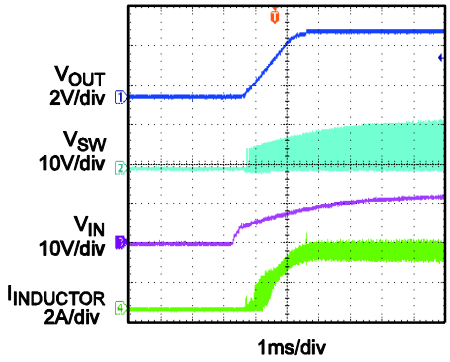
Latch Off with Output Short Circuit



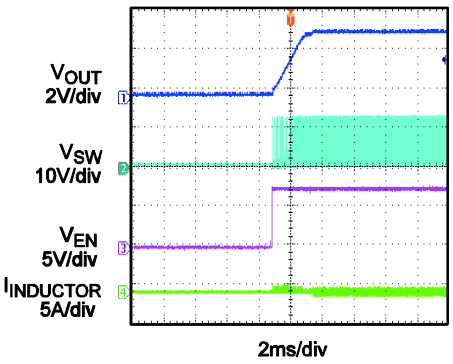
Power Up
No Load



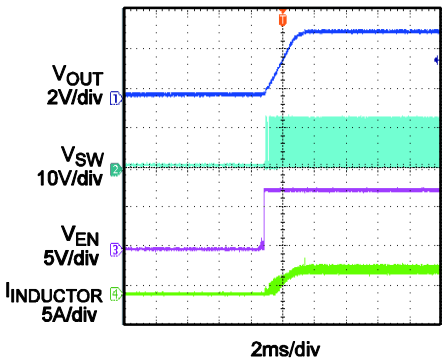
Power Up
Full Load (CR)



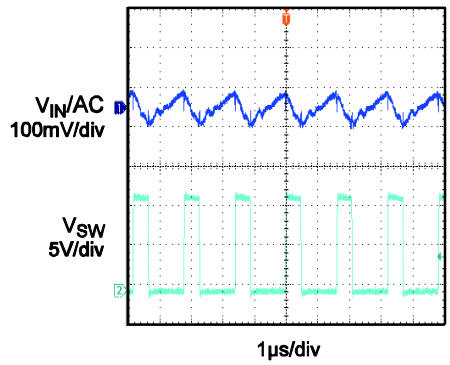
Enable Startup
No Load



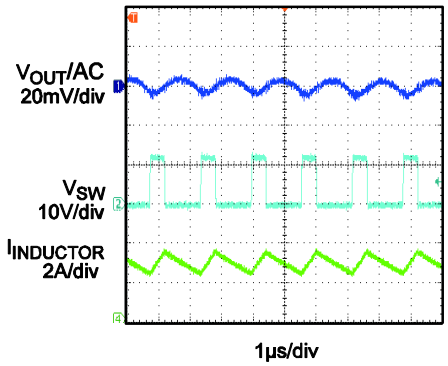
Enable Startup
Full Load (CR)



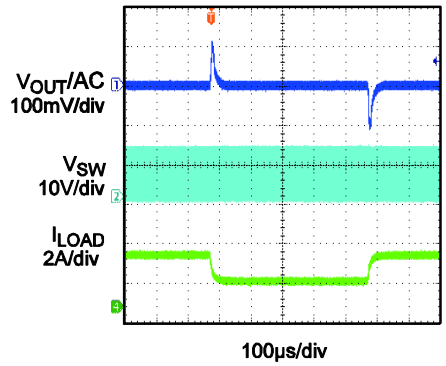
Input Ripple Voltage



Output Ripple Voltage



Load Transient Response
1.5A to 3A



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OPERATION

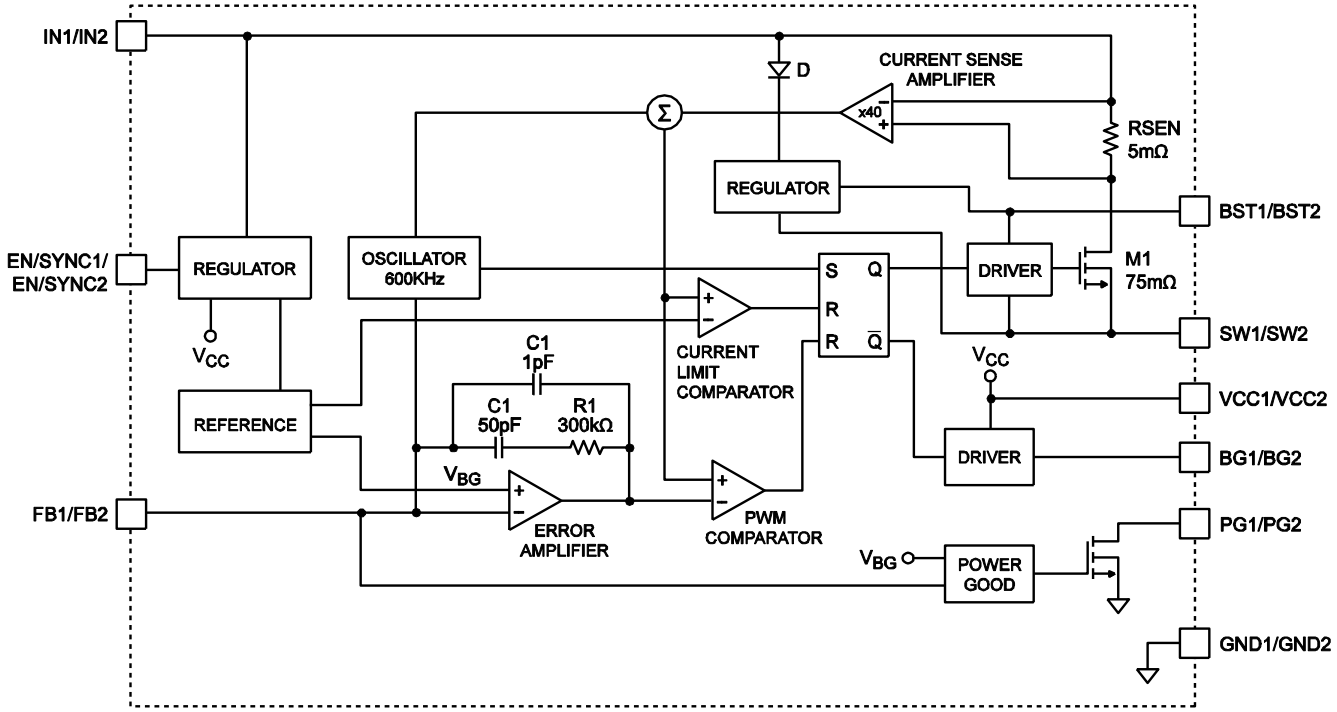

Figure 1—Functional Block Diagram (Diagram Portrays ½ of the MP8642)

The MP8642 is a dual channel, fixed frequency, synchronous, step-down switching regulator with integrated high-side power MOSFETs and gate drivers for a low-side external MOSFETs. It achieves 3A continuous output current for each output over a wide input supply range with excellent load and line regulation in each channel. It provides a single highly efficient solution with current mode control for fast loop response and easy compensation.

The MP8642 operates in a fixed frequency, peak current control mode to regulate the output voltage. On each channel, a PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases. Since this internal regulator provides the bias current for the bottom gate driver that requires significant amount of current depending upon the external MOSFET selection, a 1uF ceramic capacitor for decoupling purpose is required.

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Enable/Synch Control

The MP8642 has a dedicated Enable/Synch control pin (EN/SYNC) on each channel. By pulling it high or low, the IC can be enabled and disabled by EN. Tie EN to VIN for automatic start up. To disable the part, EN must be pulled low for at least 5µs.

The MP8642 can be synchronized to external clock range from 300kHz up to 1.4MHz through the EN/SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP8642 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.1V while its falling threshold is a consistent 3.2V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

Over-Current-Protection (OCP)

The MP8642 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a output UV is triggered, the MP8642 enters latch off mode. Mode is especially useful to ensure system safety under fault condition. The MP8642 exits the latch off mode once the EN or input power is re-cycled.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M3, C4, L1 and C2 (Figure 2). If (V_{IN}-V_{SW}) is more than 5V, U2 will regulate M3 to maintain a 5V BST voltage across C4.

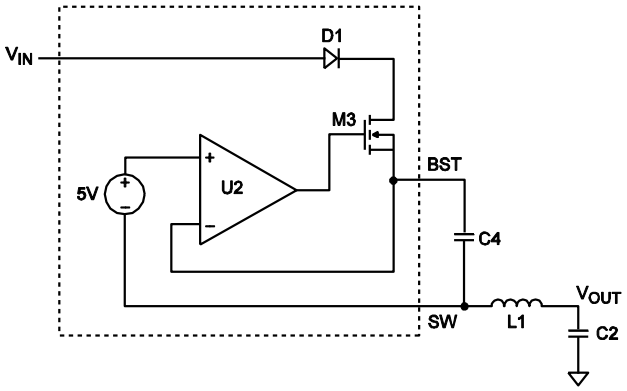

Figure 2—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

COMPONENT SELECTION

The MP8642 has two channels: 1 and 2. The following formulas are used for component selection of both channels.

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.8	40.2 (1%)	32.4 (1%)
2.5	40.2 (1%)	19.1 (1%)
3.3	40.2 (1%)	13 (1%)
5	40.2 (1%)	7.68 (1%)

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor current to be approximately 30% if the maximum load current, 3A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Synchronous MOSFET

The external synchronous MOSFET is used to supply current to the inductor when the internal high-side switch is off. It reduces the power loss significantly when compared against a Schottky rectifier.

Table 2 lists example synchronous MOSFETs and manufacturers.

Table 2—Synchronous MOSFET Selection Guide

Part No.	Manufacture
Si7112	VISHAY
Si7114	VISHAY
AM4874	Analog Power

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

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The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

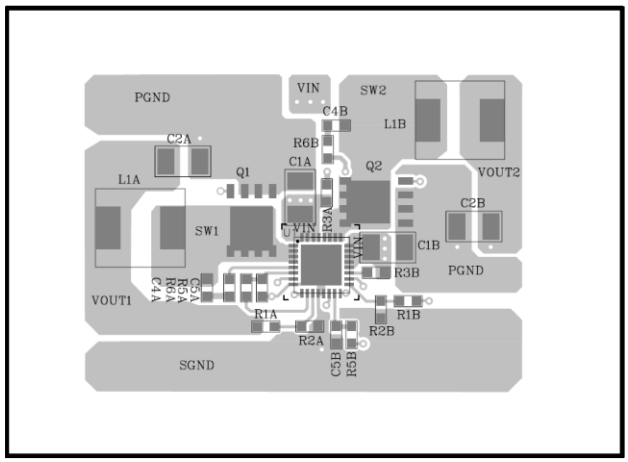
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8642 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guide

PCB layout is very important to achieve stable operation. Please follow these guidelines and take Figure3 for references.

1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side and low-side MOSFETs.
2) Keep the connection of low-side MOSFET between SW pin and input power ground as short and wide as possible.
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4) Route SW away from sensitive analog areas such as FB.
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.



Top Layer

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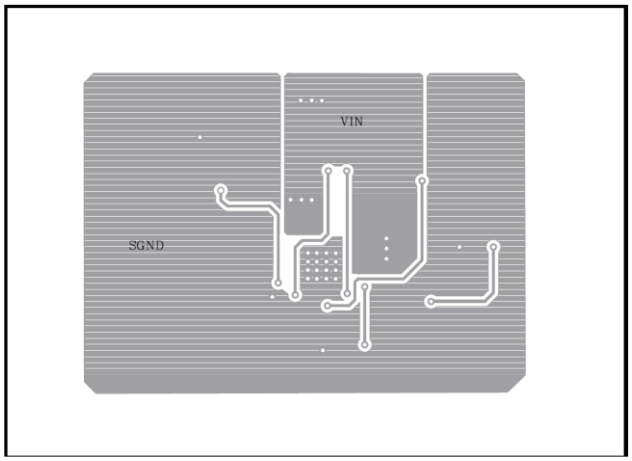

Bottom Layer

Figure 3—PCB Layout

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Fig.4

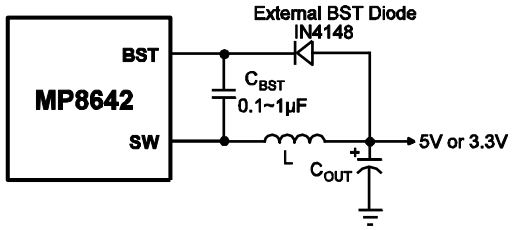

Figure 4—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1µF.

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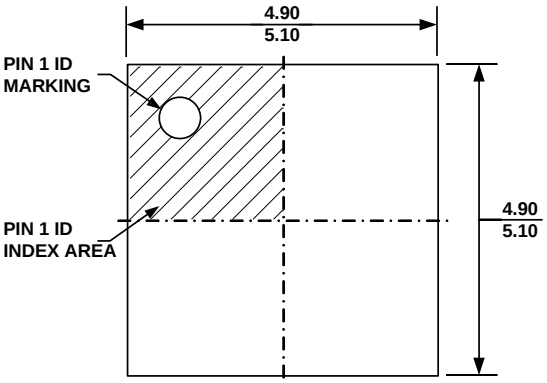
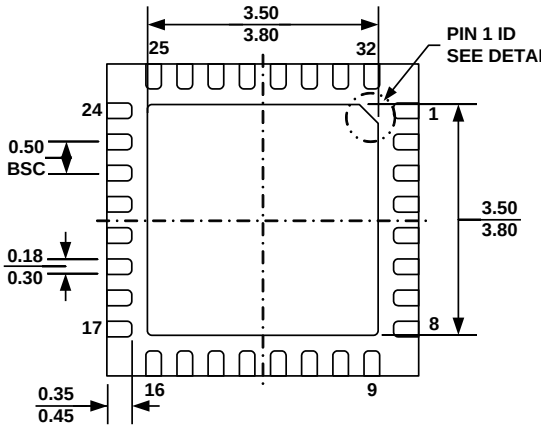
PACKAGE INFORMATION

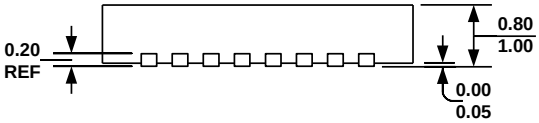
5mm x 5mm QFN32



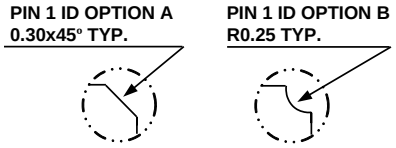
TOP VIEW



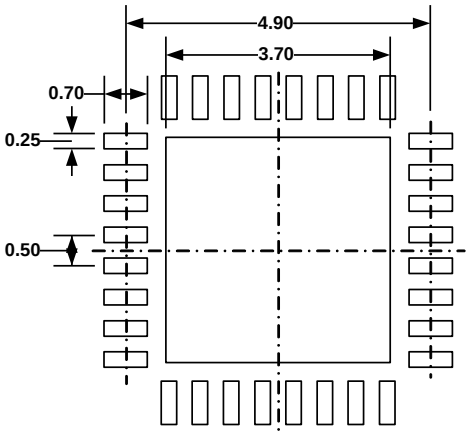
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VHHC-2.
5) DRAWING IS NOT TO SCALE.

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