MP6925A

Fast Turn-Off, CCM/DCM Compatible, Dual-LLC, Synchronous Rectifier with Improved Noise Immunity

DESCRIPTION

The MP6925A is a dual, fast turn-off, intelligent rectifier for synchronous rectification in LLC resonant converters.

The IC drives two N-channel MOSFETs and regulates their forward voltage drop to V_{FWD} (about 45mV). The IC turns the MOSFETs off before the switching current goes negative.

The MP6925A has light-load functionality to latch off the gate driver under light-load conditions, thus limiting the current below 175µA.

The MP6925A's fast turn-off enables both continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The MP6925A requires a minimal number of external components, and is available in an SOIC-8 package.

FEATURES

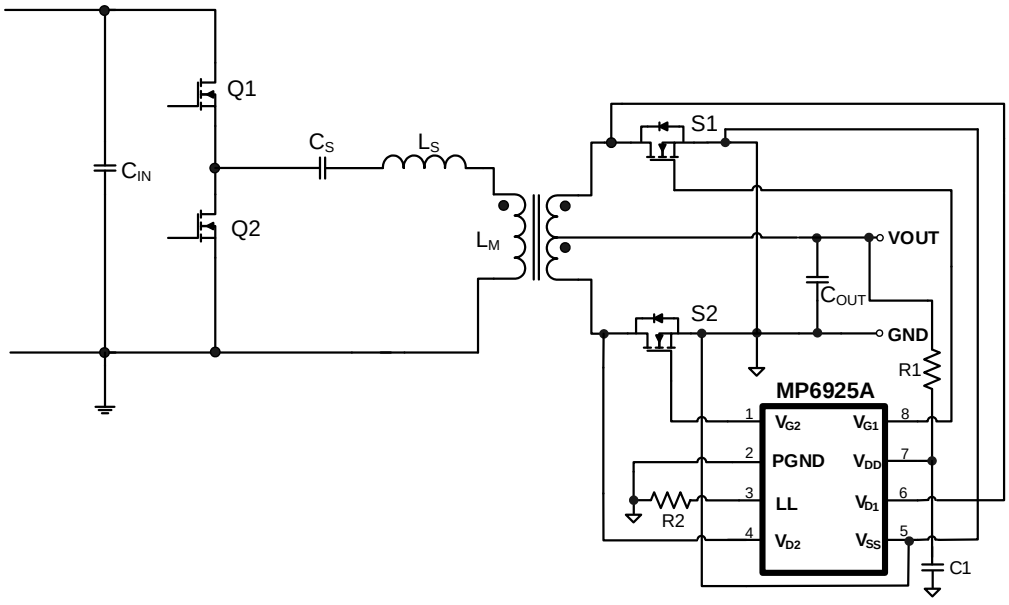
- Works with Standard and Logic Level MOSFETs
- Compatible with Energy Star
- Fast Turn-Off Total Delay of 35ns
- Wide 4.2V to 35V V_{DD} Operating Range
- 175µA Low Quiescent Current in Light-Load Mode
- Supports CCM, CrCM, and DCM Operation
- Supports High-Side and Low-Side Rectification
- Available in an SOIC-8 Package

APPLICATIONS

- AC/DC Adapters
- PC Power Supplies
- LCD and LED TVs
- Isolated DC/DC Power Converters

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marketing	MSL Rating
MP6925AGS	SOIC-8	*See Below*	2

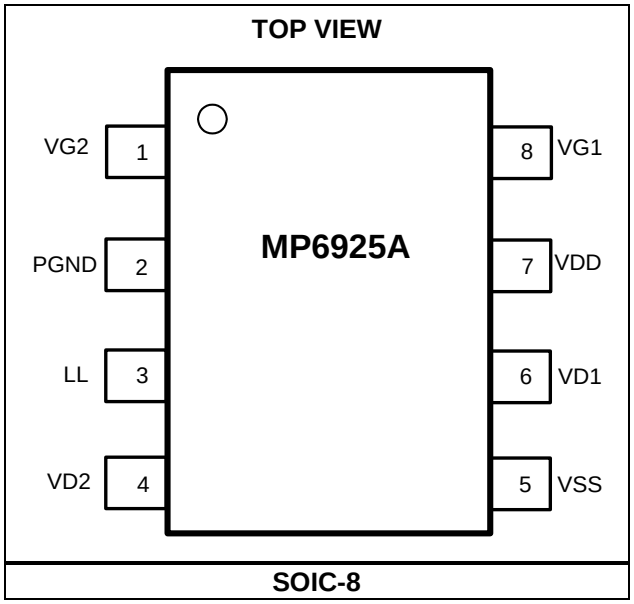
* For Tape & Reel, add suffix –Z (e.g. MP6925AGS–Z).

TOP MARKING

MP6925A
LLLLLLLL
MPSYWW

MP6925A: Part number
LLLLLLLL: Lot number
MPS: MPS prefix
Y: Year code
WW: Week code

PACKAGE REFERENCE



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	VG2	**MOSFET 2 gate driver output.**
2	PGND	**Power ground.** PGND is the power switch return.
3	LL	**Light-load timing setting.** Connect a resistor to LL to set the light-load timing. Leave LL float to disable the light-load function. If light-load is disabled, connect a capacitor to this pin. Pull LL low to disable the gate driver.
4	VD2	**MOSFET 2 voltage-sense drain.**
5	VSS	**Source pin used as reference for V_{D1} and V_{D2}.**
6	VD1	**MOSFET 1 voltage-sense drain.**
7	VDD	**Supply voltage.**
8	VG1	**MOSFET 1 gate driver output.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} to V_{SS} ..... -0.3V to +38V
PGND to V_{SS} ..... -0.3V to +0.3V
V_G to V_{SS} ..... -0.3V to +20V
V_D to V_{SS} ..... -1V to +180V
LL to V_{SS} ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8 ..... 1.4W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature ..... -55°C to +150°C

ESD Rating

Human-body model (HBM) ..... ±800V
Charged-device model (CDM)..... ±1750V

Recommended Operation Conditions (3)

V_{DD} - V_{SS} ..... 4.2V to 35V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8 ..... 90 ..... 45 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
V_{DD} voltage range			4.2		35	V
V_{DD} UVLO rising			3.7	3.95	4.2	V
V_{DD} UVLO hysteresis			0.13	0.185	0.24	V
Operating current	I_{CC}	C_{LOAD} = 4.7nF, f_{SW} = 100kHz		16	20	mA
Quiescent current	I_Q	V_{SS} - V_D = 0.5V		4.6	6	mA
Shutdown current		V_{DD} = 4V, LL = 0V		135	190	µA
		V_{DD} = 20V, LL = 0V		155	210	
Light-load mode current				175	225	µA
Thermal shutdown (5)				150		°C
Thermal shutdown hysteresis (5)				10		°C
Control Circuitry Section						
V_{SS} - V_D forward voltage	V_{FWD}		28	45	58	mV
Turn off threshold (V_{SS} - V_D)	$V_{DRV-OFF}$		-56	-40	-20	mV
Turn-on delay	t_{DON}	C_{LOAD} = 4.7nF, V_{GS} = 2V		80	140	ns
		C_{LOAD} = 10nF, V_{GS} = 2V		90	180	ns
Input bias current on V_D		V_D = 180V			1	µA
Turn-on blanking time	t_{B_ON}	C_{LOAD} = 4.7nF	0.75	1.1	1.65	µs
Turn-off blanking time (5)	t_{B_OFF}	C_{LOAD} = 4.7nF		210		ns
Turn-off blanking V_{DS} threshold	V_{B_OFF}		1	1.7	2.5	V
Light-load enter pulse width	t_{LL}	R_{LL} = 100kΩ	1.7	2.3	3	µs
Light-load turn-on pulse width hysteresis	t_{LL-H}	R_{LL} = 100kΩ		0.45		µs
Light-load enter delay	t_{LL-D}		0.5	1	1.52	ms
Light-load enter pulse-width threshold ($V_{G1/2}$ - V_{SS}) (5)	V_{LL-GS}			0.6		V
Gate disable threshold on LL	V_{LL_DIS}		0.1	0.2	0.3	V
Light-load exit switch-on threshold (V_{DS})	V_{LL_DS}		-330	-230	-130	mV
Gate Driver Section						
V_G (low)	V_{G_L}	I_{LOAD} = 1mA			0.1	V
V_G (high)	V_{G_H}	V_{DD} > 10V		11.5	13	V
		V_{DD} ≤ 10V		V_{DD}		
Turn-off propagation delay		V_D = V_{SS}		15		ns
Turn-off total delay	t_{DOFF}	V_D = V_{SS}, C_{LOAD} = 4.7nF, R_{GATE} = 0Ω, V_{GS} = 2V		35	80	ns
	t_{DOFF}	V_D = V_{SS}, C_{LOAD} = 10nF, R_{GATE} = 0Ω, V_{GS} = 2V		45	100	ns
Pull-down impedance				0.6	1.5	Ω

Note:

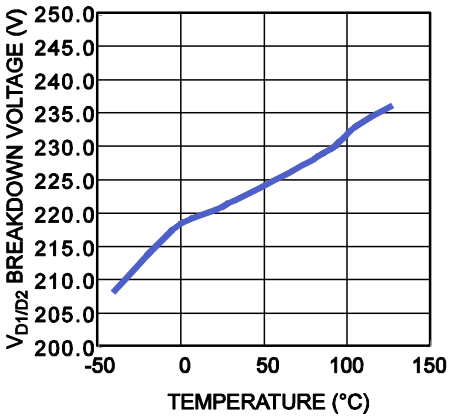
5) Guaranteed by characterization.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

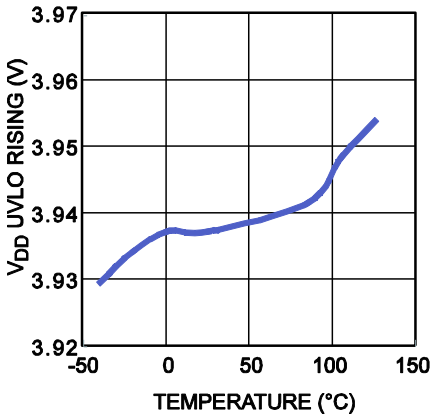
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, unless otherwise noted.

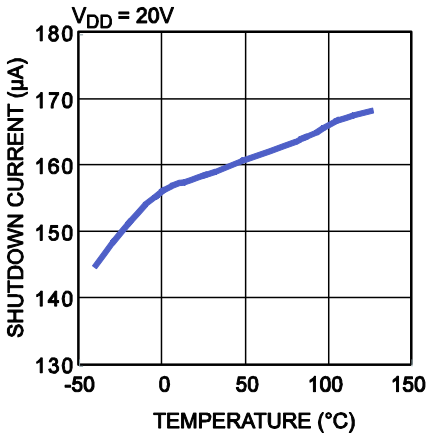
$V_{D1/D2}$ Breakdown Voltage vs. Temperature



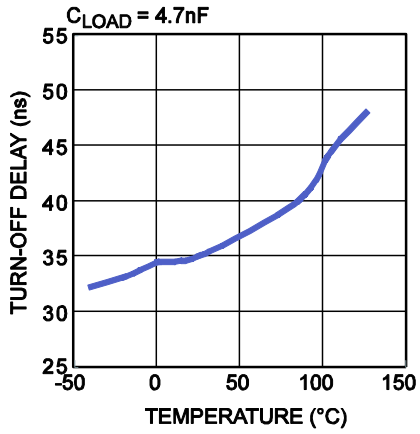
V_{DD} UVLO Rising vs. Temperature



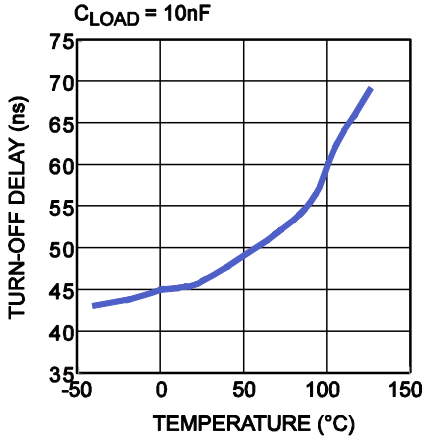
Shutdown Current vs. Temperature



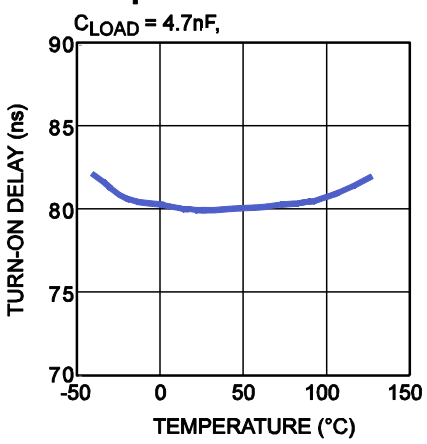
Turn-Off Delay vs. Temperature



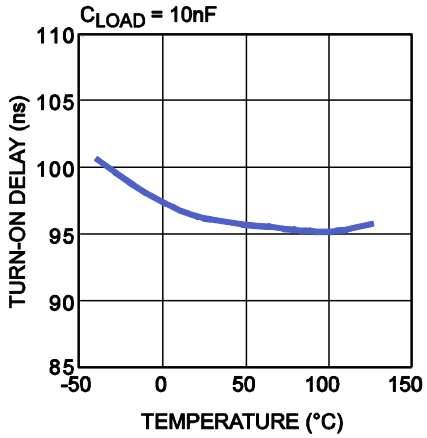
Turn-Off Delay vs. Temperature



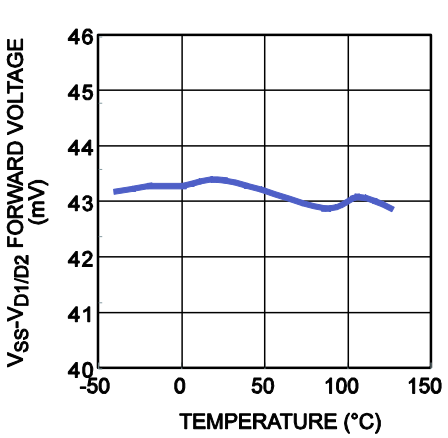
Turn-On Delay vs. Temperature



Turn-On Delay vs. Temperature



V_{SS}-$V_{D1/D2}$ Forward Voltage vs. Temperature



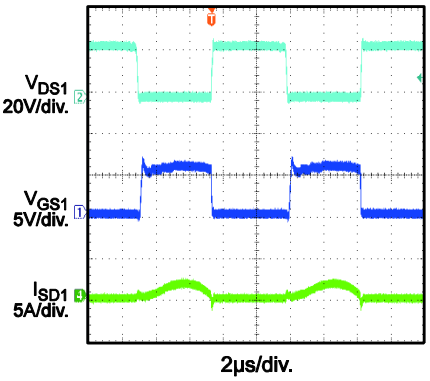
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 12V, unless otherwise noted.

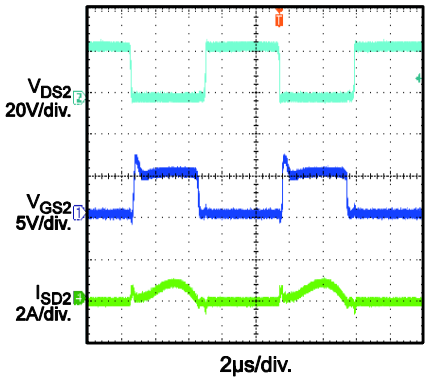
Operation in 90W LLC Converter

V_{IN} = 240V_{AC}, V_{OUT} = 12V,
I_{OUT} = 0.75A



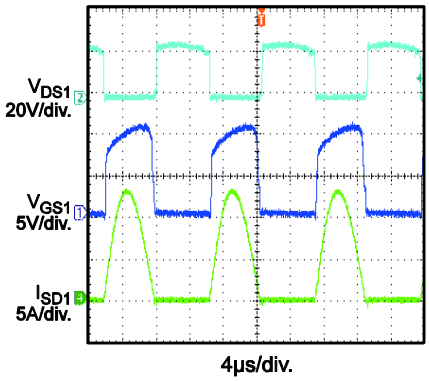
Operation in 90W LLC Converter

V_{IN} = 240V_{AC}, V_{OUT} = 12V,
I_{OUT} = 0.75A



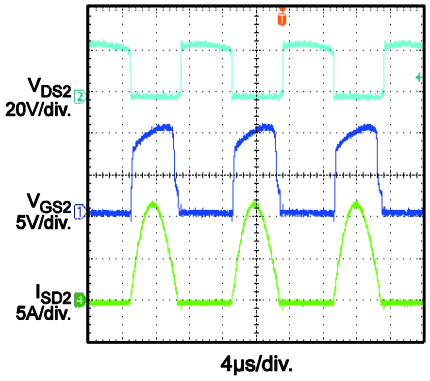
Operation in 90W LLC Converter

V_{IN} = 240V_{AC}, V_{OUT} = 12V,
I_{OUT} = 7.5A



Operation in 90W LLC Converter

V_{IN} = 240V_{AC}, V_{OUT} = 12V,
I_{OUT} = 7.5A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

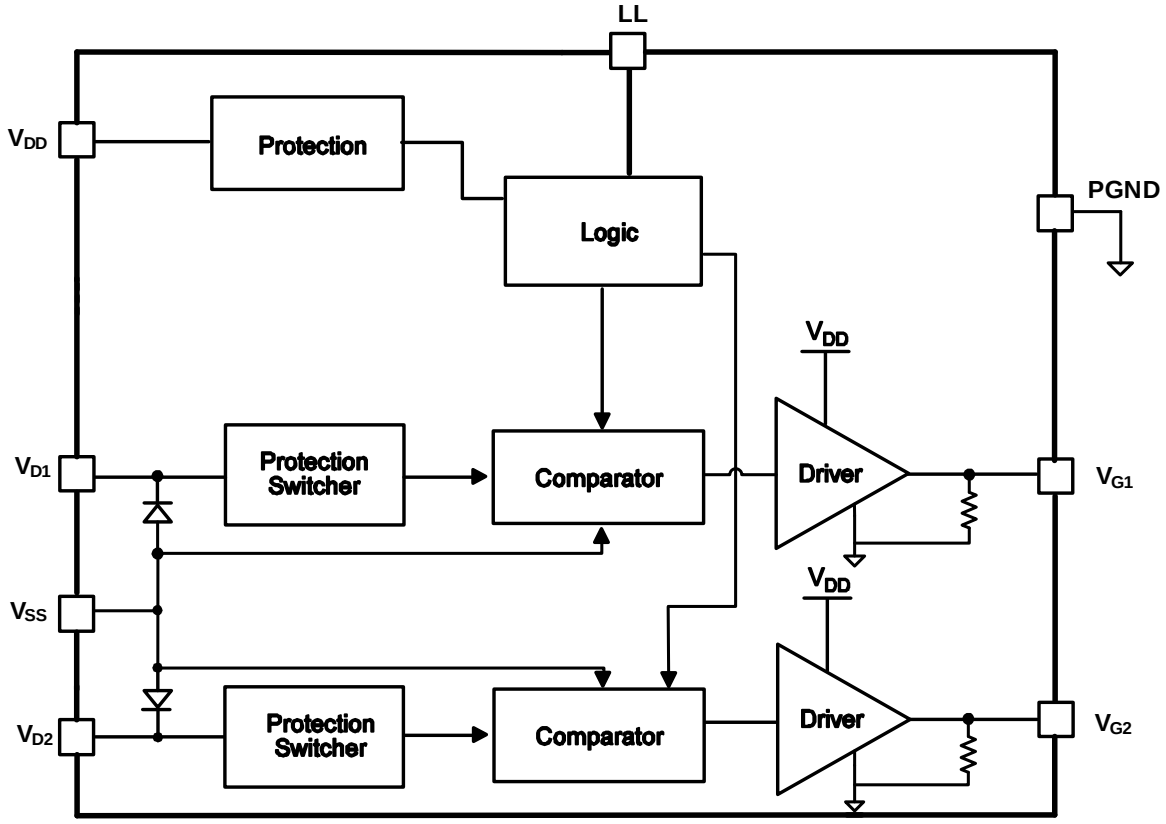


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

OPERATION

The MP6925A operates in discontinuous conduction mode (DCM), continuous conduction mode (CCM), and critical conduction mode (CrCM). When the device operates in DCM or CrCM, the control circuitry controls the gate in forward mode. The gate turns off when the MOSFET current is low. In CCM, the control circuitry turns off the gate during very fast transients.

VD Clamp

Because $V_{D1/2}$ can go as high as 180V, a high-voltage JFET is used at the input. To prevent excessive currents when $V_{D1/2}$ drops below -0.7V, place a 1kΩ resistor between $V_{D1/2}$ and the drain of the external MOSFET.

Under-Voltage Lockout (UVLO)

When V_{DD} falls below the V_{DD} UVLO threshold (about 3.75V), the MP6925A goes into sleep mode and $V_{G1/2}$ remains at a low level.

Enable

If the LL pin is pulled low, the MP6925A enters shutdown mode, which consumes 175µA of shutdown current. If LL is pulled high during the rectification cycle, the gate driver does not appear until the next rectification cycle begins (see Figure 2).

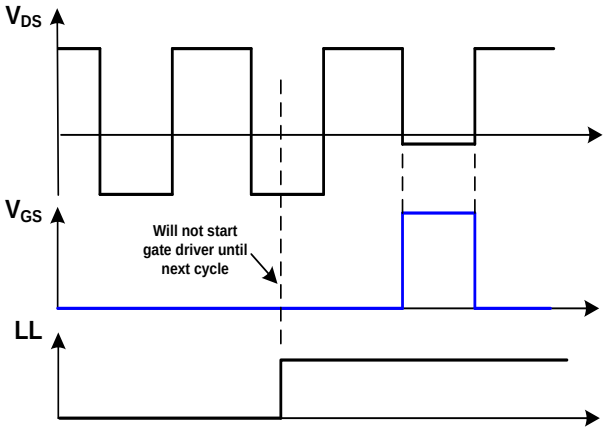


Figure 2: LL Control Scheme

Thermal Shutdown

If the junction temperature of the chip exceeds the thermal shutdown threshold 150°C, $V_{G1/2}$ pulls low, and the MP6925A stops switching. The IC resumes normal function after the junction temperature drops by 10°C.

Turn-On Phase

When the switching current flows through the MOSFET's body diode, there is a negative voltage drop (V_D - V_{SS}) across the body diode. V_{DS} falls below the turn-on threshold of the control circuitry (V_{LL-DS}), which triggers a charge current to turn on the MOSFET (see Figure 3).

Turn-On Blanking

The control circuitry offers a blanking function that ensures the MOSFET remains on or off for t_{B_ON} (about 1µs), which determines the minimum turn-on time. During the turn-on blanking period, the turn-off threshold is not blanked completely and changes to about 100mV (instead of $-V_{DRV-OFF}$ 40mv).

This ensures that the part can always turn off, though it turns off more slowly during the turn-on blanking period. To avoid shoot-through, set the synchronous period below t_{B_ON} during CCM in the LLC converter.

Conduction Phase

When V_{DS} rises above the forward voltage drop ($-V_{FWD}$) according to the decrease in switching current, the MP6925A pulls down the gate voltage. This eases the rise of V_{DS} by increasing the resistance of the synchronous MOSFET.

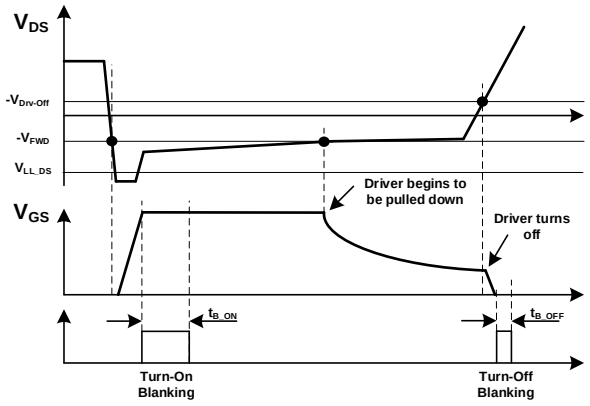


Figure 3: Turn-On/Off Diagram

Figure 3 shows how V_{DS} is adjusted to be about $-V_{FWD}$, even when the current through the MOSFET is fairly low. This function puts the driver voltage at a very low level when the synchronous MOSFET turns off, which boosts the turn-off speed.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold, the gate voltage is pulled to zero after a very short turn-off delay (see Figure 3).

Turn-Off Blanking

When V_{DS} reaches the turn-off threshold and the gate driver is pulled to zero, turn-off blanking is triggered. This ensures that the gate driver is off for a minimum time (t_{B_OFF}) to prevent any erroneous triggers on V_{DS}.

Light-Load Latch-Off Function

To improve efficiency, the MP6925A's gate driver latches off to improve efficiency and reduce driver loss under light-load conditions.

The MP6925A compares the CH1 SR gate (VG1) driver with the light-load enter pulse-width threshold (V_{LL-GS}) every cycle to determine the gate driver pulse width. If the CH1 SR gate driver pulse width remains below t_{LL} every cycle for longer than the light-load enter delay (t_{LL-D}), the MP6925A shuts down both channel gates immediately and enters light-load mode, which latches off the SR MOSFET (see Figure 4).

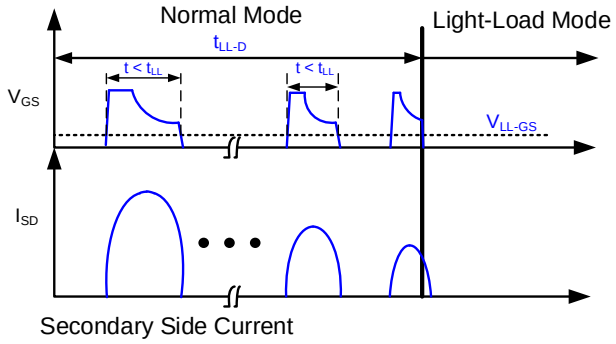


Figure 4: The MP6925A Enters Light-Load Mode

In light-load mode, the MP6925A monitors the body diode conduction time of CH1 by comparing the drain-source voltage of the SR MOSFET with the light-load exit switch-on threshold (V_{LL_DS}). If this time exceeds t_{LL} + t_{LL-H}, the IC exits light-load mode and initiates the gate driver in the next new switching cycle (see Figure 5 and Figure 6).

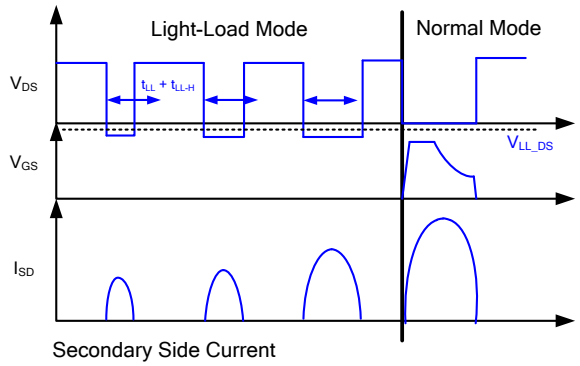


Figure 5: MP6925A Exiting Light-Load Mode

Light-load enter timing (t_{LL}) is configurable by connecting a resistor (R_{LL}) to LL. By monitoring the LL current (the LL voltage is kept at about 2V internally), t_{LL} can be calculated with Equation (1):

$$t_{LL} = R_{LL}(k\Omega) \times \frac{2.3\mu s}{100k\Omega} \quad (1)$$

If the LL pin resistor is disconnected, light-load mode is disabled. In this case, it is recommended to place a capacitor (typically 22pF) on the LL pin to avoid noise.

If the light-load mode of the MP6925A ends during the rectification cycle, the gate driver signal does not appear until the next rectification cycle begins (see Figure 6).

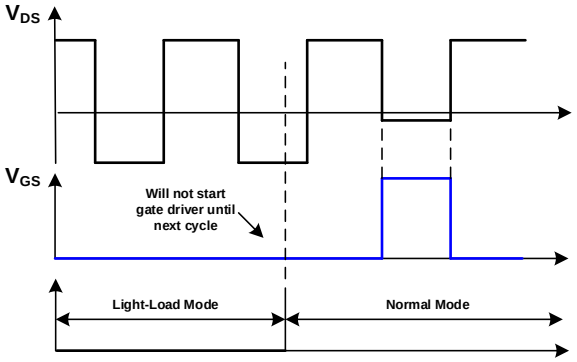


Figure 6: Gate Driver Starts after Exiting Light-Load Mode

Anti-Bounce Logic

The MP6925A has anti-bounce logic to protect the two-channel driver from cross conduction.

Figure 7 shows the anti-bounce logic for the two-channel driver. When channel 1 or 2 are turned off, the corresponding channel gate

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

driver is blanked until another channel is switched off.

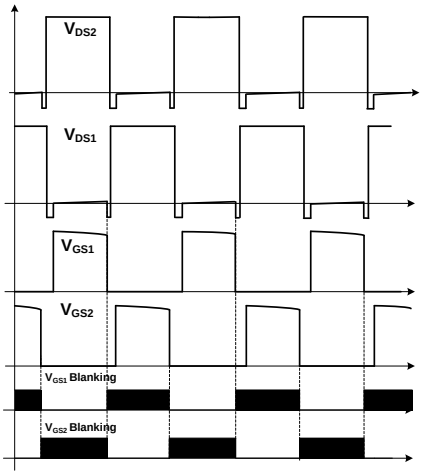


Figure 7: Gate Driver Anti-Bounce Logic

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

APPLICATION INFORMATION

SR MOSFET Selection and Driver Ability

Power MOSFET selection is a tradeoff between its resistance $R_{DS(ON)}$ and Q_G. To achieve high efficiency, a MOSFET with lower $R_{DS(ON)}$ is recommended. A higher Q_G paired with a lower $R_{DS(ON)}$ lowers the turn-on/off speed and increases power loss.

For the MP6925A, V_{DS} is adjusted at $-V_{FWD}$ during the driving period. A MOSFET with low $R_{DS(ON)}$ is not recommended because the gate driver may remain at a fairly low level, even when the system load is high. This makes the advantage of a low $R_{DS(ON)}$.

Figure 8 shows a typical LLC secondary-side waveform. To achieve a fairly high usage of the MOSFET's $R_{DS(ON)}$, it is expected that the MOSFET driver voltage is maximized until the last 25% of the SR conduction period.

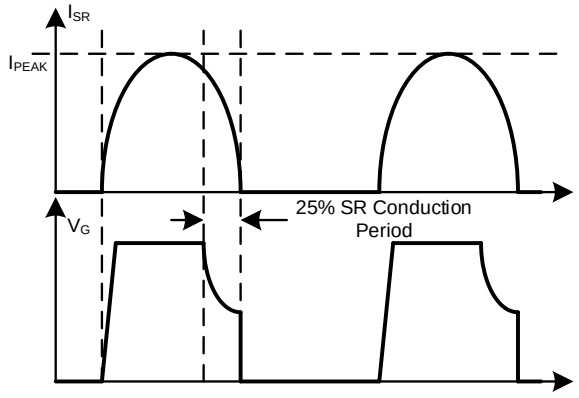


Figure 8: Typical Synchronous Rectification Waveform in LLC

V_{DS} can be calculated using Equation (2):

$$V_{DS} = -R_{DS(ON)} \times \frac{\sqrt{2}}{2} \times I_{PEAK} = -R_{DS(ON)} \times I_{OUT} = -V_{FWD} \quad (2)$$

Where V_{DS} is the drain-source voltage of the MOSFET.

It is recommended to keep the MOSFET's $R_{DS(ON)}$ above V_{FWD} / I_{OUT} (mΩ). For example, in a 10A application where V_{FWD} is set to 45mV, $R_{DS(ON)}$ should not be below 45mΩ.

The MOSFET's Q_G affects the turn-on/off delay. Figure 2 shows the turn-on delay (t_{DON}) and turn-off delay (t_{DOFF}). t_{DON} indicates how long the body diode conducts before the MOSFET turns on, while t_{DOFF} indicates how long the driver takes to turn off the MOSFET. A longer turn-on delay means the MOSFET's body diode conducts for longer, which lowers overall efficiency. A longer turn-off delay increases the risk of shoot-through during CCM.

Figure 9 shows t_{DON} according to different C_{LOAD} values.

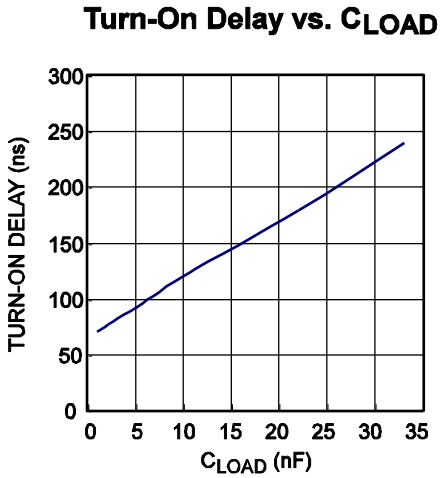


Figure 9: Turn-On Delay vs. C_{LOAD}

Figure 10 shows t_{DOFF} according to different C_{LOAD} values.

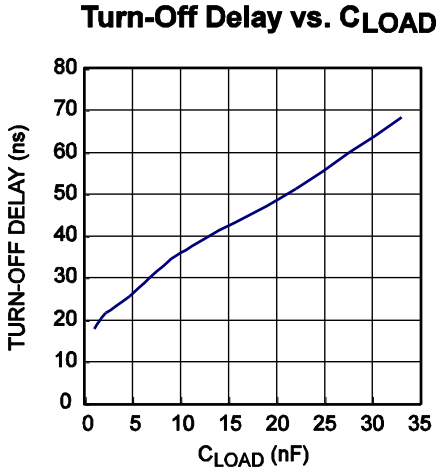


Figure 10: Turn-Off Delay vs. C_{LOAD}

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Figure 15 shows how t_{ON} affects system efficiency.

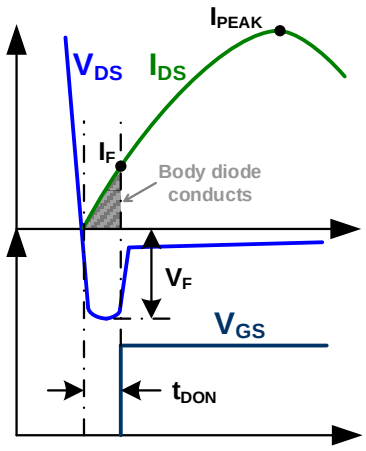


Figure 11: Turn-On Delay Effect on Efficiency

During t_{DON}, the body diode of the SR MOSFET conducts, which leads to a power loss (P_{ON}) that can be calculated with Equation (3):

$$P_{ON} \approx \frac{V_F \times I_F}{2} \times 2f_{SW} \times t_{DON} = V_F \times I_F \times f_{SW} \times t_{DON} \quad (3)$$

Where V_F is the body diode forward voltage drop, I_F is the switching current when the turn-on delay (t_{DON}) has ended, and f_{SW} is the switching frequency.

If the switching current is considered to be a complete sine wave, I_F can be estimated with Equation (4):

$$I_F = I_{PEAK} \times \sin(2 \times f_{SW} \times t_{DON} \times \pi) \quad (4)$$

Where I_{PEAK} is the peak switching current through the MOSFET, calculated with Equation (5):

$$I_{PEAK} \approx \frac{\pi}{2} \times I_{OUT} \quad (5)$$

Where I_{OUT} is the system output current.

When plugging the values from Equation (4) and Equation (5) into Equation (3), the turn-on delay power loss (P_{ON}) through the SR MOSFET's body diode can be calculated with Equation (6):

$$P_{ON} = \frac{\pi}{2} \times I_{OUT} \times V_F \times f_{SW} \times t_{DON} \times \sin(2 \times f_{SW} \times t_{DON} \times \pi) \quad (6)$$

Figure 12 shows how different turn-on delay values affect efficiency according to different output voltages. To keep the body diode conduction loss at a fairly low level (below 0.5% of the output power), the turn-on delay should be less than 5% of the switching cycle. For example, in a f_{SW} = 200kHz LLC system, the switching cycle is about 5µs. It is recommended to select the MOSFET so that t_{DON} is shorter than 250ns.

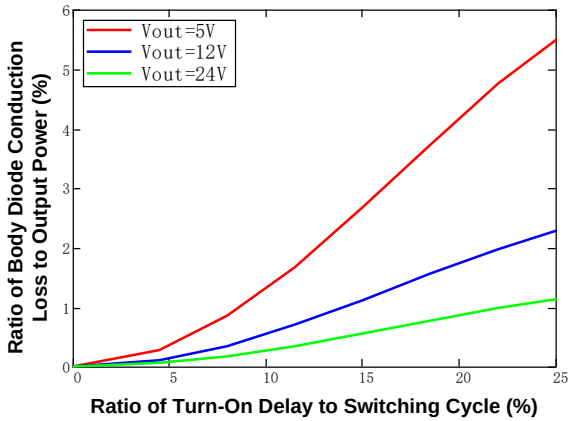


Figure 12: Turn-On Delay vs. Power Loss

The turn-off delay (t_{DOFF}) is critical in CCM applications with fast transients. Choose the MOSFET that keeps t_{DOFF} below the CCM current transient duration. Otherwise, the MOSFET may require a lower Q_G, or an external totem pole driver circuit may be added to prevent shoot-through.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PCB Layout Guidelines

PCB layout is vital for stable operation. For the best results, follow the guidelines below:

Sensing for V_D/V_S

1. Keep the sensing connections (V_{D1}/V_{SS}, V_{D2}/V_{SS}) as close to each of the MOSFETs (drain/source) as possible.
2. Keep the two channels' sensing loops separated from each other.
3. Make the sensing loop as small as possible (see Figure 13).

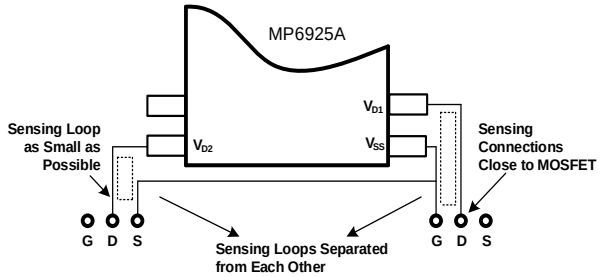


Figure 13: Sensing for V_D/V_S

Figure 14 shows a layout example of the MP6925A driving PowerPAK SOIC-8 package MOSFETs with two separate, small, sensing loops.

V_{DD} Decoupling Capacitor

1. Place a minimum 1µF decoupling capacitor from V_{DD} to PGND, close to the IC, for adequate filtering (see Figure 14).

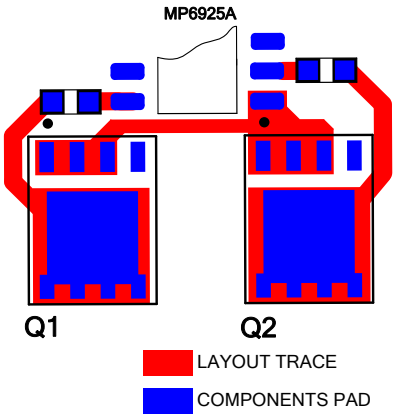


Figure 14: Layout Example for Sensing Loop and V_{DD} Decoupling

System Power Loop

1. Keep the two channels' power loops separated from each other (see Figure 15) to minimize the interaction between the two channels' power loops, which may affect the voltage sensing of the IC.
2. Make the power loop as small as possible to reduce parasitic inductance.

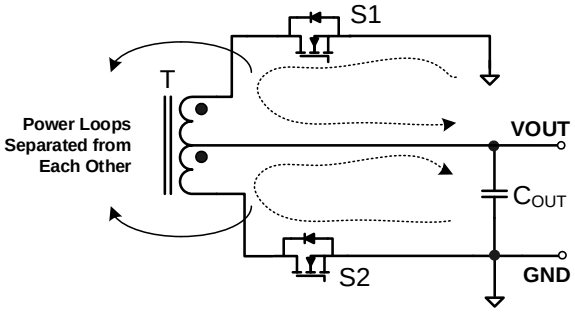


Figure 15: System Power Loop

3. Ensure the power loop trace has a minimized loop length (see Figure 16).
4. Ensure the two channel power traces do not cross one another.
5. Place the driver's sensing loop trace away from the power loop trace (see Figure 16). The sensing and power loop traces can be placed on different layers to stay separated.
6. Do not place the driver IC inside the power loop, as it may affect MOSFET voltage sensing.

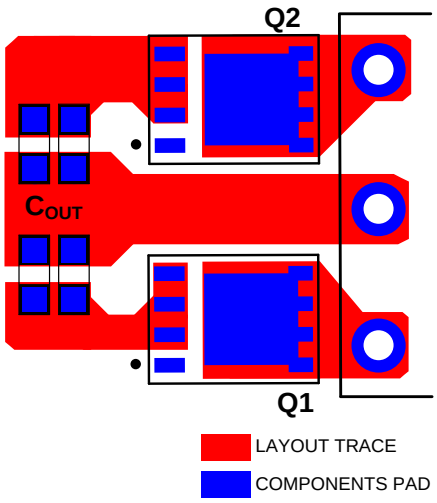
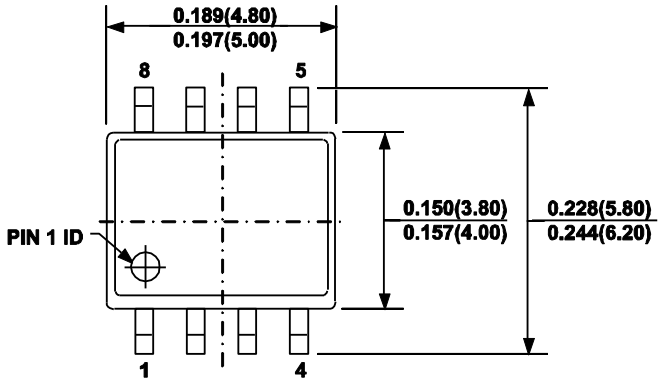


Figure 16: Layout Example for System Power Loop

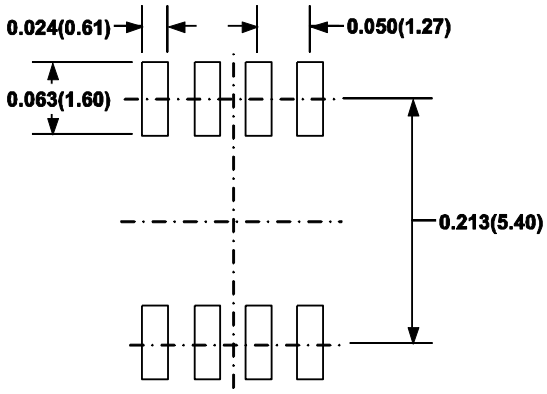
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION

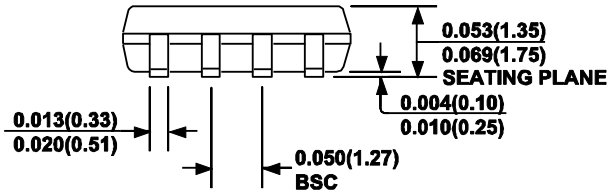
SOIC-8



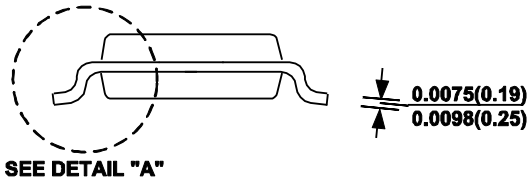
TOP VIEW



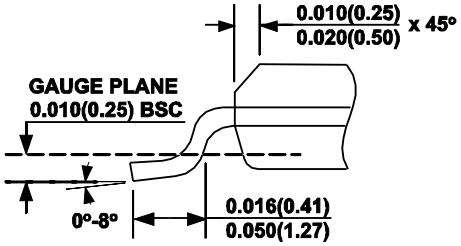
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



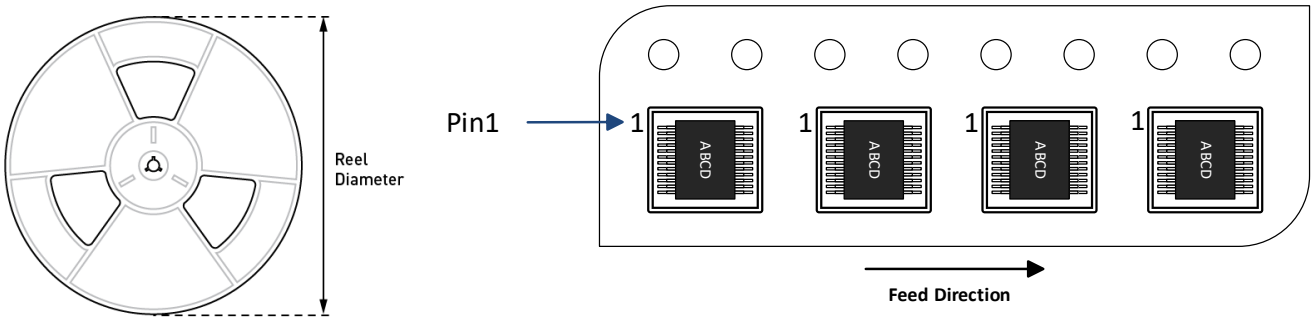
DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6925AGS	SOIC-8	2500	100	13in	12mm	8mm

Notice: The information in this document is subject to change without notice. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.