MP6922A

Dual, Fast-Turn–Off, Intelligent Rectifier

The Future of Analog IC Technology

DESCRIPTION

The MP6922A is a dual, fast-turn–off, intelligent rectifier for synchronous rectification in LLC resonant converters.

The IC drives two N-channel MOSFETs and regulates their forward voltage drop to about 30mV and turns it off before the switching current goes negative.

MP6922A has a light-load function to latch off the gate driver under light-load conditions, thus limiting the current to below 600μA.

The MP6922A's fast turn-off enables both continuous-conduction mode and discontinuous-conduction mode. An internal reverse-current protection function ensures safe MOSFET operation under high-frequency continuous-current conditions.

MP6922A requires a minimal number of readily-available standard external components and is available in SOIC8E, SOIC8, and SOIC14 packages.

FEATURES

- Works with Both Standard and Logic-Level MOSFETs
- Compatible with Energy Star's 0.5W Standby Requirements
- V_{DD} Range from 8V to 24V
- 30mV V_{DS} Regulation Function (1)
- Fast Turn-Off Total Delay of 20ns
- Reverse-Current–Protection Function
- Maximum Switching Frequency of 300kHz
- Light Load Mode Function (1) with <600μA Quiescent Current
- Supports CCM, CrCM and DCM Operation
- Available in SOIC8E, SOIC8, and SOIC14 packages
- Halogen-free

APPLICATIONS

- AC-DC Adapters
- LCDs & PDP TVs
- Telecom SMPS

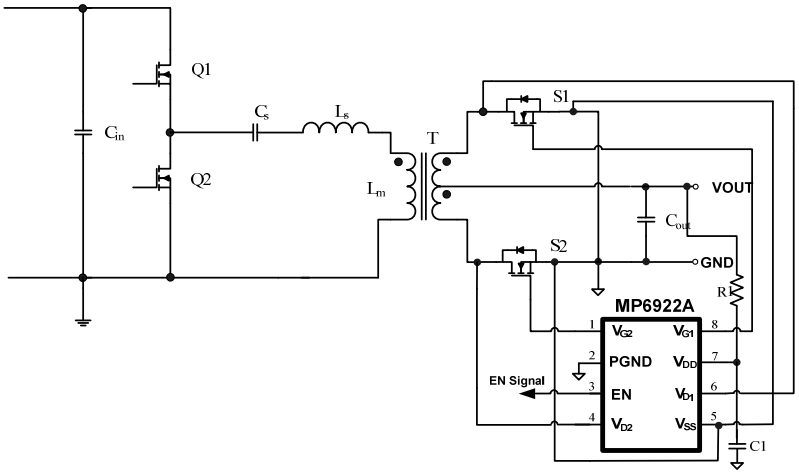
All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

Notes:

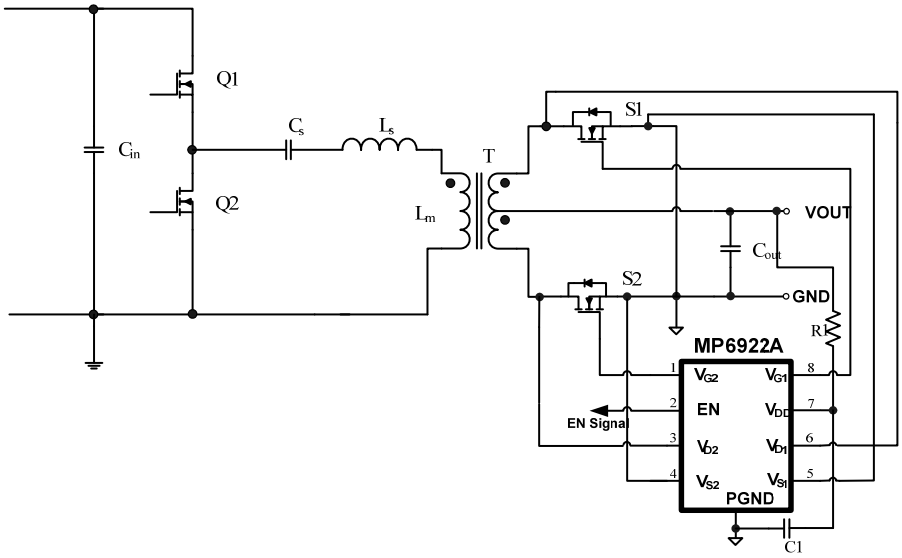
1) Related issued patent: US Patent US8,067,973; US8,400,790. CN Patent ZL201010504140.4; ZL200910059751.X. Other patents pending.

TYPICAL APPLICATION

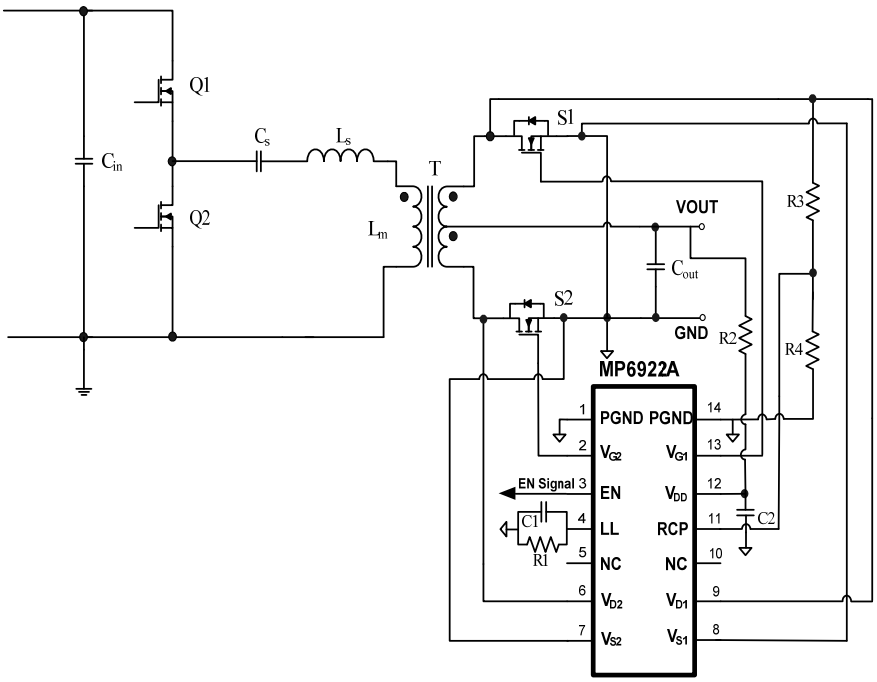


SOIC8

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.



SOIC8E



SOIC14

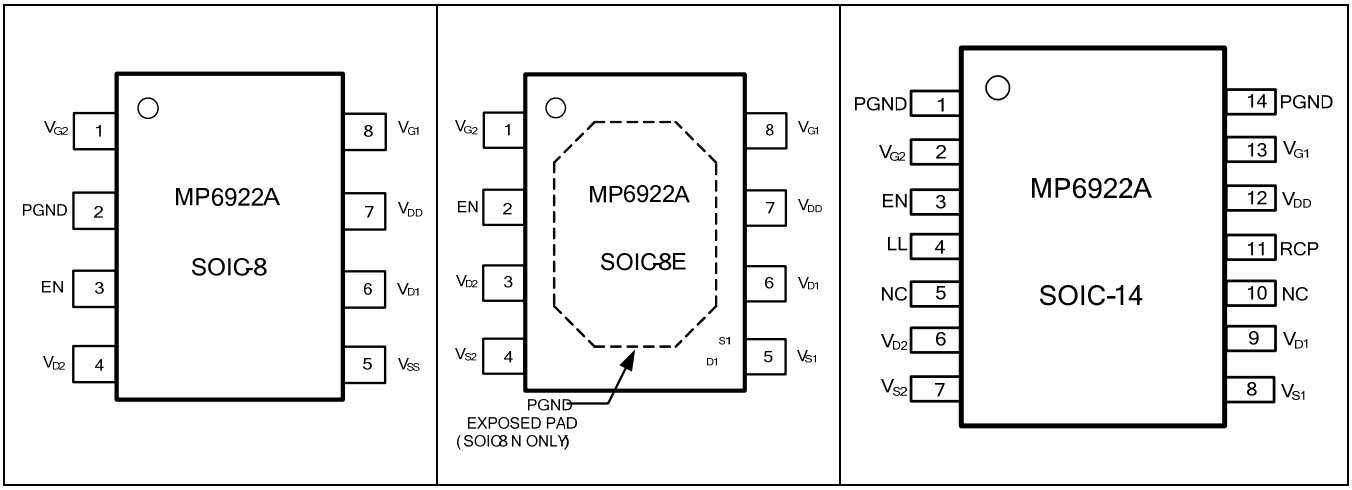
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number	Package	Top Marking
MP6922AGSE*	SOIC8	MP6922A
MP6922AGN**	SOIC8E	MP6922A
MP6922AGS***	SOIC14	MP6922A

*For Tape & Reel, add suffix –Z (e.g. MP6922AGSE–Z);
**For Tape & Reel, add suffix –Z (e.g. MP6922AGN–Z);
***For Tape & Reel, add suffix –Z (e.g. MP6922AGS–Z);

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (2)

V_{DD} to V_{S1},V_{S2}, V_{SS} .....-0.3V to +26V
PGND to V_{S1},V_{S2}, V_{SS}.....-0.3V to +0.3V
V_{G1} to V_{S1}, V_{SS}..... -0.3V to V_{DD}
V_{G2} to V_{S2}, V_{SS}..... -0.3V to V_{DD}
V_{D1} to V_{S1}, V_{SS}.....-0.7V to +180V
V_{D2} to V_{S2}, V_{SS}.....-0.7V to +180V
LL, EN to V_{S1},V_{S2}, V_{SS} .....-0.3V to +6.5V
Maximum Operating Frequency..... 300 kHz
Continuous Power Dissipation .. (T_A = +25°C) (3)
SOIC8 ..... 1.4W
SOIC8E..... 2.5W
SOIC14 ..... 1.5W
Junction Temperature.....150°C
Lead Temperature (Solder).....260°C
Storage Temperature ..... -55°C to +150°C

Recommended Operation Conditions (4)

V_{DD} to V_{S1},V_{S2}, V_{SS}.....8V to 24V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}
SOIC8	90	45 ... °C/W
SOIC8E	50	10 ... °C/W
SOIC14	86	38 ... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) T_A=+25°C. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB. Without heatsink.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V, -40°C ≤T_J≤ 125°C, unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units
V_{DD} Voltage Range				8		24	V
V_{DD} UVLO Threshold		Rising		4.8	6.0	7.0	V
		Hysteresis		0.5	1	1.5	V
Operating Current	I_{CC}	C_{LOAD}=5nF, F_{SW}=100kHz		12	18	23	mA
		C_{LOAD}=10nF, F_{SW}=100kHz		24	27	31	mA
Shutdown Current		V_{DD}=20V, EN=0V				600	µA
Light-Load Mode Current						600	µA
Thermal Shutdown					150		°C
Thermal Shutdown hysteresis					30		°C
Enable Shutdown Threshold		Rising		1.1	1.5	2.0	V
		Hysteresis			0.2	0.45	V
Enable UVLO Threshold		Rising		2.3	3	3.6	V
		Hysteresis			0.2	0.45	V
Internal Pull-up Current on EN					10	16	µA
CONTROL CIRCUITRY SECTION							
$V_{S1,2}$ –$V_{D1,2}$ Forward Voltage	V_{fwd}			15	30	45	mV
Turn-on delay	T_{Don}	C_{LOAD}=5nF	-20°C≤T_J≤125°C		150	200	ns
			-40°C≤T_J<-20°C		250		
	T_{Don}	C_{LOAD}=10nF	-20°C≤T_J≤125°C		250	300	ns
			-40°C≤T_J<-20°C		350		
Input Bias Current on $V_{D1,2}$ pin		$V_{D1,2}$ = 180V				1.5	µA
Minimum ON-Time	T_{MIN}	C_{LOAD} = 5nF			1		µs
Minimum OFF-Time	T_{OFF}				1.6		µs
Light-Load–Enter Delay	$T_{LL-Delay}$	R_{LL}=100kΩ		80	160	260	µs
Light-Load–Enter Pulse Width	T_{LL}	R_{LL}=100kΩ			2.2		µs
Light-Load Turn-On Pulse Width Hysteresis	T_{LL-H}	R_{LL}=100kΩ			0.2		µs
Light-Load–Enter OFF Period Width	T_{LL-OFF}	R_{LL}=100kΩ			50		µs
Light-Load Exit-Pulse Width Threshold ($V_{D1,2}$-$V_{S1,2}$)	V_{LL-DS}			-450	-300	-140	mV
Light-load Enter-Pulse Width Threshold ($V_{G1,2}$-$V_{S1,2}$)	V_{LL-GS}				1.0		V
Reverse-Current–Protection Threshold	V_{RCP}			2.5	3	3.5	V
Reverse-Current–Protection Latch Time	T_{RCP}			80	150	230	µs
GATE DRIVER SECTION							
$V_{G1,2}$ (Low)		I_{LOAD}=1mA				0.1	V
$V_{G1,2}$ (High)		V_{DD} >16V		13	14.5	16	V
		V_{DD} <16V			V_{DD}-2.2		
Turn-Off Threshold ($V_{S1,2}$-$V_{D1,2}$)					-30		mV
Turn-Off Propagation Delay		$V_{D1,2}$= V_{SS}			15		ns

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD} = 12V, -40°C ≤T_J≤ 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Turn-Off Total Delay	t_{Doff}	$V_{D1,2}$= V_{SS}, C_{LOAD}=5nF, R_{GATE}=0Ω		50	75	ns
		$V_{D1,2}$= V_{SS}, C_{LOAD}=10nF, R_{GATE}=0Ω		50	75	ns
Pull-Down Impedance				1	2	Ω
Pull-Down Current		3V <$V_{G1,2}$<10V		3		A

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

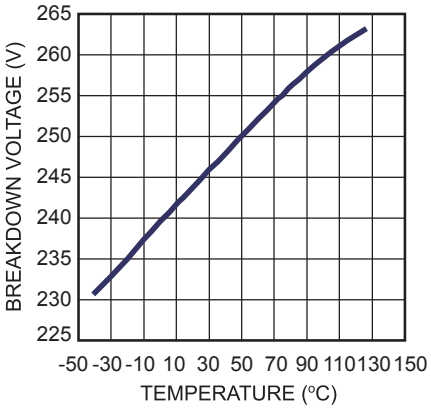
PIN FUNCTIONS

Pin # (SOIC8)	Pin # (SOIC8E)	Pin # (SOIC14)	Name	Description
1	1	2	V_{G2}	MOSFET 2 Gate Driver Output.
3	2	3	EN	Enable Pin. Enables the internal IC logic when the EN pin voltage exceeds the EN shutdown threshold; the gate driver remains latched until the EN voltage exceeds the EN UVLO threshold.
4	3	6	V_{D2}	MOSFET 2 Drain Voltage Sense.
-	4	7	V_{S2}	Source pin used as reference for V_{D2}.
-	5	8	V_{S1}	Source pin used as reference for V_{D1}.
6	6	9	V_{D1}	MOSFET 1 Drain Voltage Sense.
7	7	12	V_{DD}	Supply Voltage.
8	8	13	V_{G1}	MOSFET 1 Gate Driver Output.
2	EXPOSED PAD	1,14	PGND	Power Ground. Power switch return.
-	-	5,10	NC	No Connection.
-	-	4	LL	Light-Load–Timing Set. Connect a resistor to set the light-load timing.
-	-	11	RCP	Reverse Current Protection. Internal 5V reference.
5	-	-	V_{SS}	Common Source. Used as reference for both channels.

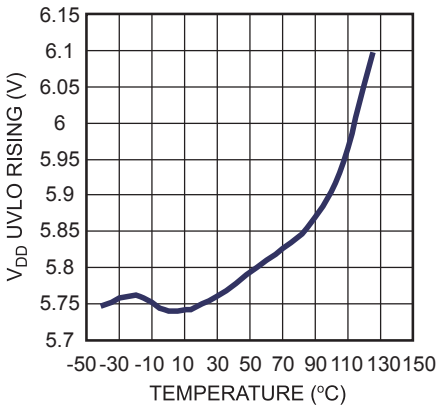
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

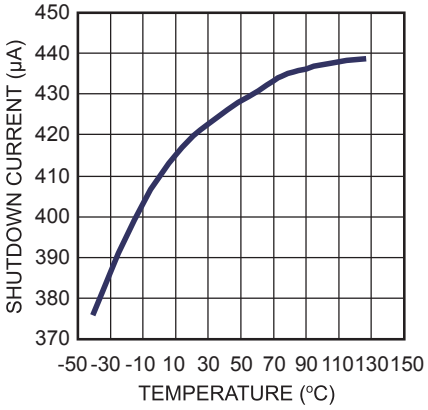
$V_{D1,2}$ Breakdown Voltage vs. Temperature



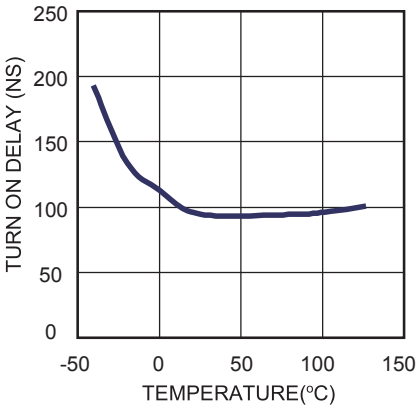
V_{DD} UVLO Rising vs. Temperature



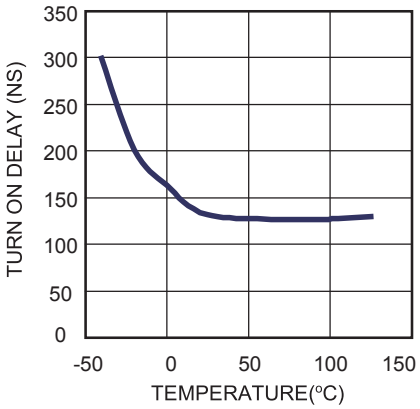
Shutdown Current (V_{DD}=20V) vs. Temperature



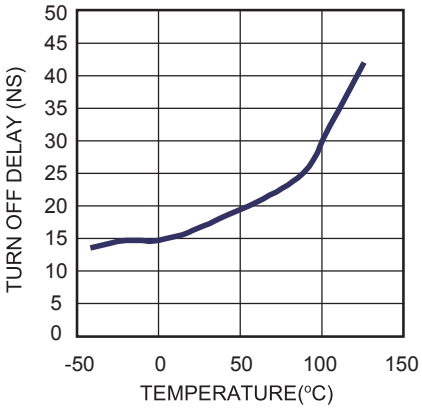
Turn On Delay (Cload=5nF) vs. Temperature



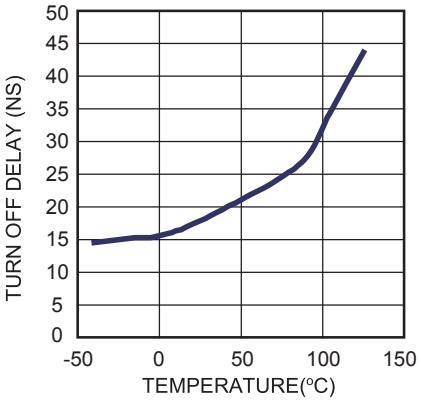
Turn On Delay (Cload=10nF) vs. Temperature



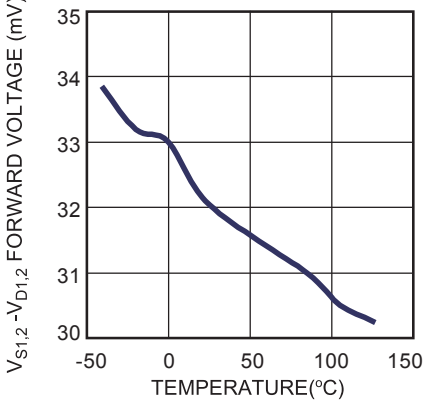
Turn Off Delay (Cload=5nF) vs. Temperature



Turn Off Delay (Cload=10nF) vs. Temperature



$V_{S1,2}$-$V_{D1,2}$ Forward Voltage vs. Temperature

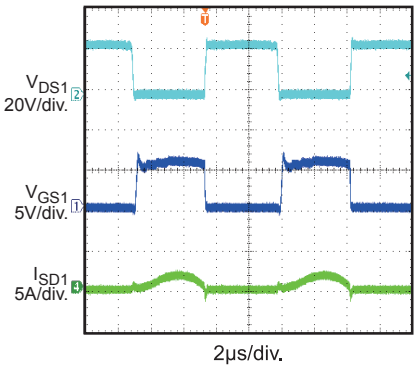


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

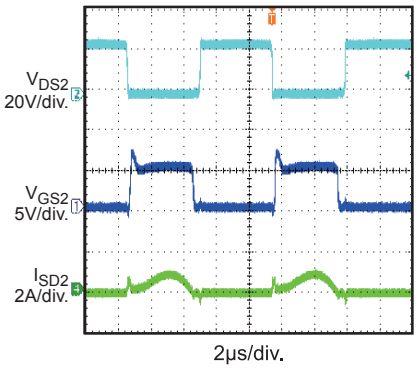
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 12V, unless otherwise noted.

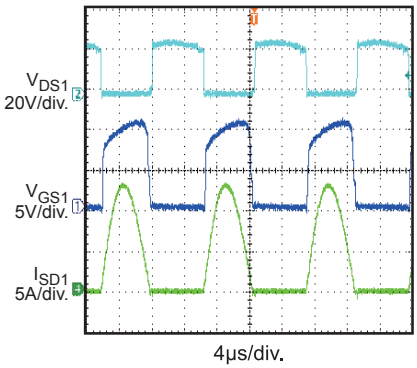
Operation in 90W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 0.75A



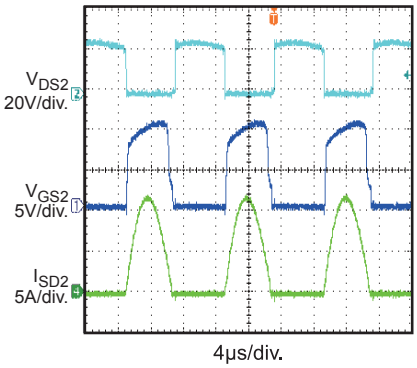
Operation in 90W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 0.75A



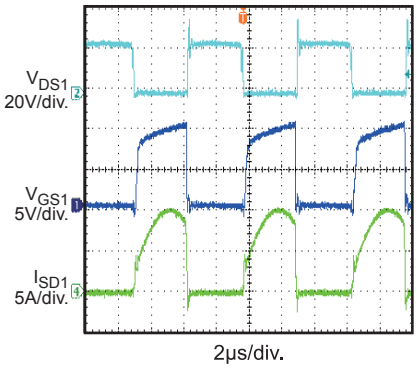
Operation in 90W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 7.5A



Operation in 90W LLC Converter
V_{IN} = 240V_{AC}, V_{OUT} = 12V, I_{OUT} = 7.5A



Operation in 90W LLC Converter
V_{IN} = 265V_{AC}, V_{OUT} = 12V, I_{OUT} = 7.5A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

BLOCK DIAGRAM

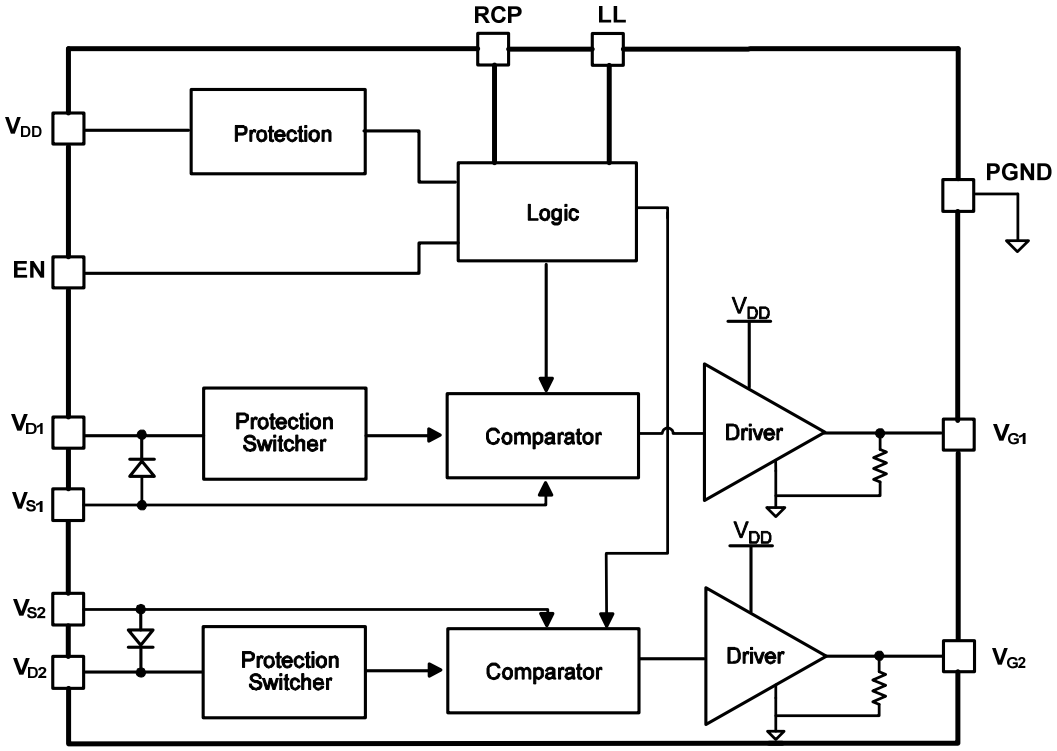


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

OPERATION

The MP6922A operates in discontinuous-conduction mode (DCM), continuous-conduction mode (CCM), and critical conduction mode (CrCM) condition. Operating in either DCM or CrCM, the control circuitry controls the gate in forward mode; it turns the gate off when the MOSFET current is low. In CCM, the control circuitry turns off the gate during very fast transients.

Blanking

The control circuitry contains a blanking function that ensure that when the MOSFET turns ON/OFF, the MOSFET remains in that state for ~1µs, which determines the minimum ON-time. During the turn-on blanking period, the turn-off threshold is not totally blanked, but changes to ~+100mV (instead of +30mV). This ensures that the part can always turn OFF even during the turn-on blanking period (albeit slower, so avoid setting the synchronous period to less than 1µs at CCM condition in the LLC converter to eliminate shoot-through).

VD Clamp

The MP6922A uses a high-voltage JFET at its input because $V_{D1,2}$ can go as high as 180V. Connect a small resistor between the $V_{D1,2}$ pin and the external MOSFET drain to avoid excessive currents when V_G goes below -0.7V.

Under-Voltage Lockout (UVLO)

When V_{DD} goes below the UVLO threshold, the part enters sleep mode and a 10kΩ resistor pulls down V_G.

Enable Pin

If EN is pulled low, the part enters sleep mode.

Thermal Shutdown

If the junction temperature of the IC exceeds 150°C, V_G is pulled low and the part stops switching. The part resumes normal operation after the junction temperature has dropped to 120°C.

Turn-On Phase

V_{DS} (V_D–V_{SS}) goes negative (<-500mV) when the switch current flows through the MOSFET's body diode. If V_{DS} is much lower than the turn-on threshold of the control circuitry (-30mV), then the MOSFET turns on after about 200ns turn-on delay (Figure 2).

Triggering the turn-on threshold (-30mV) causes the circuit to add a blanking time (minimum on-time 1µs), during which the turn-off threshold changes from +30V to +100mV. This blanking time avoids erroneous triggering caused by ringing on the synchronous power switch.

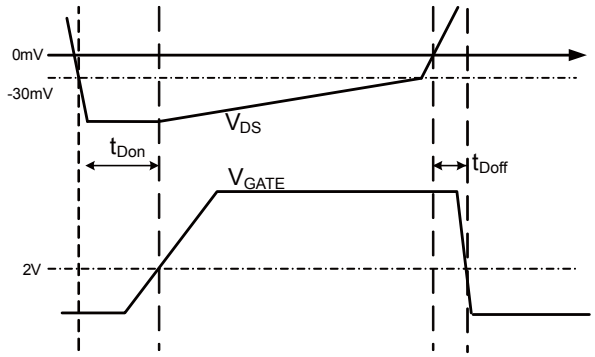


Figure 2: Turn-On and Turn-Off delay

Conducting Phase

When the MOSFET turns ON, V_{DS} ($-I_{SD}\times R_{DS(ON)}$) rise relative to the switch current (I_{SD}) drop. When V_{DS} rises above the turn-on threshold (–30mV), the control circuitry stops pulling up the gate driver and the MOSFET driver voltage drops, which increases the MOSFET's $R_{DS(ON)}$. This adjusts V_{DS} ($-I_{SD}\times R_{DS(ON)}$) to around -30mV even when the switch current I_{SD} is fairly small, and can prevent the internal driver from triggering until the current through the MOSFET has dropped to near zero.

Turn-Off Phase

When V_{DS} rises to trigger the turn-off threshold (30mV), the control circuitry pulls down the driver switch voltage after a 20ns turn-off delay (shown in Figure 2). Similarly, a 1.6µs blanking time occurs after the switch turns off, during which the MOSFET does not turn on to avoid erroneous triggering.

Figure 3 shows the MP6922A operating under a heavy-load. The high current initially saturates the driver voltage. After V_{DS} goes above –30mV, the driver voltage decreases to adjust the V_{DS} to around –30mV.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

Figure 4 shows the MP6922A operating at light-load. The low current prevents the driver voltage from saturating but decreases when the synchronous power switch turns on and adjusts V_{DS}.

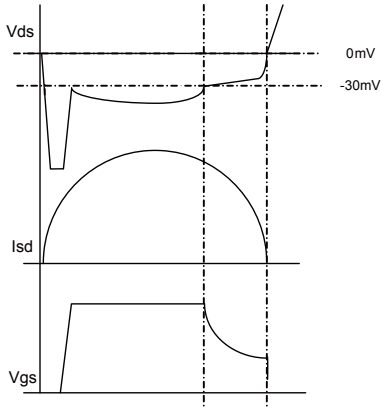


Figure 3: Synchronous Rectification Operation at Heavy Load

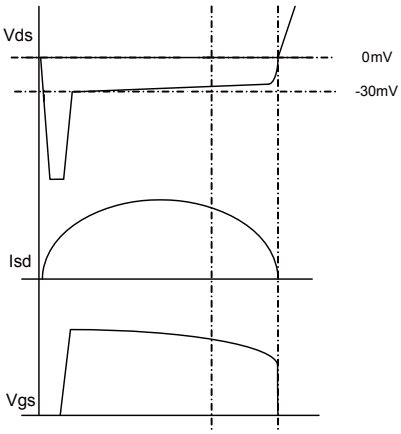


Figure 4: Synchronous Rectification Operation at Light Load

Light-Load Latch-Off Function

The gate driver of MP6922A is latched to limit driver losses under light-load condition to improve light-load efficiency.

Normal Operation Latch Off

When the MOSFET's switching-cycle conducting period falls below 2.2μs (τ_{LL}), the MP6922A enters light-load mode and latches off the MOSFET after a 160μs delay (light-load-enter delay, $\tau_{LL\text{-}Delay}$)

After entering light-load mode, the MP6922A monitors the MOSFET's body diode conducting period by sensing V_{DS} (when V_{DS} exceeds –300mV ($V_{LL\text{-}DS}$), MP6922A treats the the MOSFET's body-diode conducting period as finished). If the MOSFET's body diode conducting period exceeds 2.4μs (τ_{LL}+$\tau_{LL\text{-}H}$), light-load mode ends and the MOSFET unlatches to restart the synchronous rectification.

For the SOIC14 package. the MP6922A has an LL pin that allows τ_{LL} to be adjusted by an external resistor:

$$\tau_{LL} = 2.2\mu s \cdot \frac{R_{LL}}{100k\Omega}$$

Latch Off during Burst Operation

The IC also monitors the synchronous MOSFET OFF period. If the OFF period exceeds the light-load–enter OFF period width ($\tau_{LL\text{-}OFF}$), the MP6922A enters light-load mode and latches off the gate driver.

The gate driver is unlatched when the drain-source voltage of the synchronous MOSFET V_{DS} drops below –30mV.

Reverse Current–Protection Function

When the LLC system operates in CCM at a very high frequency, the synchronous current may reverse before the IC turns off the gate driver, which can lead to shoot-through (in center-tapped outputs with full-wave rectification topologies). The MP6922A has a protection function to latch off the gate driver when the current reverses before the driver signal is pulled low.

When the synchronous current reverses, the high spike can be observed between the MOSFET's drain/source. The MP6922A monitors the voltage through the RCP pin using a voltage divider. When the voltage of RCP pin exceeds V_{RCP}, MP6922A latches the driver signal of both channels for ~150μs (τ_{RCP}) to protect the synchronous MOSFET. At the end of τ_{RCP}, MP6922A restarts the synchronous rectification.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

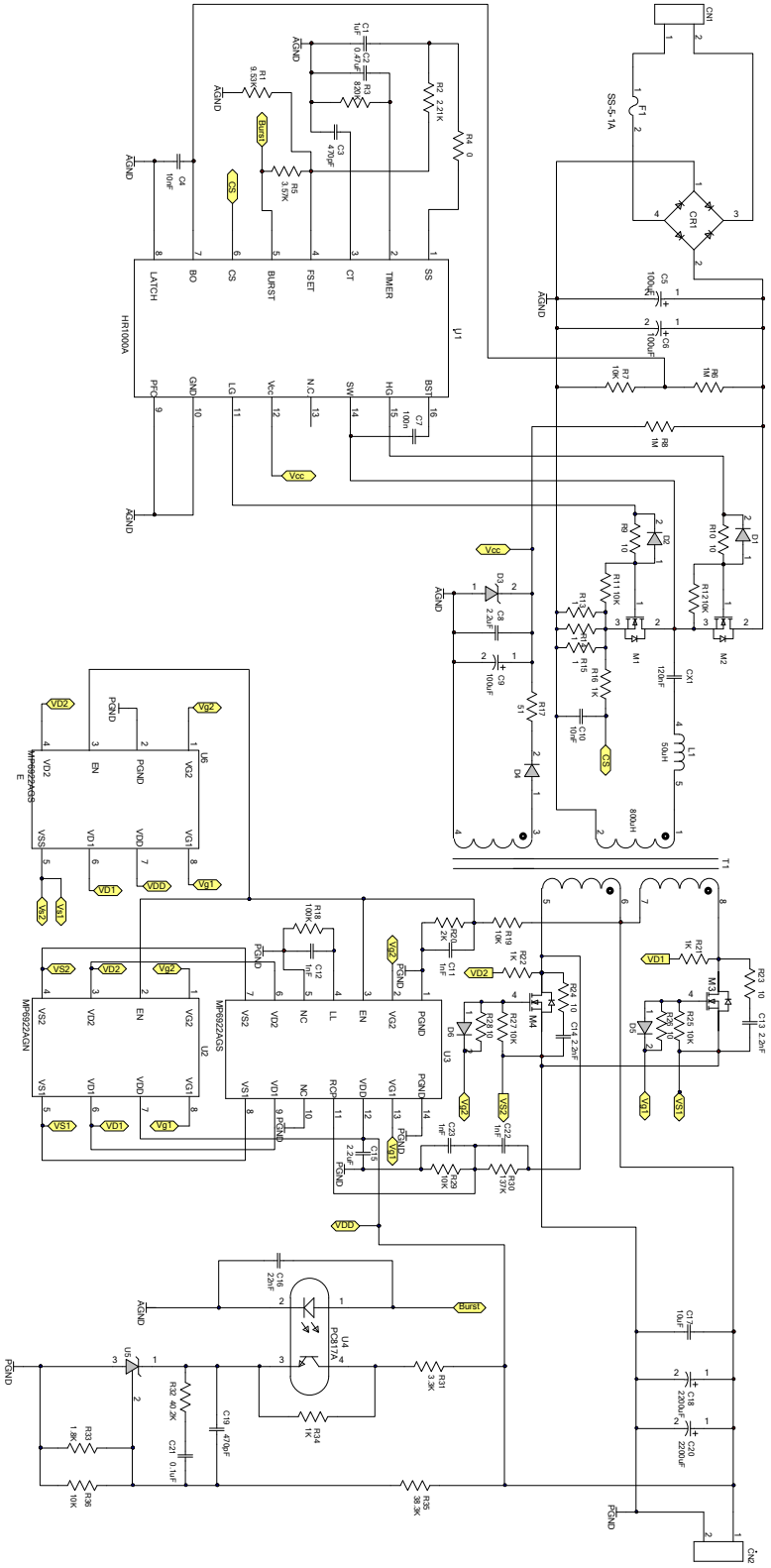
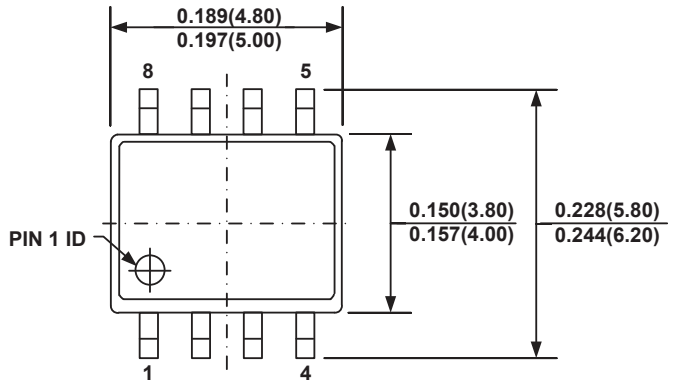


Figure 5—Synchronous Rectification in LLC with MP6922A

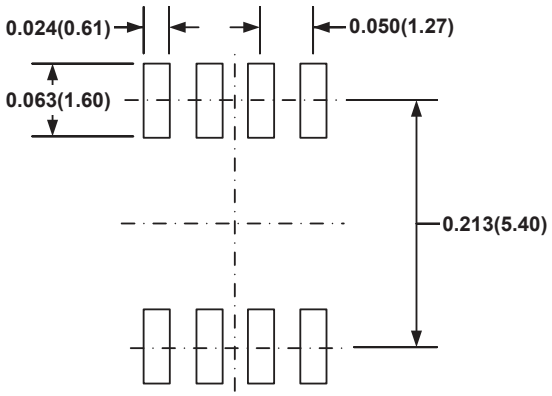
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

PACKAGE INFORMATION

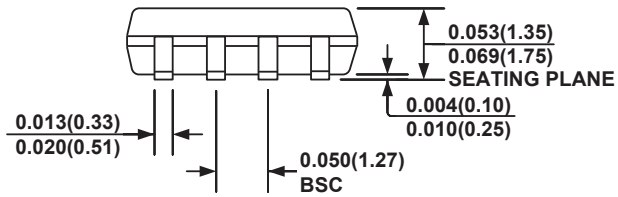
SOIC8



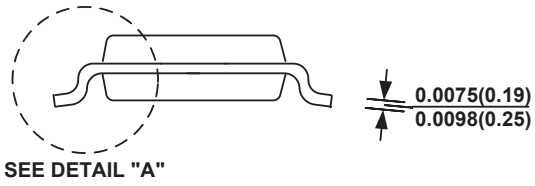
TOP VIEW



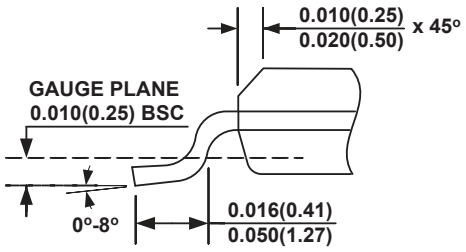
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



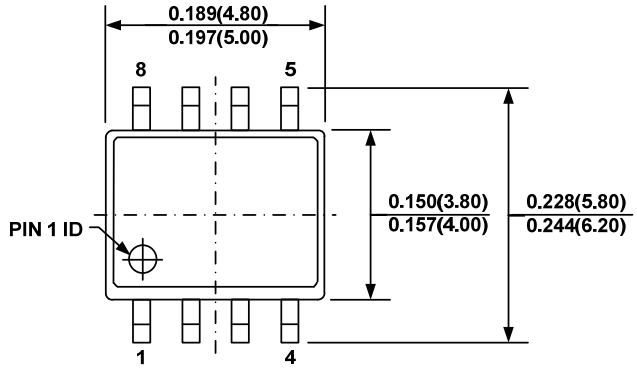
DETAIL "A"

NOTE:

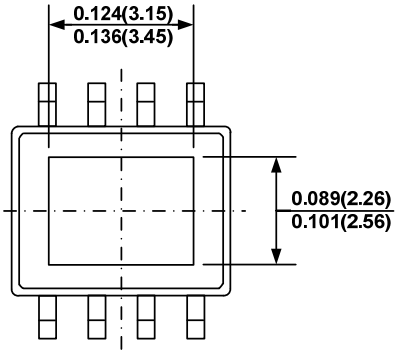
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

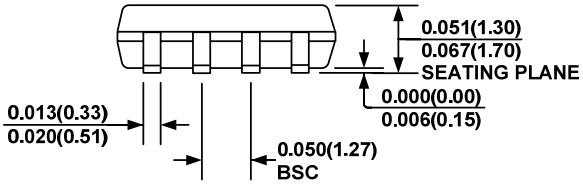
SOIC8E (EXPOSED PAD)



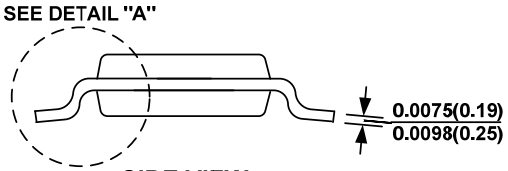
TOP VIEW



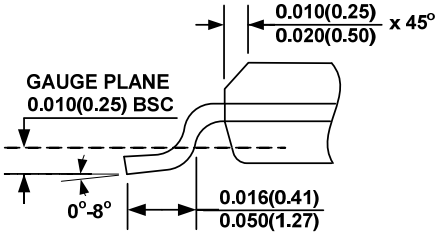
BOTTOM VIEW



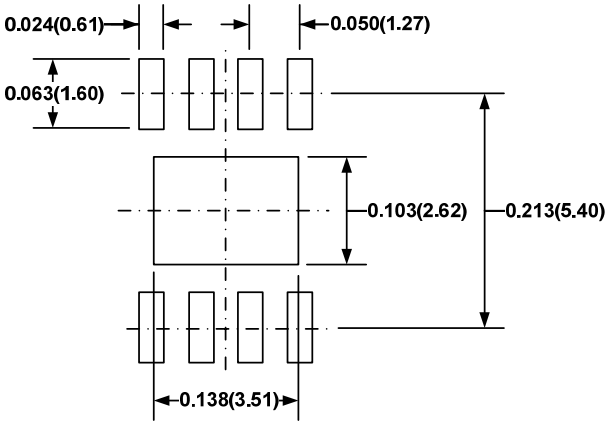
FRONT VIEW



SIDE VIEW



DETAIL "A"



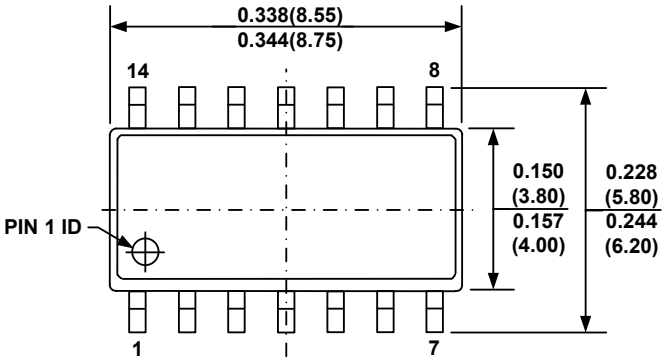
RECOMMENDED LAND PATTERN

NOTE:

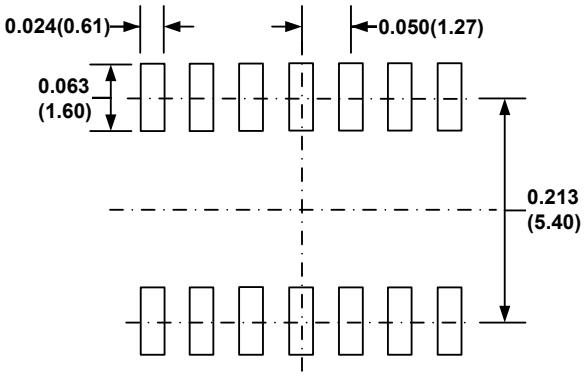
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.

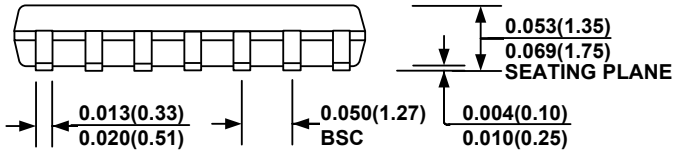
SOIC14



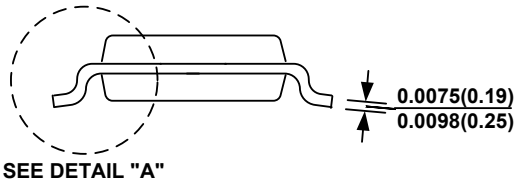
TOP VIEW



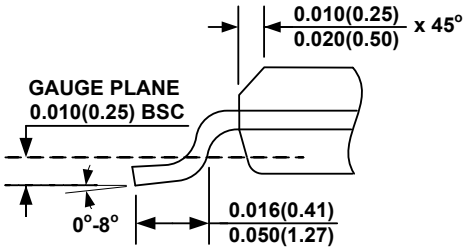
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2015 MPS. All Rights Reserved.