MP6654

18V, Single-Phase, ESD-Enhanced, BLDC Fan Driver with Integrated Hall Sensor

DESCRIPTION

The MP6654 is a single-phase brushless DC (BLDC) fan driver with integrated power MOSFETs and a Hall-effect sensor. It can achieve up to 1A of peak current (I_{PEAK}) across a wide 3V to 18V input voltage (V_{IN}) range.

The MP6654 controls the rotational speed through the pulse-width modulation (PWM) signal on the PWM pin. The device features a built-in, configurable curve speed function that is ideal for cooling fan applications, which require flexible speed curve control.

The MP6654 provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the internal Hall comparator's output. Higher speeds produce higher frequency signals.

Full protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO) protection, over-current protection (OCP), locked rotor protection, and thermal shutdown.

The MP6654 is available in TSOT23-6-SL and TSOT23-6-R packages.

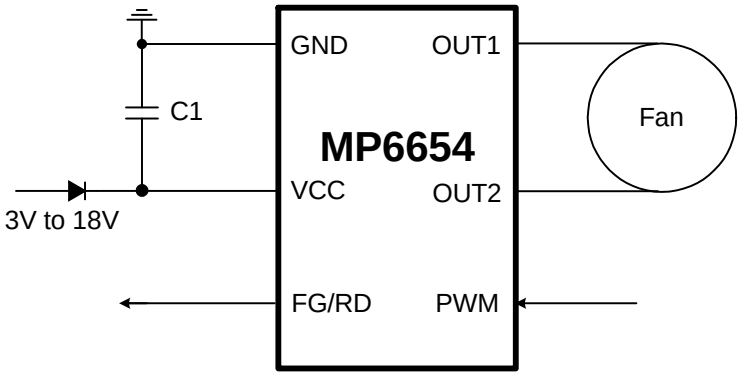
FEATURES

- On-Chip Hall Sensor
- Wide 3V to 18V Operating Input Voltage (V_{IN}) Range
- Up to 1A Peak Current (I_{PEAK})
- Integrated Power MOSFETs: Total 850mΩ High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET)
- Configurable Speed Curve
- Rotational Speed Indicator FG Signal
- Rotor Lock Protection Fault Indication
- 1kHz to 100kHz Pulse-Width Modulation (PWM) Input Frequency Range
- Configurable Soft On/Off Commutation
- 27kHz Fixed Output Switching Frequency (f_{SW})
- Configurable Soft Start (SS)
- Rotor Lock Protection with Auto-Recovery
- FG Outputs 0.5x, 1x, or 2x Original Hall Frequency
- Thermal Protection with Auto-Recovery Built-In Input Over-Voltage Protection (OVP) with Auto-Recovery
- Available in TSOT23-6-SL and TSOT23-6-R Packages

APPLICATIONS

- CPU Fans for Personal Computers or Servers
- Cooling Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Tape & Reel	Top Marking	MSL Rating
MP6654GJS-xxxx**	TSOT23-6-SL	Normal	*See Below*	1
MP6654GJR-xxxx**	TSOT23-6-R	Reverse	*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MP6654GJS-xxxx-Z).

** “xxxx” is the configuration code identifier. The four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code.

TOP MARKING (MP6654GJS-XXXX)

BUBY
LLL

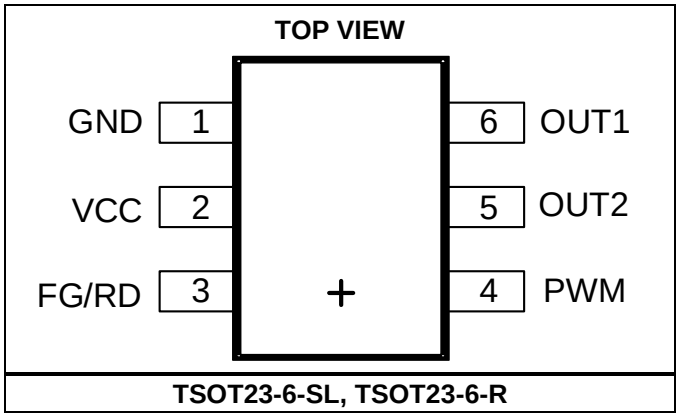
BUB: Product code
Y: Year code
LLL: Lot number

TOP MARKING (MP6654GJR-XXXX)

|BUBY

BUB: Product code
Y: Year code

PACKAGE REFERENCE



TSOT23-6-SL, TSOT23-6-R

PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input voltage supply.** The VCC pin must be bypassed locally.
3	FG/RD	**Rotational speed detection (default) or dead lock indication.** The FG and RD pins are open-drain outputs. Pull FG/RD high externally.
4	PWM	**PWM input for rotational speed control.** A 1kHz to 100kHz pulse-width modulation (PWM) input is recommended during normal operation.
5	OUT2	**Motor driver output 2.**
6	OUT1	**Motor driver output 1.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, $V_{FG/RD}$, V_{PWM} ..... -0.3V to +25V
V_{OUT1}, V_{OUT2}.....-0.3V to V_{CC} + 0.3V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = 25°C) (2)
..... 1.25W
Junction temperature ..... 150°C
Operating temperature..... -40°C to +125°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....750V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... 3V to 18V
Operating junction temp (T_J)…. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 100 ..... 55 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to 125°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			2.76		V
Input UVLO hysteresis				0.25		V
Operating supply current	I_{CC}			4		mA
Pulse-width modulation (PWM) input high voltage	V_{PWM_HIGH}		2			V
PWM input low voltage	V_{PWM_LOW}				0.4	V
PWM input internal pull-up resistance				100		kΩ
High-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) on resistance	$R_{(DS)ON}$	I_{OUT} = 100mA		0.85		Ω
Over-current protection (OCP) threshold	I_{OCP}			1		A
Input over-voltage protection (OVP) threshold	V_{OVP}		18	19.1	20.2	V
Input OVP hysteresis	V_{OVP_HYS}			1.3		V
Switching frequency	f_{SW}	T_J = 25°C	24.2	27	29.8	kHz
FG output low-level voltage	V_{FG_LOW}	$I_{FG/RD}$ = 3mA, V_{PULL} = 5V			0.35	V
Soft-on commutation angle	θ_{SON}	SON_ANG = 0x0F		46.8		deg
Soft-off commutation angle	θ_{SOFF}	SOFF_ANG = 0x0F		46.5		deg
Hall offset angle	θ_E	HAL_ANG = 0x07		22.5		deg
Rotor lock detection time (5)	t_{RD}			0.6		sec
Rotor lock off time (5)	t_{RD_OFF}	LOCK_SEL = 00		3.6		sec
Minimum recommended magnetic field			-1		+1	mT
Thermal shutdown threshold (5)				165		°C
Thermal shutdown hysteresis (5)				25		°C

Note:

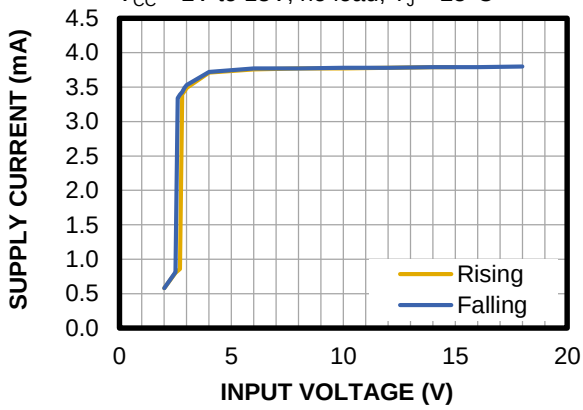
5) Guaranteed by design.

TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_A = -40°C to 125°C, unless otherwise noted.

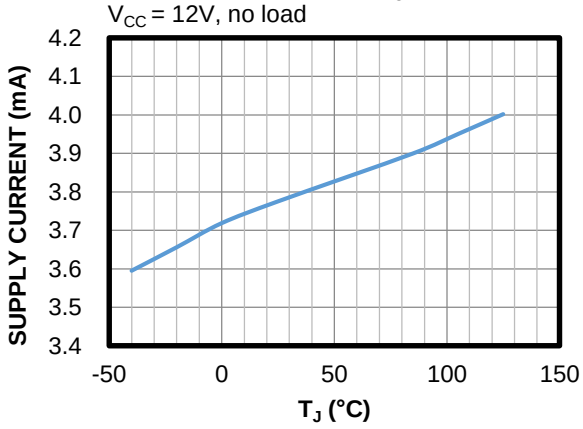
Supply Current vs. Input Voltage

V_{CC} = 2V to 18V, no load, T_J = 25°C

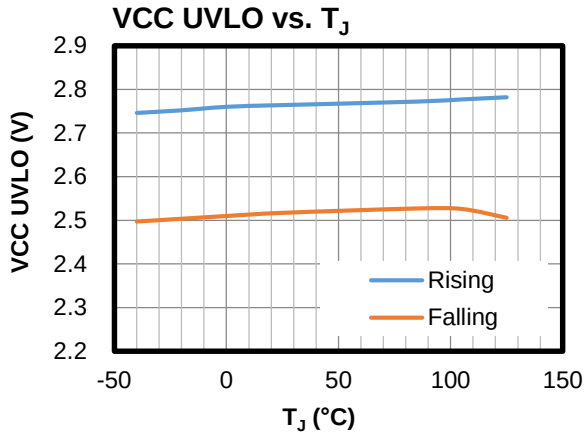


Supply Current vs. T_J

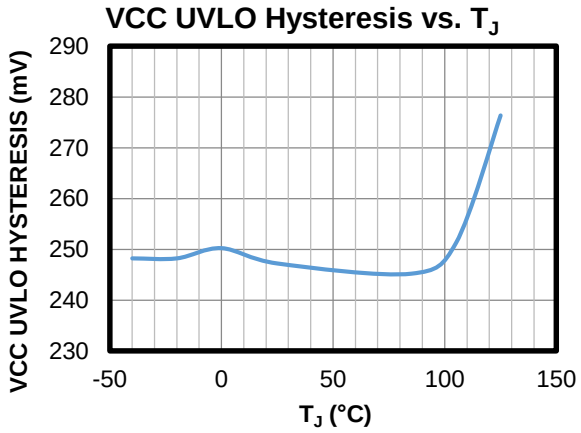
V_{CC} = 12V, no load



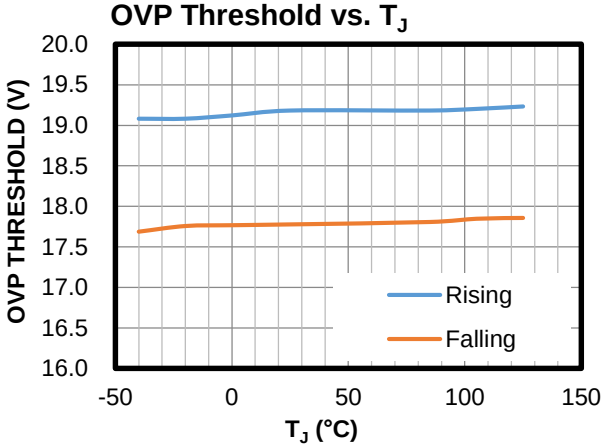
VCC UVLO vs. T_J



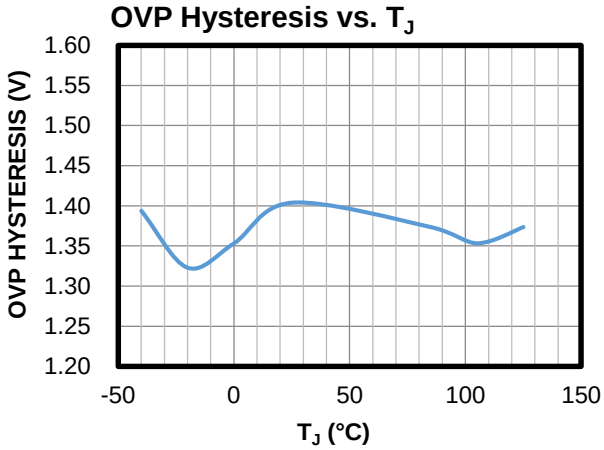
VCC UVLO Hysteresis vs. T_J



OVP Threshold vs. T_J



OVP Hysteresis vs. T_J

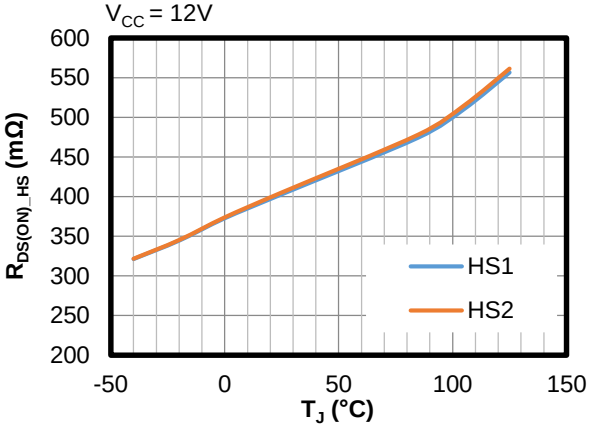


TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, T_A = -40°C to 125°C, unless otherwise noted.

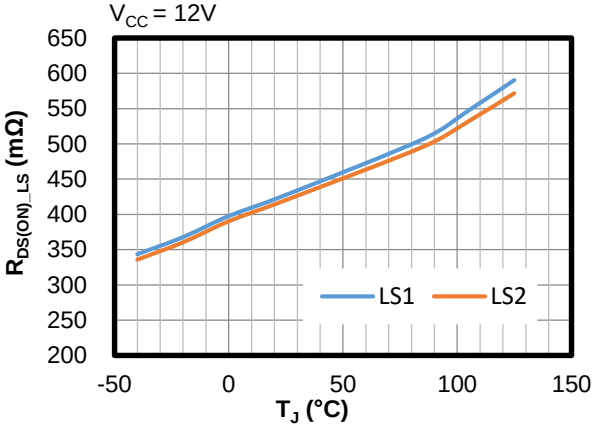
HS-FET On Resistance vs. T_J

V_{CC} = 12V



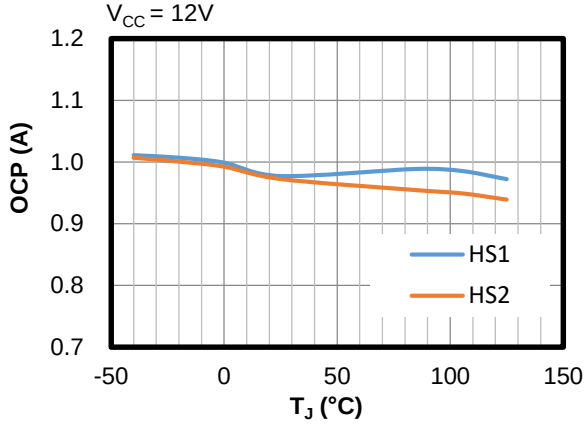
LS-FET On Resistance vs. T_J

V_{CC} = 12V



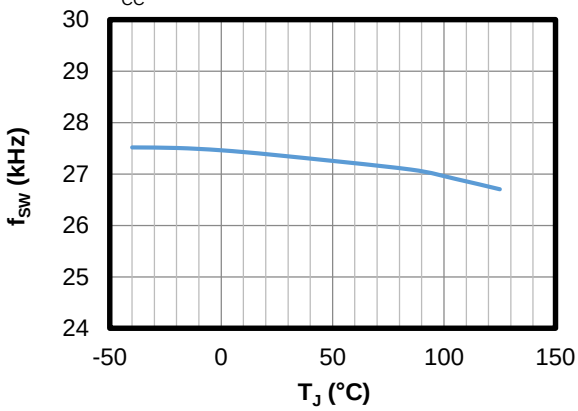
OCP vs. T_J

V_{CC} = 12V



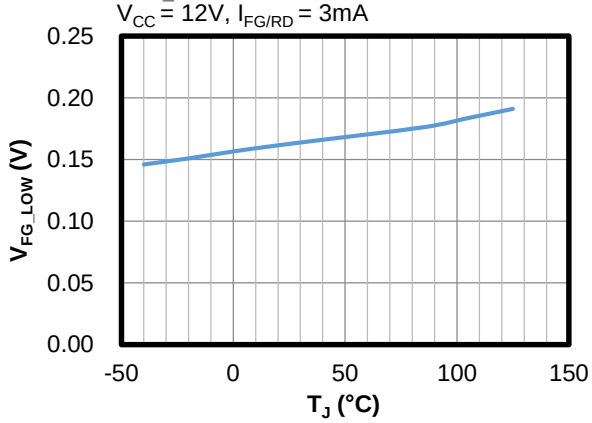
Switching Frequency vs. T_J

V_{CC} = 12V



V_{FG_LOW} vs. T_J

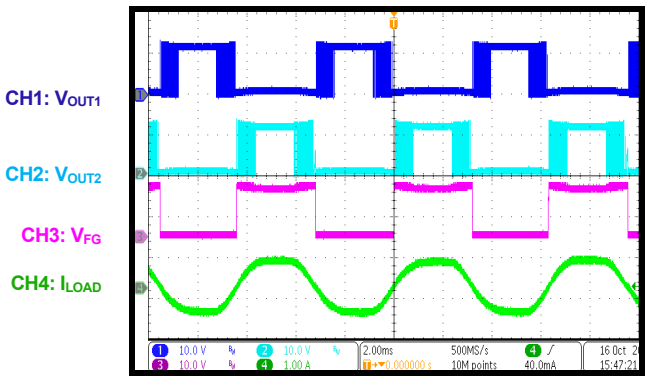
V_{CC} = 12V, $I_{FG/RD}$ = 3mA



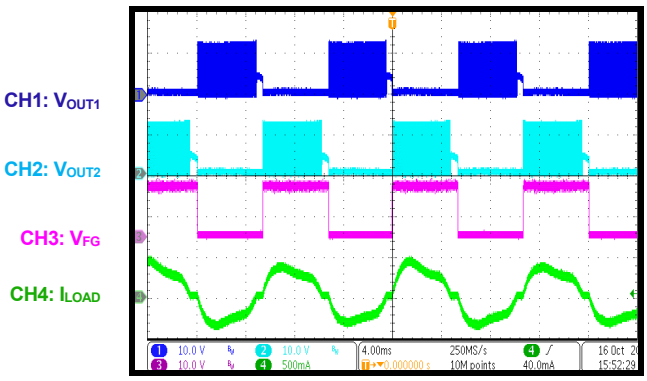
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 8025 axial fan, 450mA, 5000rpm, T_A = 25°C, unless otherwise noted.

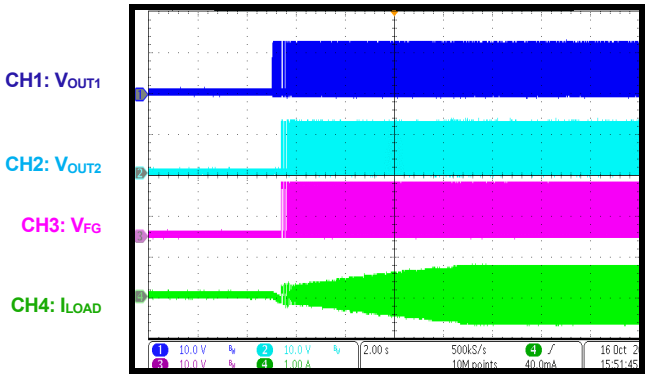
Steady State
PWM duty = 100%



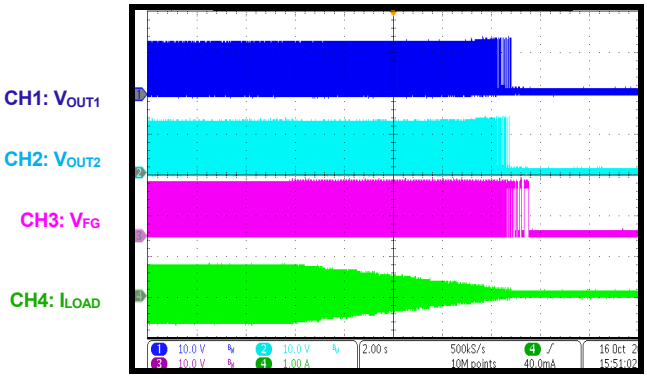
Steady State
PWM duty = 50%



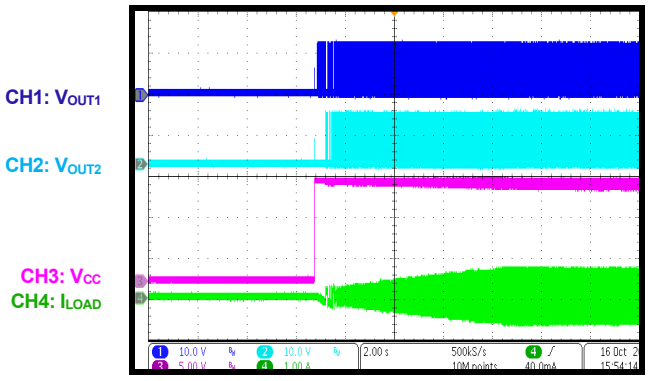
PWM On
PWM duty = 0% to 100%



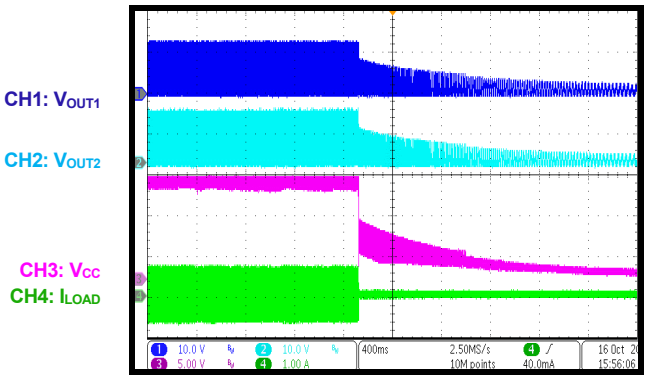
PWM Off
PWM duty = 100% to 0%



Start-Up through VCC
VCC power plugged in



Shutdown through VCC
VCC Power not plugged in

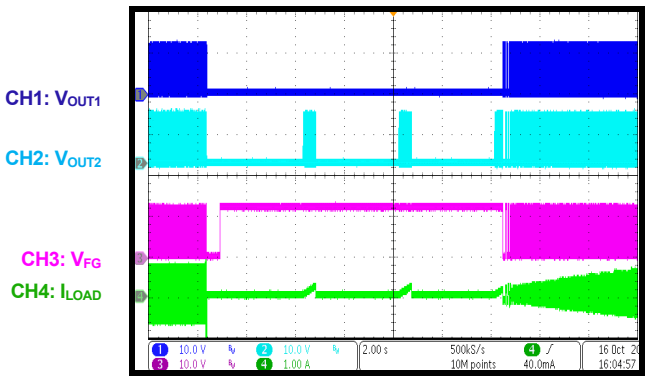


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 8025 axial fan, 450mA, 5000rpm, T_A = 25°C, unless otherwise noted.

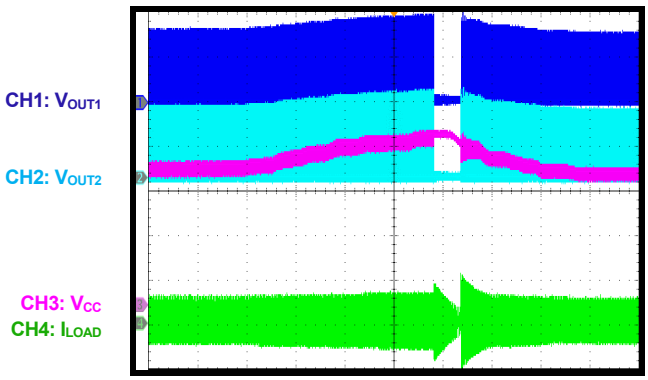
Locked Rotor Protection

Rotor is locked, then is released



Over-Voltage Protection

V_{CC} ramps up, then ramps down



FUNCTIONAL BLOCK DIAGRAM

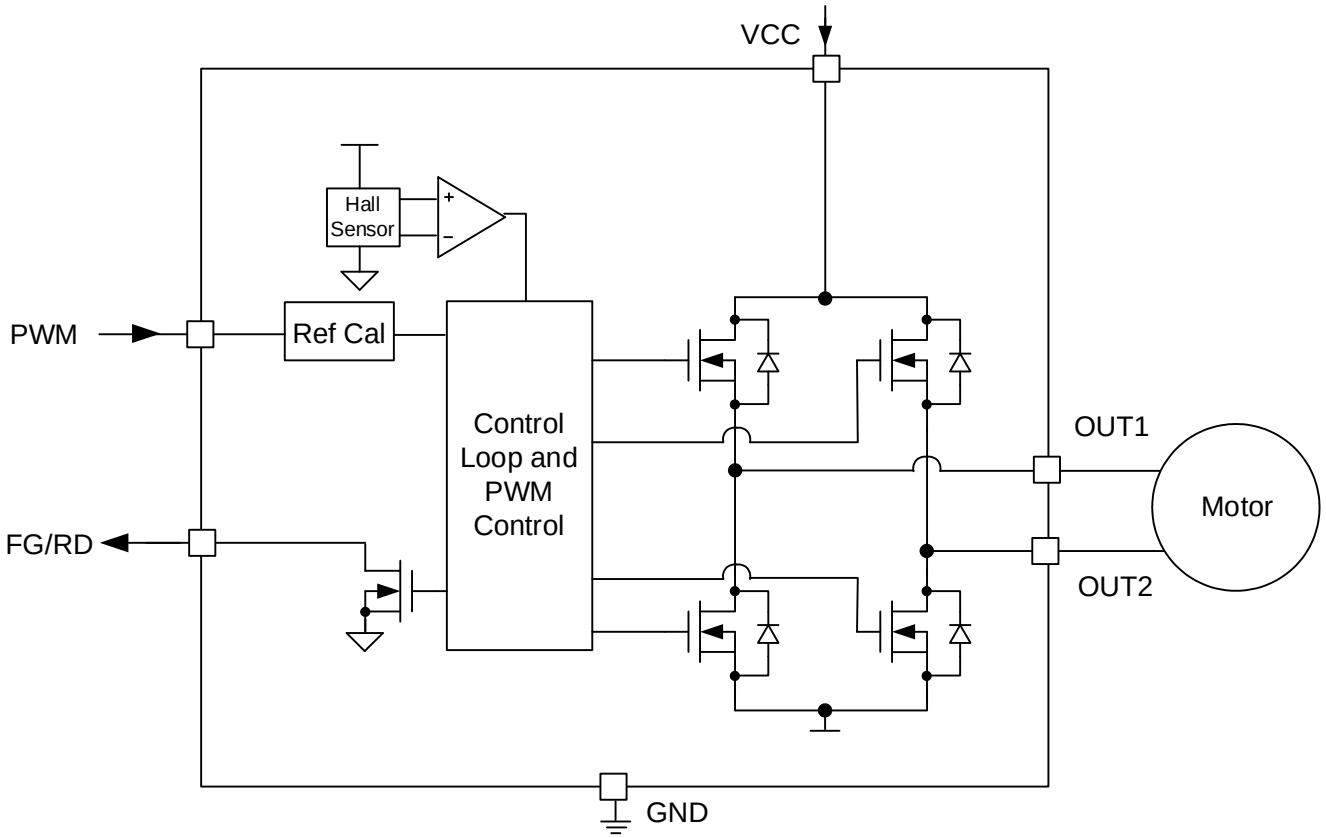


Figure 1: Functional Block Diagram

OPERATION

Speed Control

The PWM signal on the PWM pin accepts a wide input frequency range (1kHz to 100kHz). The device adjusts the motor speed by detecting the PWM signal duty cycle.

The OUT1 and OUT2 pins' output duty cycle follows the PWM input duty cycle. The DIN_MIN bits and hysteresis set the starting duty cycle. The minimum output duty is set by DOUT_MIN and SPD_ZERO, which supports two modes:

Mode 1: If SPD_ZERO = 1, then the device stops switching once the input duty cycle drops below the value set by DIN_MIN (see Figure 2).

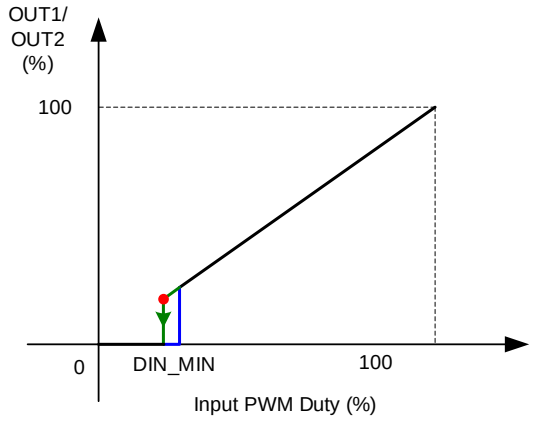


Figure 2: Speed Curve (SPD_ZERO = 1)

Mode 2: If SPD_ZERO = 0, then the minimum output duty cycle is limited by DOUT_MIN (see Figure 3).

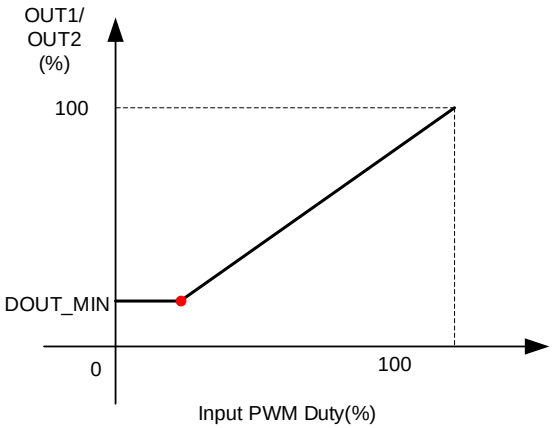


Figure 3: Speed Curve (SPD_ZERO = 0)

OUT1 and OUT2 Normal Operation

During normal operation, the MP6654 controls the H-bridge MOSFET switching according to the timing sequence.

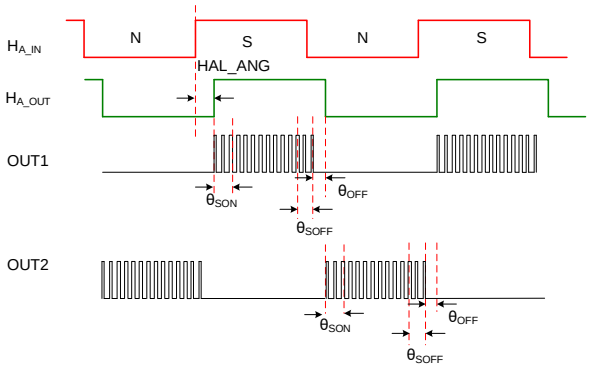


Figure 4: Hall Offset Angle and Soft Commutation

All operation sequences are based on the Hall signal coming from the embedded Hall sensor. H_{A_IN} is the original signal from the embedded Hall sensor, and H_{A_OUT} is generated based on H_{A_IN} with a phase shift. The phase shift is set by the HAL_ANG register. H_{A_OUT} is the control signal for phase commutation.

If the H_{A_OUT} signal is high, then OUT2 remains low while OUT1 switches. If the H_{A_OUT} signal is low, then OUT1 remains low while OUT2 switches.

- The phase shift between H_{A_IN} and H_{A_OUT} is set by the HAL_ANG bits.
- The phase shift leading/lag direction is set by the HAL_FLG bit.

Soft-On Commutation

During soft-on commutation, the switching phase's output duty cycle gradually increases from 0% duty cycle to the target duty cycle (see θ_{SON} in Figure 4).

The soft-on commutation angle is set by the SON_ANG register. The maximum soft-on commutation angle is 90°. The resolution is 2.8°.

Soft-Off Commutation

During soft-off commutation, the switching phase's output duty cycle gradually decreases from the steady duty cycle to 0% duty cycle (see θ_{SOFF} in Figure 4).

The soft-off commutation angle is set by the SOFF_ANG register. The maximum soft-off commutation angle is 90°. The resolution is 2.8°.

Curve Configuration

The MP6654 provides an 8-point curve configuration function (register 01H-08H), where the register sets the output duty cycle at 8 proportioned points from 12.5% through 100% (see Figure 5). With this 8-point register setting, the MP6654 can support flexible speed curves.

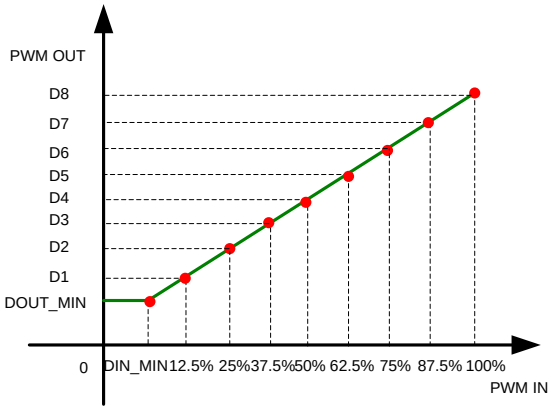


Figure 5: Curve Configuration

Soft-Start Time (t_{SS})

To reduce the input inrush current during the speed transition, the MP6654 provides a configurable soft-start time (t_{SS}) by setting T_SS (from 2.4s to 9.6s).

Rotor Speed Indication (FG)

The FG/RD pin is selectable for speed indication (FG) or rotor lock indication (RD), depending on FGRD.

- FGRD = 00: FG/RD is 1x original Hall
- FGRD = 01, FG/RD is 0.5x original Hall
- FGRD = 10, FG/RD is 2x original Hall
- FGRD = 11, FG/RD is set as the rotor lock indicator

Protection Behavior

The MP6654 is fully protected against over-voltage (OV), under-voltage (UV), over-current, and over-temperature (OT) events.

Short-Circuit Protection (SCP)

The MP6654 has an internal short-circuit protection (SCP) mode that detects the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the SCP threshold, then the MOSFET turns off after a set blanking time.

Over-Current Protection (OCP)

If the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the OCP threshold during normal operation, then the HS-FET turns off after a set blanking time. The HS-FET resumes switching in the next switching cycle.

Thermal Shutdown

Thermal monitoring is also integrated in the MP6654. If the die temperature exceeds the thermal shutdown threshold (typically 165°C), then over-temperature protection (OTP) is triggered, the output duty decreases. Once the die temperature drops below 140°C, the device resumes normal operation.

Under-Voltage Lockout (UVLO) Protection

If the VCC voltage (V_{CC}) drops below the under-voltage lockout (UVLO) threshold, then the device circuitry is disabled and the internal logic is reset. The device resumes normal operation once V_{CC} exceeds the UVLO rising threshold.

Locked Rotor Protection (RD)

The MP6654 features locked rotor protection. In locked rotor protection, the MP6654 detects the internal Hall signal and outputs a dead lock indication signal to the FG/RD pin. Set the FGRD bit to 11 to set the FG/RD for locked rotor protection indication. If the internal Hall signal edge is not detected during the detection time (0.6s), then lock rotor protection is triggered and both low-side MOSFETs (LS-FETs) of the H-bridges turn on. The FG/RD outputs depend on RD_H_L. The device automatically restarts after the lock retry time, which is set by the LOCK_SEL register. Once the locked rotor condition is released and three Hall signal edges are detected, FG/RD releases.

Over-Voltage Protection (OVP)

If V_{CC} exceeds the over-voltage protection (OVP) threshold (19V), then the device turns off the H-bridge MOSFETs. Once V_{CC} drops below 18V, then the device resumes normal operation.

Online Design Mode

To program the internal registers, the MP6654 has an online design mode. In online design mode, the internal registers can be read and written. After the design is finalized, the register value can be configured to the non-volatile memory. Refer to the MPS Phase Fan Driver GUI software for more details on easy parameter changes and memory configuration.

REGISTER MAP

Address	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00 (OTP/REG)	DOUT_MIN[7:0]							
0x01 (OTP/REG)	D1[7:0]							
0x02 (OTP/REG)	D2[7:0]							
0x03 (OTP/REG)	D3[7:0]							
0x04 (OTP/REG)	D4[7:0]							
0x05 (OTP/REG)	D5 [7:0]							
0x06 (OTP/REG)	D6[7:0]							
0x07 (OTP/REG)	D7[7:0]							
0x08 (OTP/REG)	D8[7:0]							
0x09 (OTP/REG)	RESERVED	DIN_MIN[6:0]						
0x0A (OTP/REG)	RESERVED	SPD_SEL[1:0]		SON_ANG[4:0]				
0x0B (OTP/REG)	RESERVED	TPRE[1:0]		SOFF_ANG[4:0]				
0x0C (OTP/REG)	LOCK_DIS	RESERVED	RD_HL	HAL_FLAG	HAL_ANG[3:0]			
0x0D (OTP/REG)	LOCK_SEL[1:0]		OCP_SEL[1:0]		RESERVED			TADV_EN
0x0E (OTP/REG)	ZCD_POS	TADV[1:0]		OVP	T_SS[1:0]		FGRD[1:0]	
0x0F (OTP/REG)	DUTY_ST[1:0]		SPD_ZERO	SCP_DIS	OCP_DIS	BRK_SLOW	DN_SCALE[1:0]	
0x14 (REG)	RESERVED		OTP_PAGE[1:0]		RESERVED			

Register: 0x00

Bits	Bit Name	Access	Default	Description
7:0	DOUT_MIN[7:0]	OTP/REG	0x20	Sets the minimum output duty cycle limit. Minimum output duty cycle = DOUT_MIN[7:0] / 256. The default is 12.5%. If SPD_ZERO = 1, then the device stops switching once the input PWM duty cycle drops below the duty cycle set by DIN_MIN. If SPD_ZERO = 0, then the device keeps the minimum output duty once the input PWM duty cycle drops below the duty cycle set by DIN_MIN.

Register: 0x01

Bits	Bit Name	Access	Default	Description
7:0	D1[7:0]	OTP/REG	0x20	Sets the output duty cycle when the input duty cycle = 12.5%. Output duty cycle = D1[7:0] / 256. The default is 12.5%.

Register: 0x02

Bits	Bit Name	Access	Default	Description
7:0	D2[7:0]	OTP/REG	0x40	Sets the output duty cycle when the input duty cycle = 25%. Output duty cycle = D2[7:0] / 256. The default is 25%.

Register: 0x03

Bits	Bit Name	Access	Default	Description
7:0	D3[7:0]	OTP/REG	0x60	Sets the output duty cycle when the input duty cycle = 37.5%. Output duty cycle = D3[7:0] / 256. The default is 37.5%.

Register: 0x04

Bits	Bit Name	Access	Default	Description
7:0	D4[7:0]	OTP/REG	0x80	Sets the output duty cycle when the input duty cycle = 50%. Output duty cycle = D4[7:0] / 256. The default is 50%.

Register: 0x05

Bits	Bit Name	Access	Default	Description
7:0	D5[7:0]	OTP/REG	0xA0	Sets the output duty cycle when the input duty cycle = 62.5%. Output duty cycle = D5[7:0] / 256. The default is 62.5%.

Register: 0x06

Bits	Bit Name	Access	Default	Description
7:0	D6[7:0]	OTP/REG	0xC0	Sets the output duty cycle when the input duty cycle = 75%. Output duty cycle = D6[7:0] / 256. The default is 75%.

Register: 0x07

Bits	Bit Name	Access	Default	Description
7:0	D7[7:0]	OTP/REG	0xE0	Sets the output duty cycle when the input duty cycle = 87.5%. Output duty cycle = D7[7:0] / 256. The default is 87.5%.

Register: 0x08

Bits	Bit Name	Access	Default	Description
7:0	D8[7:0]	OTP/REG	0xFF	Sets the output duty cycle when the input duty cycle = 100%. Output duty cycle = D8[7:0] / 256. The default is 100%.

Register: 0x09

Bits	Bit Name	Access	Default	Description
7	RESERVED	N/A	0	Reserved.
6:0	DIN_MIN[6:0]	OTP/REG	0x20	Sets the starting duty cycle. Starting duty cycle = DIN_MIN[6:0] / 256. The default is 12.5%.

Register: 0x0A

Bits	Bit Name	Access	Default	Description
7	RESERVED	N/A	0	Reserved.
6:5	SPD_SEL[1:0]	OTP/REG	01	Selects the digital clock. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed. These bits indicate the supported minimum speeds. 00: 100 RPM 01: 400 RPM (default) 10: 800 RPM 11: 1600 RPM
4:0	SON_ANG[4:0]	OTP/REG	10000	Sets the soft-on commutation angle. 00000: 2.8° 00001: 5.6° …. 11111: 90° Soft-on angle = (SON_ANG[4:0]+1) x 2.8°. 2.8° per step.

Register: 0x0B

Bits	Bit Name	Access	Default	Description
7	RESERVED	N/A	0	Reserved.
6:5	T_PRE[1:0]	OTP/REG	00	Sets the pre start-up timer. 00: 18.6ms/step (default) 01: 9.3ms/step 10: 4.6ms/step 11: 2.3ms/step
4:0	SOFF_ANG[4:0]	OTP/REG	10000	Sets the soft-off commutation angle. 00000: 2.8° 00001: 5.6° … 11111: 90° Soft-off angle = (SOFF_ANG[4:0] + 1) x 2.8°. 2.8° per step.

Register: 0x0C

Bits	Bit Name	Access	Default	Description
7	LOCK_DIS	OTP/REG	0	Enables locked rotor protection. 0: Locked rotor protection is enabled (default) 1: Locked rotor protection is disabled.
6	RESERVED	N/A	1	Reserved.
5	RD_HL	OTP/REG	0	Selects the RD output polarity bit when locked rotor protection is triggered. 0: Low output when locked rotor protection is triggered (default) 1: High output when locked rotor protection is triggered
4	HAL_FLAG	OTP/REG	0	Sets the Hall offset angle lag/lead. 0: Lag (default) 1: Lead
3:0	HAL_ANG[3:0]	OTP/REG	0000	Sets the Hall offset angle. 0000: 2.8° (default) 0001: 5.6° … 1111: 45° Hall offset angle = (HAL_ANG[3:0] + 1) x 2.8°. 2.8° per step.

Register: 0x0D

Bits	Bit Name	Access	Default	Description
7:6	LOCK_SEL[1:0]	OTP/REG	00	Selects the lock protection retry time. 00: 3.6s (default) 01: 4.8s 10: 6s 11: 8.5s
5:4	OCP_SEL[1:0]	OTP/REG	11	Selects the current limit threshold. 00: 0.35A 01: 0.5A 10: 0.75A 11: 1A (default)
3:1	RESERVED	N/A	011	Reserved.
0	TADV_EN	OTP/REG	1	Enables the advanced off time. 0: Disabled 1: Enabled (default)

Register: 0x0E

Bits	Bit Name	Access	Default	Description
7	ZCD_POS	OTP/REG	0	Selects the angle position zero-current detection (ZCD). 0: ZCD is active once soft-on commutation ends (default) 1: ZCD is active after 90°.
6:5	TADV[1:0]	OTP/REG	00	Sets the advanced off time. 00: Auto (default) 01: 5.6° 01: 11.2° 11: 22.5°
4	OVP	OTP/REG	0	OVP protection disable bit. 0: OVP protection is enabled (default); 1: OVP protection is disabled.
3:2	T_SS[1:0]	OTP/REG	00	Sets the soft transition time. This is the time that it takes for the output duty to transition from 0 to 100%. 00: 2.4s (default) 01: 4.8s 10: 7.2s 11: 9.6s
1:0	FGRD[1:0]	OTP/REG	00	Selects the FG/RD pin output. 00: 1x (default) 01: 0.5x 10: 2x 11: RD

Register: 0x0F

Bits	Bit Name	Access	Default	Description
7:6	DUTY_ST[1:0]	OTP/REG	01	Sets the initial output duty at start-up. 00: Initial output duty is 0% 01: Initial output duty is 12.5% (default) 10: Initial output duty is 18.5% 11: Initial output duty is 25%
5	SPD_ZERO	OTP/REG	1	Enables zero speed. 0: Keeps the minimum output duty cycle if the input PWM duty cycle drops below DIN_MIN 1: Stops switching if the input PWM duty cycle drops below DIN_MIN (default)
4	SCP_DIS	OTP/REG	0	Enables short-circuit protection (SCP). 0: SCP is enabled (default) 1: SCP is disabled
3	OCP_DIS	OTP/REG	0	Enables over-current protection (OCP). 0: OCP is enabled (default) 1: OCP protection is disabled
2	BRK_SLOW	OTP/REG	0	Sets the threshold at which the fan speed drops below its speed threshold, then the IC initiates a PWM cycle immediately after start-up. 0: 800RPM (default) 1: 400 RPM
1:0	DN_SCALE[1:0]	OTP/REG	00	Sets the PWM output duty ramp-down scale as the output duty cycle drops from 100% to 0%. 00: 1 x T_SS (default) 01: 2 x T_SS 10: 3 x T_SS 11: 4 x T_SS

Register: 0x14

Bits	Bit Name	Access	Default	Description
7:6	RESERVED	N/A	00	Reserved.
5:4	OTP_PAGE[1:0]	REG	00	Sets the OTP page indicator (read-only). 00: No OTP page is configured 01: First OTP page is configured 10: Second OTP page is configured
3:0	RESERVED	N/A	0000	Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor near VCC, as close as possible to the VCC and GND pins, to keep the input voltage (V_{IN}) stable and to reduce V_{IN} noise. The input capacitor impedance should be low at the switching frequency (f_{SW}).

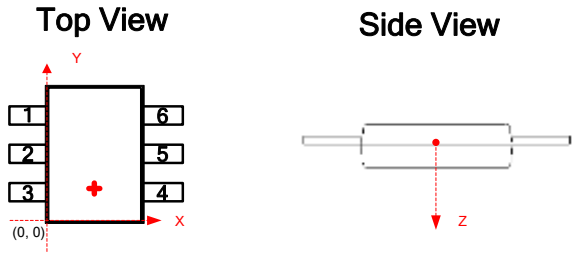
Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. The capacitance of the ceramic capacitor drops when the voltage across the capacitor rises; the ceramic capacitor can lose more than 50% of its capacitance when the voltage across the capacitor is close to its rated voltage.

Leave enough voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient.

For certain applications, it is recommended to use an additional, large electrolytic capacitor to absorb motor energy.

Hall Sensor Position

Figure 6 shows the Hall sensor position in the lower-left corner of the package (see Figure 6).



(X, Y, Z) = (800µm, 783µm, 80µm)

Figure 6: Hall Sensor Position

Selecting the Reverse Blocking Diode

To avoid damage if the fan experiences a reverse plug-in, a reverse blocking diode is required. The reverse blocking diode prevents the bus voltage (V_{BUS}) from charging via the fan's reverse current.

The blocking diode's maximum reverse voltage should exceed 30V, and its forward current rating should exceed the input current (I_{IN}).

System-Level ESD Enhancement

Some fan products must pass system-level ESD testing. Compared to the HBM ESD ratings, system-level ESD follows the IEC61000-4-2 standard. There are two different modes for the IEC61000-4-2 ESD test: air discharge and contact discharge. Contact discharge mode is the first choice for testing.

Figure 7 shows the equivalent circuit of a HBM ESD circuit.

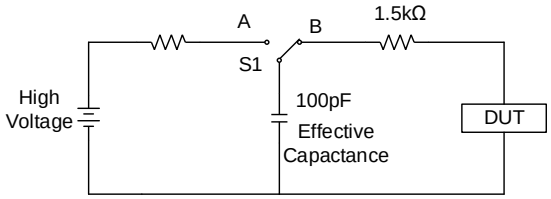


Figure 7: Equivalent Circuit of HBM ESD Circuit

Figure 8 shows that the IEC61000-4-2 sets the equivalent circuit.

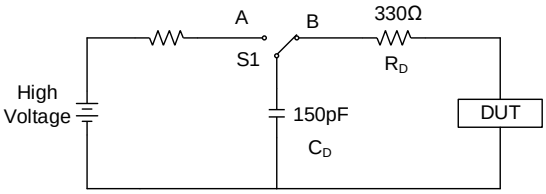


Figure 8: Equivalent Circuit of System-Level ESD

Compared to the HBM ESD ratings, the discharge capacitance exceeds the human body's effective capacitance, and the discharge resistor of the IEC level ESD is much smaller.

The MP6654 can pass IEC61000-4-2 4kV ESD testing without any additional components.

If a higher level is required, then an external circuit may be required to enhance the ESD capability (see Figure 9).

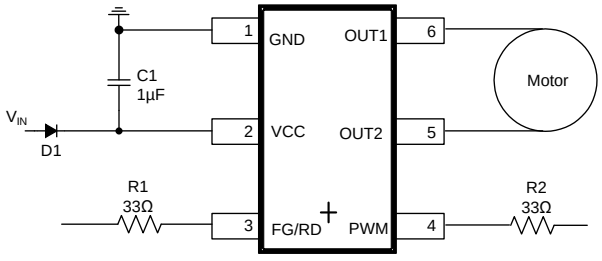


Figure 9: External ESD-Enhanced Circuit with a Resistor

An external Zener diode or ESD diode may be required for a higher system-level ESD requirement (e.g. above 10kV contact ESD).

Figure 10 shows an external ESD-enhanced circuit using a Zener/ESD diode.

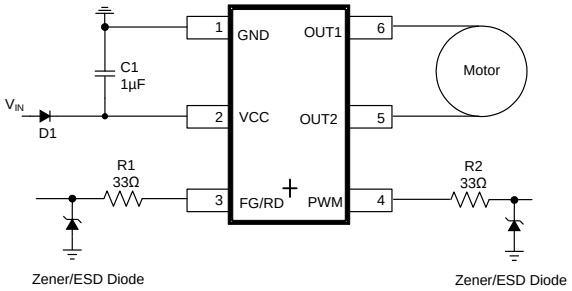


Figure 10: External ESD-Enhanced Circuit with a Zener/ESD Diode

Input Clamping Circuit

To avoid high voltage spikes caused by the energy stored in the motor, a voltage-clamping circuit may be required (especially for large current and fan inertial applications). A 15V/SOD-123 package TVS diode or Zener diode is sufficient for most 12V applications.

Input Snubber

Due to the input capacitor energy charge/discharge during phase commutation, I_{IN} has switching cycle ringing. If necessary, add a 2Ω resistor in series with a 1µF capacitor as an RC snubber in parallel with an input capacitor. This prevents switching cycle ringing.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 11 and follow the guidelines below:

1. Place the input capacitor as close to VCC and GND as possible.

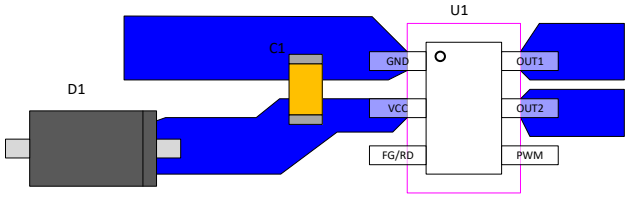


Figure 11: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

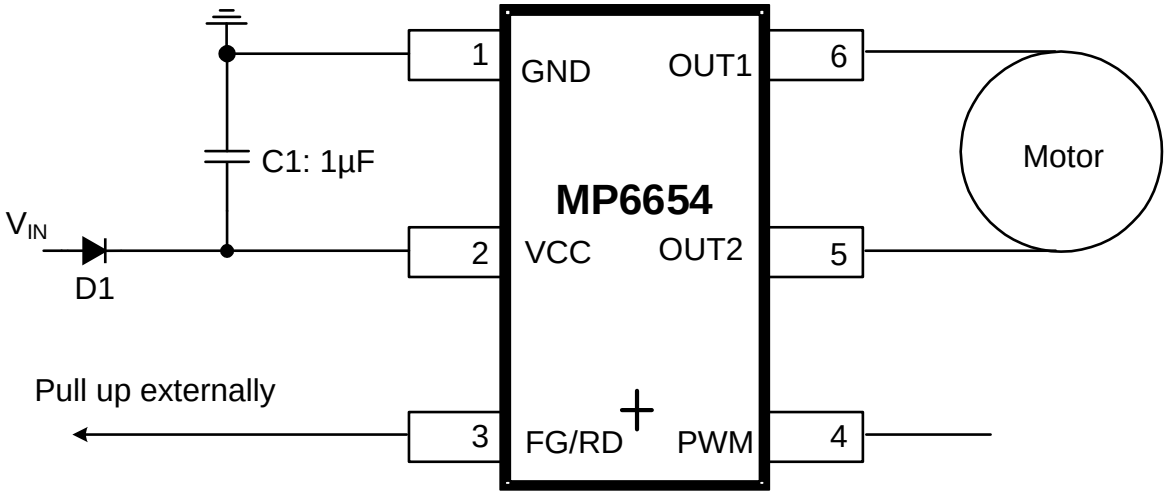


Figure 12: Typical Application Circuit for Normal Applications

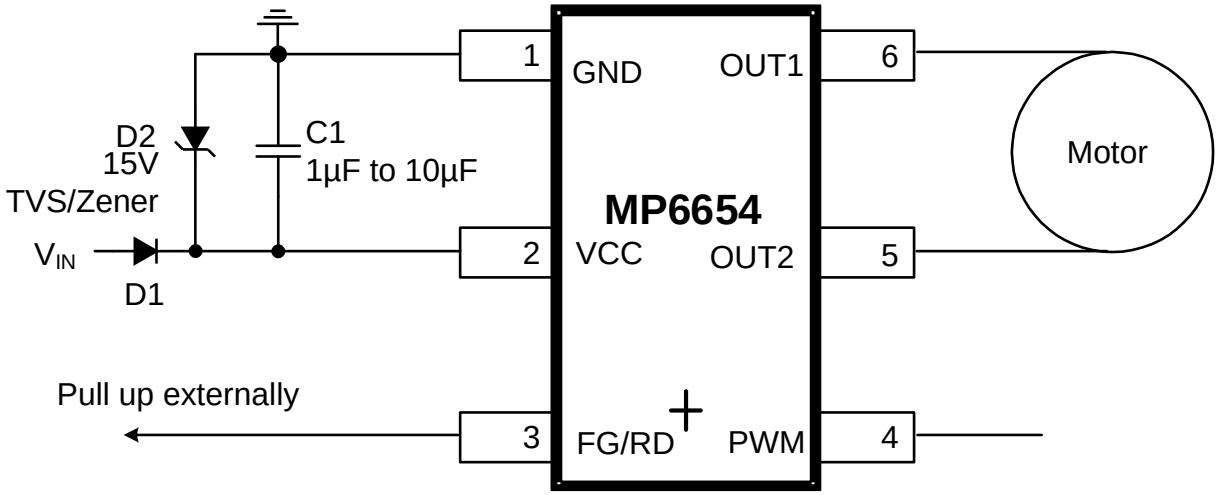
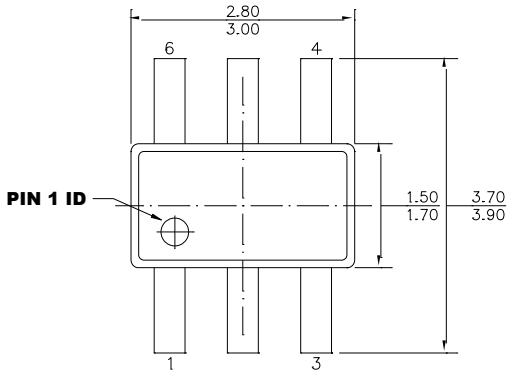


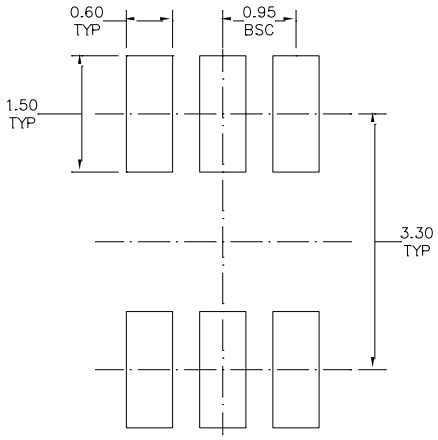
Figure 13: Typical Application Circuit for High-Current, Large-Inertia Fan Applications

PACKAGE INFORMATION

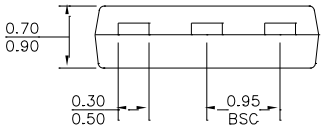
TSOT23-6-SL



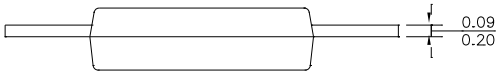
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



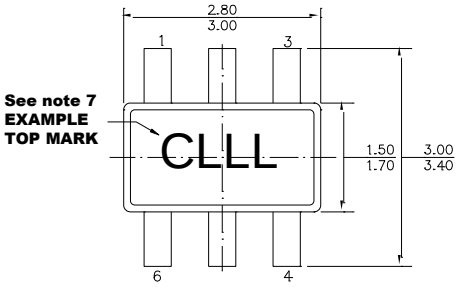
SIDE VIEW

NOTE:

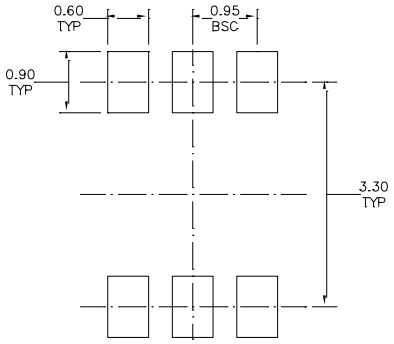
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193,
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

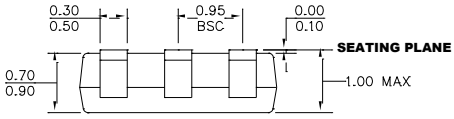
TSOT23-6-R



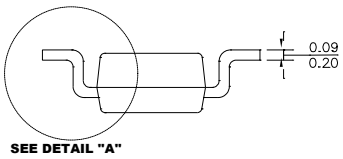
TOP VIEW



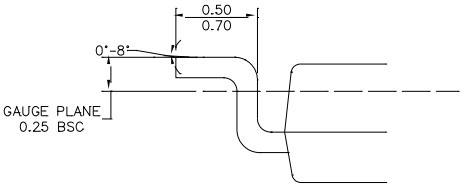
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



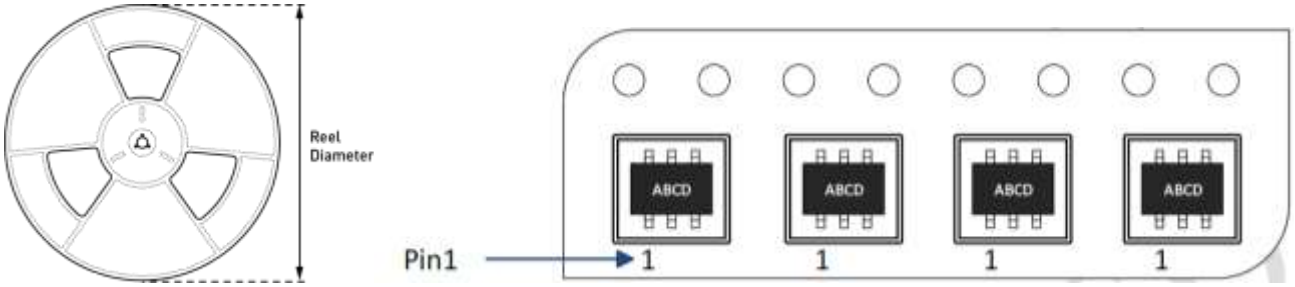
DETAIL "A"

NOTE:

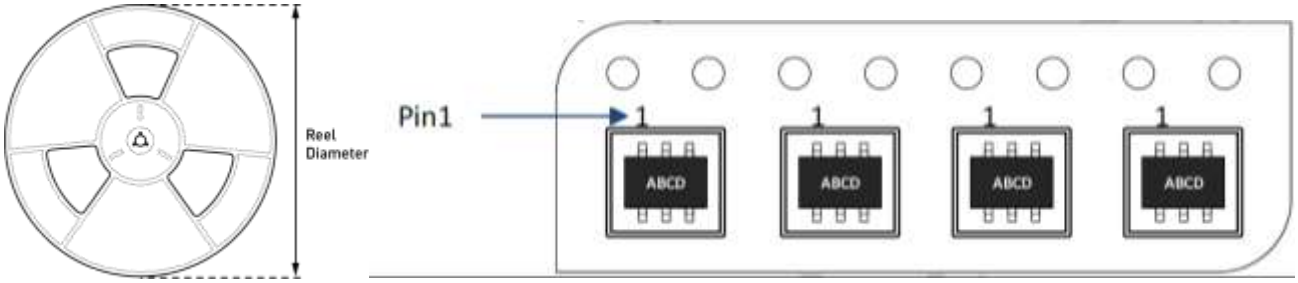
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE TO JEDEC MO-193.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS UPPER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION

TSOT23-6-SL



TSOT23-6-R



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6654GJS-xxxx-Z	TSOT23-6-SL	5000	N/A	13in	12mm	8mm
MP6654GJR-xxxx-Z	TSOT23-6-R	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/25/2022	Initial Release	-