



MP6637A

5.5V, 1.3A Peak, Three-Phase, Sensorless Sinusoidal BLDC Motor Driver with Integrated MOSFETs

DESCRIPTION

The MP6637A is a three-phase, sensorless, brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sinusoidal sensorless drive for better efficiency and low vibration, with up to 1.3A of peak phase current. The input voltage (V_{CC}) ranges from 2.5V to 5.5V.

The MP6637A controls the motor speed via a pulse-width modulation (PWM) signal with a 1kHz to 100kHz PWM input frequency.

The MP6637A features rotational speed detection. The FG/RD pin outputs a pulse signal, and the pulse signal's frequency indicates the fan speed.

Rich protection features include short-circuit protection (SCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

The MP6637A is available in an SOT583 package.

FEATURES

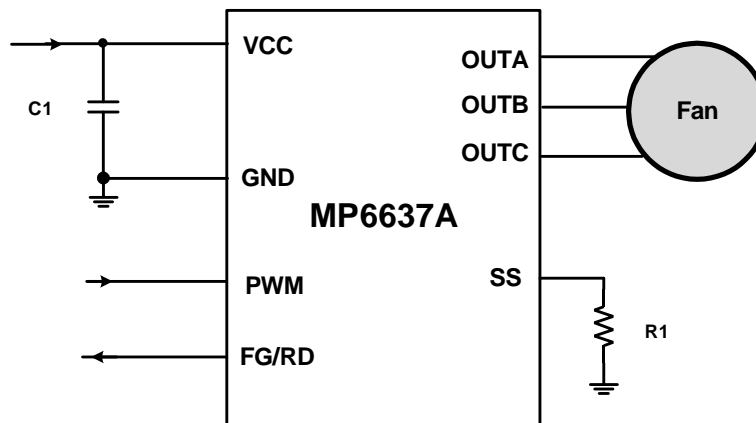
- 2.5V to 5.5V Input Voltage (V_{CC}) Operating Range
- Up to 1.3A of Peak Phase Current
- Up to 0.9A of RMS Phase Current
- Sinusoidal Sensorless Drive
- Integrated 350m Ω High-Side MOSFETs (HS FETs) and Low-Side MOSFETs (LS-FETs)
- Supports 1kHz to 100kHz Pulse-Width Modulation (PWM) Input
- Power-Save Mode
- 30kHz Switching Frequency (f_{sw})
- Current Limiting
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Under-Voltage Lockout (UVLO)
- Over-Current Protection (OCP)
- Locked-Rotor Protection
- Selectable FG or RD Output
- Available in an SOT583 Package

APPLICATIONS

- Notebook Fans
- Gaming Fans
- General Three-Phase Fans

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6637AGTL-xxxx**	SOT583	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MP6637AGTL-xxxx-Z).

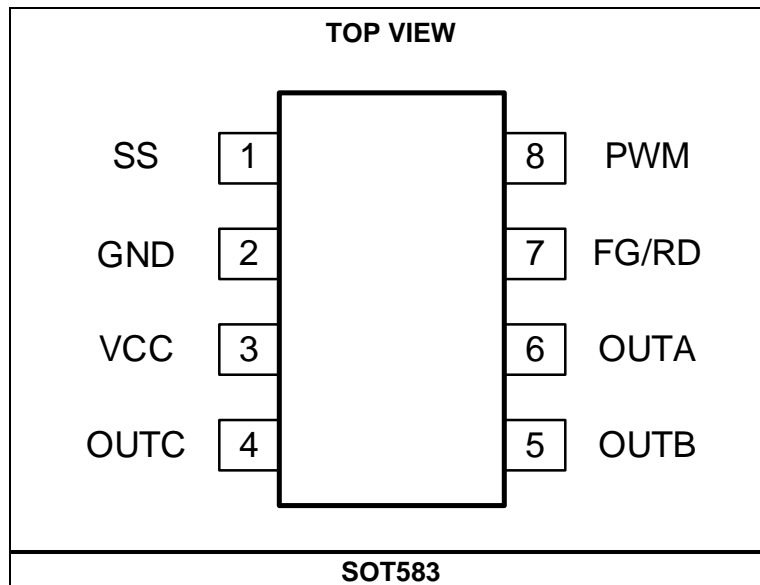
** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for non-default function options. The default code is “0000”.

TOP MARKING

CEJY
LLL

CEJ: Product code
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	SS	Soft-start setting pin. Connect a resistor to select the soft start (SS) parameters to meet different loads.
2	GND	Ground.
3	VCC	Input supply voltage. The VCC pin requires a bypass capacitor. Place the bypass capacitor as close to the VCC and GND pins as possible.
4	OUTC	Phase C terminal.
5	OUTB	Phase B terminal.
6	OUTA	Phase A terminal.
7	FG/RD	Speed (FG) or locked-rotor (RD) indication. The FG/RD pin is an open-drain output, and must be pulled up externally.
8	PWM	Speed control input pin. Apply a pulse-width modulation (PWM) signal to the PWM pin. The PWM signal's duty cycle controls the motor speed. The PWM frequency (f_{PWM}) is 1kHz to 100kHz.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

All pins	-0.3V to +6.5V
Lead temperature	260°C
Continuous power dissipation ($T_A = 25^\circ\text{C}$) ⁽²⁾	0.96W
Junction temperature (T_J)	150°C
Input supply voltage (V_{CC}).....	2.5V to 5.5V
Operating temperature.....	-40°C to +125°C

ESD Ratings

Human body model (HBM)	4kV
Charged-device model (CDM)	2kV

Recommended Operating Conditions ⁽³⁾

Input supply voltage (V_{CC}).....	2.5V to 5.5V
Operating junction temp (T_J)....	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
SOT583	130	60... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

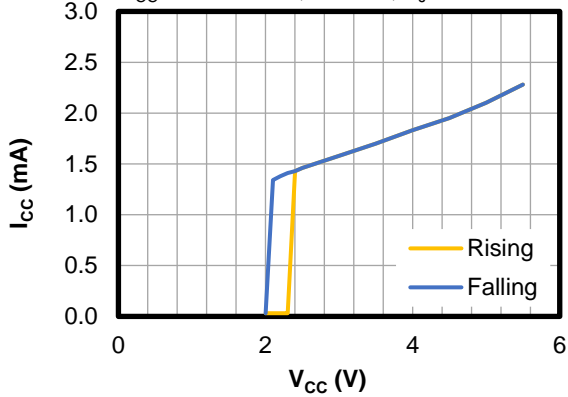
Parameters	Symbol	Condition	Min	Typ	Max	Units
Input voltage (V_{CC}) under-voltage lockout (UVLO) rising threshold	V_{CC_UVLO}			2.3	2.4	V
V_{CC} UVLO with hysteresis				0.23		V
Operating input supply current	I_{CC}	No load		2.1		mA
Standby current	I_{ST}	PWM low		45	70	μA
Pulse-width modulation (PWM) input high voltage	V_{PWM_H}		2			V
PWM input low voltage	V_{PWM_L}				0.8	V
PWM input internal pull-up resistance				40		k Ω
Soft start (SS) output current	I_{SS}			50		μA
Switching frequency	f_{SW}	$T_J = 25^{\circ}C$	29.1	30	30.9	kHz
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	$I_{OUT} = 100mA$		200		m Ω
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	$I_{OUT} = 100mA$		150		m Ω
Over-current (OC) limit protection threshold	I_{OCP}			1.3		A
Short-circuit protection (SCP) threshold	I_{SCP}			1.9		A
FG/RD output low-level voltage	V_{FG_L}	$I_{FG/RD} = 3mA$			0.2	V
Locked-rotor off time	t_{RE}			4.4		sec
Input over-voltage protection (OVP) threshold	V_{OVP}			5.8		V
OVP hysteresis	V_{OVP_HYS}			0.44		V
Thermal shutdown threshold				150		$^{\circ}C$
Thermal shutdown hysteresis				20		$^{\circ}C$

TYPICAL CHARACTERISTICS

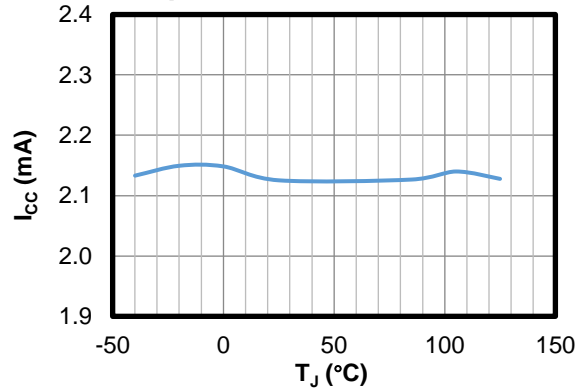
$V_{CC} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.

Supply Current vs. Input Supply Voltage

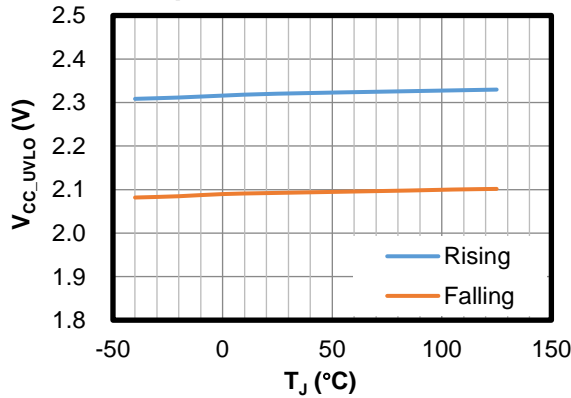
$V_{CC} = 2V$ to $5.5V$, no load, $T_J = 25^{\circ}C$



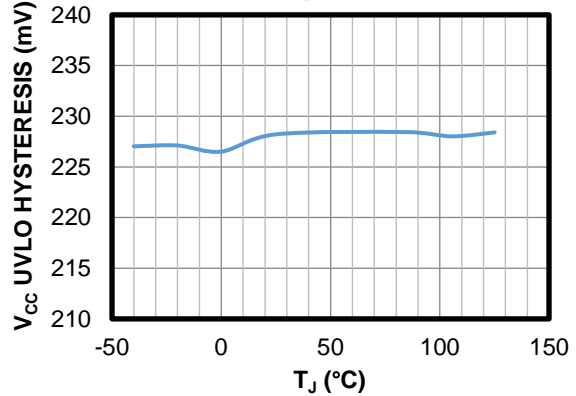
Supply Current vs. Junction Temperature



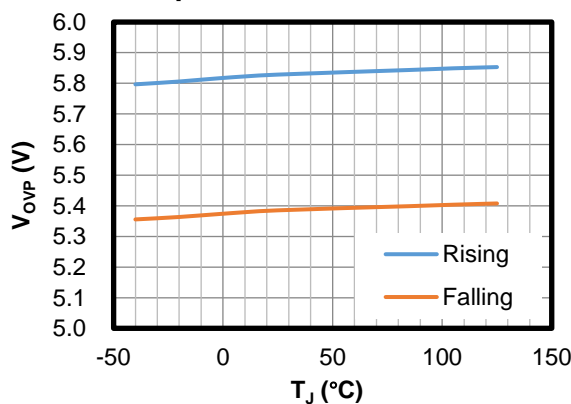
V_{CC} UVLO vs. Junction Temperature



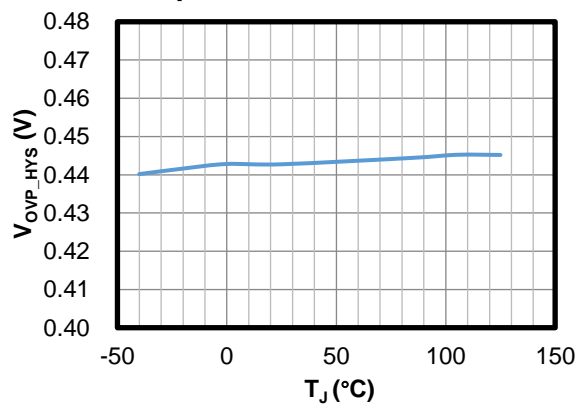
V_{CC} UVLO Hysteresis vs. Junction Temperature

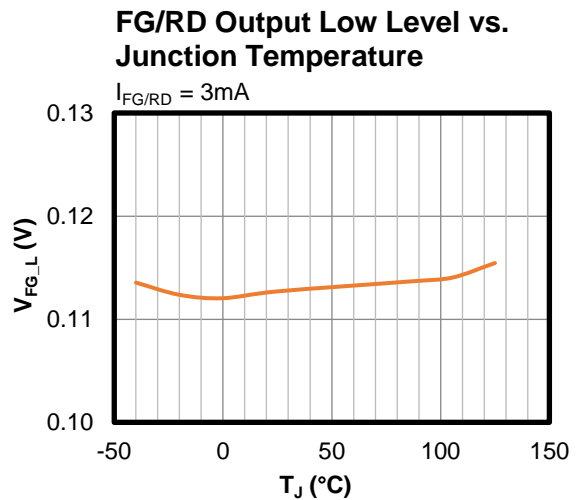
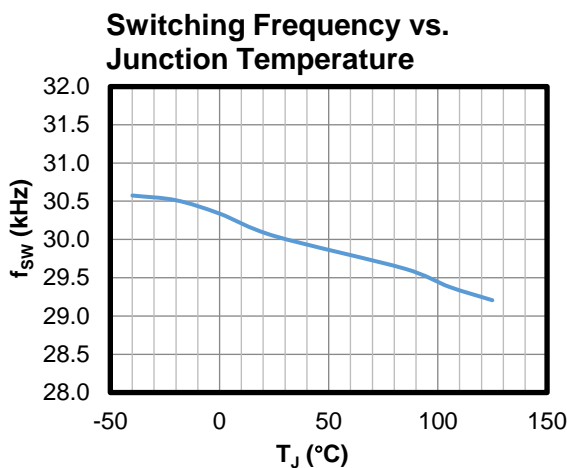
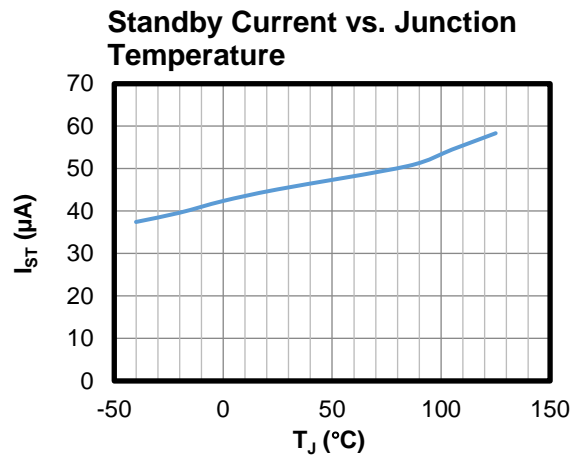
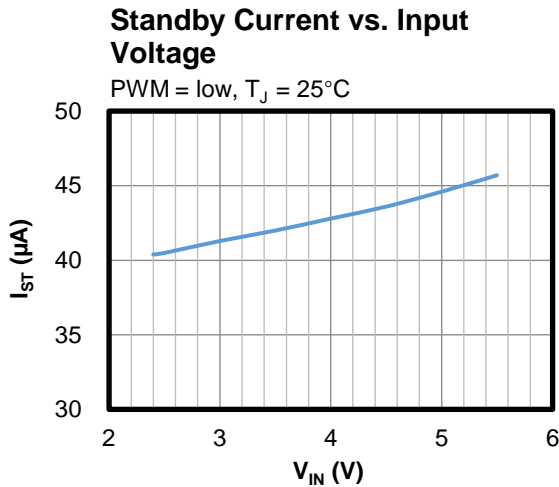
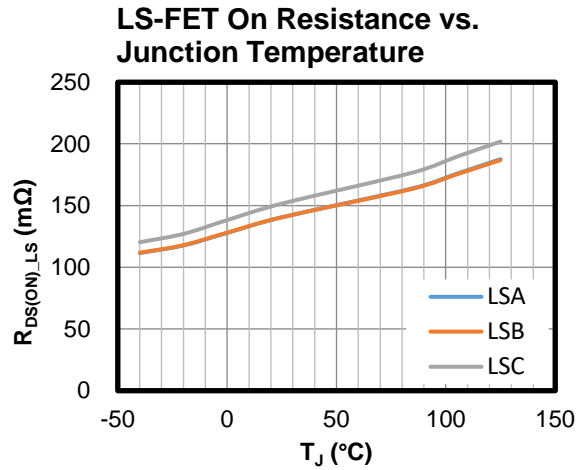
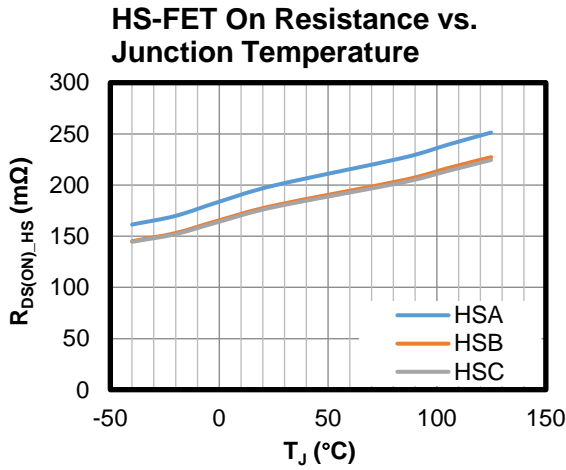


OVP Threshold vs. Junction Temperature



OVP Hysteresis vs. Junction Temperature



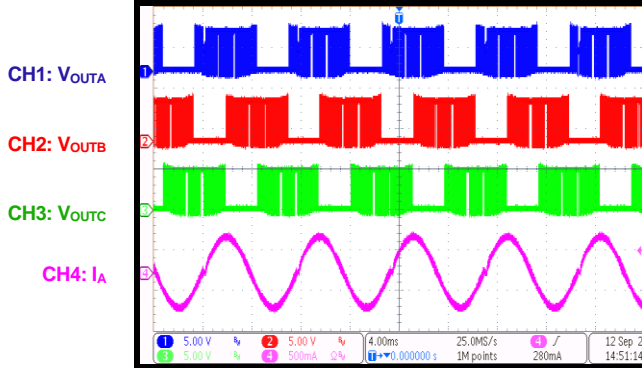
TYPICAL CHARACTERISTICS (continued)
 $V_{CC} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. SS pin floating, $V_{CC} = 5V$, $f_{PWM} = 20kHz$, $T_A = 25^{\circ}C$, unless otherwise noted.

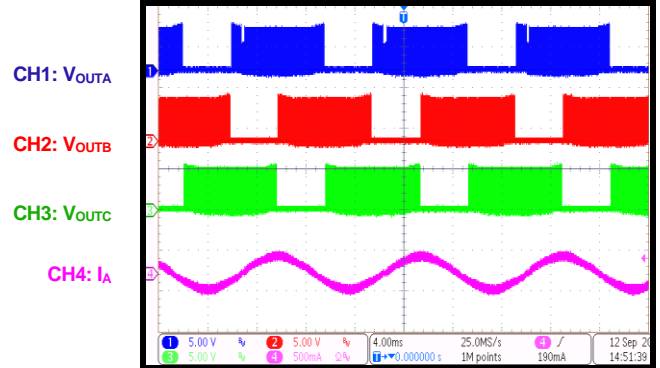
Steady State

Input PWM duty cycle = 100%



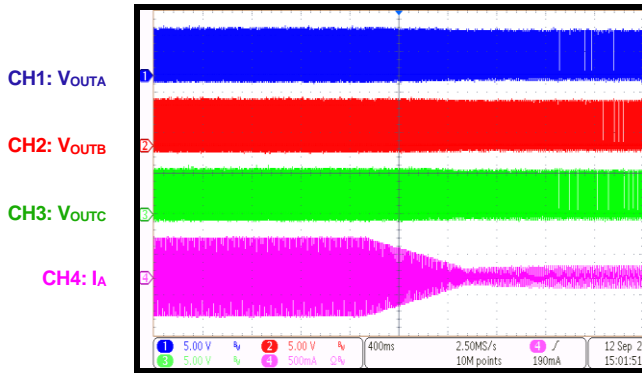
Steady State

Input PWM duty cycle = 50%



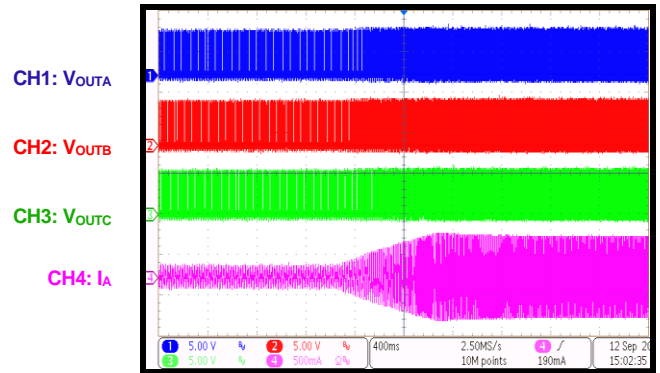
PWM Duty Transient Response

Input PWM duty cycle = 100% to 25%



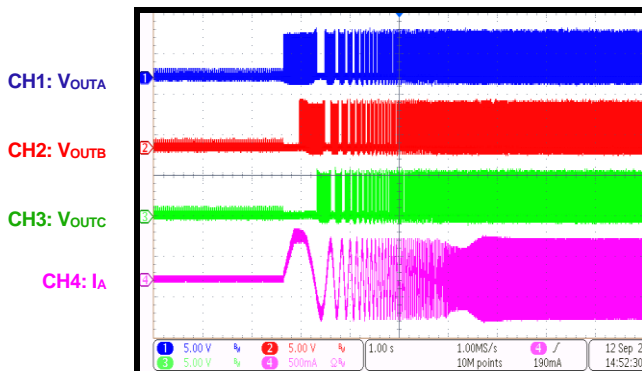
PWM Duty Transient Response

Input PWM duty cycle = 25% to 100%



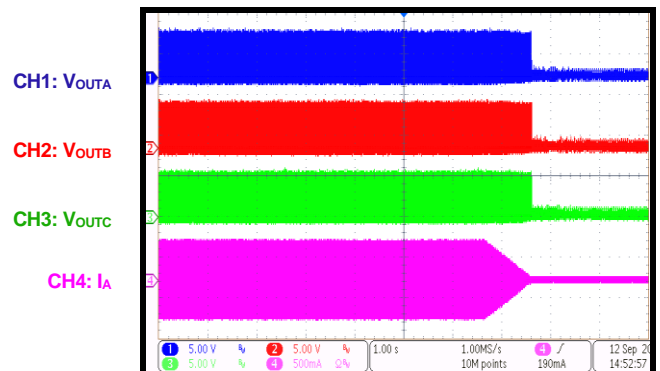
PWM On

Input PWM duty cycle = 1% to 100%



PWM Off

Input PWM duty cycle = 100% to 1%

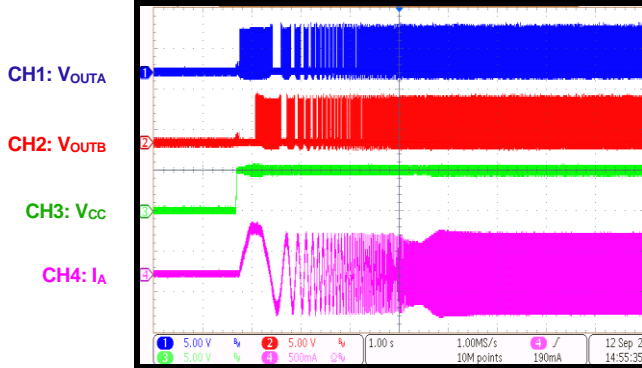


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. SS pin floating, $V_{CC} = 5V$, $f_{PWM} = 20kHz$, $T_A = 25^{\circ}C$, unless otherwise noted.

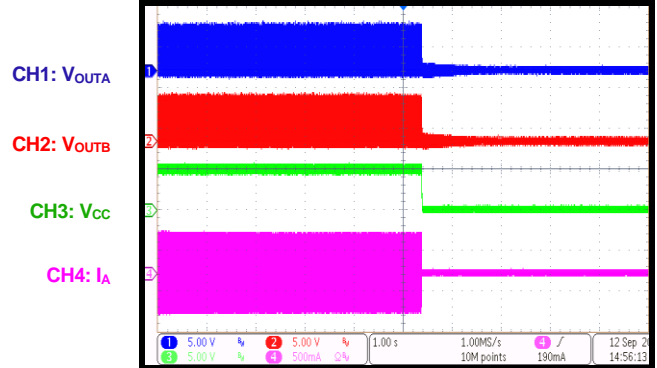
Start-Up

$V_{CC} = 0V$ to $5V$



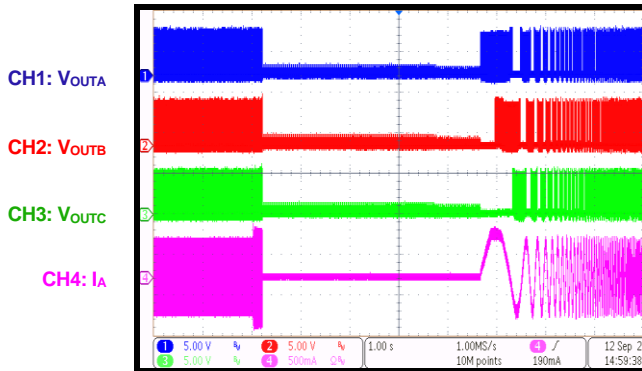
Shutdown

$V_{CC} = 5V$ to $0V$



Rotor Lock and Retry

Lock rotor then release



FUNCTIONAL BLOCK DIAGRAM

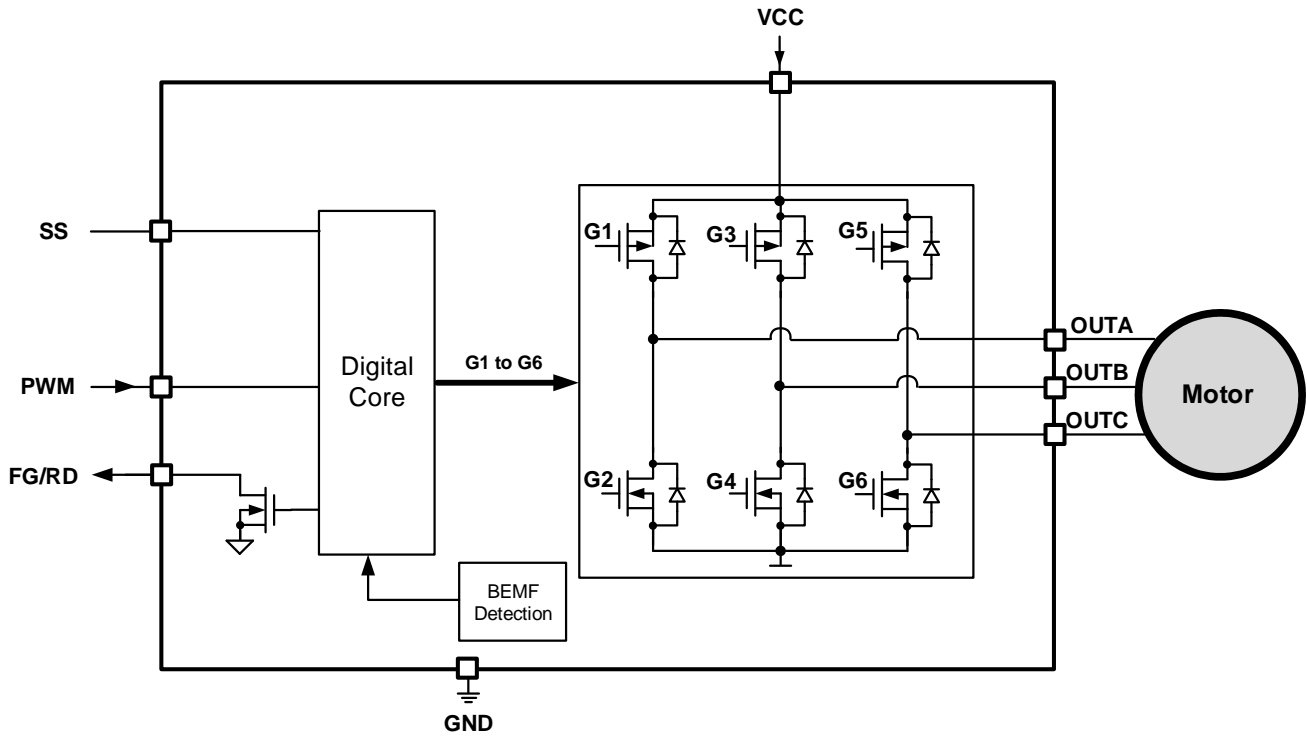


Figure 1: Functional Block Diagram

OPERATION

The MP6637A is a three-phase, sensorless, brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sinusoidal sensorless control for better efficiency and low vibration, with up to 1.3A of peak phase current. The input voltage (V_{CC}) ranges from 2.5V to 5.5V.

Speed Control

The PWM pin controls the speed via an input pulse-width-modulation (PWM) signal. The input PWM signal ranges from 1kHz to 100kHz. The input duty cycle determines the motor speed.

Starting Duty Cycle

The starting duty cycle can be configured via `CURVE_WINDOW_PWM_DUTY` (01h), bits[2:0]. When `SPD_ZERO = 1`, if the input PWM duty cycle is lower than the duty cycle set by these bits, the MP6637A stops switching. If the input PWM duty cycle exceeds `DIN_MIN + 1.2%` (hysteresis), the MP6637A starts the output duty cycle and the motor starts rotating (see Figure 2). The default starting duty cycle is 12.5%.

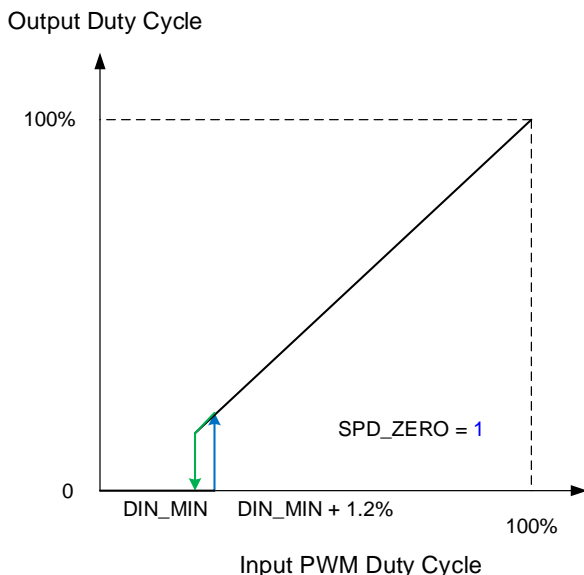


Figure 2: Starting Duty when `SPD_ZERO = 1`

When `SPD_ZERO = 0`, the MP6637A maintains the minimum speed when the input PWM duty cycle falls below the duty cycle set via `CURVE_WINDOW_PWM_DUTY` (01h), bits[2:0] (see Figure 3).

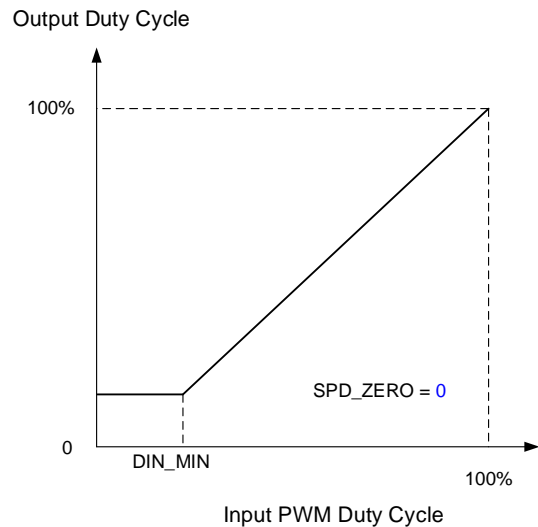


Figure 3: Minimum Speed when `SPD_ZERO = 0`

Open-Loop Acceleration Start-Up

After V_{CC} powers up, the MP6637A increases the driven vector's frequency to openly accelerate the motor. The acceleration slew rate is selected via the `SS` pin or `SOFT_START` (00h), bits[3:2]. When the motor speed reaches the handoff threshold, the MP6637A enters sinusoidal sensorless control.

Soft Dynamic

After entering sinusoidal sensorless control, the MP6637A's output duty cycle reaches its target smoothly depending on the soft-start time (t_{SS}). t_{SS} is configured via the `SS` pin or `SOFT_START` (00h), bits[5:4].

Steady State

In steady-state operation, the device selects sensorless sinusoidal control. To obtain the motor position, the device detects the motor's back electromotive force (BEMF) zero-crossing and drives the motor with a sinusoidal drive based on the rotor position.

Standby Mode

If V_{CC} exceeds the under-voltage lockout (UVLO) rising threshold and the PWM pin is pulled low, the MP6637A enters standby mode. The device exits standby mode when it detects the PWM input signal or the power is cycled.

Soft Start (SS) Selection

Connect a resistor (R_{SS}) between the `SS` and `GND` pins to select different open-loop

acceleration start-up settings and t_{SS} (see Table 1 on page 14). If the SS pin is floating, the start-up and t_{SS} settings follow the register settings.

Rotor Speed (FG) and Rotor Lock Indication (RD)

The FG/RD pin is an open-drain output, and must be pulled up externally via an external resistor.

The FG/RD pin can be configured for speed indication. Different FG outputs can be configured via WINDOW_START_OVP_FGRD (02h), bits[3:2]:

- If FG_DIV[1:0] = 00, the FG/RD pin outputs 1 cycle every 3 electrical cycles.
- If FG_DIV[1:0] = 01 or 11, the FG/RD pin outputs 1 cycle each electrical cycle.
- If FG_DIV[1:0] = 10, the FG/RD pin outputs 1 cycle every 2 electrical cycles.

The FG/RD pin can be configured for locked-rotor (RD) protection. The FG/RD pin has a low output when RD protection is triggered.

Protections

The MP6637A features rich protection features, described below.

Short-Circuit Protection (SCP)

The MP6637A employs internal overload and short-circuit protection (SCP) by detecting the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the protection threshold (typically 1.9A), all MOSFET turns off immediately after a blanking

time. After a lock-retry time, the IC attempts to restart and resume normal operation.

Over-Current Protection (OCP)

During normal switching, if the current flowing through any MOSFET exceeds the over-current protection (OCP) threshold (typically 1.3A) after a set blanking time, the output duty cycle decreases to limit the load current.

Thermal Shutdown (TSD)

The MP6637A employs thermal monitoring. If the die temperature exceeds 150°C, all MOSFETs turn off. Once the die temperature drops to its low threshold (typically 130°C), the IC restarts and resumes normal operation.

Under-Voltage Lockout (UVLO)

If V_{CC} falls below the under-voltage lockout (UVLO) threshold, all device circuitries are disabled and the internal logic resets. Once V_{CC} exceeds the UVLO threshold again, the device restarts and resumes normal operation.

Locked-Rotor Protection (RD)

If locked-rotor (RD) protection is triggered, all MOSFETs turn off. After a lock-retry time (typically 4.4s), the IC restarts and attempts to resume normal operation.

Over-Voltage Protection (OVP)

The MP6637A employs input over-voltage protection (OVP). If V_{CC} exceeds the OVP threshold (typically 5.8V), all MOSFETs turn off. Once V_{CC} drops below 5.3V, the device restarts and attempts to resume normal operation.

OVP can be disabled via internal register.

REGISTER DESCRIPTION

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	OC_VF[1:0]		T_SS[1:0]		F_SLEW[1:0]		F_TAR[1:0]	
01h (OTP/REG)	VOL	PWM_POL	WD_BLK	WD_ANG	SPD_ZERO	DIN_MIN[2:0]		
02h (OTP/REG)	WD_BLK_MD	QUICK_ST	BEMF_SAMP	RESERVED	FG_DIV[1:0]		OVP	FGRD

Note:

5) Ensure that $V_{CC} = 6.5V$ when configuring the one-time programmable (OTP) memory.

SOFT_START (00h)

The SOFT_START command configures the start-up parameters.

Bits	Access	Bit Name	Default	Description
7:6	R/W	OC_VF[1:0]	10	Sets the current limit threshold during open-loop acceleration. 00: $1/4 \times I_{OCP}$ 01: $1/4 \times I_{OCP}$ 10: $1/2 \times I_{OCP}$ 11: $1 \times I_{OCP}$
5:4	R/W	T_SS[1:0]	11	Sets the soft-start time (t_{SS}). This is the time duration that outputs the duty cycle from 0% to 100%. 00: 8.7s 01: 4.4s 10: 2.2s 11: 1.1s
3:2	R/W	F_SLEW[1:0]	01	Sets the frequency slew rate during open-loop acceleration. Start-up is faster with a higher value. 00: 15Hz 01: 59Hz 10: 234Hz 11: 938Hz
1:0	R/W	F_TAR[1:0]	01	Sets the target electrical speed during open-loop acceleration. 00: 20Hz 01: 39Hz 10: 78Hz 11: 156Hz

CURVE_WINDOW_PWM_DUTY (01h)

The CURVE_WINDOW_PWM_DUTY command configures the starting duty cycle, PWM input polarity, detection window, and duty cycle limit.

Bits	Access	Bit Name	Default	Description
7	R/W	VOL	0	Sets the duty cycle limit during open-loop acceleration. 0: 87.5% 1: 50%
6	R/W	PWM_POL	0	Selects the PWM pin polarity. 0: Positive duty cycle 1: Negative duty cycle
5	R/W	WD_BLK	0	Sets the back EMF (BEMF) detection window blanking time. 0: 33 μ s 1: 100 μ s

4	R/W	WD_ANG	1	Selects the BEMF detection window. 0: 30° 1: 15°
3	R/W	SPD_ZERO	1	Enables zero speed. 0: Keeps the minimum speed when the input duty cycle is below the duty cycle set by DIN_MIN 1: Stops when the input duty cycle is below the duty cycle set by DIN_MIN
2:0	R/W	DIN_MIN[2:0]	010	Sets the starting duty cycle. 000: 6.25% 001: 9.375% 010: 12.5% 011: 15.625% 100: 18.75% 101: 21.875% 110: 25% 111: 28.125%

WINDOW_START_OVP_FGRD (02h)

The WINDOW_START_OVP_FGRD command configures the BEMF window, quick start, the FG/RD pin output, and over-voltage protection (OVP).

Bits	Access	Bit Name	Default	Description
7	R/W	WD_BLK_MD	0	Selects the BEMF blanking time. 0: Automatic 1: Fixed time
6	R/W	QUICK_ST	0	Enables quick start-up with a faster alignment and open-loop acceleration. 0: Disabled 1: Enabled
5	R/W	BEMF_SAMP	0	Sets the BEMF detection activation. 0: During the BEMF detection window 1: At the end of BEMF detection window
4	NA	RESERVED	0	Reserved.
3:2	R/W	FG_DIV	01	Selects the FG/RD pin output. FG_DIV is only active when FGRD = 0. 00: 1/3x. The FG/RD pin outputs 1 pulse every 3 electrical cycles 01: 1x. The FG/RD pin outputs 1 pulse each electrical cycle 10: 1/2x. The FG/RD pin outputs 1 pulse every 2 electrical cycles 11: 1x. The FG/RD pin outputs 1 pulse each electrical cycle
1	R/W	OVP	0	Enables input over-voltage protection (OVP). 0: OVP is enabled 1: OVP is disabled
0	R/W	FGRD	0	Selects the FG or RD output for the FG/RD pin. 0: FG/RD pin outputs FG 1: FG/RD pin outputs RD

APPLICATION INFORMATION

Selecting an Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input voltage (V_{CC}) and reduce noise at the input. C_{IN} must have a low impedance at the switching frequency (f_{SW}).

Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. The effective capacitance decreases when the voltage across the ceramic capacitor increases. If the ceramic capacitor is biased with its voltage rating, the effective capacitance drops below 50%. Ensure that a sufficient larger-value input capacitance is applied.

Ensure that the voltage rating of the ceramic capacitor is high enough to guarantee no over-voltage (OV) rating events.

Input Clamping TVS Diode

High-voltage spikes are caused by the energy stored in the motor charging back to the side of C_{IN} . To avoid these spikes, add a voltage-clamping transient voltage suppressor (TVS) diode or Zener diode. For a 5V application, a 6V/SOD-123 package TVS or Zener diode is typically sufficient.

Selecting the SS Resistor

The start-up settings can be configured via internal registers or the SS resistor (R_{SS}).

Float the SS pin if the internal registers are used for the start-up settings. Otherwise, the SS setting follow the R_{SS} settings.

Different resistances set different start-up values to meet different application requirements (see Table 1).

OC_VF sets the current limit during open-loop acceleration. A higher value means a higher start-up torque.

F_TAR sets the handoff threshold speed from open-loop acceleration to sensorless sinusoidal control. A higher value means the open-loop acceleration lasts longer.

F_SLEW sets the frequency slew rate target during open-loop acceleration. A higher value means a faster start-up and frequency increase rate.

T_{SS} sets t_{SS} . The time duration that outputs the duty cycle goes from 0% to 100%.

Table 1: Start-Up Settings with Different SS Resistances

R_{SS}	OC_VF	F_TAR	F_SLEW	T_{SS}
MP6637AGTL-0000				
$\leq 1k\Omega$	$1/4 \times I_{OCP}$	20Hz	59Hz	2.2s
1.9k Ω	$1/4 \times I_{OCP}$	39Hz	59Hz	2.2s
3k Ω	$1/4 \times I_{OCP}$	78Hz	59Hz	2.2s
4.7k Ω	$1/4 \times I_{OCP}$	20Hz	234Hz	1.1s
7.2k Ω	$1/4 \times I_{OCP}$	39Hz	234Hz	1.1s
10k Ω	$1/4 \times I_{OCP}$	78Hz	234Hz	1.1s
16k Ω	$1/4 \times I_{OCP}$	78Hz	938Hz	1.1s
26k Ω	$1/4 \times I_{OCP}$	156Hz	938Hz	1.1s
MP6637AGTL-0001				
$\leq 1k\Omega$	$1/2 \times I_{OCP}$	20Hz	59Hz	2.2s
1.9k Ω	$1/2 \times I_{OCP}$	39Hz	59Hz	2.2s
3k Ω	$1/2 \times I_{OCP}$	78Hz	59Hz	2.2s
4.7k Ω	$1/2 \times I_{OCP}$	20Hz	234Hz	1.1s
7.2k Ω	$1/2 \times I_{OCP}$	39Hz	234Hz	1.1s
10k Ω	$1/2 \times I_{OCP}$	78Hz	234Hz	1.1s
16k Ω	$1/2 \times I_{OCP}$	78Hz	938Hz	1.1s
26k Ω	$1/2 \times I_{OCP}$	156Hz	938Hz	1.1s
Float	Follow internal register setting, Below is the default register setting			
	$1/2 \times I_{OCP}$	39Hz	59Hz	1.1s

PCB Layout Guidelines

Efficient PCB layout is crucial for stable operation and to avoid noise effects on the functions. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the input capacitors ($C1$ and $C2$) as close to the VCC and GND pins as possible to minimize the switching loop area. A small-package ceramic capacitor ($C1$) is recommended to improve high-frequency noise performance.
2. If R_{SS} is applied, place it close to the SS and GND pins. Keep R_{SS} 's ground trace away from the power loop trace.

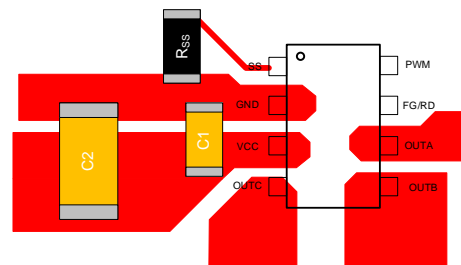


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

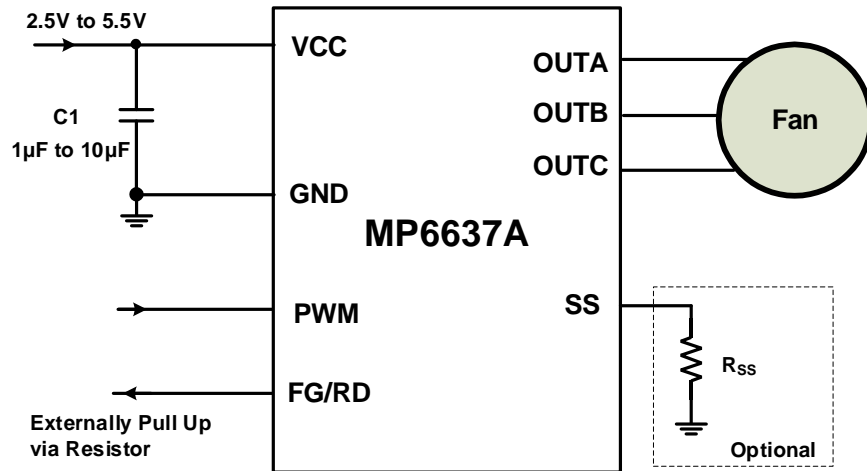


Figure 6: Typical Application Circuit

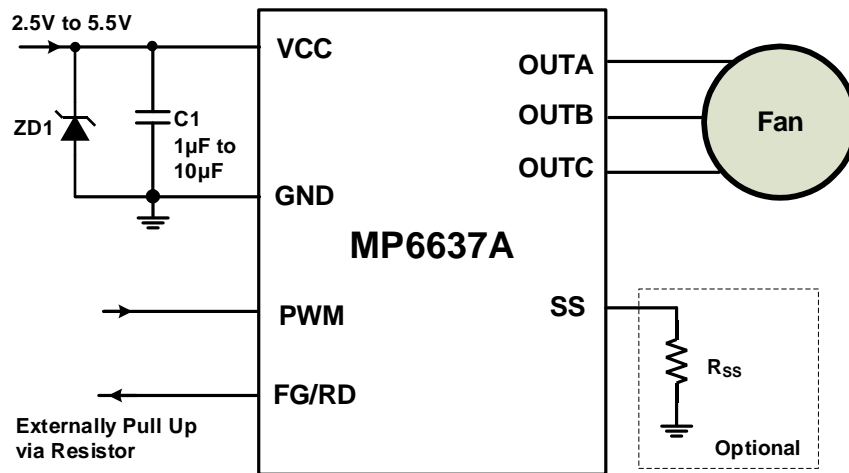
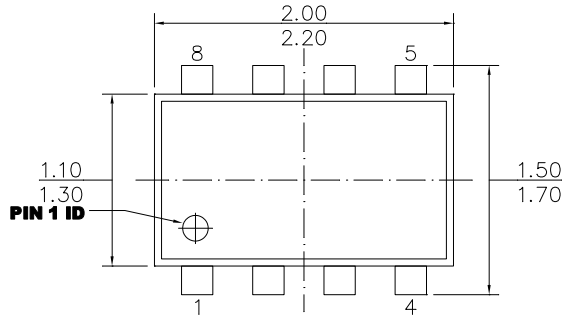


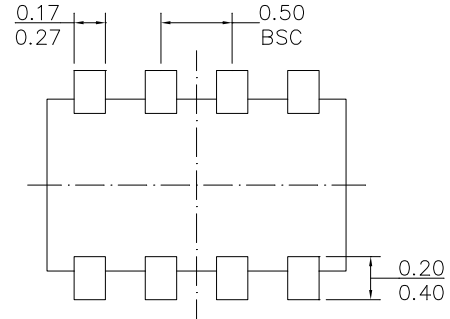
Figure 7: Typical Application Circuit with Input Clamping

PACKAGE INFORMATION

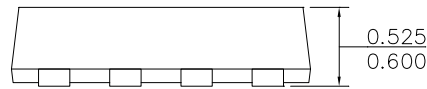
SOT583



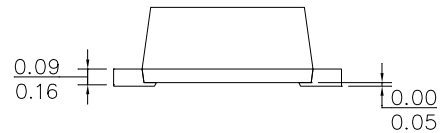
TOP VIEW



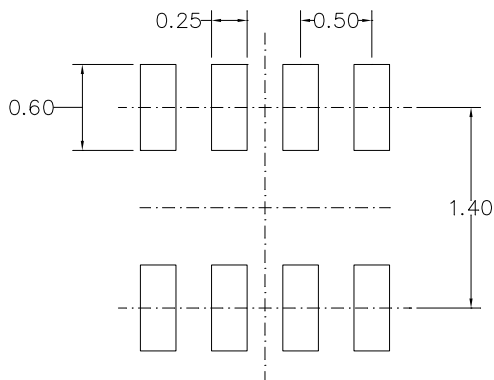
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

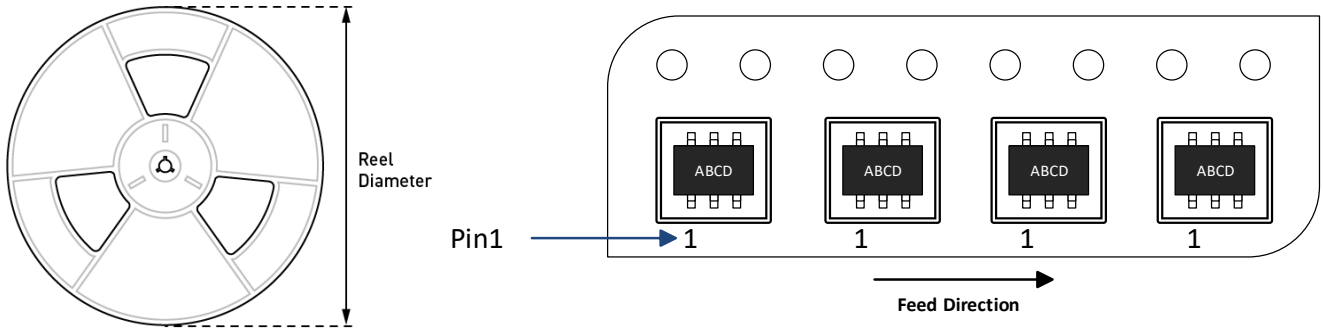


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6637AGTL-xxxx-Z	SOT583	5000	N/A	N/A	7in	8mm	4mm



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/8/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.