MP6636

18V, 4A Peak, Three-Phase, Sensorless BLDC Motor Driver with Integrated MOSFETs

DESCRIPTION

The MP6636 is a three-phase, sensorless, brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sensorless field-oriented control (FOC) for better efficiency and low vibration, with up to 2A of operational current. The input voltage (V_{CC}) ranges from 3.3V to 18V.

The MP6636 controls the motor speed via the PWM signal with a 50Hz to 50kHz PWM input frequency. The device also supports DC input for speed control.

The MP6636 features rotational speed detection. The rotational speed is an open-drain output via the FG pin.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, phase loss protection, over-current protection (OCP), and thermal shutdown.

The MP6636 is available in an SOIC-8EP and TQFN-10 (4mmx4mm) package.

FEATURES

- 3.3V to 18V Input Voltage (V_{CC}) Range
- Up to 2A of Continuous Current
- Sensorless Field-Oriented Control (FOC)
- Integrated 190mΩ High-Side MOSFETs (HS-FET) and Low-Side MOSFETS (LS-FET)
- Supports 0.3V to 3.15V DC Input or 50Hz to 50kHz Pulse-Width Modulation (PWM) Input for Speed Control
- Starting Duty Cycle Set with Hysteresis
- Curve Configuration
- Selectable Open-/Closed-Loop Speed
- Configurable Soft Acceleration and Align Time
- Configurable Direction Control
- Power-Save Mode
- 24kHz PWM Output Frequency
- Up to 4A of Configurable Current Limiting
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Phase-Loss Protection
- Over-Temperature Protection (OTP)
- Locked-Rotor Protection
- Selectable FG and RD Output
- Available in SOIC-8EP and TQFN-10 (4mmx4mm) Packages

APPLICATIONS

- Server Fans
- General Three-Phase BLDC Fans
- BLDC Motors

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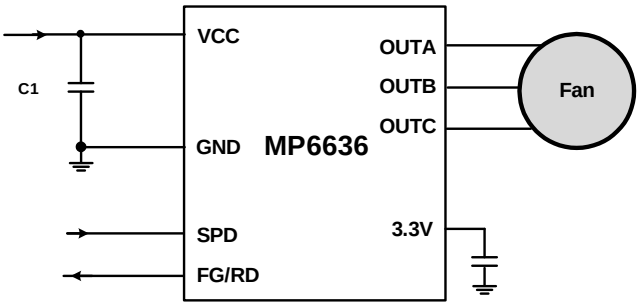
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP6636GN-xxxx**	SOIC-8EP	*See Below*	2a
MP6636GRT-xxxx**	TQFN-10 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6636GN-xxxx-Z).

** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for non-default function options. The default code is “0000”.

TOP MARKING (MP6636GN)

MP6636
LLLLLLLL
MPSYWW

MP: MPS prefix
Y: Year code
WW: Week code
6636: First four digits of the part number
LLLLLLLL: Lot number

TOP MARKING (MP6636GRT)

MPSYWW
MP6636
LLLLLL

MP: MPS prefix
Y: Year code
WW: Week code
6636: First four digits of the part number
LLLLLL: Lot number

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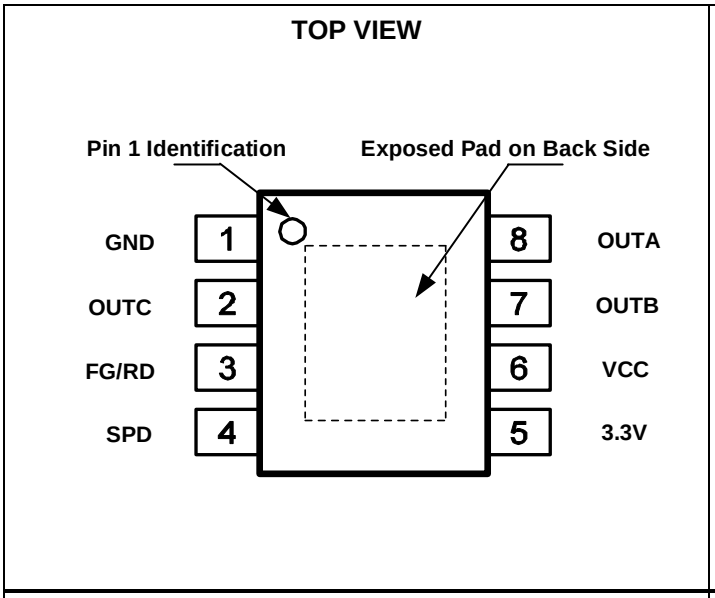
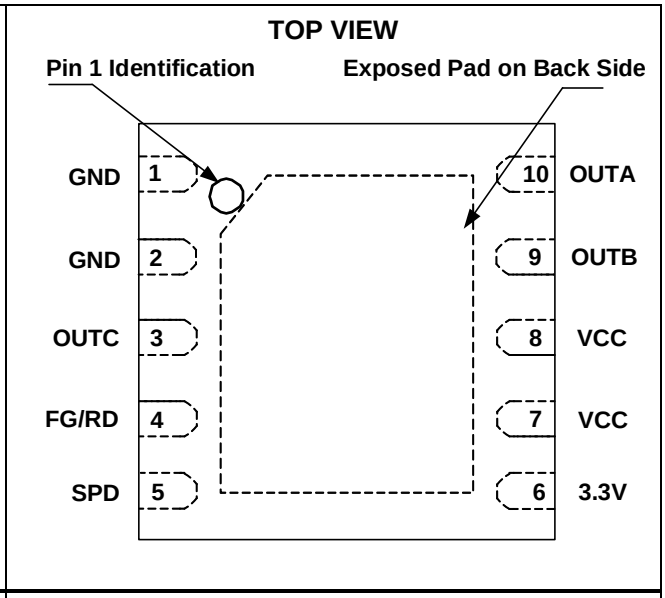
PACKAGE REFERENCE



SOIC-8EP (5mmx6mm)



TQFN-10 (4mmx4mm)

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PIN FUNCTIONS

SOIC-8EP Pin #	TQFN-10 Pin #	Name	Description
1	1, 2	GND	**Ground pin.**
2	3	OUTC	**Phase C terminal.**
3	4	FG/RD	**Rotational speed indicator (FG) and locked-rotor indicator (RD).** The FG/RD pin is an open-drain output, and must be pulled up externally. This pin can also be used as SCL in test mode for I^2C communication.
4	5	SPD	**Rotating speed control pin.** The SPD pin supports either a pulse-width modulation (PWM) input signal or DC input signal. This pin can also be used as SDA in test mode for I^2C communication.
5	6	3.3V	**3.3V LDO output.** The 3.3V pin must be bypassed locally.
6	7, 8	VCC	**Input voltage supply pin.** The VCC pin must be bypassed locally.
7	9	OUTB	**Phase B terminal.**
8	10	OUTA	**Phase A terminal.**
-	-	Exposed pad	**Exposed pad.** Connect the exposed pad to ground.

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, SPD, FG/RD 24V
$V_{OUTA/B/C}$ ..... -0.3V to V_{CC} + 0.3V
All other pins .....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2)
SOIC-8EP 2.6W
TQFN-10 (4mmx4mm) 2.66W
Junction temperature (T_J).....150°C
Lead temperature.....260°C
Storage temperature ..... -60°C to +150°C

ESD Rating

Human body model (HBM)..... 2000V
Charged-device model (CDM).....2000V

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....3.3V to 18V
Operating junction temp (T_J) ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-8EP ..... 48 ..... 9.... °C/W
TQFN-10 (4mmx4mm)..... 47 ..... 7.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			3.1	3.3	V
Input UVLO hysteresis	V_{UVLO_HYS}			0.3		V
Operating supply current	I_{CC}	SPD float, no load		5		mA
Standby current	I_{ST}	SPD low		70	110	μA
SPD input high voltage	V_{PWMH}		1.5			V
SPD input low voltage	V_{PWML}				0.4	V
SPD input internal pull-up resistance	R_{SPD}			50	100	kΩ
SPD DC input high threshold	V_{SPD_DCH}		3	3.15	3.3	V
SPD DC input low threshold	V_{SPD_DCL}			0.3		V
Switching frequency	f_{SW}		23.52	24	24.48	kHz
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	I_{OUT} = 100mA		110		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	I_{OUT} = 100mA		80		mΩ
Over-current protection (OCP) threshold	I_{OCP}	OC_THR = 0		4		A
Short-circuit protection (SCP) threshold	I_{SCP}			6		A
3.3V low-dropout (LDO) output voltage	$V_{3.3V}$	V_{CC} ≥ 4.5V	3.135	3.3	3.465	V
3.3V LDO load regulation		Load current = 30mA	3			V
FG/RD output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 3mA			0.35	V
Locked-rotor off time	t_{RE}			5.3		sec
Input over-voltage protection (OVP) threshold	V_{OVP}			19	20	V
OVP hysteresis	V_{OVP_HYS}			1.5		V
Thermal shutdown threshold	T_{TSD}			150		°C
Thermal shutdown hysteresis	T_{TSD_HYS}			25		°C
I^2C Interface (1)						
Input logic low	V_{IL}	V_{DD} = 3.3V	0		0.3 x V_{DD}	V
Input logic high	V_{IH}	V_{DD} = 3.3V	0.7 x V_{DD}			V
Output logic low	V_{OL}	I_{LOAD} = 3mA			0.4	V
SCL clock frequency	f_{SCL}		100		400	kHz
Capacitance bus for each bus line	C_B				400	pF

Note:

1) Guaranteed by design.

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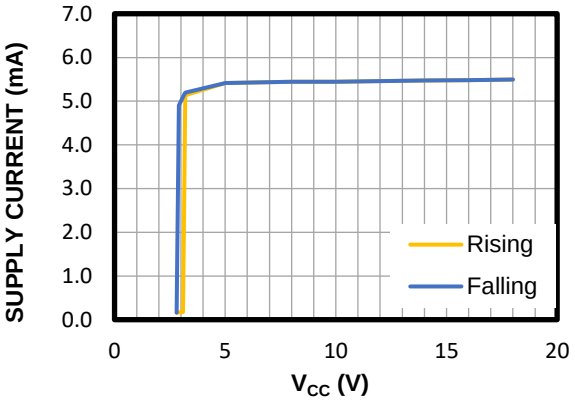
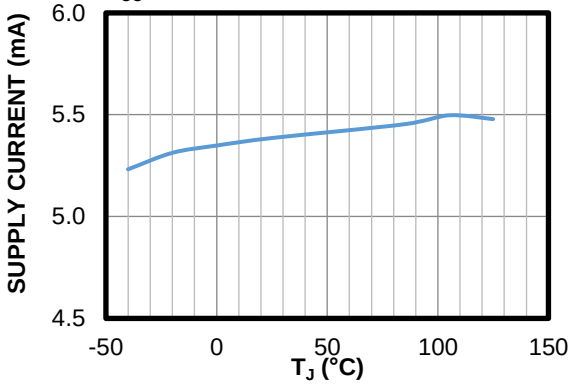
TYPICAL CHARACTERISTICS

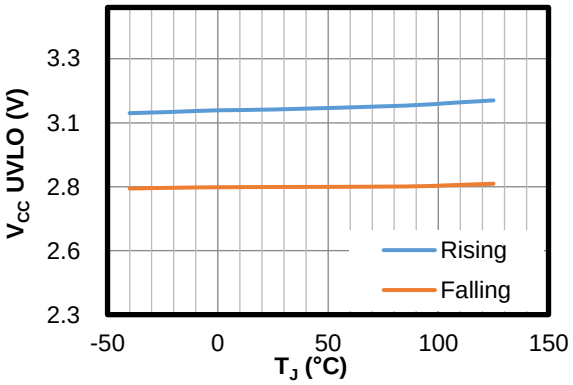
Supply Current vs. Input Voltage
V_{CC} = 2.8V to 18V, no load, T_J = 25°C



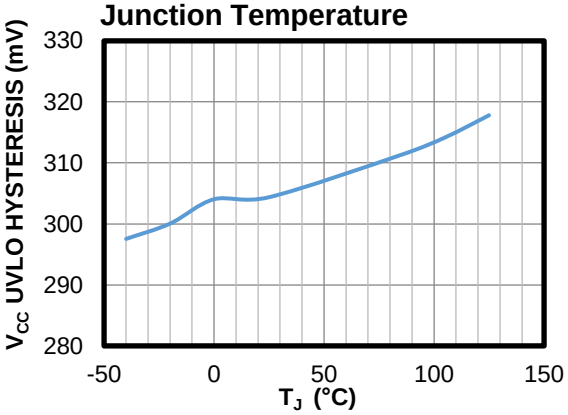
Supply Current vs. Junction Temperature
V_{CC} = 12V, no load



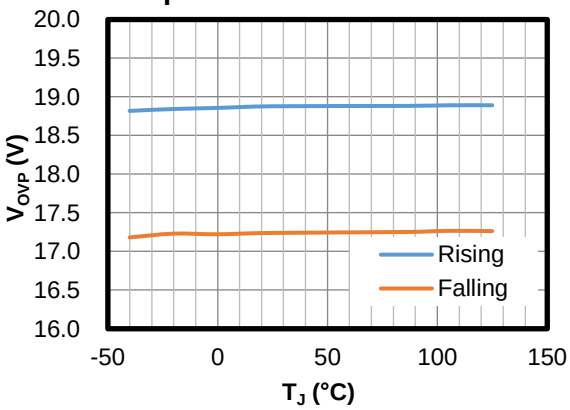
V_{CC} UVLO vs. Junction Temperature



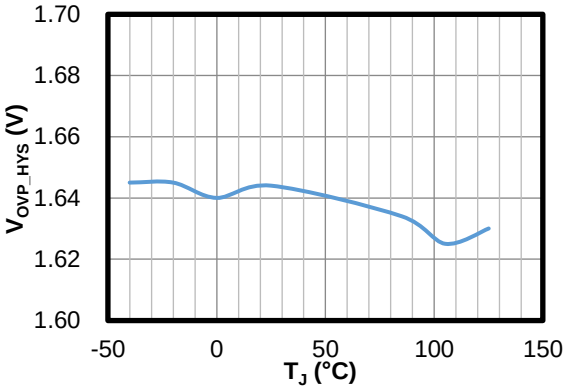
V_{CC} UVLO Hysteresis vs. Junction Temperature



OVP Threshold vs. Junction Temperature



OVP Hysteresis vs. Junction Temperature



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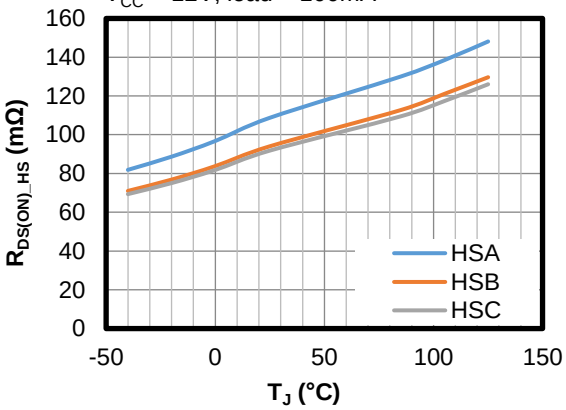
TYPICAL CHARACTERISTICS *(continued)*

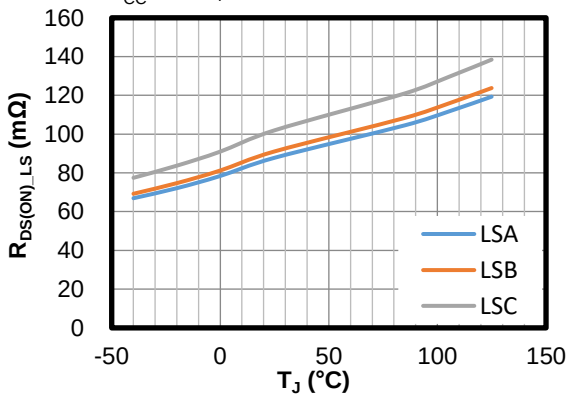
HS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V, load = 100mA



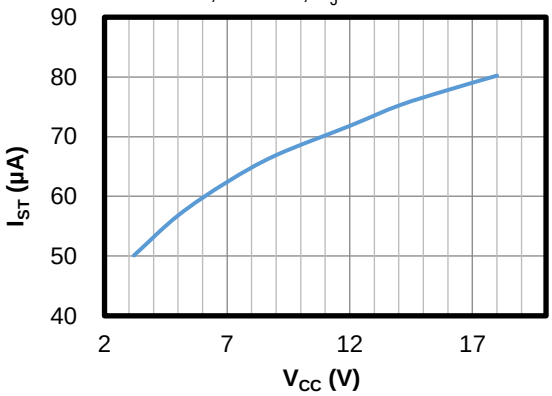
LS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V, load = 100mA



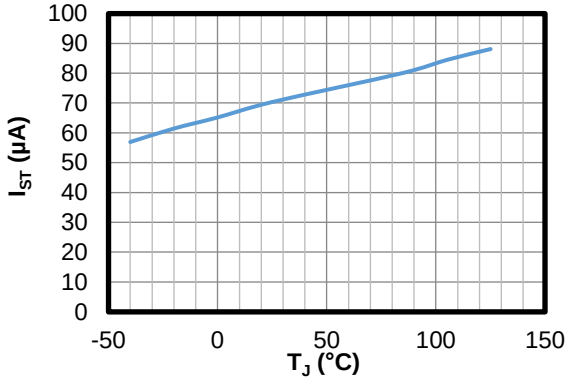
Standby Current vs. Input Voltage

SPD = low, no load, T_J = 25°C



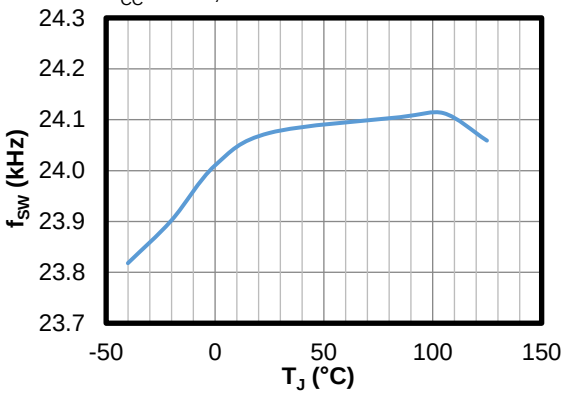
Standby Current vs. Junction Temperature

V_{CC} = 12V, SPD = low, no load



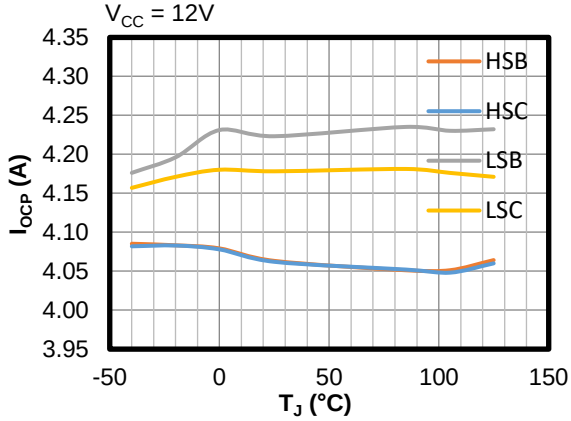
Switching Frequency vs. Junction Temperature

V_{CC} = 12V, no load



OCP Threshold vs. Junction Temperature

V_{CC} = 12V



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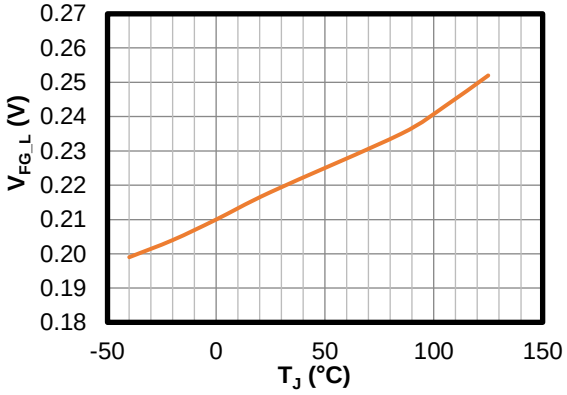
TYPICAL CHARACTERISTICS *(continued)*

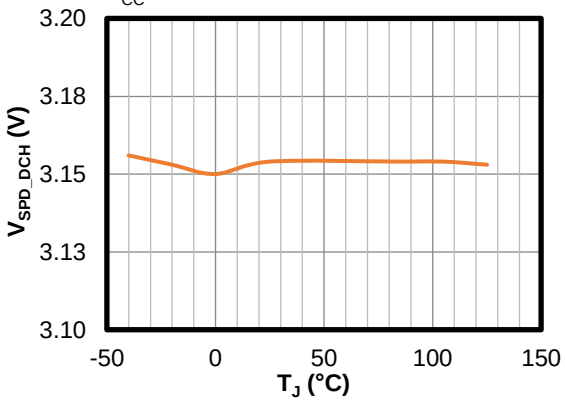
FG/RD Low-Level Voltage vs. Junction Temperature

V_{CC} = 12V, $I_{FG/RD}$ = 3mA



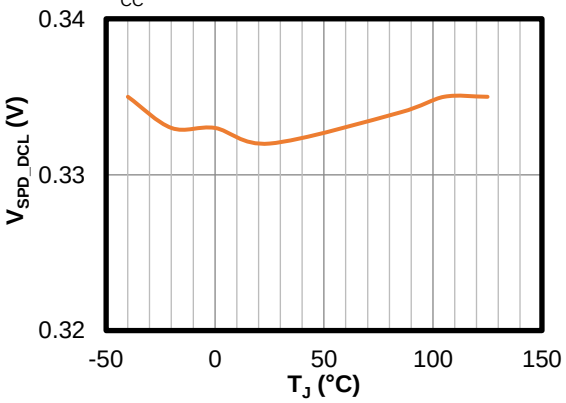
SPD DC Input High Threshold vs. Junction Temperature

V_{CC} = 12V



SPD DC Input Low Threshold vs. Junction Temperature

V_{CC} = 12V



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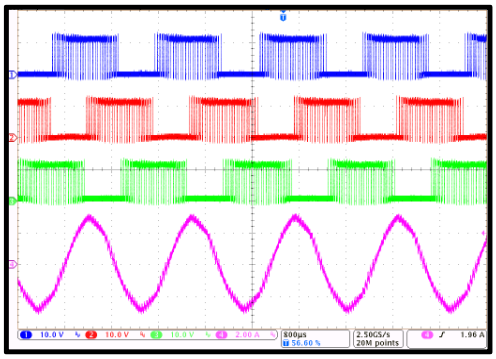
TYPICAL PERFORMANCE CHARACTERISTICS

Steady State

Anti-over modulation disabled, 12V/2.1A, 16000rpm, 6S4P cooling fan, V_{CC} = 12V, input PWM duty cycle = 100%

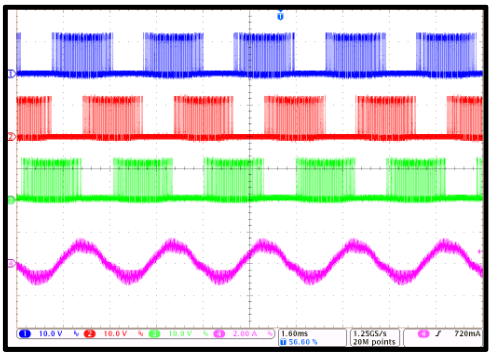
CH1: V_{OUTA}
CH2: V_{OUTB}
CH3: V_{OUTC}
CH4: I_A



Steady State

Anti-over modulation disabled, 12V/2.1A, 16000rpm, 6S4P cooling fan, V_{CC} = 12V, input PWM duty cycle = 50%

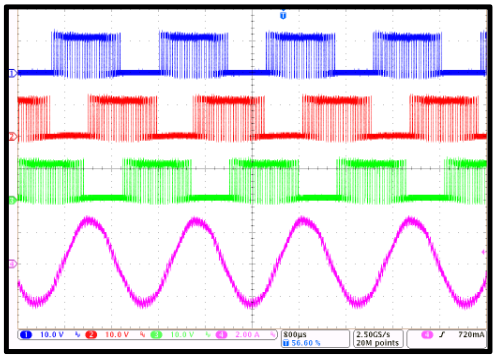
CH1: V_{OUTA}
CH2: V_{OUTB}
CH3: V_{OUTC}
CH4: I_A



Steady State

Anti-over modulation enabled, 12V/2.1A, 16000rpm, 6S4P cooling fan, V_{CC} = 12V, input PWM duty cycle = 100%

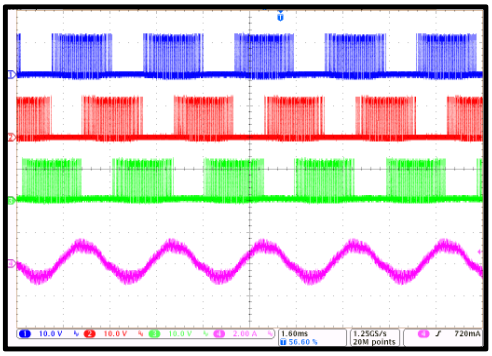
CH1: V_{OUTA}
CH2: V_{OUTB}
CH3: V_{OUTC}
CH4: I_A



Steady State

Anti-over modulation enabled, 12V/2.1A, 16000rpm, 6S4P cooling fan, V_{CC} = 12V, input PWM duty cycle = 50%

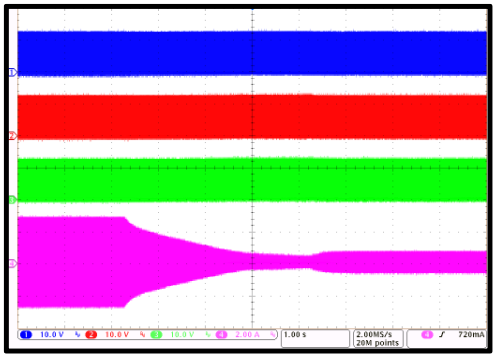
CH1: V_{OUTA}
CH2: V_{OUTB}
CH3: V_{OUTC}
CH4: I_A



PWM Duty Transient Response

12V/2.1A, 16000rpm, 6S4P cooling fan, input PWM duty cycle = 100% to 25%, V_{CC} = 12V

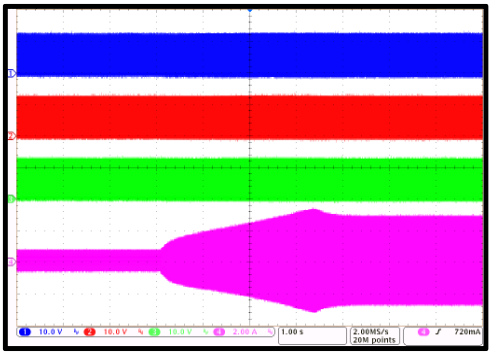
CH1: V_{OUTA}
CH2: V_{OUTB}
CH3: V_{OUTC}
CH4: I_A



PWM Duty Transient Response

12V/2.1A, 16000rpm, 6S4P cooling fan, input PWM duty cycle = 25% to 100%, V_{CC} = 12V

CH1: V_{OUTA}
CH2: V_{OUTB}
CH3: V_{OUTC}
CH4: I_A



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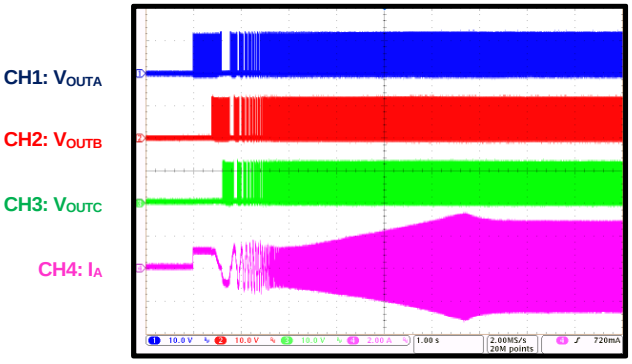
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

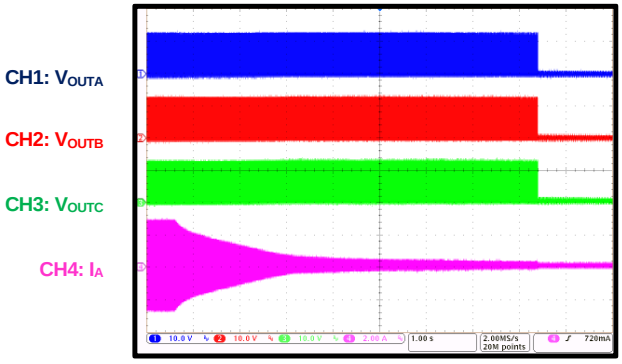
PWM On

12V/2.1A, 16000rpm, 6S4P cooling fan, soft-start time (t_{SS}) = 3.5s, V_{CC} = 12V, input PWM duty cycle = 1% to 100%



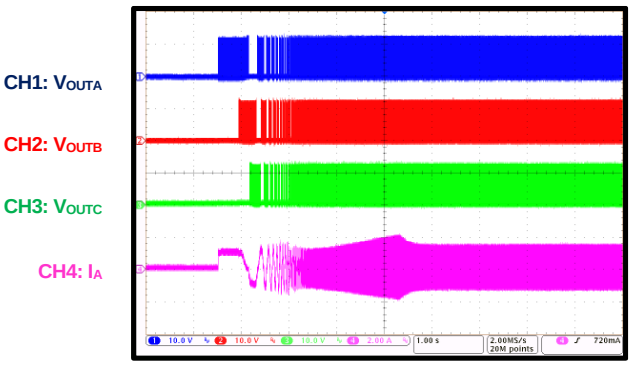
PWM Off

12V/2.1A, 16000rpm, 6S4P cooling fan, soft brake enabled, V_{CC} = 12V, input PWM duty cycle = 100% to 1%



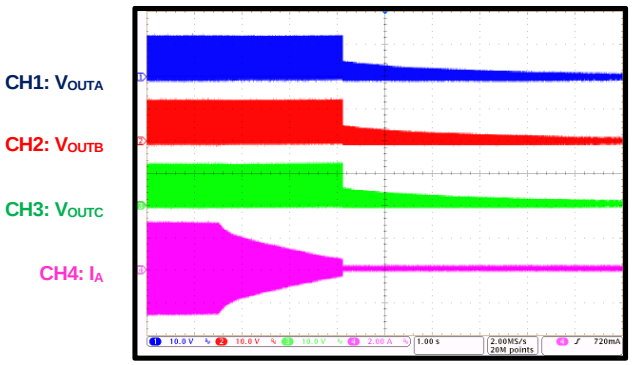
PWM On

12V/2.1A, 16000rpm, 6S4P cooling fan, t_{SS} = 3.5s, V_{CC} = 12V, input PWM duty cycle = 1% to 50%



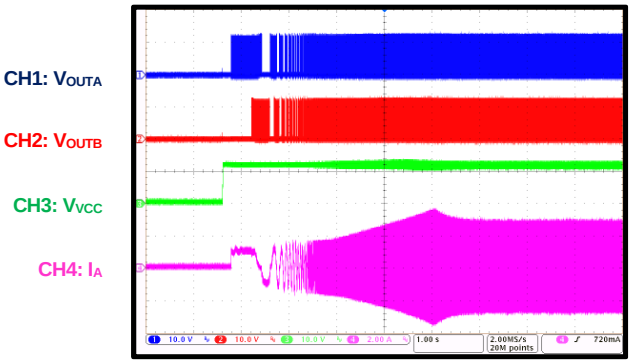
PWM Off

12V/2.1A, 16000rpm, 6S4P cooling fan, fast-stop enabled, V_{CC} = 12V, input PWM duty cycle = 50% to 1%



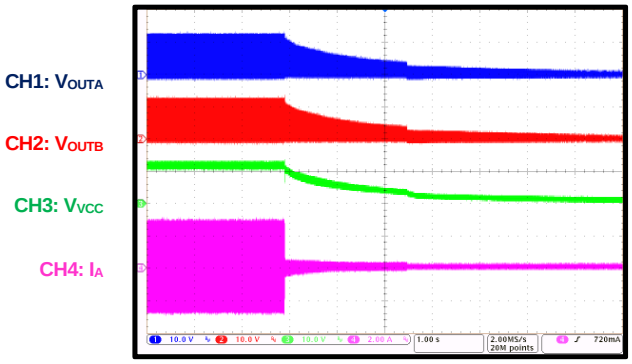
Start-Up

12V/2.1A, 16000rpm, 6S4P cooling fan, t_{SS} = 3.5s, SPD = float, V_{CC} = 0V to 12V



Shutdown

12V/2.1A, 16000rpm, 6S4P cooling fan, fast-stop enabled, t_{SS} = 3.5s, SPD = float, V_{CC} = 12V to 0V



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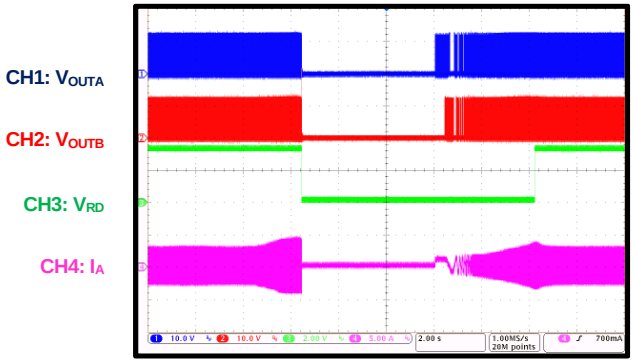
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

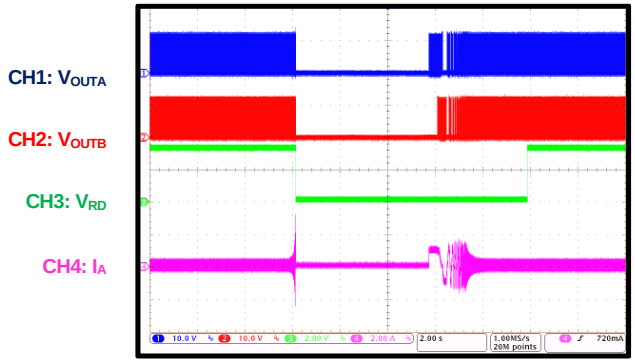
Locked-Rotor Protection

12V/2.1A, 16000rpm, 6S4P cooling fan, lock rotor then release, RD M1 and M2 enabled, V_{CC} = 12V, PWM = 100%



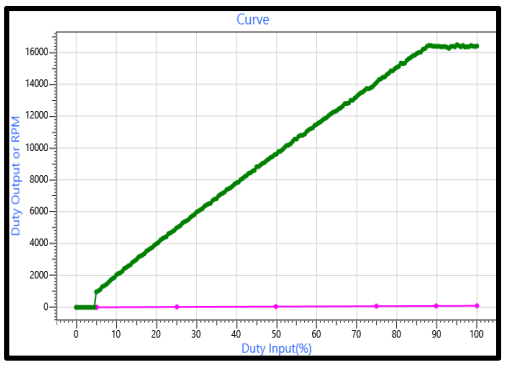
Locked-Rotor Protection

12V/2.1A, 16000rpm, 6S4P cooling fan, lock rotor then release, RD M1 and M2 enabled, V_{CC} = 12V, PWM = 10%



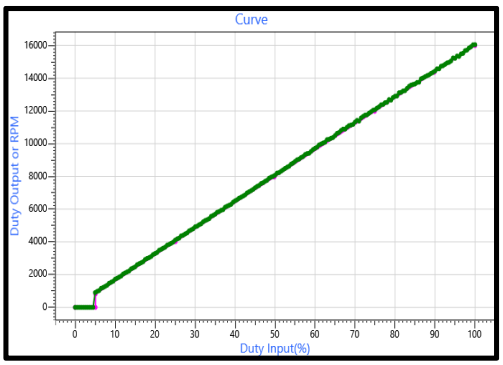
Open-Loop Curve

Default curve, captured with GUI, 12V/2.1A, 16000rpm, 6S4P cooling fan, V_{CC} = 12V



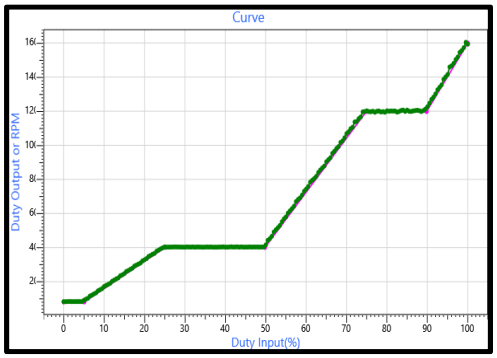
Closed-Loop Curve

Linear curve, captured with GUI, 12V/2.1A, 16000rpm, 6S4P cooling fan, MAX_SPEED = 16000prm, V_{CC} = 12V



Closed-Loop Curve

Non-linear curve, captured with GUI, 12V/2.1A, 16000rpm, 6S4P cooling fan, MAX_SPEED = 16000prm, V_{CC} = 12V



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FUNCTIONAL BLOCK DIAGRAM

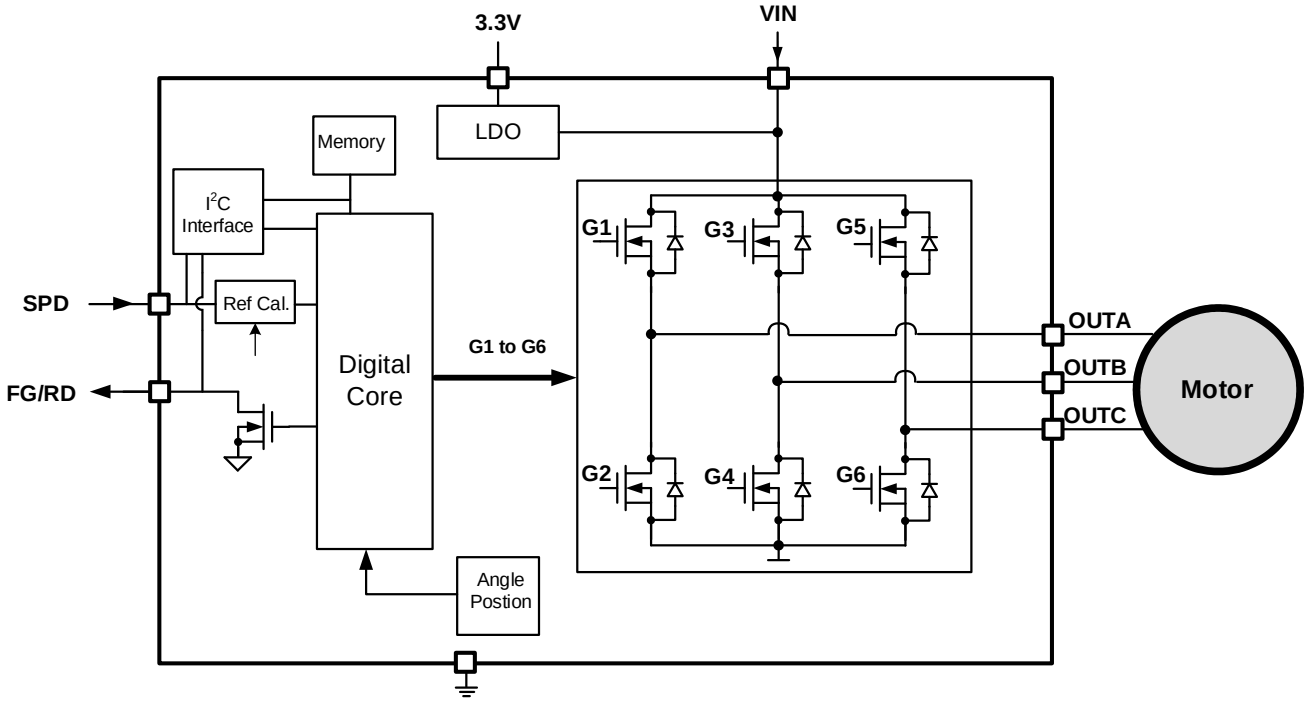

Figure 1: Functional Block Diagram

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OPERATION

The MP6636 is a three-phase, sensorless, brushless DC (BLDC) motor driver with integrated power MOSFETs. It features sensorless field-oriented control (FOC) for better efficiency and low vibration, with up to 2A of operational current. The input voltage (V_{CC}) ranges from 3.3V to 18V.

Since no Hall sensor is applied, the MP6636 employs sensorless FOC. Figure 2 shows the output duty cycle and output current (I_{OUT}) of each phase.

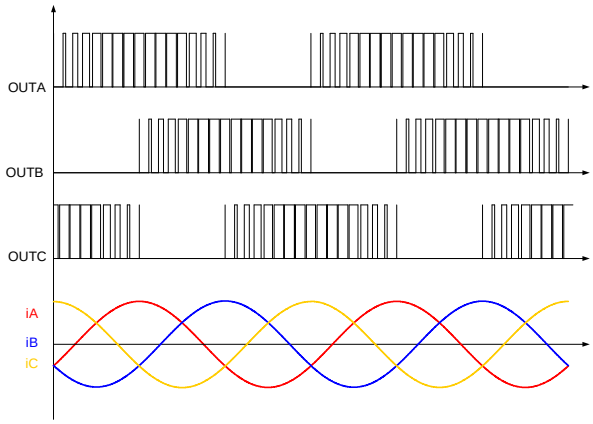

Figure 2: Output Duty Cycle and Current

Speed Control

The SPD pin controls the motor speed for open-loop or closed-loop control via a pulse-width modulation (PWM) signal or a DC voltage (V_{DC}). The PWM signal ranges from 50Hz to 50kHz and V_{DC} ranges from 0.3V to 3.15V.

If SPD_IN_SEL = 1, the motor speed is controlled by V_{DC} via the SPD pin. If SPD_IN_SEL = 0, the motor speed is controlled via the input PWM signal duty cycle.

Direction Control

The rotation direction is configured via CFR_2 (09h), bit[7].

If DIR = 0, the fan operates in forward rotation (A → B → C). If DIR = 1, the fan operates in reverse rotation (A → C → B).

When the fan direction changes during operation, the IC decreases the output duty cycle to the minimum speed, then applies the reverse voltage to change the motor fan's direction.

Initial State Detection (ISD)

At the beginning of start-up, the motor's initial state is detected. Different start-up strategies are used for different initial states.

If the motor is stationary, the align stage spins up the motor.

If the motor is rotating and the direction is the same as the commanded direction, the motor accelerates or decelerates to the commanded speed.

If the motor is rotating and the direction does not match the commanded direction, the motor decelerates to a low speed, then accelerates in the commanded direction.

Rotor Alignment

If the motor is stationary at the beginning of start-up, a set voltage vector configured by the register U_START is applied to align the rotor to the target alignment position. The voltage vector amplitude can be configured by U_START as well. The register ALIGN_TIME sets the different alignment times for different motors.

Open-Loop Acceleration

After rotor alignment, the motor accelerates openly by increasing the driven vector amplitude and frequency.

The voltage amplitude, accelerating ramp, accelerating target, and handoff target threshold can be set via their corresponding registers. Figure 3 shows the electrical frequency in the voltage/frequency (V/F) stage.

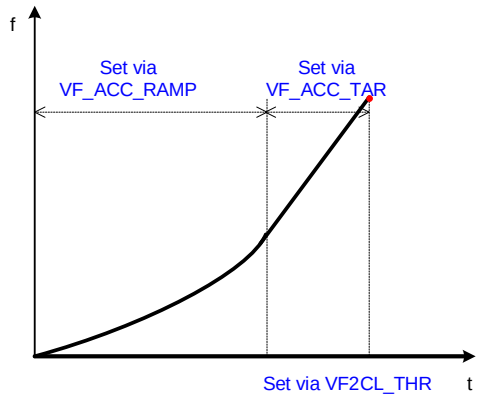

Figure 3: Electrical Frequency in the V/F Stage

Once the motor reaches the handoff threshold, the MP6636 enters sensorless FOC.

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Open-/Closed-Loop Speed Control

The MP6636 supports open-loop and closed-loop speed control via CFR_2 (09h), bit[0].

In closed-loop speed mode (V_LOOP = 1), the IC internally detects the speed and sends feedback to the control loop, which adjusts the output PWM duty cycle in a closed loop. In closed-loop control, the motor speed follows the reference exactly.

In open-loop speed mode (V_LOOP = 0), the output duty cycle directly depends on the PWM input duty cycle.

Curve Configuration

The MP6636 features curve configuration. The input duty cycle, output duty cycle, and speed can be configured via SPEED_CURVE_1 (0Bh), to SPEED_CURVE_10 (10h).

6 programmable points are supported, MAX_SPEED_2 (04h), bits[7:4] combine with MAX_SPEED_1 (03h), bits[7:0] sets the maximum speed during closed-loop control.

MAX_SPEED_1 (03h), bits[7:0] sets the output duty cycle when the input duty cycle is 100% during open-loop control.

S0, SPEED_CURVE_6 (10h) sets the output duty cycle or speed at the starting corner duty cycle, which is set via D0, SPEED_CURVE_1 (0Bh).

S1, S2, S3, and S4, SPEED_CURVE_7 (11h) to SPEED_CURVE_10 (14h) sets the speed and output duty cycle when the input duty cycle is D1, D2, D3, and D4, SPEED_CURVE_2 (0Ch) to SPEED_CURVE_5 (0Fh), respectively (see Figure 4).

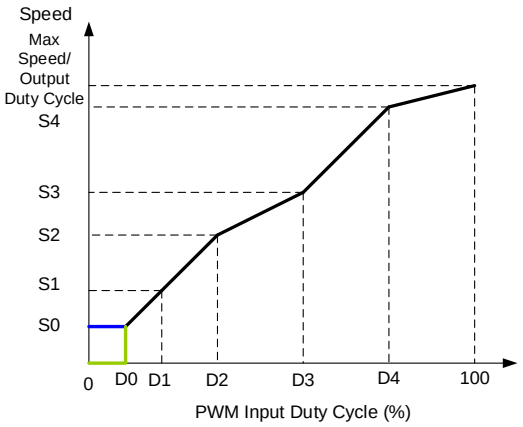

Figure 4: Curve Configuration

The input duty cycle can be calculated with Equation (1):

$$\text{Input duty cycle} = Dx / 255 \quad (1)$$

The output duty cycle in open-loop speed mode can be calculated with Equation (2):

$$\text{Output duty cycle} = Sx / 255 \quad (2)$$

The speed in closed-loop speed mode can be calculated with Equation (3):

$$\text{Closed-loop speed} = Sx / 255 \times \text{MAX SPEED} \quad (3)$$

D0 sets the starting corner duty cycle. When the input PWM duty cycle is below the duty cycle set by D0, the motor stops rotating or keeps the minimum speed, depending on SPD_LZERO, which is set via CFR_1 (08h), bit[4].

When the PWM duty cycle is below the output duty cycle set via CFR_1 (08h), bit[5], the motor can change to MAX_SPEED or the maximum output duty cycle.

This function is enabled via SPD_LMAX, which is set via CFR_1 (08h), bit[5]. If SPD_LMAX = 1 and the PWM input duty cycle falls below SPD_LMAX_THR (1.56% by default), then the fan changes to the maximum speed (see Figure 5).

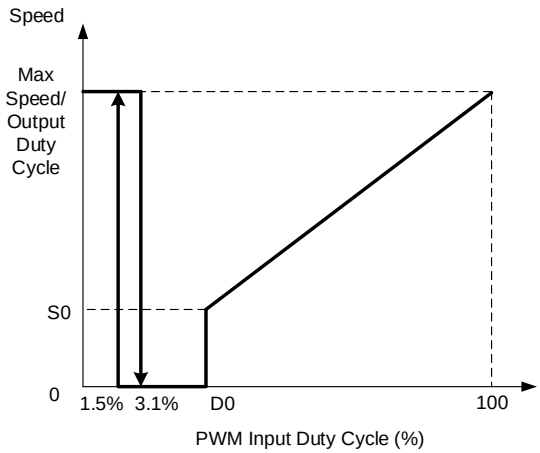

Figure 5: Speed Configuration (SPD_LZERO = 1)

If the PWM input duty cycle exceeds 3.125%, the MP6636 stops switching or keeps the minimum output duty cycle, depending on CFR_1 (08h), bit[4] (see Figure 6 on page 15).

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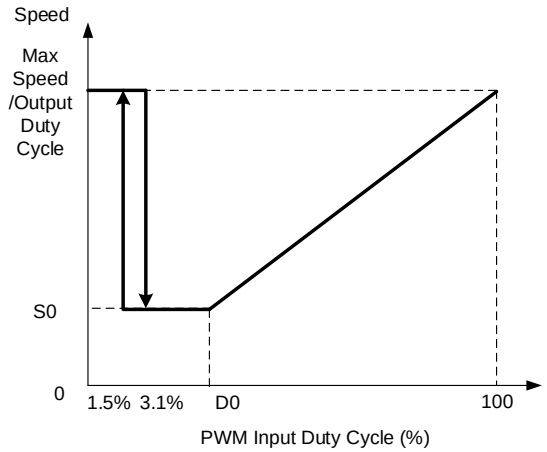

Figure 6: Speed Configuration (SPD_LZERO = 0)

Standby Mode

If the VCC voltage (V_{CC}) exceeds its under-voltage lockout (UVLO) rising threshold, the SPD pin remains low, SPD_LZERO = 1, and switching stops for more than 80ms, the IC enters standby mode. Once the PWM input signal is detected via the SPD pin or the power is cycled, the IC exits standby mode.

Rotor Speed Indication (FG)

The FG/RD pin can be configured for speed indication, locked-rotor indication, or fault indication.

If FGRD_SEL = 00, the FG/RD pin outputs 1 cycle every electrical cycle.

If FGRD_SEL = 01, the FG/RD pin outputs 2 cycles every 1 electrical cycles.

If FGRD_SEL = 10, the FG/RD pin is configured for locked-rotor detection.

If FGRD_SEL = 11, the FG/RD pin is configured for fault detection.

The RD and FT outputs are configured as active low, and must be pulled up externally.

Protection Circuits

The MP6636 features rich protections, including over-voltage protection (OVP), UVLO, over-current protection (OCP), short-circuit protection (SCP), phase loss protection, locked-rotor (RD) protection, and over-temperature protection (OTP).

Short-Circuit Protection (SCP)

The MP6636 employs internal overload protection and SCP by detecting the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the protection threshold (typically 6A), all MOSFETs turn off immediately after a blanking time.

Over-Current Protection (OCP)

If the phase current exceeds the threshold set via CFR_2 (09h), bit[2] during normal switching, the output duty cycle decreases to reduce the load current after a blanking time. The overload current limit function can be configured via CFR_4 (15h), bit[1].

Thermal Shutdown (TSD)

The MP6636 employs thermal monitoring. If the die temperature rises above 150°C, all MOSFETs turn off. Once the die temperature drops to its low threshold (125°C), the IC restarts and resumes normal operation.

Under-Voltage Lockout (UVLO)

If V_{CC} falls below its UVLO threshold, all device circuitries are disabled and the internal logic resets. Once V_{CC} exceeds its UVLO threshold, the device restarts and resumes normal operation.

Locked-Rotor Protection (RD)

If the rotor is locked, RD protection triggers and the MP6636 turns off all MOSFETs. After a 5.3s lock-retry time, the IC attempts to restart and resume normal operation.

RD protection can be configured through two modes via CFR_4 (15h), bit[2] and bit[3]. For better locked-rotor detection sensitivity, it is recommended to enable both RD modes.

RD protection can be configured to latch-off mode via CFR_2 (09h), bit[3]. The IC remains off after RD protection is triggered. Latch-off mode can be cleared by pulling SPD low or resetting the power on VCC.

Over-Voltage Protection (OVP)

The MP6636 employs OVP, which can be configured by CFR_2 (09h), bit[1].

If V_{CC} exceeds the OVP threshold (typically 19V), the IC turns off all MOSFETs. Once V_{CC} drops below the OVP falling threshold, the IC attempts to restart and resume normal operation.

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Phase-Loss Protection (PLOS)

The MP6636 monitors each phase voltage and current during rotor alignment. If phase loss protection (PLOS) is triggered, the IC stops switching and latches off. The latch can be cleared by pulling SPD low or resetting the power on VCC.

PLOS can be configured via CFR_4 (15h), bit[0].

Fault Diagnosis

The RD, OCP, SCP, TSD, OVP, and PLOS protections have fault bits to indicate each respective fault. The fault bits reset after being read.

Test Mode and Factory Mode

The MP6636 supports test mode to configure the internal registers. All internal registers can be read and written via the I^2C interface. After finalizing the design, the non-volatile memory (NVM) can configure the MP6636's register values up to 3 times using the "0000" default code. The MPS BLDC Virtual Bench provides easy parameter changes and memory configuration. For more details, contact an MPS FAE.

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REGISTER DESCRIPTION

Register Map

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPEED_CONSTANT							
01h (OTP/REG)	KU							
02h (OTP/REG)	KC_1							
03h (OTP/REG)	MAX_SPEED_1							
04h (OTP/REG)	MAX_SPEED_2				U_START			
05h (OTP/REG)	PLL_KI				PLL_KP			
06h (OTP/REG)	SPD_BW				CUR_BW			
07h (OTP/REG)	VF2CL_THR		VF_ACC_RAMP		VF_ACC_TAR		ALIGN_TIME	
08h (OTP/REG)	UIN_COM	SOFT_ BRAKE	SPD_ LMAX	SPD_ LZERO	FGRD_SEL		SOFT_START	
09h (OTP/REG)	DIR	PWM_POR	PWM_ FREQ_ SEL	SPD_IN_ SEL	RETRY_ SEL	OC_THR	OVP_EN	V_LOOP
0Ah (OTP/REG)	KC_2	DIR_BRK	SPD_ LMAX_ THR	RESERVED	SLEW_ RATE	SLP_LDO	GAIN	
0Bh (OTP/REG)	D0							
0Ch (OTP/REG)	D1							
0Dh (OTP/REG)	D2							
0Eh (OTP/REG)	D3							
0Fh (OTP/REG)	D4							
10h (OTP/REG)	S0							
11h (OTP/REG)	S1							
12h (OTP/REG)	S2							
13h (OTP/REG)	S3							
14h (OTP/REG)	S4							
15h (OTP/REG)	RESERVED	FG_RVS	FAST_ STOP	OMOD_ DIS	RD_M1_ EN	RD_M2_EN	OCP_EN	PL_EN
30h (REG)	RESERVED	DEBUG	RESERVED					
33h (REG)	RESERVED				ENABLE	RESERVED		
34h (REG)	RESERVED				TSD_EN	RESERVED	SCP_EN	RESERVED
37h (REG)	RESERVED		OCP	OVP	TSD	PL	SCP	RD

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SPEED_CONSTANT (00h)

The SPEED_CONSTANT command is a key internal control parameter. To generate a value for this parameter, it is recommended to use the GUI software.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPEED_CONSTANT	0x00	Sets the speed constant for internal control.

KU (01h)

The KU command sets the 8 bits of the observer voltage coefficient (KU) and is a key internal control parameter. To generate a value for this parameter, it is recommended to use the GUI software.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KU	0x00	Sets the observer voltage coefficient for internal control.

KC_1 (02h)

The KC_1 command sets the lower 8 bits of the observer current coefficient (KC) and is a key internal control parameter. To generate a value for this parameter, it is recommended to use the GUI software.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KC_1	0x00	Sets the observer current coefficient lower 8 bits for internal control.

MAX_SPEED_1 (03h)

The MAX_SPEED_1 command sets the lower 8 bits of MAX_SPEED, and configures the maximum output duty cycle or speed.

Bits	Access	Bit Name	Default	Description
7:0	R/W	MAX_SPEED_1	0x00	Sets the maximum output duty cycle. V_LOOP = 0: Sets the maximum output duty cycle in open-loop control V_LOOP = 1: Sets the maximum output speed in closed-loop control MAX SPEED = MAX_SPEED[11:0] x 22 / POLE PAIRS

MAX_SPEED_2/U_START (04h)

The MAX_SPEED_2/U_START command sets the higher 4 bits of MAX_SPEED for closed-loop speed control and the initial start-up voltage.

Bits	Access	Bit Name	Default	Description
7:4	R/W	MAX_SPEED_2	4’b 0000	Sets the higher 4-bits for closed-loop speed control.
3:0	R/W	U_START	4’b 0000	Sets the initial start-up voltage, which can be calculated with the following equation: U = value x 0.018 x UIN, where UIN = 18V

PLL_KI/PLL_KP (05h)

The PLL_KI/PLL_KP command sets the phase-locked loop parameter. To generate a value for these parameters, it is recommended to use the GUI software.

Bits	Access	Bit Name	Default	Description
7:4	R/W	PLL_KI	4’b 0000	Sets the KI parameter for phase-locked loop.
3:0	R/W	PLL_KP	4’b 0000	Sets the KP parameter for phase-locked loop.

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SPD_BW/CUR_BW (06h)

The SPD_BW/CUR_BW command configures the speed loop and current loop. To generate a value for these parameters, it is recommended to use the GUI software.

Bits	Access	Bit Name	Default	Description
7:4	R/W	SPD_BW	4'b 0000	Sets the bandwidth parameter for speed loop.
3:0	R/W	CUR_BW	4'b 0000	Sets the bandwidth parameter for current loop.

START_UP (07h)

The START_UP command sets the start-up parameters during the voltage/frequency (V/F) stage. To generate a value for these parameters, it is recommended to use the GUI software.

Bits	Access	Bit Name	Default	Description
7:6	R/W	VF2CL_THR	2'b 00	Sets the speed handoff threshold for V/F to sensorless control. For open-loop control, the handoff speed = 54095.4 x V_{CC} x N / (UIN x SPEED CONSTANT x POLE PAIRS). 2'b 00: N = 1 2'b 01: N = 2 2'b 10: N = 4 2'b 11: N = 8 UIN = 18V. For closed-loop control, the handoff speed = MAX SPEED x VF2CL_THR. 2'b 00: 3.125% 2'b 01: 6.25% 2'b 10: 12.5% 2'b 11: 25%
5:4	R/W	VF_ACC_RAMP	2'b 00	Sets the electrical frequency acceleration ramp during the V/F stage. 2'b 00: 754rpm/s^2 2'b 01: 1509rpm/s^2 2'b 10: 3018rpm/s^2 2'b 11: 6035rpm/s^2
3:2	R/W	VF_ACC_TAR	2'b 00	Sets the electrical frequency acceleration target during the V/F stage. 2'b 00: 515rpm/s 2'b 01: 1030rpm/s 2'b 10: 2060rpm/s 2'b 11: 3605rpm/s
1:0	R/W	ALIGN_TIME	2'b 00	Sets the rotor alignment time before the V/F stage. 2'b 00: 0.35s 2'b 01: 0.7s 2'b 10: 1.4s 2'b 11: 2s

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CFR_1 (08h)

The CFR_1 command configures the UIN compensation, soft-start time (t_{SS}), soft brake, start-up duty cycle and stopping duty cycle, SPD_LMAX maximum duty cycle when the PWM duty cycle is below its lower threshold, and the FG/RD pin's output.

Bits	Access	Bit Name	Default	Description
7	R/W	UIN_COM	1'b 0	Sets the UIN compensation. This is only valid for open-loop control. 1'b 0: Disabled 1'b 1: Enabled
6	R/W	SOFT_BRAKE	1'b 0	Sets the soft brake. 1'b 0: Disabled 1'b 1: Enabled
5	R/W	SPD_LMAX	1'b 0	Enables the output maximum duty cycle or speed when the PWM input duty cycle is below the threshold set via CFR_3, bit[5]. 1'b 0: Disabled 1'b 1: Enabled
4	R/W	SPD_LZERO	1'b 0	Disables the stop output when the PWM input duty cycle is below SPEED_CURVE_1. 1'b 0: Disabled 1'b 1: Enabled This bit must be set to 1'b 1 when entering power-saving mode.
3:2	R/W	FGRD_SEL	2'b 00	Selects the FG/RD pin's output. 2'b 00: 1 x FG 2'b 01: 2 x FG 2'b 10: RD 2'b 11: nFT
1:0	R/W	SOFT_START	2'b 00	Selects t_{SS}, the time during which the duty cycle changes from 0% to 100% or 100% to 0%. 2'b 00: 3.5s 2'b 01: 5.4s 2'b 10: 7s 2'b 11: 10.5s

CFR_2 (09h)

The CFR_2 command configures the direction polarity, pulse-width modulation (PWM) input polarity, PWM input frequency range, SPD pin input type, behavior after protection, over-current protection (OCP) threshold, over-voltage protection (OVP), and speed control loop.

Bits	Access	Bit Name	Default	Description
7	R/W	DIR	1'b 0	Sets the direction polarity. 1'b 0: Normal direction (A → B → C) 1'b 1: Reverse direction (A → C → B)
6	R/W	PWM_POR	1'b 0	Sets the PWM input polarity. 1'b 0: Original signal 1'b 1: Reversed high and low signal

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5	R/W	PWM_FREQ_SEL	1’b 0	Sets the PWM input frequency range. 1’b 0: 50Hz to 3kHz 1’b 1: 1kHz to 50kHz
4	R/W	SPD_IN_SEL	1’b 0	Sets the SPD pin input type. 1’b 0: PWM signal 1’b 1: DC voltage
3	R/W	RETRY_SEL	1’b 0	Sets the behavior after a protection occurs. 1’b 0: Retry after a rotor dead-lock time 1’b 1: Latch off
2	R/W	OC_THR	1’b 0	Sets the over-current (OC) threshold. 1’b 0: 4A 1’b 1: 2A
1	R/W	OVP_EN	1’b 0	Enables OVP. 1’b 0: Disabled 1’b 1: Enabled
0	R/W	V_LOOP	1’b 0	Sets the speed loop control. 1’b 0: Open-loop control 1’b 1: Closed-loop control

CFR_3 (0Ah)

The CFR_3 command configures the current coefficient most significant bits (MSB) for internal control, output behavior during reverse rotation, SPD_LMAX threshold, output switching slew rate, low-dropout (LDO) state in standby mode, and loop gain.

Bits	Access	Bit Name	Default	Description
7	R/W	KC_2	1’b 0	Observer current coefficient MSB for internal control.
6	R/W	DIR_BRK	1’b 0	Sets the output behavior during reverse rotation. 1’b 0: Coast 1’b 1: Brake
5	R/W	SPD_LMAX_THR	1’b 0	Sets the SPD_LMAX falling threshold. 1’b 0: 1.56% falling, 3.125% rising 1’b 1: 10.94% falling, 12.5% rising
4	R	RESERVED	1’b 0	Reserved.
3	R/W	SLEW_RATE	1’b 0	Sets the output switching slew rate. 1’b 0: Fast 1’b 1: Slow
2	R/W	SLP_LDO	1’b 0	Disables LDO behavior during standby mode. 1’b 0: Disable the 3.3V LDO 1’b 1: Enable the 3.3V LDO
1:0	R/W	GAIN	2’b 00	Sets the loop gain for internal sensorless FOC. 2’b 00: Maximum 2’b 01: High 2’b 10: Medium 2’b 11: Low

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SPEED_CURVE_1 (0Bh)

The SPEED_CURVE_1 command configures the input PWM duty cycle (D0).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D0	0x00	Sets the input PWM duty cycle (D0), which can be calculated with the following equation: Input PWM duty cycle = D0[7:0] / 255

SPEED_CURVE_2 (0Ch)

The SPEED_CURVE_2 command configures the input PWM duty cycle (D1).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D	0x40	Sets the input PWM duty cycle (D1), which can be calculated with the following equation: Input PWM duty cycle = D1[7:0] / 255

SPEED_CURVE_3 (0Dh)

The SPEED_CURVE_3 command configures the input PWM duty cycle (D2).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D2	0x80	Sets the input PWM duty cycle (D2), which can be calculated with the following equation: Input PWM duty cycle = D2[7:0] / 255

SPEED_CURVE_4 (0Eh)

The SPEED_CURVE_4 command configures the input PWM duty cycle (D3).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D3	0xC0	Sets the input PWM duty cycle (D3), which can be calculated with the following equation: Input PWM duty cycle = D3[7:0] / 255

SPEED_CURVE_5 (0Fh)

The SPEED_CURVE_5 command configures the input PWM duty cycle (D4).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D4	0xFF	Sets the input PWM duty cycle (D4), which can be calculated with the following equation: Input PWM duty cycle = D4[7:0] / 255

SPEED_CURVE_6 (10h)

The SPEED_CURVE_6 command configures the output duty cycle or speed when the input PWM duty cycle is D0.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S0	0x00	Sets the output duty cycle or output speed (S0) when the input PWM is D0. For open-loop control, the output duty cycle = S0[7:0] / 255 For closed-loop control, the output speed = S0[7:0] / 255 x MAX_SPEED[11:0] x 22 / pole pairs Units are in rpm.

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SPEED_CURVE_7 (11h)

The SPEED_CURVE_7 command configures the output duty cycle or speed when the input PWM duty cycle is D1.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S1	0x40	Sets the output duty cycle or the output speed S1 when the input PWM is D1. For open-loop control, the output duty cycle = S1[7:0] / 255 For closed-loop control, the output speed = S1[7:0] / 255 x MAX_SPEED[11:0] x 22 / pole pairs Units are in rpm.

SPEED_CURVE_8 (12h)

The SPEED_CURVE_8 command configures the output duty cycle or speed when the input PWM duty cycle is D2.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S2	0x80	Sets the output duty cycle or the output speed S1 when the input PWM is D2. For open-loop control, the output duty cycle = S2[7:0] / 255 For closed-loop control, the output speed = S2[7:0] / 255 x MAX_SPEED[11:0] x 22 / pole pairs Units are in rpm.

SPEED_CURVE_9 (13h)

The SPEED_CURVE_9 command configures the output duty cycle or speed when the input PWM duty cycle is D3.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S3	0xC0	Sets the output duty cycle or the output speed S1 when the input PWM is D3. For open-loop control, the output duty cycle = S3[7:0] / 255 For closed-loop control, the output speed = S3[7:0] / 255 x MAX_SPEED[11:0] x 22 / pole pairs Units are in rpm.

SPEED_CURVE_10 (14h)

The SPEED_CURVE_10 command configures the output duty cycle or speed when the input PWM duty cycle is D4.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S4	0xFF	Sets the output duty cycle or the output speed S1 when the input PWM is D4. For open-loop control, the output duty cycle = S4[7:0] / 255 For closed-loop control, the output speed = S4[7:0] / 255 x MAX_SPEED[11:0] x 22 / pole pairs Units are in rpm.

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CFR_4 (15h)

The CFR_4 command configures the FG pin, fast stop, anti-over modulation, locked-rotor (RD) protection modes, OCP, and phase loss protection (PLOS).

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	1'b 0	Reserved.
6	R/W	FG_RVS	1'b 0	Sets the FG pin behavior under reverse rotation conditions. 1'b 0: FG maintains its output during reverse rotation 1'b 1: FG pin floating (output high with a pull-up resistor)
5	R/W	FAST_STOP	1'b 0	Disables fast stop. 1'b 0: Disabled 1'b 1: Enabled
4	R/W	OMOD_DIS	1'b 0	Enables anti-over modulation function. 1'b 0: Enabled 1'b 1: Disabled
3	R/W	RD_M1_EN	1'b 0	Disables RD protection mode 1. 1'b 0: Disabled 1'b 1: Enabled
2	R/W	RD_M2_EN	1'b 0	Disables RD protection mode 2. 1'b 0: Disabled 1'b 1: Enabled
1	R/W	OCP_EN	1'b 0	Disables OCP. 1'b 0: Disabled 1'b 1: Enabled
0	R/W	PL_EN	1'b 0	Disables PLOS. 1'b 0: Disabled 1'b 1: Enabled

DEBUG (30h)

The DEBUG command enables I^2C debugging mode.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	1'b 0	Reserved.
6	R/W	DEBUG	1'b 0	Enables I^2C debugging mode. 1'b 0: I^2C debugging mode; the internal SCL connects to FG/RD and SDA connects to SPD 1'b 1: Exit I^2C debugging mode; the FG/RD and SPD pins resume their original function
5:0	R/W	RESERVED	6'b 000000	Reserved.

ENABLE (33h)

The ENABLE command sets the chip's global enable of the digital control and analog circuits.

Bits	Access	Bit Name	Default	Description
7:4	R	RESERVED	5'b 00000	Reserved.
3	R/W	ENABLE	1'b 1	Sets the chip's global enable of the digital control and analog circuits. 1'b 0: Stop operation 1'b 1: Normal operation

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2:0	R	RESERVED	0x00	Reserved.

CFR_5 (34h)

The CFR_5 command sets the parameters for thermal shutdown (TSD) and short-circuit protection (SCP).

Bits	Access	Bit Name	Default	Description
3	R/W	TSD_EN	1’b 1	Enables TSD. 1’b 0: Disabled 1’b 1: Enabled
2	R	RESERVED	1’b 1	Reserved.
1	R/W	SCP_EN	1’b 1	Enables SCP. 1’b 0: Disabled 1’b 1: Enabled
0	R	RESERVED	1’b 1	Reserved.
3	R/W	TSD_EN	1’b 1	Enables TSD. 1’b 0: Disabled 1’b 1: Enabled

PROTECTION_ INDICATOR (37h)

The PROTECTION_INDICATOR command reports the protection statuses.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	2’b 00	Reserved.
5	R	OCP	1’b 0	OCP indicator. 1’b 0: No OCP 1’b 1: OCP
4	R	OVP	1’b 0	OVP indicator. 1’b 0: No OVP 1’b 1: OVP
3	R	TSD	1’b 0	TSD indicator. 1’b 0: No TSD 1’b 1: TSD
2	R	PL	1’b 0	PLOS indicator. 1’b 0: No PLOS 1’b 1: PLOS
1	R	SCP	1’b 0	SCP indicator. 1’b 0: No SCP 1’b 1: SCP
0	R	RD	1’b 0	RD protection indicator. 1’b 0: No RD 1’b 1: RD

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APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible. The VCC pin stabilizes the input voltage (V_{IN}) and reduces input switching voltage noise and ripple. The C_{IN} impedance must be low at the switching frequency (f_{SW}). Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics, where the effective ceramic capacitance is dependent on the voltage rating. The DC biased voltage and value can lose as much as 50% of its capacitance at its rated voltage rating. Leave a sufficient voltage rating margin when selecting the component.

Selecting the Input Snubber

Due to C_{IN}'s energy charge and discharge during the soft switching phase transition, the input current (I_{IN}) has switching cycle ringing. If required, add an RC snubber (a 2Ω resistor in series with a 4.7µF capacitor) in parallel with C_{IN} to prevent switching cycle ringing.

Input Clamping TVS Diode

Add a voltage-clamping transient voltage suppressor (TVS) diode to avoid high voltage spikes caused by the energy stored in the motor inductor as it charges back to C_{IN}.

Selecting the LDO Output Capacitor

The LDO pin outputs 3.3V, which can supply the internal or external circuit. The LDO pin must be locally bypassed with a capacitor. A 1µF or greater capacitor in series with a 10Ω resistor is recommended. This bypass capacitor and its resistor in series must be connected to a 3.3V output pin, and the GND return path must be separated from power GND. See the PCB Layout Guidelines section on page 28 for more information.

System-Level ESD Enhancement

Some fan products must pass system-level electrostatic discharge (ESD) testing. Compared to HBM ESD ratings, system-level ESD follows the IEC 61000-4-2 standard. There are two different modes for the IEC 61000-4-2 ESD test: air discharge and contact discharge. Contact discharge mode is the first choice for testing.

Figure 7 shows the equivalent circuit of a HBM ESD circuit.

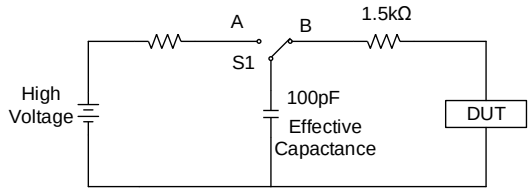

Figure 7: Equivalent Circuit of HBM ESD Circuit

Figure 8 shows that the IEC 61000-4-2 sets the equivalent circuit.

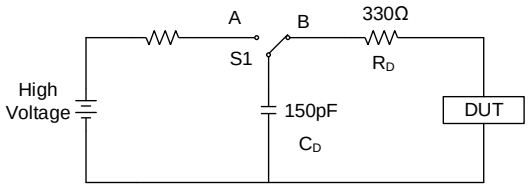

Figure 8: Equivalent Circuit of System-Level ESD

Compared to the HBM ESD ratings, the discharge capacitance exceeds the human body's effective capacitance, and the discharge resistor of the IEC level ESD is much smaller.

To pass ±8kV for IEC 61000-4-2 contact discharge mode, an external circuit may be required to enhance the ESD capability. Figure 9 shows an example to enhance the ESD capability with external components. Due to differences between the components and practical PCB layouts, the test results may vary slightly.

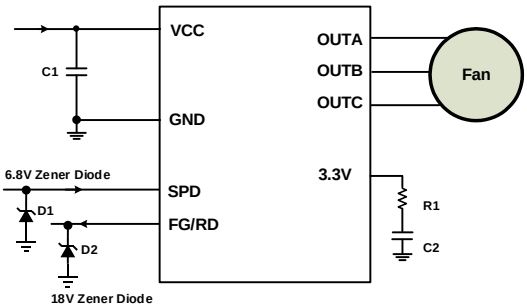

Figure 9: External ESD-Enhanced Circuit

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Motor Parameters Measurement

The motor phase resistance and phase inductance are key parameters for sensorless FOC. The motor's phase resistance and inductance refer to the resistance and inductance from the phase output to the winding center tap, respectively.

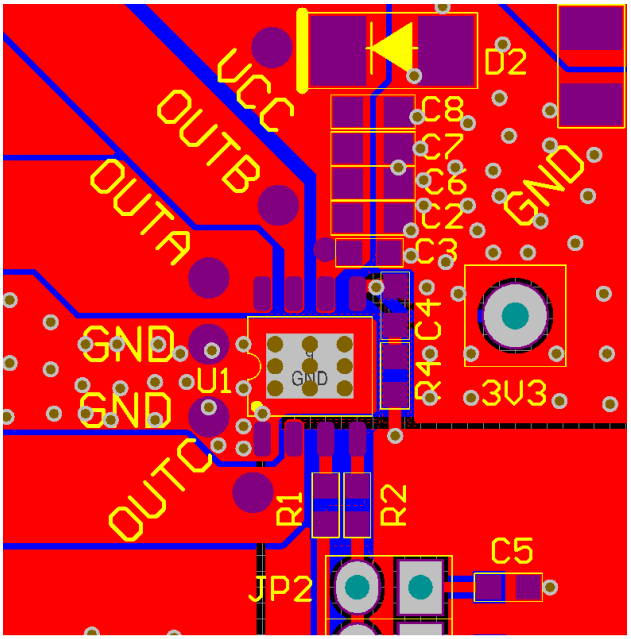
To get the phase resistance, measure the resistance between two phase terminals using a multimeter or LCR meter, then divide the value by 2.

To get the phase inductance, measure the inductance between two phase terminals via the LCR meter, then divide the value by 2. The LCR frequency and voltage setting are referenced to the 1kHz and 1V measurement from the LCR meter.

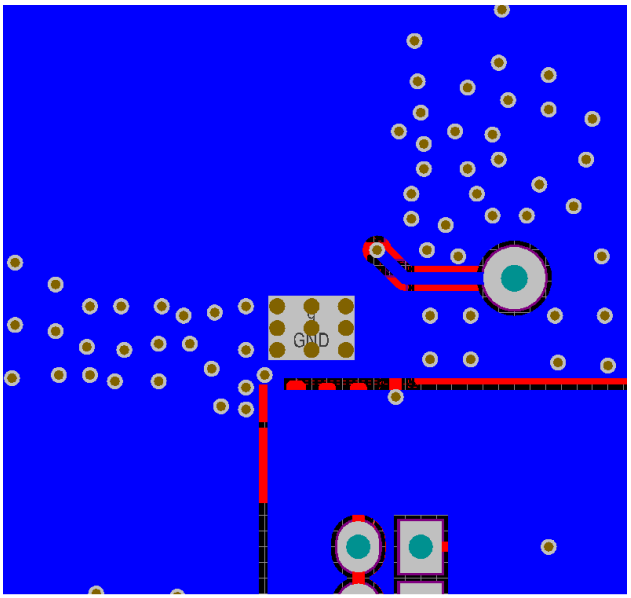
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 10 and follow the guidelines below:

1. Place the VCC bypass capacitors as close to the VCC and GND pins as possible. See the placement for the 100nF (C3) and 4.7μF X4 (C2, C6, C7, and C8) capacitors.
2. Place the 3.3V bypass capacitor as close to the 3.3V pin as possible. To minimize noise, use a 1μF (C4) capacitor in series with a 10Ω (R4) resistor. Ensure that the ground of the 3.3V bypass circuit's return path is separated from the power ground plane and connected with a single point at the GND pin.
3. A 2-layer PCB layout is strongly recommended.
4. Place multiple vias on the bottom of the exposed pad to reduce thermal resistance and noise caused by switching.



Top Layer



Bottom Layer

Figure 10: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

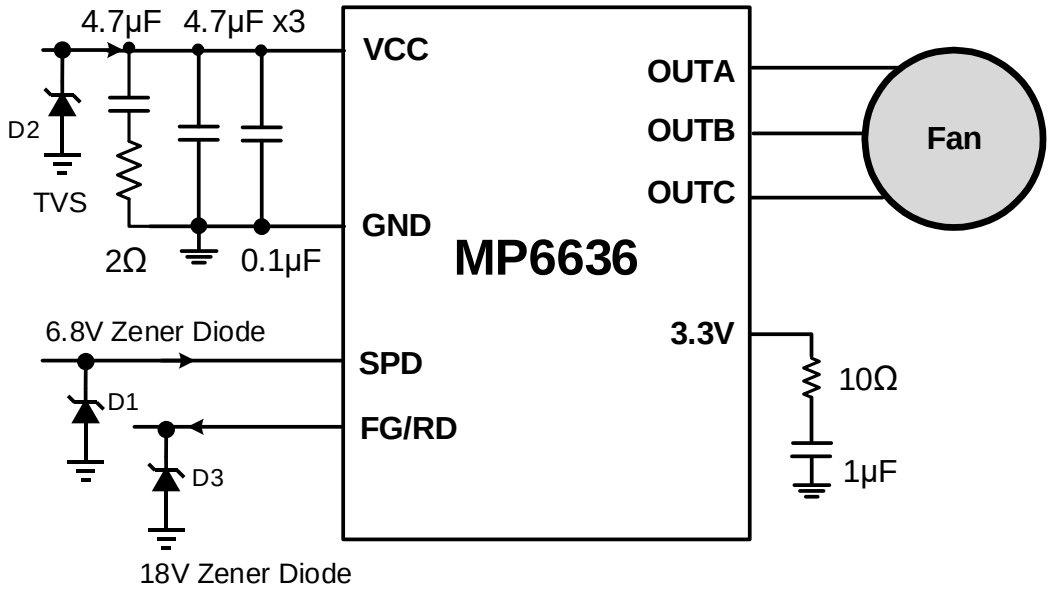

Figure 11: Typical Application Circuit

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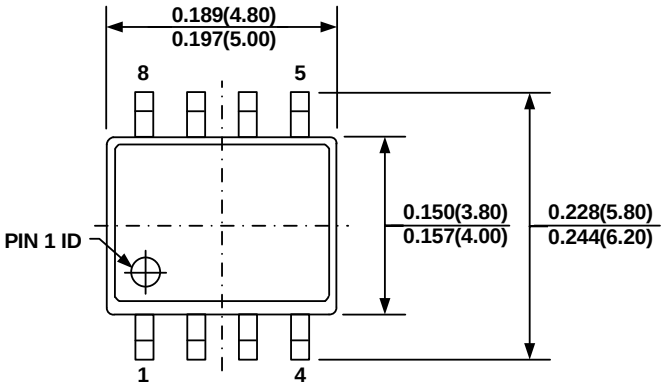
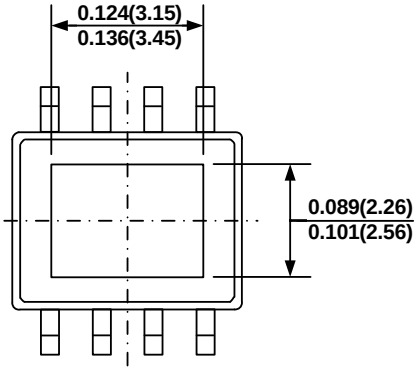
PACKAGE INFORMATION

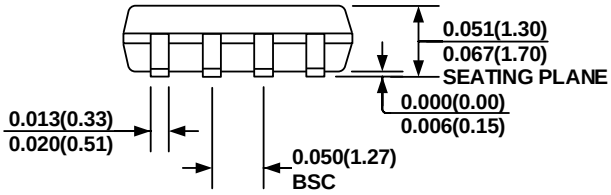
SOIC-8EP



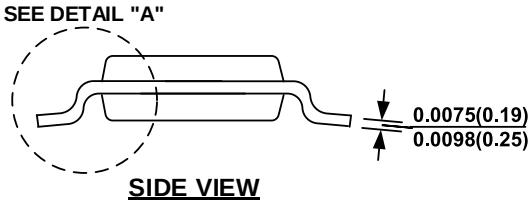
TOP VIEW



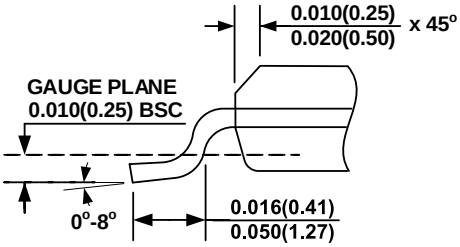
BOTTOM VIEW



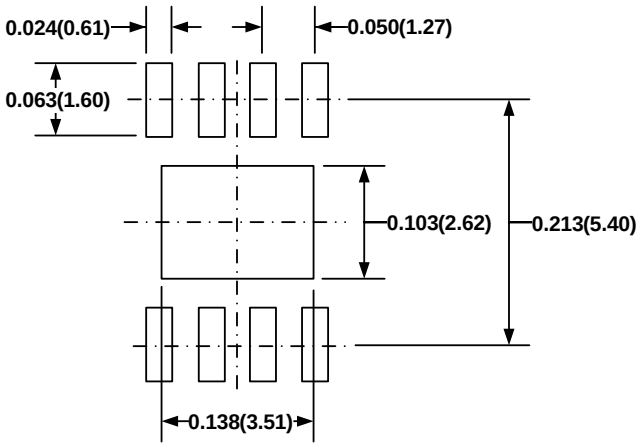
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.

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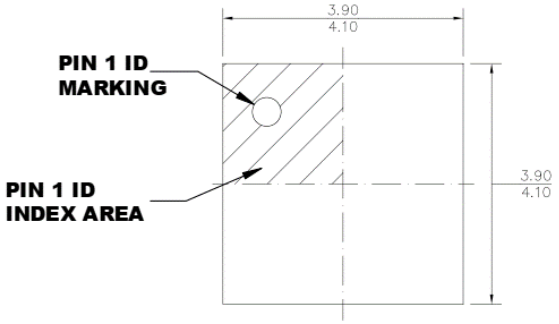
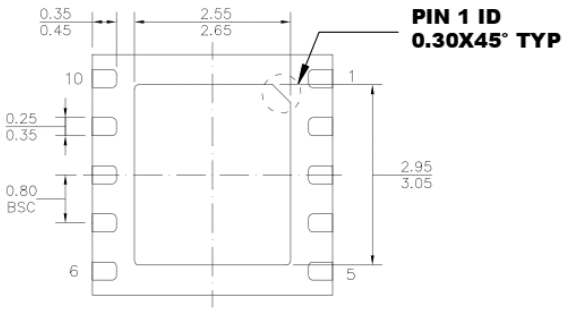
PACKAGE INFORMATION

TQFN-10 (4mmx4mm)

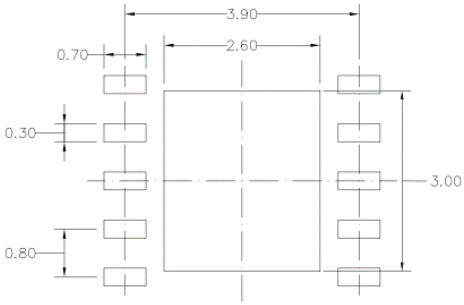


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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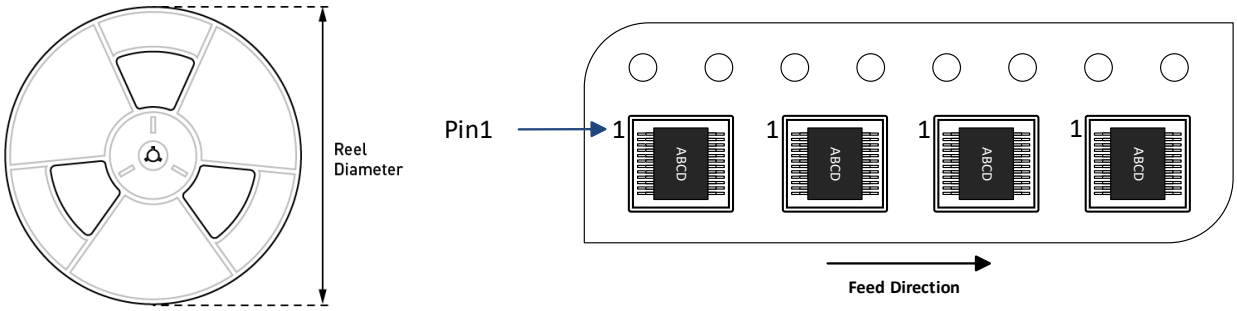
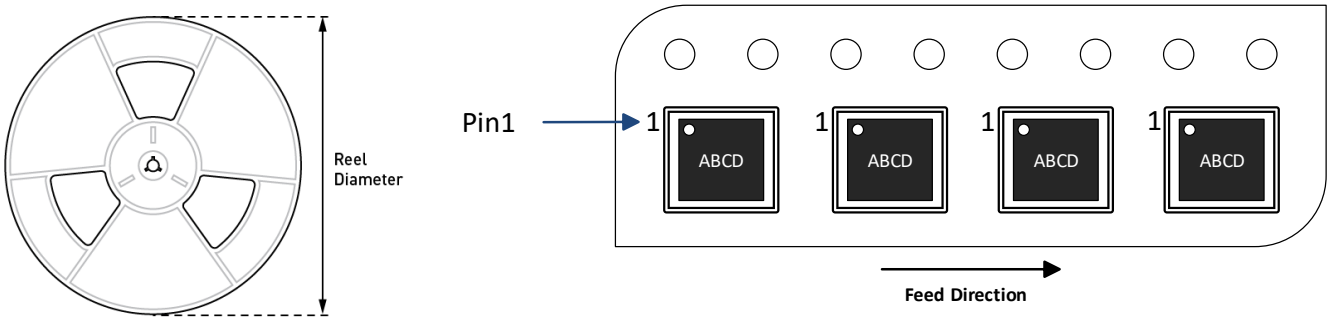
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6636GN-xxxx-Z	SOIC-8EP	2500	100	N/A	13in	12mm	8mm



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6636GRT-xxxx-Z	TQFN-10 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/28/2025	Initial Release	-

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