



MP6631A

35V Input, 3A Peak Phase Current, Three-Phase BLDC Motor Driver with Closed-Loop Control

DESCRIPTION

The MP6631A is a three-phase brushless DC (BLDC) motor driver with integrated power MOSFETs. The device supports a single external Hall-effect sensor or triple external Hall-effect sensors to drive a three-phase BLDC motor, with up to 3A of peak phase current and a 3.6V to 35V input voltage (V_{IN}) range.

The MP6631A controls the motor speed through the pulse-width modulation (PWM) signal or the DC signal on the PWM/DC pin with closed-/open-loop control. The device features a built-in, configurable speed curve function. It also features a sinusoidal drive for maximum torque, as well as low speed ripple and noise across the full speed range.

The MP6631A provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the Hall comparator's output. Direction control is achieved via the DIR pin's input.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

The MP6631A is available in a QFN-26 (3mmx4mm) package.

FEATURES

- 3.6V to 35V Operating Input Voltage (V_{IN}) Range
- Up to 3A of Peak Phase Current
- Integrated 160m Ω High-Side MOSFETs (HS-FETs) and Low-Side MOSFETs (LS-FETs)
- Sinusoidal Drive
- Supports 0V to 1.2V DC Input or 1kHz to 100kHz Pulse-Width Modulation (PWM) Input
- Supports Triple-Hall or Single-Hall Element Differential Input
- Closed-/Open-Loop Speed Control
- Direction/Brake Input
- Power-Save Mode
- 0.5s/4.5s Lock Protection
- Over-Current Protection (OCP)
- Single-Pulse or Triple-Pulse FG Output per Electrical Cycle
- FG Signal: Rotational Speed Indication
- Soft Start (SS) for Low Noise and Current Overshoot
- Available in a QFN-26 (3mmx4mm) Package

APPLICATIONS

- Fans
- General Three-Phase Brushless DC (BLDC) Motors
- Pumps

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TYPICAL APPLICATION

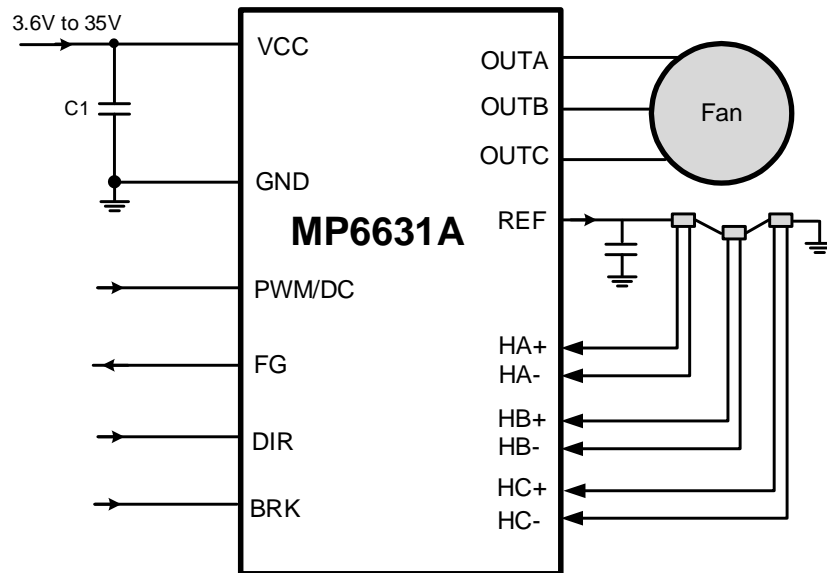


Figure 1: Typical Application (Triple Hall-Effect Sensor)

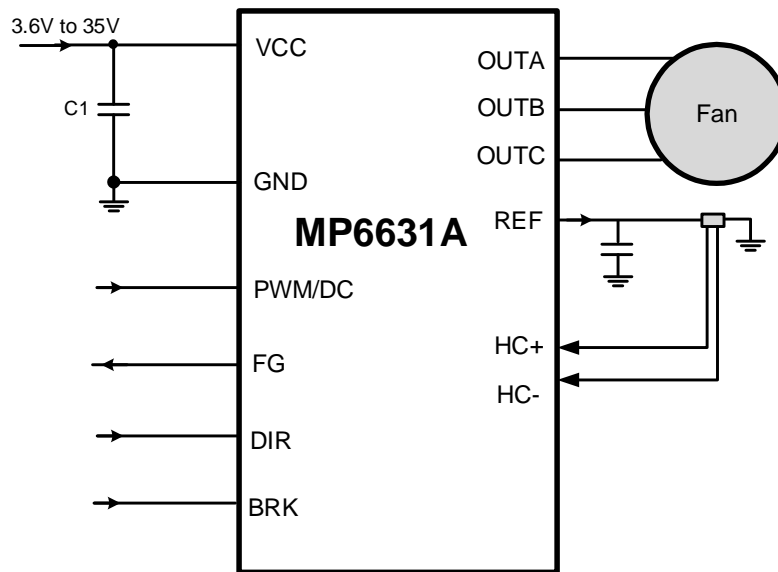


Figure 2: Typical Application (Single Hall-Effect Sensor)

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Level
MP6631AGL-xxxx**	QFN-26 (3mmx4mm)	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MP6631AGL-xxxx-Z).

** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for a non-default function option. “0000” is the default function value.

TOP MARKING

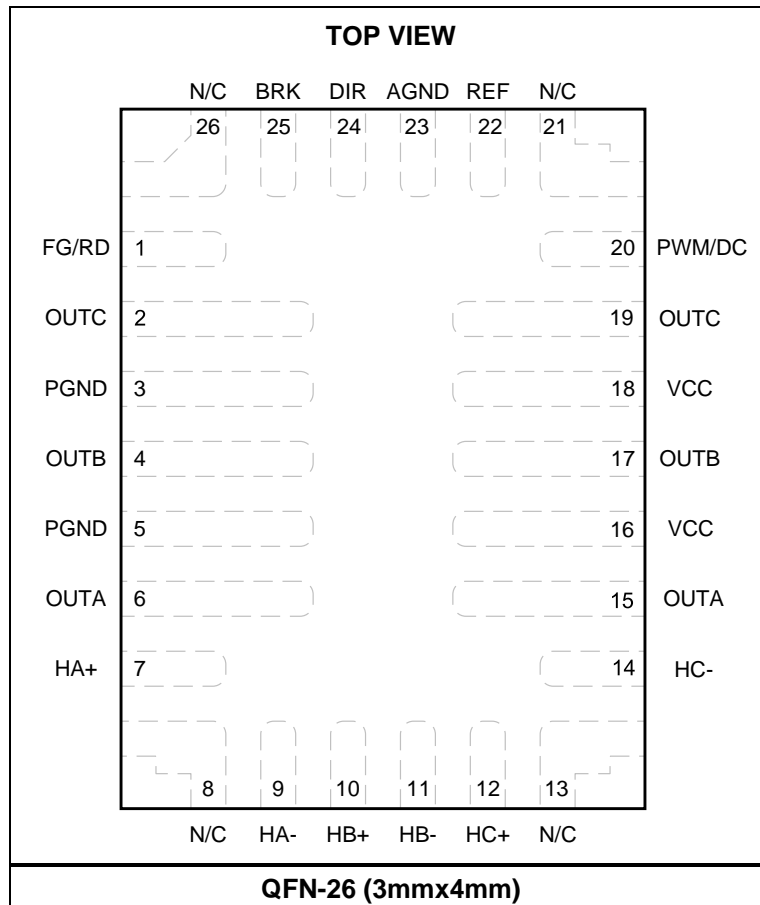
MPYW

6631

ALLL

MP: MPS prefix
 Y: Year code
 W: Week code
 6631A: Part number
 LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	FG/RD	Speed or rotor lock indication. Open-drain output. FG/RD can be used for speed indication (FG) or rotor lock indication (RD). Pull this pin up externally.
2, 19	OUTC	Phase C terminal.
3, 5	PGND	Power ground.
4, 17	OUTB	Phase B terminal.
6, 15	OUTA	Phase A terminal.
7	HA+	Phase A positive Hall input terminal.
9	HA-	Phase A negative Hall input terminal.
10	HB+	Phase B positive Hall input terminal.
11	HB-	Phase B negative Hall input terminal.
12	HC+	Phase C positive Hall input terminal.
14	HC-	Phase C negative Hall input terminal.
16, 18	VCC	Input voltage supply pin. The VCC pin must be locally bypassed.
20	PWM/DC	Rotational speed control input. Pull the PWM/DC pin high internally using a 500kΩ resistor. When DC_PWM = 0, apply a 1kHz to 100kHz pulse-width modulation (PWM) signal for speed control. When DC_PWM = 1, apply a 0V to 1.2V DC voltage for speed control.
22	REF	5V LDO output. The REF pin must be locally bypassed.
23	AGND	Analog ground.
24	DIR	Direction control pin. Pull the DIR pin low for forward rotation (A → B → C); pull it high for reverse rotation (A → C → B). Pull DIR down internally using a resistor.
25	BRK	Brake pin. Pull the BRK pin high to brake the motor. Pull BRK down internally using a resistor.
8, 13, 21, 26	NC	Not connected.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V _{CC}	-0.3V to +38V
OUTA, OUTB, OUTC	-0.3V to V _{CC} + 0.3V
All other pins	-0.3V to +5.8V
Lead temperature	260°C
Continuous power dissipation (T _A = 25°C) ⁽²⁾	2.6W
Junction temperature (T _J)	150°C
Storage temperature	-60°C to +150°C

ESD Ratings

Human body model (HBM)	2kV
Charged-device model (CDM)	2kV

Recommended Operating Conditions ⁽³⁾

Supply voltage (V _{CC})	3.6V to 35V
Operating junction temp (T _J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-26 (3mmx4mm)	48	11... °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. ⁽⁵⁾

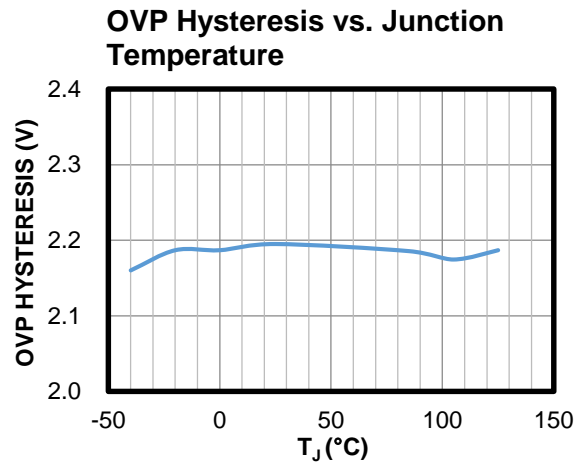
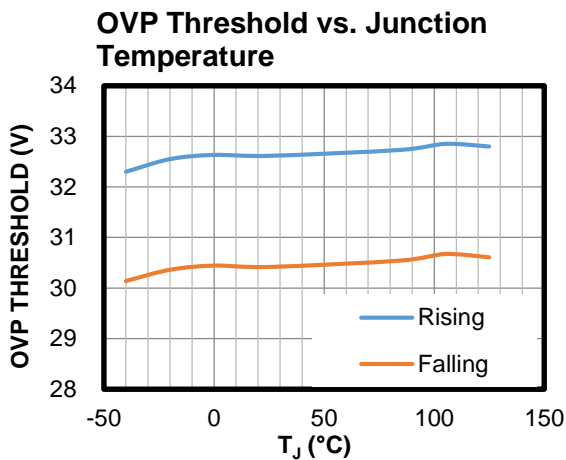
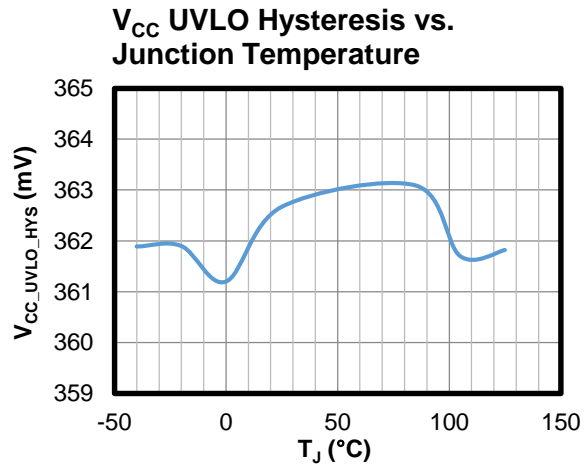
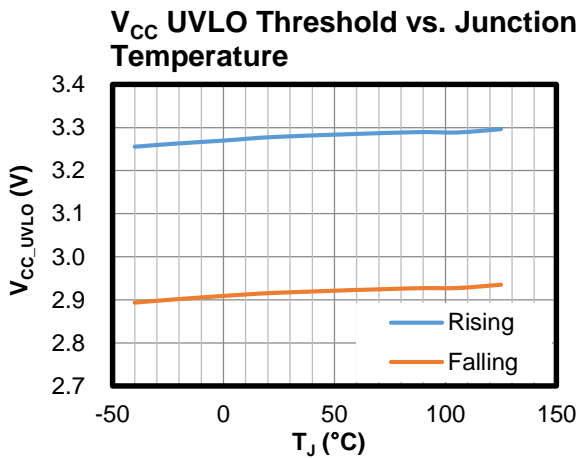
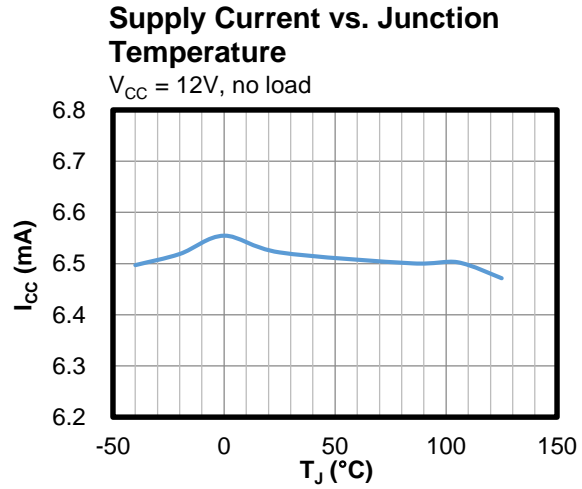
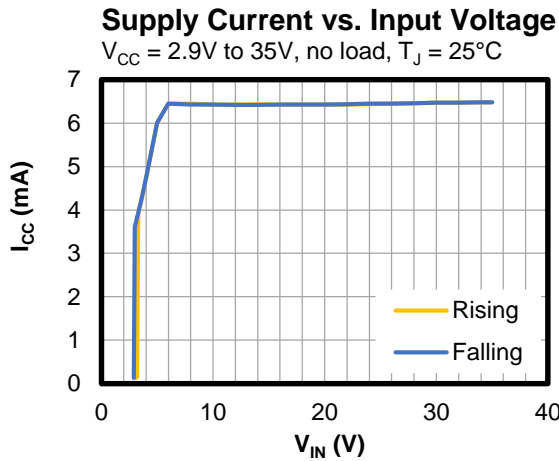
Parameter	Symbol	Condition	Min	Typ	Max	Units
VCC voltage (V_{CC}) under-voltage lockout (UVLO) rising threshold	$V_{CC_UVLO_RISING}$		3	3.3	3.5	V
Input UVLO hysteresis	V_{UVLO_HYS}			360		mV
Operating supply current	I_{CC}			6.7		mA
Standby current	$I_{STANDBY}$			130		μA
DIR input high voltage	V_{DIR_H}		1.5			V
DIR input low voltage	V_{DIR_L}				0.4	V
BRK input high voltage	V_{BRK_H}		1.5			V
BRK input low voltage	V_{BRK_L}				0.4	V
Pulse-width modulation (PWM) input high voltage	V_{PWM_H}	DC_PWM = 0	1.5			V
PWM input low voltage	V_{PWM_L}	DC_PWM = 0			0.4	V
PWM pull-up resistance	R_{PWM}	DC_PWM = 0		500		k Ω
DC input high voltage	V_{DC_H}	DC_PWM = 1	1.08	1.2	1.32	V
DC input low voltage	V_{DC_L}	DC_PWM = 1		0		V
REF output voltage	V_{REF}			5.24		V
REF load regulation	I_{REF_LO}	$I_{REF} = 30mA$		5.2		V
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	$I_{OUT} = 100mA$		85		m Ω
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	$I_{OUT} = 100mA$		75		m Ω
Over-current protection (OCP) threshold	I_{OCP}	OCP_SEL = 11, $T_J = 25^{\circ}C$	2.7	3		A
Switching frequency	f_{SW}	$T_J = 25^{\circ}C$	24.5	25	25.8	kHz
FG output low-level voltage	V_{FG_L}	$I_{FG/RD} = 3mA$		0.2	0.4	V
Locked-rotor detection time	t_{RD}			0.5		s
Zero-current detection (ZCD) threshold	I_{ZCD}			5		mA
Hall input common-mode low voltage	V_{HCM_LO}			1		V
Hall input common-mode high voltage	V_{HCM_HI}			4.5		V
Hall input voltage, differential mode	V_{HDM}	$V_{HCM} = 1V$ to $4.5V$		30		mV
Thermal shutdown threshold ⁽⁵⁾				160		$^{\circ}C$
Thermal shutdown hysteresis ⁽⁵⁾				25		$^{\circ}C$

Notes:

5) Guaranteed by design.

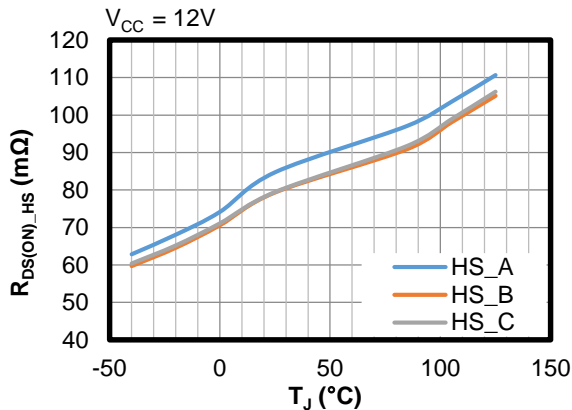
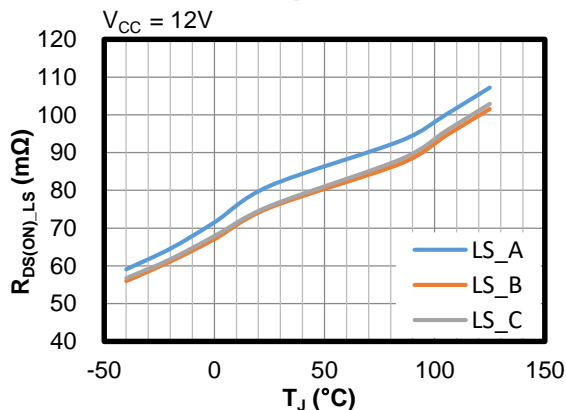
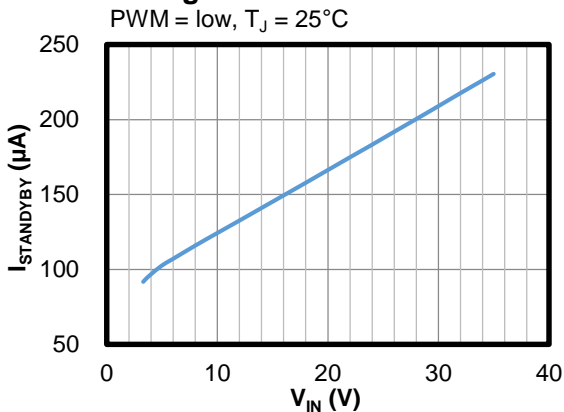
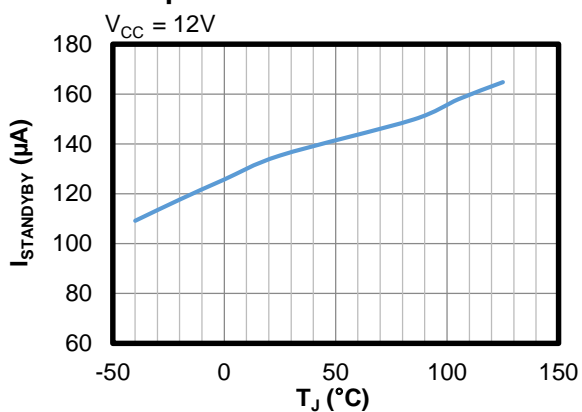
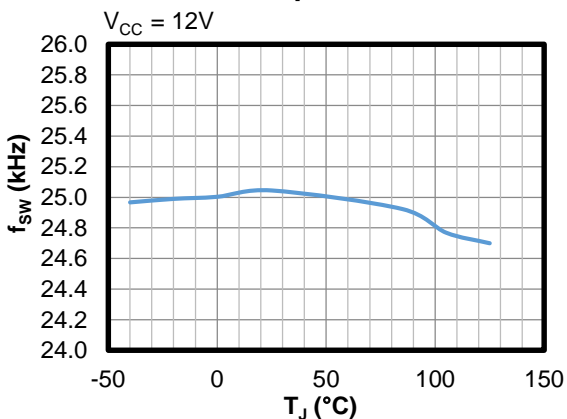
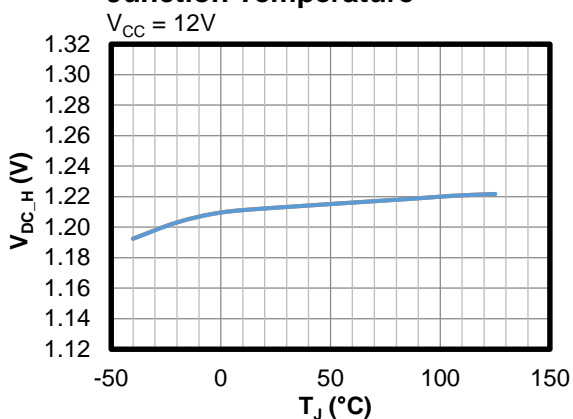
TYPICAL CHARACTERISTICS

$V_{CC} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.



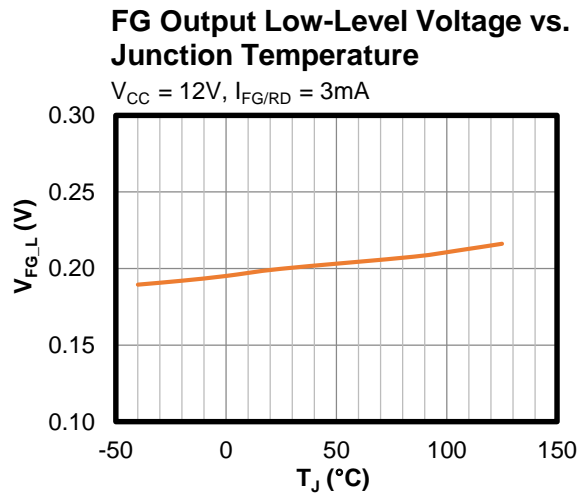
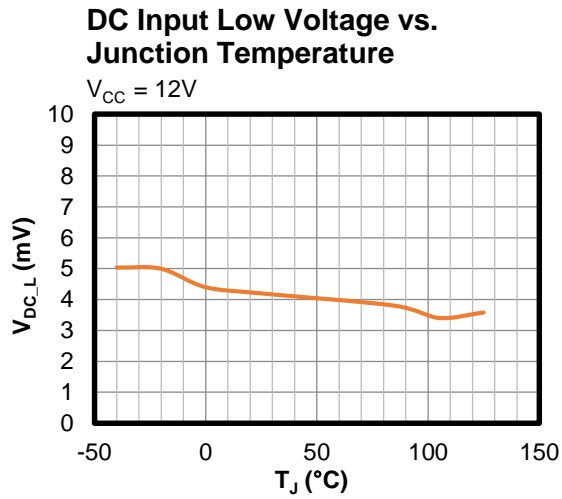
TYPICAL CHARACTERISTICS (*continued*)

 V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

HS-FET On Resistance vs. Junction Temperature

LS-FET On Resistance vs. Junction Temperature

Standby Current vs. Input Voltage

Standby Current vs. Junction Temperature

PWM Output Frequency vs. Junction Temperature

DC Input High Voltage vs. Junction Temperature


TYPICAL CHARACTERISTICS (continued)

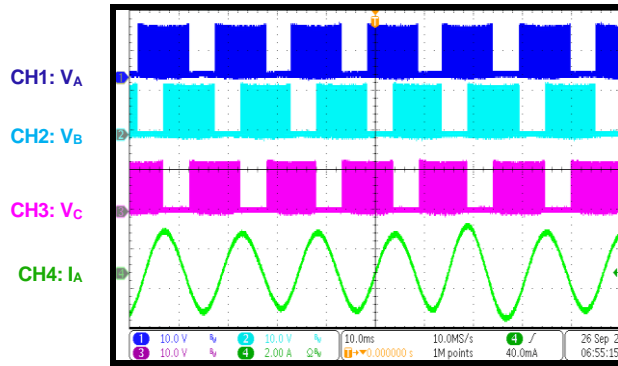
$V_{CC} = 12V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted.



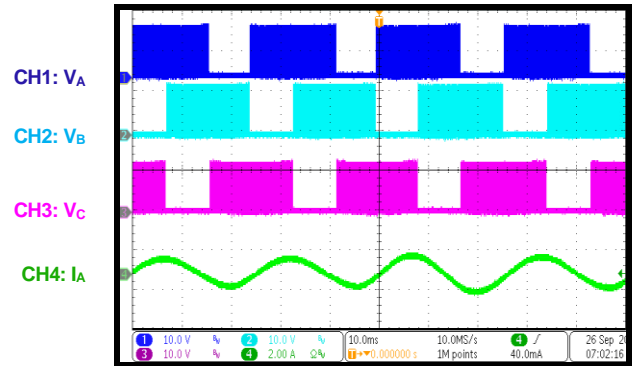
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, PWM input frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

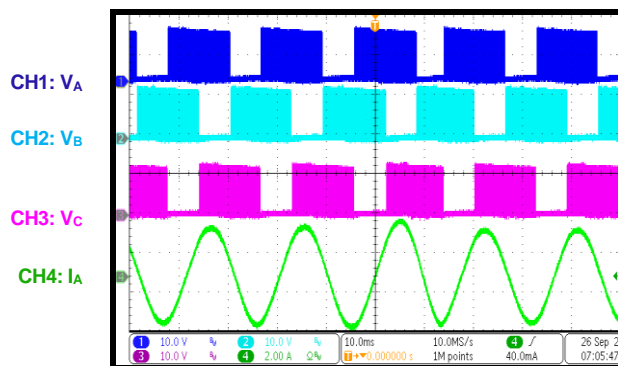
Steady State
PWM duty = 100%, DIR = low, counterclockwise



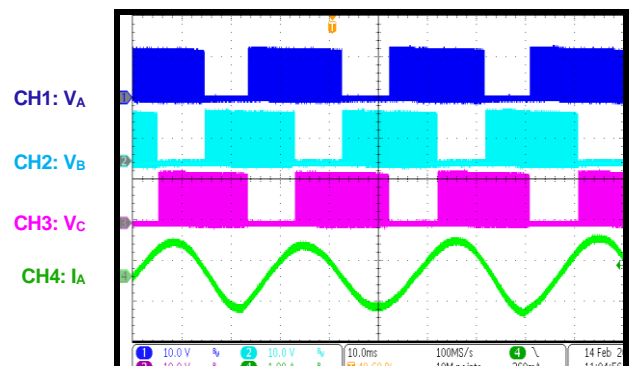
Steady State
PWM duty = 50%, DIR = low, counterclockwise



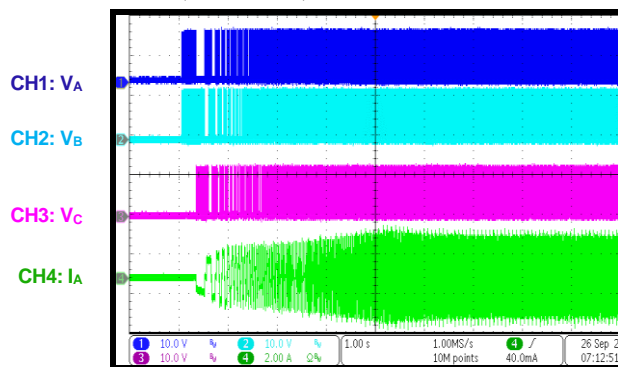
Steady State
PWM duty = 100%, DIR = high, clockwise



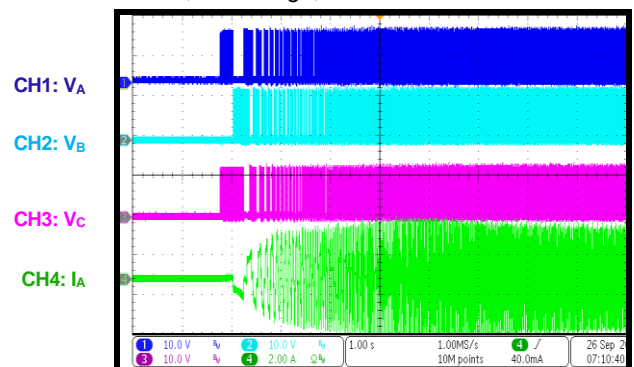
Steady State
PWM duty = 50%, DIR = high, clockwise



PWM On
PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = low, counterclockwise



PWM On
PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = high, clockwise

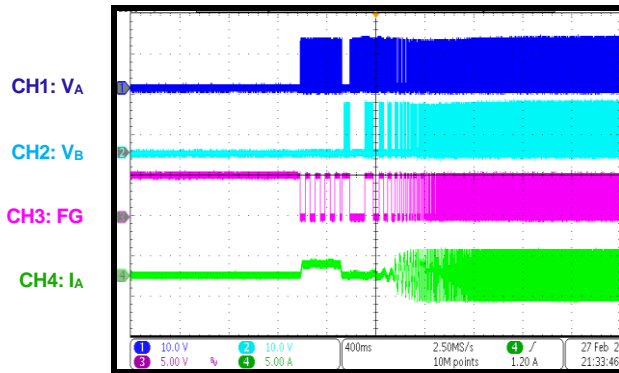


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, PWM input frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

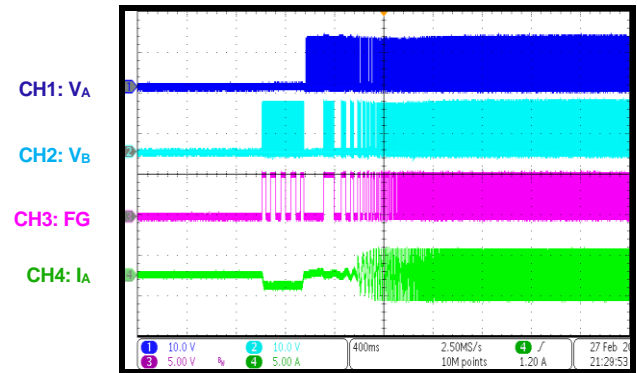
PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = low, counterclockwise



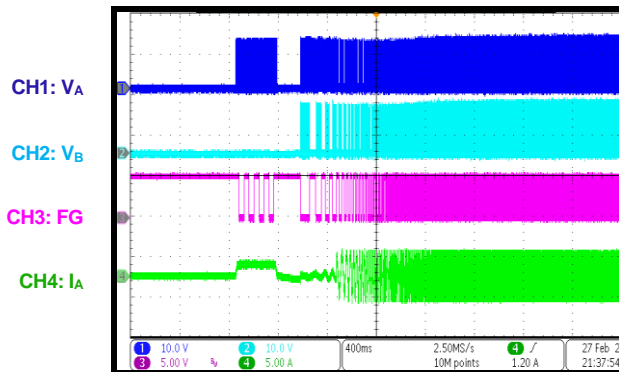
PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = low, counterclockwise



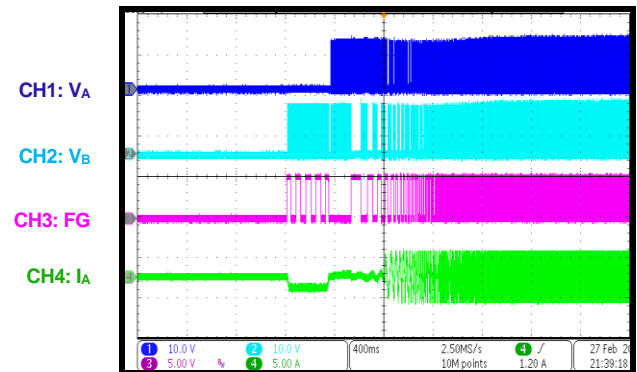
PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = high, clockwise



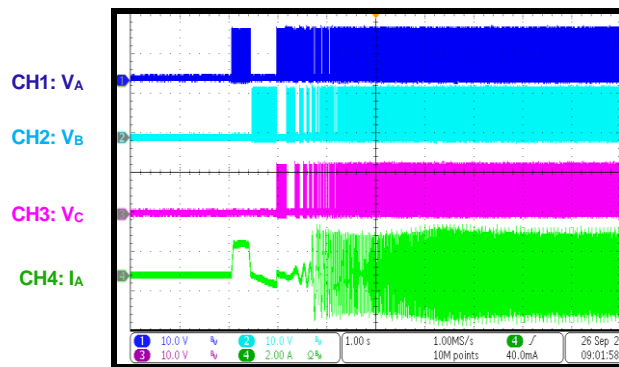
PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = high, clockwise



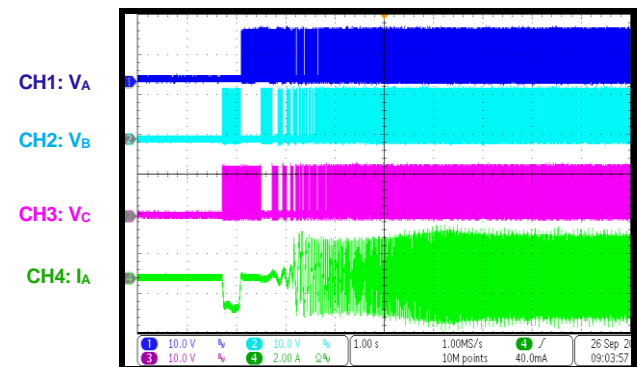
PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = low, counterclockwise



PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = low, counterclockwise

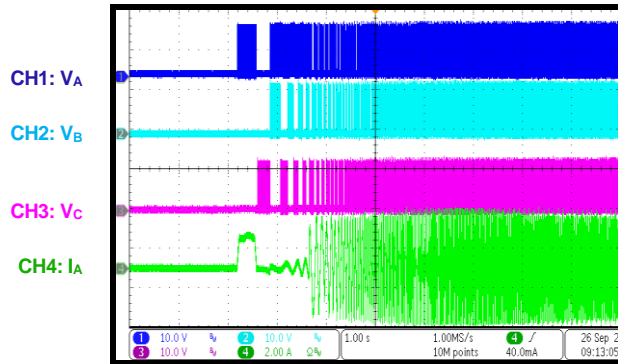


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, PWM input frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

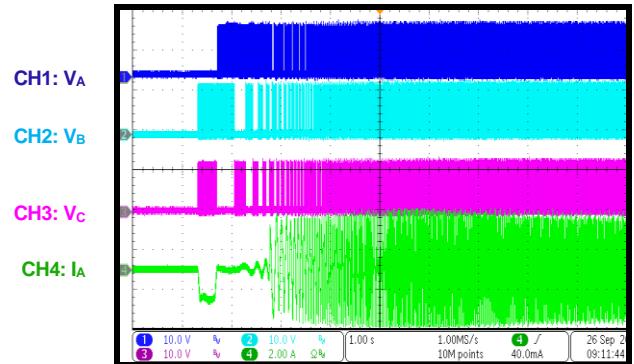
PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = high, clockwise



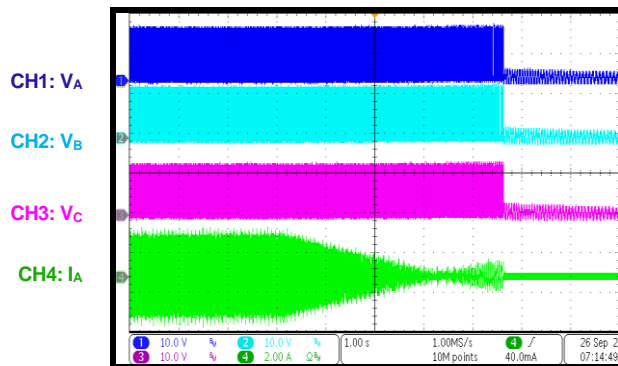
PWM On

PWM duty = 0% to 100%, single Hall-effect sensor, DIR = high, clockwise



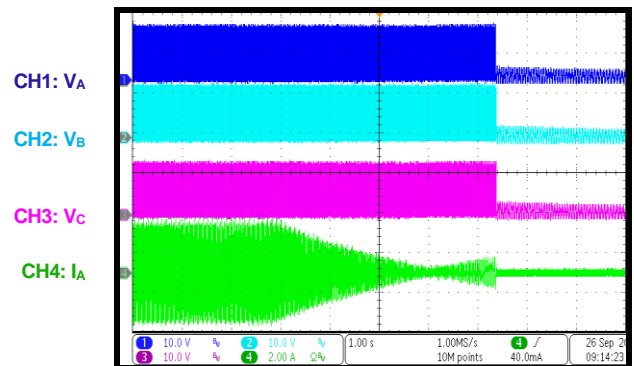
PWM Off

PWM duty = 100% to 0%, DIR = low, counterclockwise



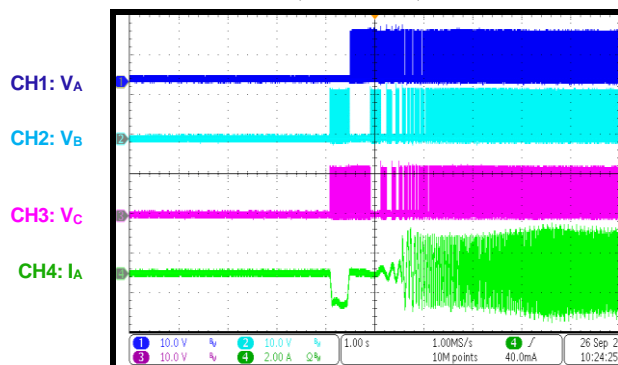
PWM Off

PWM duty = 100% to 0%, DIR = high, clockwise



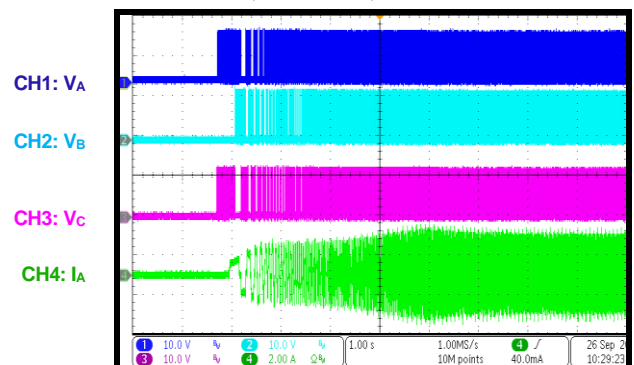
Start-Up through VCC

$V_{CC} = 0V$ to 12V, PWM duty = 100%, single Hall-effect sensor, DIR = low, counterclockwise



Start-Up through VCC

$V_{CC} = 0V$ to 12V, PWM duty = 100%, triple Hall-effect sensor, DIR = low, counterclockwise

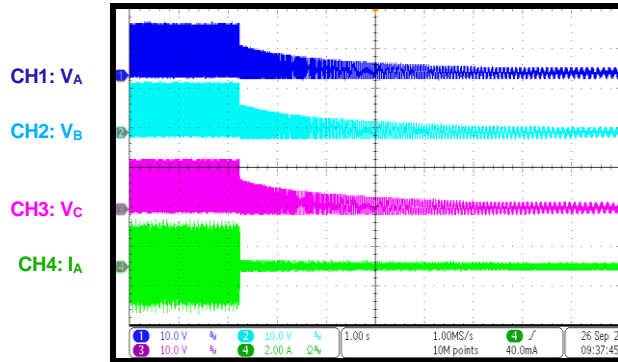


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. $V_{IN} = 12V$, PWM input frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

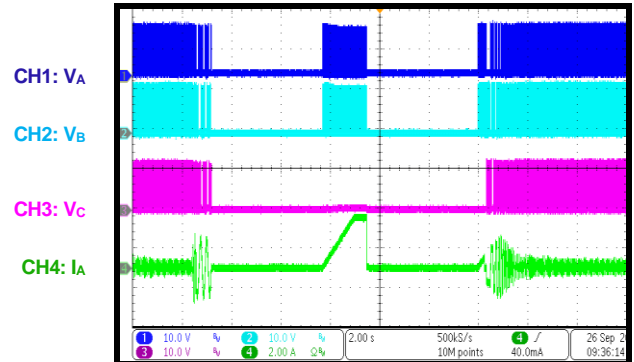
Shutdown through VCC

$V_{CC} = 0V$ to 12V, PWM duty = 100%, DIR = low, counterclockwise



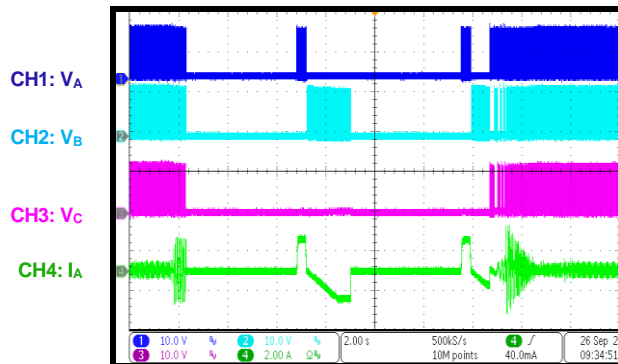
Rotor Lock and Retry

PWM duty = 25%, triple Hall-effect sensor, lock rotor then release



Rotor Lock and Retry

PWM duty = 25%, single Hall-effect sensor, lock rotor then release



FUNCTIONAL BLOCK DIAGRAM

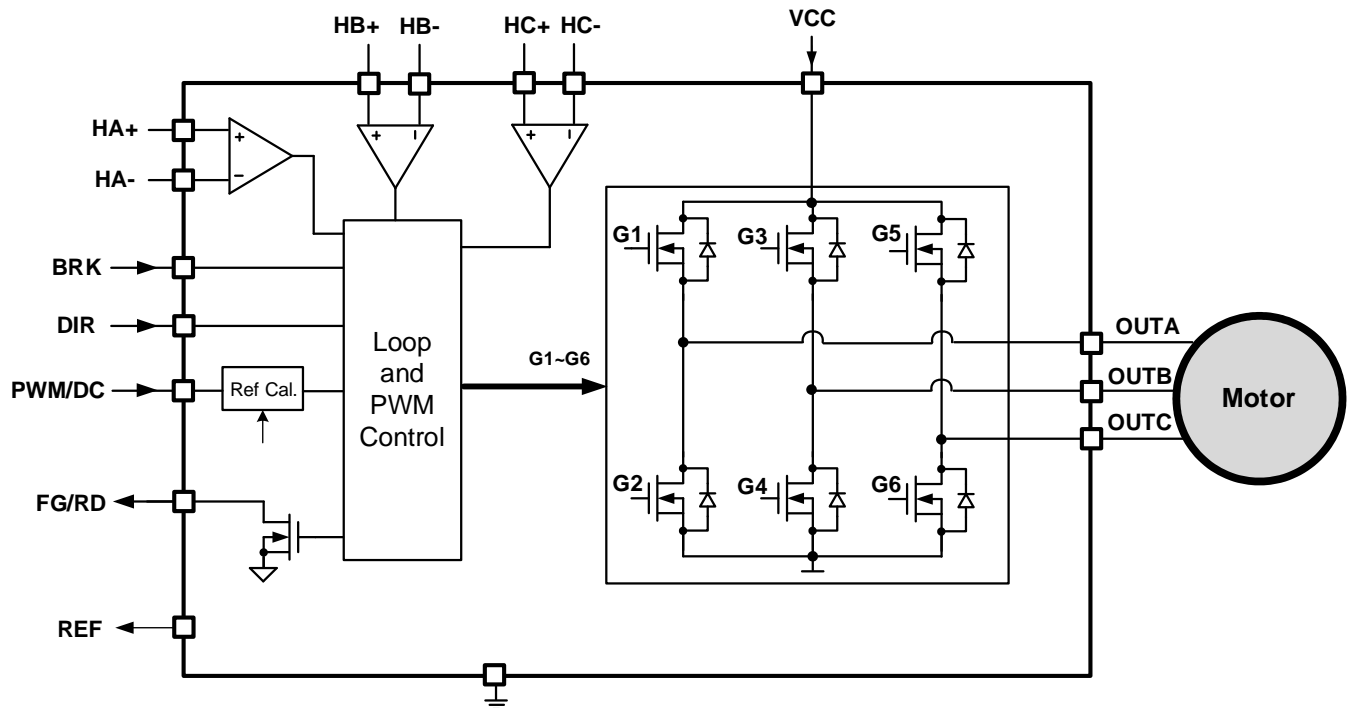


Figure 3: Functional Block Diagram

OPERATION

The MP6631A is a three-phase brushless DC (BLDC) motor driver with integrated power MOSFETs. The MP6631A controls the motor speed via the pulse-width modulation (PWM) signal or the DC voltage on the PWM/DC pin, with closed/open-loop speed control and a built-in, configurable speed curve function.

The MP6631A also features a rotational speed detector. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the external Hall signal. Additionally, direction control is achieved via the DIR pin's input, and the BRK pin is used to brake the motor.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

A sinusoidal drive is employed in the MP6631A. Figure 4 shows the MP6631A's output drive, where HA, HB, and HC are the output of Hall A, Hall B, and Hall C, respectively. OUTA, OUTB, and OUTC are the output duty of the OUTA, OUTB, and OUTC pins, respectively.

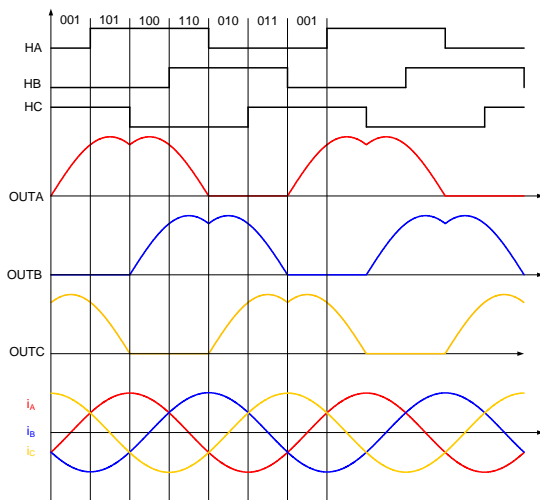


Figure 4: MP6631A Hall Output and Output Drive

Speed Control

The PWM/DC pin controls the motor speed in an open loop or closed loop via the PWM signal or the DC voltage. PWM/DC accepts a wide input frequency range (1kHz to 100kHz) or a 0V to 1.2V voltage.

If DC_PWM = 1, then the motor speed is controlled via the DC voltage on the PWM/DC pin.

If DC_PWM = 0, then the motor speed is controlled via the input PWM signal duty cycle.

Starting Duty and Minimum Speed

The starting duty is configured by the DIN_MIN bits. When PWM input duty is below the duty set by DIN_MIN, the fan speed supports two modes:

1. The speed maintains the minimum speed when SPD_ZERO is set to 0.
2. The speed is at 0 when SPD_ZERO is set to 1.

Speed Curve Configuration

The SPD_MAX registers configure the speed when the input duty is at 100%. Otherwise, the MP6631A provides a five-point curve configuration function where the output speed can be configured when the input duty is 37.5%, 50%, 62.5%, 75%, or 87.5%. Linear interpolation occurs between the adjacent duty cycles.

The DIN_MIN register sets the minimum input duty, and SPD_MIN sets the minimum output duty and minimum speed.

Figure 5 shows the curve configuration when SPD_ZERO = 1.

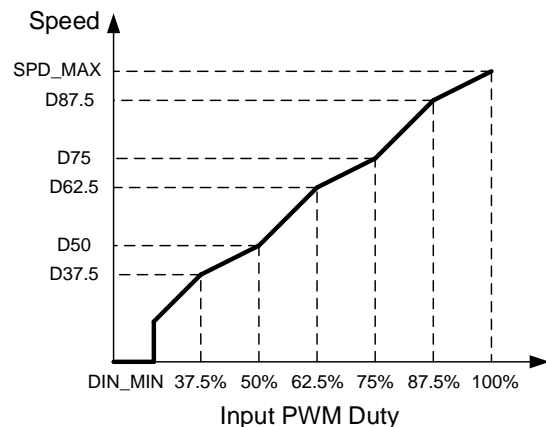


Figure 5: Curve Configuration when SPD_ZERO = 1

Figure 6 shows the curve configuration when `SPD_ZERO = 0`.

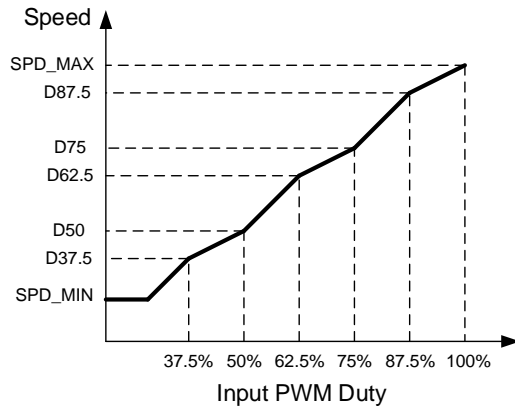


Figure 6: Curve Configuration when `SPD_ZERO = 0`

Speed Open-/Closed-Loop Control

In closed-loop mode (`OPEN_L = 0`, `CLOSE_H = 1`), the MP6631A internally detects the Hall signal speed and feedback to the control loop, which adjusts the output PWM duty in a closed loop. By doing this, the motor speed follows the reference exactly.

In open-loop mode (`OPEN_L = 1`), the OUT1 and OUT2 output duty cycles directly depend on the PWM input duty.

In mixed mode (`OPEN_L = 0`, `CLOSE_H = 0`), the MP6631A operates in closed-loop mode when the PWM input duty is below 87.5%, and operates in open-loop mode when the input duty exceeds 87.5%.

Soft-Start Time

To reduce the input inrush current during start-up, the MP6631A provides the reference speed's configurable soft-start time (t_{SS}) by setting register bits `TDYN[1:0]`. t_{SS} can be configured between 1.3s and 10.4s.

Closed-Loop Integrator Gain

In closed-loop mode, the closed-loop integrator gain depends on registers `KI[7:0]` and `KP[7:0]`.

Higher `KI` and `KP` values lead to quick loop response. `KI` and `KP` should be adjusted according to the dynamic response and steady state operation.

Single- or Triple-Hall Input Mode

The MP6631A supports either a single Hall-effect sensor or triple Hall-effect sensors. If a single Hall-effect sensor is employed, the Hall selecting bit must set the single Hall sensor, and Hall C is used as the control.

Direction Control

The direction is controlled by the DIR pin's polarity. When DIR is pulled low, the MP6631A operates in forward rotation in the following sequence: A → B → C → A...

When DIR is pulled high, the MP6631A operates in reverse rotation in the following sequence: A → C → B → A...

Alignment

At the beginning of start-up in single Hall-effect sensor applications, the MP6631A aligns the rotor in certain positions depending on the Hall outputs, and the FG pin outputs a 12Hz signal.

After the alignment time set by register `TPOS` completes, the MP6631A enters pre-startup. This function is only enabled in single Hall-effect sensor applications.

Pre-Startup Timer

During pre-startup, the MP6631A gradually increases the output duty cycle with the timer set by the `TPRE[1:0]` bits. This provides sufficient torque for robust start-up and avoids current overshoot during start-up.

- `TPRE = 0`: Timer period is 2.5ms
- `TPRE = 1`: Timer period is 5ms
- `TPRE = 2`: Timer period is 10ms
- `TPRE = 3`: Timer period is 20ms

A higher timer period leads to lower soft pre-startup current, but increases pre-startup time.

Over-Current Protection (OCP)

During normal switching, if the current flowing through the MOSFET exceeds the threshold set by register bits `OCP[1:0]` after a set blanking time, then the high-side MOSFETs (HS-FETs) turn off and the low-side MOSFETs (LS-FETs) turn on immediately. The MP6631A resumes normal switching during the next switching cycle.

Maximum Peak Current Limit

If the load current is not limited by OCP and the current exceeds the maximum peak current limit threshold (typically 6A), all MOSFETs turn off and the MP6631A tries to re-enable after a lock-retry time.

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall change signal for speed indication. Different FG signal frequencies are provided. The frequencies are selected by setting the FGRD bit to 00, 01, or 10.

FG/RD is an open-drain output, and must be pulled up externally by a resistor.

Locked-Rotor Protection

If the motor rotor is locked and the Hall signal edge is not detected during the 0.5s detection time, then the MP6631A turns on all LS-FETs and auto-restarts after the recovery time (4.5s). By setting the FGRD bit to 11, the signal on FG/RD is set to locked-rotor indication. During a locked-rotor fault status, FG/RD remains low.

Over-Voltage Protection (OVP)

If the voltage on the VCC pin (V_{CC}) exceeds the over-voltage protection (OVP) threshold (34V), then the HS-FETs turn off and the LS-FETs turn on. Once V_{CC} drops below 32V, the device resumes normal operation.

Thermal Shutdown

The MP6631A also provides thermal monitoring. If the MP6631A's die temperature exceeds 160°C, then the output duty decreases to reduce power consumption until the die temperature drops below 135°C.

Under-Voltage Lockout (UVLO)

If V_{CC} falls below the UVLO threshold, all circuitry in the device is disabled and the internal logic is reset. Once V_{CC} exceeds the UVLO threshold, the device resumes normal operation.

Test Mode and Factory Mode

To configure the internal registers, the MP6631A supports test mode. In test mode, all internal registers can be read/written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM), which can be configured twice. Refer to the MPS Fan Driver GUI Software for easy parameter changes and memory configuration.

REGISTER DESCRIPTION

Register Map

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPD_MAX[7:0]							
01h (OTP/REG)	SPD_MAX[15:8]							
02h (OTP/REG)	SPD_MIN[7:0]							
03h (OTP/REG)	HI_FREQ	RESERVED	DIN_MIN[5:0]					
04h (OTP/REG)	OVP_EN	WAIT_TM[1:0]		RESERVED	MAX_EN	CLOSE_H	OPEN_L	RESERVED
05h (OTP/REG)	RESERVED	TDYN[1:0]		TPRE[1:0]		SPD_ZERO	SINGLE	RESERVED
06h (OTP/REG)	RESERVED		DC_PWM	FGRD[1:0]		OCP[1:0]		TPOS
07h (OTP/REG)	RESERVED	SW_SEL	THETA_COMP[5:0]					
08h (OTP/REG)	KI[7:0]							
09h (OTP/REG)	KP[7:0]							
0Ah (OTP/REG)	RESERVED		WAIT_SEL	RESERVED		OCP_EN	OCP_BH	OVP_BH
0Bh (OTP/REG)	D37.5							
0Ch (OTP/REG)	D50							
0Dh (OTP/REG)	D62.5							
0Eh (OTP/REG)	D75							
0Fh (OTP/REG)	D87.5							
10h (REG)	RESERVED		OTP_PAGE[1:0]		RESERVED			DEBUG

MAX_SPEED_1 (00h)

The MAX_SPEED_1 command sets the maximum speed in closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MAX[7:0]	0xFF	Sets the maximum speed when the input duty is 100%. 8-bit least significant bit (LSB). Electrical speed = 7.5rpm / LSB

MAX_SPEED_2 (01h)

The MAX_SPEED_2 command sets the maximum speed in closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MAX[15:8]	0x08	Sets the maximum speed when the input duty is 100%. 8-bit most significant bit (MSB). Combined with SPD_MAX[7:0] to set the maximum speed (electrical speed).

MIN_SPEED (02h)

The MIN_SPEED command sets the minimum speed in closed-loop speed control or the minimum output duty in open-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	SPD_MIN[7:0]	0x20	Sets the minimum speed or minimum output duty. In closed-loop mode, this bit sets the minimum speed (electrical speed), depending on the HI_FREQ, where: HI_FREQ = 0, the minimum speed = 60rpm / LSB HI_FREQ = 1, the minimum speed = 480rpm / LSB In open-loop mode, this bit sets the minimum output duty, where the minimum output duty = SPD_MIN[7:0] / 255, and the default is 12.5%.

CFR_1 (03h)

The CFR_1 command refers to the control function register and sets the switching frequency (f_{sw}) and starting duty.

Bits	Access	Bit Name	Default	Description
7	R/W	HI_FREQ	0	Selects the high frequency. 0: High frequency is not selected (default) 1: High frequency is selected The SW bit must be set to 1 if HI_FREQ = 1.
6	R	RESERVED	-	Reserved.
5:0	R/W	DIN_MIN[5:0]	0x10	Sets the starting duty, where the starting duty = DIN_MIN / 128, and the default is 12.5%.

CFR_2 (04h)

The CFR_2 command enables over-voltage protection (OVP), and sets the wait status, maximum speed below starting duty, and open-loop/closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_EN	0	Enables OVP. 0: Disabled (default) 1: Enabled

6:5	R/W	WAIT_TM[1:0]	00	<p>Selects the waiting time or speed threshold at start-up. Combined with WAIT_SEL, these bits can select the fixed time that the IC waits before output switching or the motor speed threshold at which the IC starts driving the motor.</p> <p>The waiting time or speed threshold can be selected as follows:</p> <p>If WAIT_SEL = 1, wait for a fixed time. The time setting is WAIT_TM = 00: 1.2s, 01: 1.8s, 10: 3s, 11: 4.2s.</p> <p>If WAIT_SEL = 0, wait for the motor speed to drop to a certain speed, where WAIT_TM = 00: 1000rpm (electrical speed), 01: 600rpm, 10: 150rpm, 11: 60rpm.</p> <p>This is active for triple Hall-effect sensor applications.</p>
4	R	RESERVED	-	Reserved.
3	R/W	MAX_EN	0	<p>Enables the maximum speed when the pulse-width modulation (PWM) input duty < DIN_MIN.</p> <p>0: Disabled (default) 1: Maximum output speed or maximum output duty when PWM input duty < DIN_MIN</p> <p>This is active only when SPD_ZERO = 0.</p>
2	R/W	CLOSE_H	0	<p>Enables closed-loop speed control when the PWM input duty > 87.5%.</p> <p>0: Open-loop speed control when the PWM input duty > 87.5% (default) 1: Closed-loop speed control when the PWM input duty > 87.5%</p>
1	R/W	OPEN_L	1	<p>Enables open-loop speed control.</p> <p>0: Closed-loop speed control when the PWM input duty < 87.5% 1: Open-loop speed control (default)</p>
0	R	RESERVED	-	Reserved.

START_HALL (05h)

The START_HALL command sets the start-up, Hall-effect sensor, and dynamic operation.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	-	Reserved.
6:5	R/W	TDYN[1:0]	00	<p>Sets the soft dynamic time. The output duty reference time ranges from 0% to 100%.</p> <p>00: 1.3s (default) 01: 2.6s 10: 5.2s 11: 10.4s</p>
4:3	R/W	TPRE[1:0]	10	<p>Pre-startup time bits. The output duty's time duration increases by 1 step.</p> <p>00: 2.5ms 01: 5ms 10: 10ms (default) 11: 20ms</p>
2	R/W	SPD_ZERO	1	<p>Enables zero speed.</p> <p>0: Maintains the minimum speed when the PWM input duty < DIN_MIN 1: Stops when the PWM input duty < DIN_MIN</p>
1	R/W	SINGLE	1	<p>Selects the number of Hall-effect sensors.</p> <p>0: Triple Hall-effect sensor application 1: Single Hall-effect sensor application (default)</p>

0	R	RESERVED	-	Reserved.
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CFR_3 (06h)

The CFR_3 command sets the pulse-width modulation (PWM) input, FG/RD output, over-current protection (OCP) threshold, and alignment time.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	-	Reserved.
5	R/W	DC_PWM	0	Selects the DC input or PWM input for the PWM/DC pin. 0: PWM input (default) 1: DC input
4:3	R/W	FGRD[1:0]	00	Selects the FG/RD pin output. 00: 1x (default) 01: 1/2x 10: 1/4x for single Hall-effect sensor applications, 3x for triple Hall-effect sensor applications 11: RD
2:1	R/W	OCP[1:0]	11	Sets the OCP threshold. 00: 0.7A 01: 1.5A 10: 2.2A 11: 3A (default)
0	R/W	TPOS	0	Sets the alignment time. 0: 320ms (default) 1: 650ms

PWM_SW_COMP (07h)

The PWM_SW_COMP command sets f_{sw} and the compensation angle.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	-	Reserved.
6	R/W	SW_SEL	0	Selects the output f_{sw} . 0: 25kHz (default) 1: 50kHz
5:0	R/W	THETA_COMP [5:0]	0x00	Sets the leading/lag compensation angle. 0x00: Auto compensation The non-zero value sets the fixed leading/lag angle compensation. The MSB is the signed bit. MSB = 0: Leading MSB = 1: Lag Leading compensation angle = $THETA_COMP[5:0] \times 15 / 8^\circ + 0.94^\circ$ Lag compensation angle = $119.06^\circ - THETA_COMP[5:0] \times 15 / 8^\circ$

KI (08h)

The KI command configures the integral parameter for closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KI[7:0]	0x01	Sets the integral parameter for closed-loop speed control.

KP (09h)

The KP command configures the gain parameter during closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	R/W	KP[7:0]	0x01	Sets the gain during closed-loop speed control.

CFR_4 (0Ah)

The CFR_4 command sets the wait configuration, enables OCP, and selects the OCP and over-voltage protection (OVP) response.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	-	Reserved.
5	R/W	WAIT_SEL	0	Selects the waiting function at start-up. 0: The IC does not output a drive signal until the speed drops below the threshold during start-up (default) 1: The IC does not output a drive signal for a fixed time during start-up
4:3	R	RESERVED	-	Reserved.
2	R/W	OCP	0	Enables OCP. 0: Enabled 1: Disabled
1	R/W	OCP_BH	0	Selects the OCP response. 0: Turns on the LS-FETs and resumes switching during the next switching cycle (default) 1: Decreases the output duty
0	R/W	OVP_BH	0	Selects the OVP response. 0: Turns on the LS-FETs when OVP is triggered 1: Turns off all the MOSFETs

SPEED_CURVE_1 (0Bh)

The SPEED_CURVE_1 command configures the output duty or speed when the input PWM duty cycle is at 37.5%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D37.5[7:0]	0x60	Sets the output duty or speed when the input PWM duty = 37.5%. For open-loop control, set the output duty when the input PWM duty = 37.5%. Output duty = D37.5[7:0] / 256. For closed-loop control, set the reference speed when the input PWM duty = 37.5%. Speed = D37.5[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_2 (0Ch)

The SPEED_CURVE_2 command configures the output duty or speed when the input PWM duty cycle is at 50%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D50[7:0]	0x80	Sets the output duty or speed when the input PWM duty = 50%. For open-loop control, set the output duty when the input PWM duty = 50%. Output duty = D50[7:0] / 256. For closed-loop control, set the reference speed when the input PWM duty = 50%. Speed = D50[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_3 (0Dh)

The SPEED_CURVE_3 command configures the output duty or speed when the input PWM duty cycle is at 62.5%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D62.5[7:0]	0xA0	Sets the output duty or speed when the input PWM duty = 62.5%. For open-loop control, set the output duty when the input PWM duty = 62.5%. Output duty = $D62.5[7:0] / 256$. For closed-loop control, set the reference speed when the input PWM duty = 62.5%. Speed = $D62.5[7:0] / 256 \times SPD_MAX[15:0]$.

SPEED_CURVE_4 COMMAND (0x0E)

The SPEED_CURVE_4 COMMAND configures the output duty or speed when input PWM duty cycle is 75%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D75[7:0]	0xC0	Sets the output duty or speed when the input PWM duty = 75%. For open-loop control, set the output duty when the input PWM duty = 75%. Output duty = $D75[7:0] / 256$. In closed-loop control, set the reference speed when the input PWM duty = 75%. Speed = $D75[7:0] / 256 \times SPD_MAX[15:0]$.

SPEED_CURVE_5 (0Fh)

The SPEED_CURVE_5 command configures the output duty or speed when the input PWM duty cycle is at 87.5%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	D87.5[7:0]	0xE0	Sets the output duty or speed when the input PWM duty = 87.5%. For open-loop control, set the output duty when the input PWM duty = 87.5%. Output duty = $D87.5[7:0] / 256$. For closed-loop control, set the reference speed when the input PWM duty = 87.5%. Speed = $D87.5[7:0] / 256 \times SPD_MAX[15:8]$.

CFR_5 (10h)

The CFR_5 command indicates the one-time programmable (OTP) memory page and sets the debugging mode.

Bits	Access	Bit Name	Default	Description
7:6	R	RESERVED	-	Reserved.
5:4	R	OTP_PAGE[1:0]	00	OTP memory page indicator. 00: No OTP is configured 01: OTP Page 1 is configured 10: OTP Page 2 is configured
3:1	R	RESERVED	-	Reserved.
0	R/W	DEBUG	0	Sets the debugging mode. Write 1 to this bit to exit debugging mode.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible. A sufficient capacitance must be applied to maintain a stable input voltage (V_{IN}) and reduce input switching voltage noise and ripple. C_{IN} 's impedance must be low at the switching frequency (f_{sw}). Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics.

The capacitance depends on the DC voltage applied on the capacitor. A ceramic capacitor can lose more than 50% of its capacitance when the voltage is close to the voltage rating. Leave a sufficient voltage rating margin when selecting the capacitor.

It is recommended to use an additional electrolytic capacitor to absorb chargeback energy.

Input Clamping Transient Voltage Suppressor (TVS)

High voltage spikes are created when the energy stored in the motor charges back to C_{IN} . To avoid these spikes, a voltage-clamping transient voltage suppressor (TVS) diode is recommended. The maximum clamping voltage should be below the MP6631A's maximum operating V_{IN} .

Hall Placement and Connection

Hall-effect sensors are required to operate the MP6631A, which supports Hall elements with differential inputs. When Hall elements are used, the Hall-effect sensors can be connected in series or in parallel.

Figure 7 shows the Hall-effect sensors connected in series.

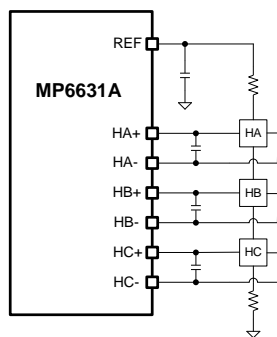


Figure 7: Series Hall Elements Connection

Figure 8 shows the Hall-effect sensors connected in parallel.

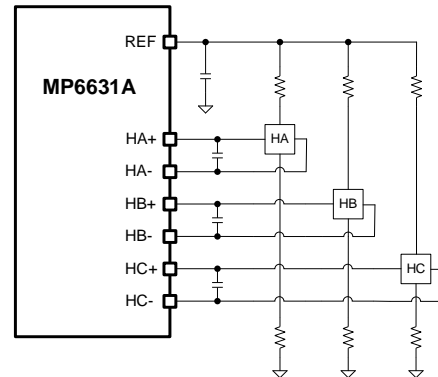


Figure 8: Parallel Hall Elements Connection

The MP6631A's Hall-sensor IC outputs logic polarity with an open-drain output, and requires an external pull-up resistor.

Figure 9 shows the Hall-sensor IC connection.

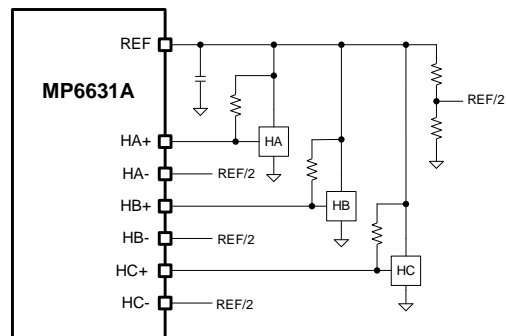


Figure 9: Hall Sensor Connection

Hall Sensor Placement Example

The MP6631A supports either a single or triple Hall-effect sensor. Consider the Hall sensor placement for a 4-pole, 6-slot motor. There are two conditions to evaluate:

1. When the current flows into the stator phase winding, the north magnetic field is generated.
2. Whether the Hall sensor output is high when the north pole is close to the Hall sensor's branded side.

If both conditions are satisfied, then the Hall sensor placement is as follows (see Figure 10 on page 24):

- Hall A is aligned with phase B's central line.
- Hall B is aligned with phase C's central line.

- Hall C is aligned with phase A's central line. In single Hall-effect sensor applications, Hall C is the active Hall-effect sensor.

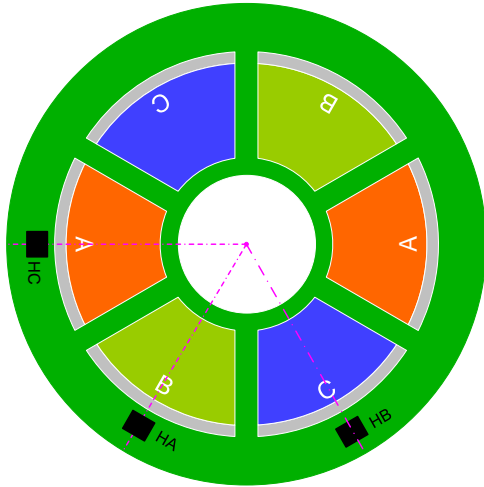


Figure 10: Hall Sensor Placement Option 1

If one of these conditions is not satisfied, then the Hall sensor placement can be shifted 180° into an electrical angle, resulting in the following Hall sensor placement (see Figure 11):

- Hall A is aligned with the central line of phase A and phase C.
- Hall B is aligned with the central line of phase A and phase B.
- Hall C is aligned with the central line of Phase B and Phase C.

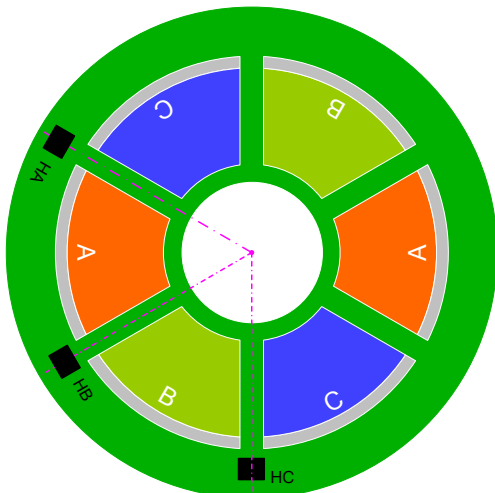


Figure 11: Hall Sensor Placement Option 2

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and Figure 13, and follow the guidelines below:

- After selecting C_{IN} , place a 100nF/X7R bypass capacitor as close to the VCC and GND pins as possible.
- Figure 12 shows the recommended PCB layout when the MP6631A is placed on the top layer and the bypass capacitor is placed on the bottom layer.

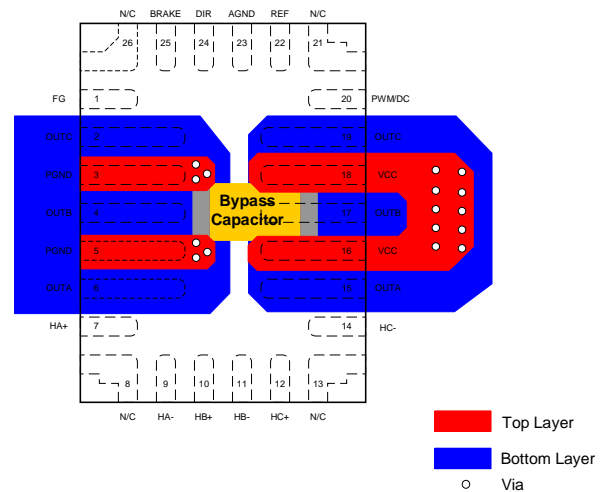


Figure 12: Recommended PCB Layout (Top View)

- Figure 13 shows the side view of the MP6631A's recommended PCB layout.

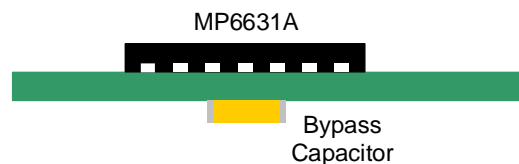


Figure 13: Recommended PCB Layout (Side View)

TYPICAL APPLICATION CIRCUIT

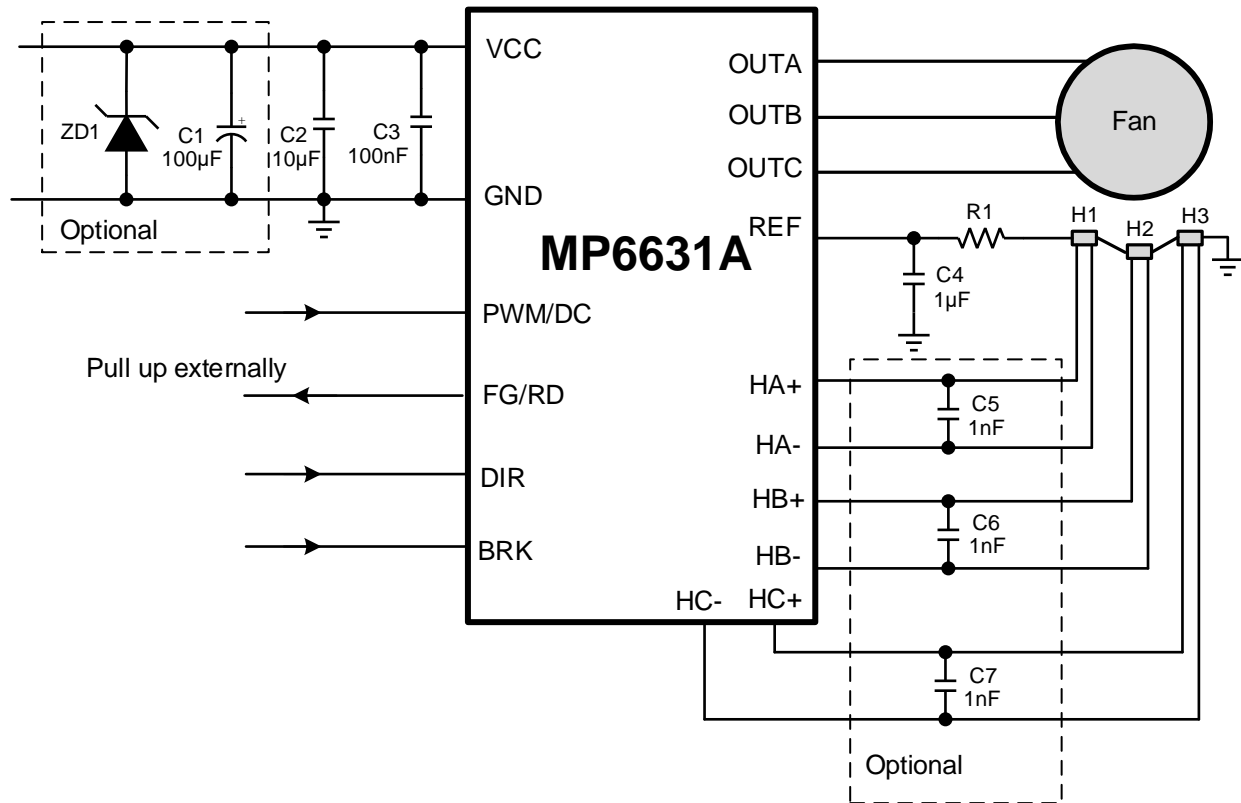
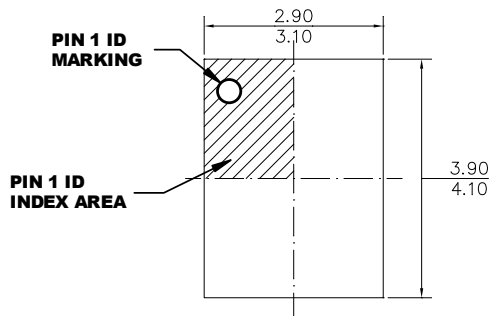


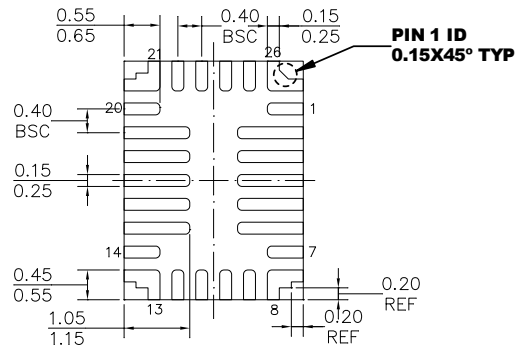
Figure 12: Triple Hall-Effect Sensor Application

PACKAGE INFORMATION

QFN-26 (3mmx4mm)



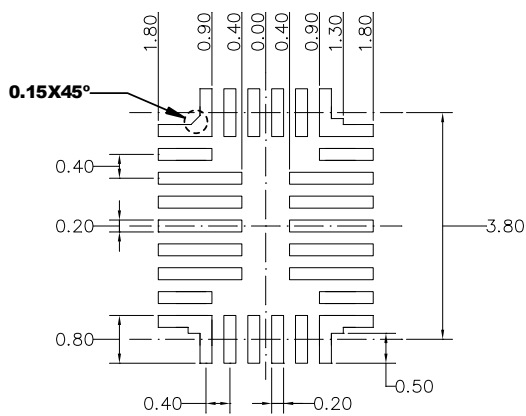
TOP VIEW



BOTTOM VIEW



SIDE VIEW

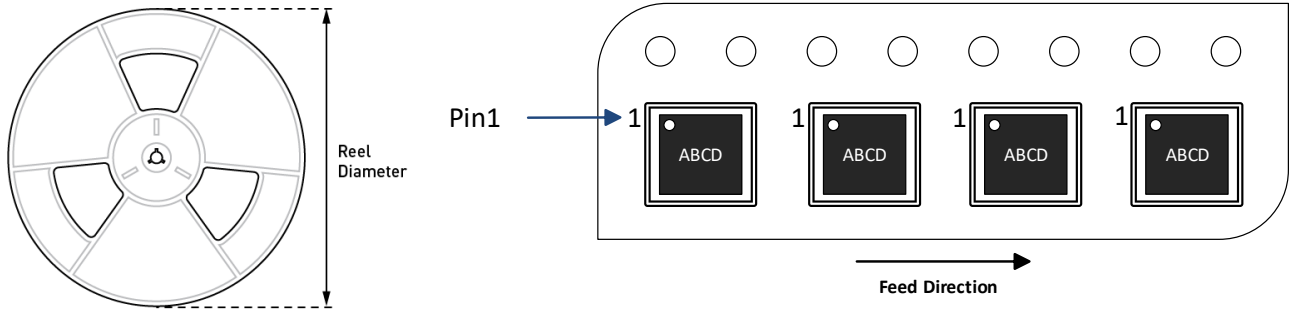


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6631AGL-xxxx-Z	QFN-26 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm



REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/15/2023	Initial Release	-

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